Passive operator panel featuring an intelligent display and a keyboard; according to the model ordered the display can be LCD backlit or fluorescent, alphanumeric 2 rows by 20 characters or 4 rows by 20 characters or graphic 140x16 or 32 pixel. Such panel is a passive device therefore there is always need for an external CPU section to make it work. The display can be alphanumeric or graphic. Section to generate contrast for LCD display, set by a trimmer. 24 keys matrix keyboard. Also featuring 16 LEDs of two different colors, 12 matched to 12 keys and 4 matched to customizable slots. Size: 185 x 139 x 57 mm (L x H x D) with possibility of front panel or back panel mounting or direct to Phoenix CombiCard® industrial instrument cases. Protection level of frontal is IP 65. On board resources management is performed completely by the firmware running on an external CPU board. Such board communicates with the operator panel through a 20 pins low profile connector. This latter is a standard I/O ABACO® connector that connects 16 I/O TTL signals to manage the operator panel. For the user, a great number of example programs for several different CPUs are available. On board power supply capable to accept input voltages in the range 8÷24 Vac or 12÷34 Vdc. QTP24P can also supply +5 Vdc for external loads by a 2 pins specific connector.
Tutte le informazioni contenute sul presente manuale sono state accuratamente verificate, ciononostante grifo® non si assume nessuna responsabilità per danni, diretti o indiretti, a cose e/o persone derivanti da errori, omissioni o dall'uso del presente manuale, del software o dell'hardware ad esso associato. grifo® altresì si riserva il diritto di modificare il contenuto e la veste di questo manuale senza alcun preavviso, con l'intento di offrire un prodotto sempre migliore, senza che questo rappresenti un obbligo per grifo®

Per le informazioni specifiche dei componenti utilizzati sui nostri prodotti, l'utente deve fare riferimento agli specifici Data Book delle case costruttrici o delle seconde sorgenti.

**LEGENDA SIMBOLI**

Nel presente manuale possono comparire i seguenti simboli:

- **Attenzione: Pericolo generico**
- **Attenzione: Pericolo di alta tensione**
- **Attenzione: Dispositivo sensibile alle cariche elettrostatiche**

**Marchi Registrati**

GENERAL INDEX

INTRODUCTION ................................................................................................................... 1

CARD VERSION ................................................................................................................... 3

GENERAL INFORMATION ................................................................................................... 4
  KEYBOARD ....................................................................................................................... 6
  DISPLAY ........................................................................................................................ 6

TECHNICAL FEATURES .................................................................................................... 8
  GENERAL FEATURES ........................................................................................................ 8
  PHYSICAL FEATURES ...................................................................................................... 8
    DIMENSIONS OF OPERATOR PANEL QTP 24P ................................................................. 9
  ELECTRIC FEATURES ..................................................................................................... 10

INSTALLATION ................................................................................................................... 12
  CONNECTIONS ................................................................................................................ 12
    CN1 - EXTERNAL POWER SUPPLY CONNECTOR ....................................................... 12
    CN3 - KEYBOARD CONNECTOR ................................................................................ 14
    CN2 - DIGITAL I/O LINES CONNECTOR .................................................................. 16
    CN4 - FIRST DISPLAY CONNECTOR ......................................................................... 18
    CN5 - SECOND DISPLAY CONNECTOR .................................................................... 20
    CN6 - THIRD DISPLAY CONNECTOR ........................................................................ 22

JUMPERS .............................................................................................................................. 24
  DISPLAYS MANAGED ........................................................................................................ 24
  CONTRAST REGULATION TRIMMER ........................................................................... 25
  I/O CONNECTION ............................................................................................................ 25
  POWER SUPPLY ................................................................................................................ 25

SOFTWARE DESCRIPTION .................................................................................................. 26
  HIGH LEVEL MANAGEMENT ......................................................................................... 26
  LOW LEVEL MANAGEMENT .......................................................................................... 28
  KEYBOARD ...................................................................................................................... 28
  DISPLAY ........................................................................................................................ 30
  LEDS ............................................................................................................................... 30

BIBLIOGRAPHY .................................................................................................................... 32

APPENDIX A: ELECTRIC DIAGRAM ................................................................................. A-1

APPENDIX B: DISPLAY CHARACTERS ............................................................................. B-1

APPENDIX C: ON BOARD DEVICES DESCRIPTION ......................................................... C-1

APPENDIX D: QTP 24P LABELS INSERTION ..................................................................... D-1

APPENDIX E: ALPHABETICAL INDEX ............................................................................... E-1

QTP24P Rel. 5.00
FIGURES INDEX

FIGURE 1: LOCATION OF REVISION NUMBER AND CARD NAME ................................................................. 3
FIGURE 2: BLOCKS DIAGRAM ................................................................................................................... 5
FIGURE 3: PHOTO OF QTP 24P WITHOUT DISPLAY ............................................................................... 7
FIGURE 4: DIMENSION OF OPERATOR PANEL QTP 24P ....................................................................... 9
FIGURE 5: CONSUMPTIONS TABLE ......................................................................................................... 10
FIGURE 6: SOME CONFIGURATIONS AVAILABLE FOR QTP 24P ....................................................... 11
FIGURE 7: CN1 - EXTERNAL POWER SUPPLY CONNECTOR ................................................................. 13
FIGURE 8: CN3 - EXTERNAL KEYBOARD CONNECTOR ......................................................................... 14
FIGURE 9: JUMPER, CONNECTORS, TRIMMER, ETC. LOCATION ........................................................... 15
FIGURE 10: CN2 - DIGITAL I/O LINES CONNECTOR ............................................................................. 16
FIGURE 11: QTP 24P COMPONENTS MAP (COMPONENT SIDE) .......................................................... 17
FIGURE 12: QTP 24P COMPONENTS MAP (SOLDER SIDE) ................................................................. 17
FIGURE 13: CN4 - FIRST DISPLAY CONNECTOR .................................................................................... 18
FIGURE 14: PHOTO OF QTP 24P-C4 .................................................................................................... 19
FIGURE 15: PHOTO OF QTP 24P-GF4 .................................................................................................. 19
FIGURE 16: CN5 - SECOND DISPLAY CONNECTOR ................................................................................ 20
FIGURE 17: PHOTO OF QTP 24P-F2 .................................................................................................... 21
FIGURE 18: PHOTO OF QTP 24P-F4 .................................................................................................... 21
FIGURE 19: CN6 - THIRD DISPLAY CONNECTOR .................................................................................. 22
FIGURE 20: PHOTO OF QTP 24P-C2 .................................................................................................... 23
FIGURE 21: PHOTO OF QTP 24P-GF2 .................................................................................................. 23
FIGURE 22: JUMPER TABLE ................................................................................................................ 24
FIGURE 23: DISPLAYS CONNECTABLE .................................................................................................. 24
FIGURE 24: KEYS MAP ......................................................................................................................... 27
FIGURE 25: LEDS MAP ......................................................................................................................... 29
FIGURE 26: AVAILABLE CONNECTIONS DIAGRAM ......................................................................... 31
FIGURE A1: ELECTRIC DIAGRAM (PART 1) ............................................................................................ A-1
FIGURE A2: ELECTRIC DIAGRAM (PART 2) ............................................................................................ A-2
FIGURE B1: QTP 24P-F2, F4, F24, GF2, GF4 CHARACTERS TABLE IN ALPHANUMERIC MODE .... B-1
FIGURE B2: QTP 24P-C2, C4 CHARACTERS TABLE ............................................................................. B-2
FIGURE B3: QTP 24P-GF2, GF4 CHARACTERS TABLE WITH MINIFONT GRAPHIC MODE .......... B-4
FIGURE B4: QTP 24P-GF2, GF4 CHARACTERS TABLE WITH KATAKANA GRAPHIC FONT ............ B-5
FIGURE B5: QTP 24P-GF2,GF4 CHARACTERS TABLE WITH EUROPEAN GRAPHIC FONT .......... B-6
FIGURE D1: LABELS INSERTION IN QTP 24P ......................................................................................... D-1
INTRODUCTION

The use of these devices has turned - IN EXCLUSIVE WAY - to specialized personnel. This device is not a safe component as defined in directive 98-37/CE.

Pins of Mini Module are not provided with any kind of ESD protection. They are connected directly to their respective pins of microcontroller. Mini Module is affected by electrostatic discharges. Personnel who handles Mini Modules is invited to take all necessary precautions to avoid possible damages caused by electrostatic discharges.

The purpose of this handbook is to give the necessary information to the cognizant and sure use of the products. They are the result of a continual and systematic elaboration of data and technical tests saved and validated from the manufacturer, related to the inside modes of certainty and quality of the information.

The reported data are destined- IN EXCLUSIVE WAY- to specialized users, that can interact with the devices in safety conditions for the persons, for the machine and for the enviroment, impersonating an elementary diagnostic of breakdowns and of malfunction conditions by performing simple functional verify operations, in the height respect of the actual safety and health norms.

The informations for the installation, the assemblage, the dismantlement, the handling, the adjustment, the reparation and the contingent accessories, devices etc. installation are destined - and then executable - always and in exclusive way from specialized warned and educated personnel, or directly from the TECHNICAL AUTHORIZED ASSISTANCE, in the height respect of the manufacturer recommendations and the actual safety and health norms.

The devices can't be used outside a box. The user must always insert the cards in a container that respect the actual safety normative. The protection of this container is not threshold to the only atmospheric agents, but specially to mechanic, electric, magnetic, etc. ones.

To be on good terms with the products, is necessary guarantee legibility and conservation of the manual, also for future references. In case of deterioration or more easily for technical updates, consult the AUTHORIZED TECHNICAL ASSISTANCE directly.
To prevent problems during card utilization, it is a good practice to read carefully all the informations of this manual. After this reading, the user can use the general index and the alphabetical index, respectly at the begining and at the end of the manual, to find information in a faster and more easy way.
CARD VERSION

This handbook make reference to card QTP24P with printed circuit version 101095. The validity of the information contained in this manual is subordinated to the card version number.

**Figure 1: Location of Revision Number and Card Name**
GENERAL INFORMATION

The QTP 24P family card is composed by interesting boards that solve the operator interface problems inside the automation field, in a low cost and efficient way. All the cards are composed by two indipendent sections: one for an external matrix keyboard acquisition and the other for LCD or Fluorescent (VFD) display management. Both the sections are driven by only two 8 bit parallel ports, at TTL level. In this manner all the cards provided of at least 16 TTL lines on a standard 20 pins I/O ABACO® connector, can be connected to QTP 24P modules and they can easily exchange data and informations with the user.

The greater part of grifo® control cards can be connected to these cards with the possibility to use many different microprocessors (Z80, 8086, 8051, 68HC11, etc.) and proper software packages (BASIC, C, PASCAL, etc.). For some coupling of control cards and software tools, together with QTP 24P is provided a proper management firmware that drives the keyboard and the display at high level, with considerable facility and time saving. In fact this firmware let the user manage display and keyboard directly with the high level console instructions as PRINT, PRINTK, KBHIT, INPUT, SCANF, KEYHIT, etc.

The wide range of different displays models let the user select the best configuration according with the application requirements, in terms of: price, visibility, dimension, graphic, alphanumeric, consumption, etc.

The QTP 24P hardware structure is designed to simplify the software management of the card and to minimize the necessary lines for its management; moreover the connectors position and the mounting holes ensure a fast installation of the card inside the electric panel.

- Dimension: 185 x 139 x 57 mm (W x H x D)
- Mounting as front or back panel or Phoenix CombiCard® industrial instrumental case
- Protection level IP 65
- Matrix keyboard with 6 x 4 = 24 keys
- Intelligent display, in the following models (it must be specified during order phase):
  - QTP 24P-C2  -> alphanumeric LCD display, backlit, with 2 lines for 20 characters;
  - QTP 24P-C4  -> alphanumeric LCD display, backlit, with 4 lines for 20 characters;
  - QTP 24P-F2  -> alphanumeric VFD display with 2 lines for 20 characters;
  - QTP 24P-F4  -> alphanumeric VFD display with 4 lines for 20 characters.
  - QTP 24P-GF2  -> graphic VFD display with 140x16 pixel;
  - QTP 24P-GF4  -> graphic VFD display with 140x32 pixel;
- Section that generates contrast voltage for LCD display.
- Complete software management of the card sections with 16 TTL I/O lines on standard 20 pins, low profile, I/O ABACO® connector.
- Wide range of management firmware supplied as driver, library, console input output redirection, etc., available for:
  - Z80 based cards through GDOS or FGDOS romate operating system,
  - I51 based cards through BASIC 52, BASCOM 8051 and µC/51,
  - I86 based cards through GCTR,
  - AVR based cards through BASCOM AVR and ICC AVR etc. etc.
- Power supply in the range 8÷24 Vac or 12÷34 Vdc
- Possibility to supply external loads

Here follows a description of the board's functional blocks, with an indication of the operations performed by each one.
**Figure 2: Blocks diagram**
KEYBOARD

QTP 24P has a matrix keyboard with 6 columns by 4 rows that can manage up to 24 keys. Some of the 10 lines necessary for keyboard acquisition are used also by display interface, so a specific firmware must solve this situation and avoid complications. Twelve red LEDs are driven directly by driver M5480 and are matched to as many keys. Above mentioned keys can be customized by inserting description labels in specific slots, other slot allow to customize the remaining four LEDs (green) by inserting more labels. Thanks to this simple keyboard QTP 24P solves in an inexpensive way the problem of data input, even in case of several data.

DISPLAY

QTP 24P is available with Fluorescent VFD or backlit LCD displays provided of different features. In detaily, following alphanumeriс displays can be connected:

- LCD 20x2 characters -> QTP 24P-C2
- LCD 20x4 characters -> QTP 24P-C4
- VFD 20x2 characters -> QTP 24P-F2
- VFD 20x4 characters -> QTP 24P-F4

and the following graphic displays:

- VFD 140x16 pixels -> QTP 24P-GF2
- VFD 140x32 pixels -> QTP 24P-GF4

LEDs backlighting of LCD models ensures a good visibility even when the environmental lighting changes and if it necessary the user can modify the contrast regulation by acting on a specific trimmer. Another important features of QTP 24P displays is their wide viewing angle that allows a good visibility from each frontal position. The user must choose the right display (so the right QTP 24P model) that is sufficient for the information to visualize and for his visibility requirements. For specific requirements on current consumption, visibility and price the card can be provided with LCD display not backlit: for detailed information about these options and their availability, please contact directly grifo® offices.

On the board there are three specific connectors that has been designed to simplify the connection of each displays, which is made through a direct soldering on the printed circuit (default configuration) or trough a simple flat cable. The user receives the board with the display already mounted and tested by grifo® technicians, so the board is ready to be used. Further information on each display are reported in DISPLAYS MANAGED chapter.
Figure 3: Photo of QTP 24P without display
TECHNICAL FEATURES

GENERAL FEATURES

Resources:  Alphanumeric or graphic display in six different models
            Trimmer to set LCD display contrast
            Matrix keyboard
            On board power supply

Displays:  Alphanumeric
           LCD: 20x2 or 20x4
           Fluorescent VFD: 20x2 or 20x4
           Graphic
           Fluorescent VFD: 140x16 or 140x32

Management lines:  16 digital I/O at TTL level:
                   12 outputs
                   4 inputs

PHYSICAL FEATURES

Size:  See outline dimension in figure 4

Weight:  700 g max.

Mounting:  Front panel or back panel mounting, or direct mounting on
           industrial instrument case Phoenix CombiCard®

Front panel protection:  IP65

Temperature range:  From 0 to 50 °C

Relative humidity:  20% up to 90% (without condense)

Connectors:  CN1: screw terminal connector, vertical, 2 pins
             CN2: low profile connector, male, vertical, 20 pins
             CN3: strip connector, male, vertical, 10 pins
             CN4: strip connector pods, male, 16 pins
             CN5: strip connector pods, male, 20 pins
             CN6: strip connector pods, male, 16 pins
DIMENSIONS OF OPERATOR PANEL QTP 24P

Here follow the dimensions, in millimeters, of operator panel QTP 24P seen from behind and by the side where input connectors are. Please remark that figures are not scaled.

**Figure 4: Dimension of Operator Panel QTP 24P**
ELECTRIC FEATURES

Power voltage: 8÷24 Vac, 12÷34 Vdc or only OEM orders +5 Vdc ± 5% (without on board power supply)

Voltage for external loads: +5 Vdc

Power supply current: 1300 mA

Current for external loads: 1300 mA deduct QTP 24P consumption (see next table)

Power consumption: See next table

Here follows the list of QTP 24P power consumption referred to the different display types, in typical applications use.

To reduce consumptions of QTP 24P with LCD display it is possible to order them only OEM without backlighting, for further information please contact directly grifo®.

(*) The data are referred to 20°C work temperature (for further information please refer to chapter "POWER SUPPLY VOLTAGE").

<table>
<thead>
<tr>
<th>DISPLAY</th>
<th>CONSUMPTION (LEDs OFF)</th>
<th>CONSUMPTION (LEDs ON)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Alphanumeric LCD 20x2 backlit</strong> Maximum current for external loads (at 20°C)</td>
<td>150 mA - +5vdc 1150 mA</td>
<td>400 mA - +5vdc 900 mA</td>
</tr>
<tr>
<td><strong>Alphanumeric LCD 20x4 backlit</strong> Maximum current for external loads (at 20°C)</td>
<td>100 mA - +5vdc 1200 mA</td>
<td>350 mA - +5vdc 950 mA</td>
</tr>
<tr>
<td><strong>Alphanumeric VFD 20x2</strong> Maximum current for external loads (at 20°C)</td>
<td>130 mA - +5vdc 1170 mA</td>
<td>380 mA - +5vdc 920 mA</td>
</tr>
<tr>
<td><strong>Alphanumeric VFD 20x4</strong> Maximum current for external loads (at 20°C)</td>
<td>220 mA - +5vdc 1080 mA</td>
<td>470 mA - +5vdc 830 mA</td>
</tr>
<tr>
<td><strong>Graphic VFD 140x16</strong> Maximum current for external loads (at 20°C)</td>
<td>260 mA - +5vdc 1040 mA</td>
<td>510 mA - +5vdc 790 mA</td>
</tr>
<tr>
<td><strong>Graphic VFD 140x32</strong> Maximum current for external loads (at 20°C)</td>
<td>460 mA - +5vdc 840 mA</td>
<td>710 mA - +5vdc 490 mA</td>
</tr>
</tbody>
</table>

**Figure 5: Consumptions table**
Figure 6: Some configurations available for QTP 24P
INSTALLATION

In this chapter there are the information for a right installation and correct use of the QTP 24P card. In detail there are the locations and functions of each connector, of the user settable jumper, of the trimmer and some explanatory diagrams.

CONNECTIONS

QTP 24P terminal has 6 connectors that can be linkeded to other devices or directly to the field, according to system requirements.

In this paragraph there are connectors pin out, a short signals description (including the signals direction) and connectors location (see figure 9), that simplify and speed the installation phase. Connectors are accessible from top and bottom of the printed circuit board, to easy insertion and extraction.

CN1 - EXTERNAL POWER SUPPLY CONNECTOR

CN1 is a 4 pins screw terminal connector, with 5 mm pitch.
On CN1 can be connected an external power supply voltage for the high consumption sections of the card (LCD backligt, VFD, etc.) whenever the power available on the control card, connected through CN3, is not sufficient.
For further information please refer to chapter "POWER SUPPLY VOLTAGE".
QTP 24P features a power supply section capable to supply itself and an external load with a stabilized voltage of +5 Vdc.
This allows to reduce the cost of the application because QTP 24P can provide a remarkable current intensity to the external load also in the worst conditions.
For further information please refer to chapter "ELECTRIC FEATURES".

NOTE: Only for OEM orders, it is possible to obtain QTP 24P optionally without power supply. In this case it can be supplied providing +5 Vdc ± 5% through the pins of CN1 that here are used to fetch the voltage for external loads.
FIGURE 7: CN1 - EXTERNAL POWER SUPPLY CONNECTOR

Signals description:

8÷24 Vac, 12÷34 Vdc = O - 8÷24 Vac or 12÷34 Vdc from external power supply (see jumper J1)
+5 Vdc OUT = O - +5 Vdc to supply eventual external loads
GND = - Ground signal.
CN3 - KEYBOARD CONNECTOR

CN3 is a 10 pins, vertical, male strip connector, with 2.54 mm pitch.
CN2 features all the signals needed to connect the matrix keyboard featuring 24 keys.

Figures 8: CN3 - External keyboard connector

Signals description:

Col n = O - Output line for n-th column of 4x6 external matrix keyboard.
Row n = I - Input line for n-th row of 4x6 external matrix keyboard.

External keys must be connected so that pressing one key connects input Row n and output Col n.
Figure 9: Jumper, Connectors, Trimmer, etc. Location
CN2 - DIGITAL I/O LINES CONNECTOR

CN2 is a 20 pins, male, vertical, low profile connector with 2.54mm pitch. On CN2 are connected the 16 digital I/O lines used to manage all the sections of QTP 24P interface. All these signals follow TTL standard and I/O ABACO® standard pin out.

![Diagram of CN2 - Digital I/O Lines Connector]

<table>
<thead>
<tr>
<th>Signal</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>PA.n</td>
<td>I/O - Digital line n of first management port, named Port A</td>
</tr>
<tr>
<td>PC.n</td>
<td>I/O - Digital line n of second management port, named Port C</td>
</tr>
<tr>
<td>+5 Vdc</td>
<td>+5 Vdc power supply from control card (see jumper J1)</td>
</tr>
<tr>
<td>GND</td>
<td>Ground signal</td>
</tr>
<tr>
<td>N.C.</td>
<td>Not connected</td>
</tr>
</tbody>
</table>

**Figure 10: CN2 - Digital I/O Lines Connector**
**Figure 11:** QTP 24P components map (component side)

**Figure 12:** QTP 24P components map (solder side)
CN4 - FIRST DISPLAY CONNECTOR

CN4 is 16 pins strip connector pods, with 2.54 mm pitch. CN4 features all the control and command signals of LCD display (or LCD compatible) with standard pin out that allows direct connection to most of them. In detail this connector is used to interface the following displays:

- alphanumeric LCD 20x4  QTP 24P-C4
- alphanumeric VFD 20x4  QTP 24PF4
- graphic VFD 140x32  QTP 24P-GF4

![Diagram of CN4 Connector Pinout](image)

**FIGURE 13: CN4 - FIRST DISPLAY CONNECTOR**
Signals description:

A (+) = O - Anod or positive terminal for LED backlighting of LCD display.
K (-) = O - Kathod or negative terminal for LED backlighting of LCD display.
DBx = I/O - Line x of display 8 bit data bus.
R/W = O - Control signal to select read or write operation.
E = O - Display enable signal.
RS = O - Control signal to select between command or data operation.
Vo , Vlc = O - Contrast tension for LCD display.
+5 Vdc , VDD = O - Display power supply voltage.
GND , VSS = - Ground signal.

Figure 14: Photo of QTP 24P-C4

Figure 15: Photo of QTP 24P-GF4
CN5 - SECOND DISPLAY CONNECTOR

CN5 is 20 pins low profile connector pods, with 2.54 mm pitch. CN5 features all the control and command signals of FUTABA VFD display with standard pin out that allows direct connection to most of them. Actually this connector is no more used for the described QTP 24P models but it is maintained for compatibility or for specific customer requirements.

**FiguRE 16: CN5 - SECOND DISPLAY CONNECTOR**

Signals description:

- **DBx** = I/O - Line x of display 8 bit data bus.
- **/WR** = O - Control signal to select read or write operation.
- **/SEL** = O - Display enable signal.
- **/TEST** = O - Display test mode enable signal.
- **BUSY** = I - Status signal to indicate whether display is busy.
- **+5 Vdc** = O - Display power supply voltage.
- **GND** = - Ground signal.
- **N.C.** = - Not connected.

<table>
<thead>
<tr>
<th>DB7</th>
<th>1</th>
<th>2</th>
<th>+5 Vdc</th>
</tr>
</thead>
<tbody>
<tr>
<td>DB6</td>
<td>3</td>
<td>4</td>
<td>+5 Vdc</td>
</tr>
<tr>
<td>DB5</td>
<td>5</td>
<td>6</td>
<td>+5 Vdc</td>
</tr>
<tr>
<td>DB4</td>
<td>7</td>
<td>8</td>
<td>GND</td>
</tr>
<tr>
<td>DB3</td>
<td>9</td>
<td>10</td>
<td>GND</td>
</tr>
<tr>
<td>DB2</td>
<td>11</td>
<td>12</td>
<td>GND</td>
</tr>
<tr>
<td>DB1</td>
<td>13</td>
<td>14</td>
<td>GND</td>
</tr>
<tr>
<td>DB0</td>
<td>15</td>
<td>16</td>
<td>/TEST</td>
</tr>
<tr>
<td>/WR</td>
<td>17</td>
<td>18</td>
<td>/SEL</td>
</tr>
<tr>
<td>N.C.</td>
<td>19</td>
<td>20</td>
<td>BUSY</td>
</tr>
</tbody>
</table>
Figure 17: Photo of QTP 24P-F2

Figure 18: Photo of QTP 24P-F4
CN6 - THIRD DISPLAY CONNECTOR

CN6 is a 16-pin low profile connector pod, with 2.54 mm pitch. CN6 features all the control and command signals of LCD display (or LCD compatible) with standard pinout, allowing direct connection to most of them. In detail, this connector is used to interface the following displays:

- Alphan. LCD 20x2: KDX-C2
- Alphan. LCD 40x2: KDX-C24
- Alphan. VFD 20x2: KDX-F2
- Alphan. VFD 40x2: KDX-F24
- Graph. VFD 140x16: KDX-GF2
- Graph. VFD 140x16: KDX-GF2

**FIGURE 19: CN6 - THIRD DISPLAY CONNECTOR**

Signals description:

A (+) = O - Anode or positive terminal for LED backlighting of LCD display.
K (-) = O - Cathode or negative terminal for LED backlighting of LCD display.
DBx = I/O - Line x of display 8-bit data bus.
R/W = O - Control signal to select read or write operation.
E = O - Display enable signal.
RS = O - Control signal to select between command or data operation.
Vo, VLC = O - Contrast tension for LCD display.
+5 Vdc, VDD = O - Display power supply voltage.
GND, VSS = - Ground signal.
Figure 20: Photo of QTP 24P-C2

Figure 21: Photo of QTP 24P-GF2
JUMPERS

On **QTP 24P** there are 2 jumpers used for card configuration. By configuring this jumpers, the user can define the power supply modalities as below described:

<table>
<thead>
<tr>
<th>JUMPER</th>
<th>CONNECTION</th>
<th>PURPOSE</th>
<th>DEF.</th>
</tr>
</thead>
<tbody>
<tr>
<td>J1</td>
<td>not connected</td>
<td>Power supply of control board is not connected to power supply of <strong>QTP24P</strong> through CN2.</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>connected</td>
<td>Power supply of control board is connected to power supply of <strong>QTP24P</strong> through CN2.</td>
<td></td>
</tr>
<tr>
<td>J2</td>
<td>not connected</td>
<td>Does not connect the ground of <strong>QTP24P</strong> to frontal and rear metallic carter.</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>connected</td>
<td>Connects the ground of <strong>QTP24P</strong> to frontal and rear metallic carter.</td>
<td></td>
</tr>
</tbody>
</table>

**FIGURE 22: JUMPER TABLE**

To recognize these valid connections, please refer to the board printed diagram (serigraph) or to figures 11 and 12 of this manual, where the pins numeration is listed; for recognizing jumper location, please refer to figure 9.

The "*" denotes the default connection, or on the other hand the connection set up at the end of testing phase, that is the configuration the user receives.

Further information about purpose of jumpers are reported in the paragraph “POWER SUPPLY”.

DISPLAYS MANAGED

Hardware structure of **QTP 24P** can use most alphanumeric and graphic intelligent displays currently in commerce, both LCD and VFD fluorescent.

<table>
<thead>
<tr>
<th>TYPE</th>
<th>MODEL</th>
<th>MANUFACTURER</th>
<th>CONNECTOR</th>
</tr>
</thead>
<tbody>
<tr>
<td>Alphanumeric LCD 20x2</td>
<td>SSC2A20DLYY-02</td>
<td>SDEC</td>
<td>CN6</td>
</tr>
<tr>
<td>Alphanumeric VFD 20x2</td>
<td>CU20025ECPB-U1J</td>
<td>NORITAKE ITRON</td>
<td>CN6</td>
</tr>
<tr>
<td>Alphanumeric LCD 20x4</td>
<td>SSC4A20DLYY-02</td>
<td>SDEC</td>
<td>CN4</td>
</tr>
<tr>
<td>Alphanumeric LCD 20x4</td>
<td>AC204AYILY02</td>
<td>AMPIRE</td>
<td>CN4</td>
</tr>
<tr>
<td>Alphanumeric VFD 20x4</td>
<td>CU20045SCP8-U1J</td>
<td>NORITAKE ITRON</td>
<td>CN4</td>
</tr>
<tr>
<td>Graphic VFD 140x16</td>
<td>GU140x16G-7806</td>
<td>NORITAKE ITRON</td>
<td>CN6</td>
</tr>
<tr>
<td>Graphic VFD 140x32</td>
<td>GU140x32F-7806</td>
<td>NORITAKE ITRON</td>
<td>CN4</td>
</tr>
</tbody>
</table>

**FIGURE 23: DISPLAYS CONNECTABLE**
CONTRAST REGULATION TRIMMER

On QTP 24P board there is a trimmer that defines the contrast on LCD displays. This trimmer, named RV1, is set by grifo® to obtain the best display visibility in each working conditions and normally the user must not change its position. In case of specific requirements, as external light very low or very high, it can be changed by little rotation in both directions until the visibility is improved. For recognizing the location of contrast regulation trimmer, please refer to figure 9.

I/O CONNECTION

To prevent possible connecting problems between QTP 24P and the external systems, the user has to read carefully the previous paragraph information and he must follow these instructions:

- For all TTL signals the user must follow the rules of this electric standard. The connected digital signal must be always referred to card digital ground. For TTL signals, the 0V level corresponds to logic state 0, while 5V level corresponds to logic state 1.

- To avoid driving problems and minimize the effects of eventual noises from the field, connector CN2 can be connected with cables of maximum length 40 cm.

POWER SUPPLY

QTP 24P interface is provided of two different connectors that solve in a efficient and comfortable way the problem to supply the boards in any situation. On the boards there are some different sections (keyboard interface, display, LCD backlight, LCD contrast, etc) featured by different consumptions but with the same power supply voltage: +5 Vdc ±5%.

Connector CN1 allows to connect, to pins 3 and 4, 8+24 Vac or 12+34 Vdc that the on board power supply in the above mentioned +5 Vdc.

Also, jumper J1 can connect on board generated +5 Vdc and the +5 Vdc voltage on connector CN2, allowing to supply the control card too. So:

- If the control card connected to CN2 does not have its power supply source, J1 must be connected to allow QTP 24P to supply it. Please refer to paragraph “ELECTRIC FEATURES” for further information.

- If the control card connected to CN2 has its own power supply source, J1 must be not connected to avoid conflicts. Alternatively, the control card can supply QTP 24P if no power supply is connected to this latter and J1 is connected.

The card is also provided with a distributed filtering circuitry that saves the terminal from disturbs or noise from the field, improving the overall system performances.
SOFTWARE DESCRIPTION

In the previous paragraphs all the hardware lines have been described and here follows a detailed description of function and meaning of digital I/Os (please always refer to the connectors figures to understand completely the following informations or to electric diagram in APPENDIX A).

In the following paragraphs the indications D0÷D7 or 0+.7 are used to refer the bits of the byte involved in the I/O operations. Obviously this manual doesn't report information about the management of the 16 digital I/O lines in fact these depend on the used control system and the user must search them in the proper technical manual.

The software management of QTP 24P can be performed in two different manners: high level and low level mode as described in the following paragraphs.

HIGH LEVEL MANAGEMENT

This modality coincide with a firmware already developed and supplied by grifo® under the form of drivers or libraries.

By adding this firmware to the used high level programming language (C, BASIC, PASCAL, etc.) the user can manage the keyboard as a console input device and the display as a console output device.

So all the high level instructions dedicated to console management are available for QTP 24P management too, and the typical problems of data insertion, functions execution, formatted information visualization, and so on, are easily solved.

In detail, according with programming languages, the following instructions directly act on QTP 24P resources:

- BASIC -> Print ; Input ; Inkey
- C -> Printf ; Puts ; Putch ; Getch ; Getche ; Scanf ; Kbhit
- PASCAL -> Write ; Writeln ; Read ; Readln ; Keypressed

Thanks to the high level management the part of application software dedicated to operator interface, that often is one of the most important and difficult problems, is easily solved by any user with a great reduction of development time.

Actually grifo® has several ready to use high level management firmware for many microprocessors and some different software tools, as:

- Z80 based cards through GDOS or FGDOS romate operating system,
- 151 based cards through BASIC 52, BASCOM 8051 and μC/51,
- I86 based cards through GCTR,
- AVR based cards through BASCOM AVR and ICC AVR.

and detailed information about firmware integration, initialization procedures, console redirection, etc. are reported in the user manual of the same software tools.
Figure 24: Keys map
LOW LEVEL MANAGEMENT

In this modality all the QTP 24P resources are managed directly by user application program that must use the 16 digital I/O lines to drive display and acquire keyboard. Thus the application development will require more time and more knowledge, because everything (timing, lines, interrupts, formatting, ....) must be realized by the user.

KEYBOARD

The keyboard management coincide with a periodic operation that checks if there is a pressed key in that specific sample time or, in other words, if there is a cross row - column of the matrix connected by a closed contact of the relative key. Each sampling time the scan procedure composed by the following steps, must be performed:

a) Disable the connected display by setting properly its control signals.
b) Set the first column (Col 1) to low level by resetting the relative output lines to 0 logic state, and maintain all the other columns to high level (logic state 1).
c) Acquire the four rows status (Row 4 ÷ Row 1) by reading the status of the relative input lines.
d) Check if some of the four acquired Rows are at low level (logic state 0): in this condition the key connected on the cross Col 1 - Row n is pressed and viceversa.
e) Save an index, counter, number, code according with software requirements, of the found pressed keys.
f) Repeat the steps b, c, d, e for the remaining columns (Col 2 ÷ Col 6).

To ensure that no key pressed are lost it is suggested to perform the described scan at regular time interval, for example each 5 msec, by using a periodic interrupt response routine associated to a pre-setted hardware Timer. To avoid wrong identifications of not stable pressed keys (recoils are typical in these conditions) it must be used a debouncing technique that defines the key really pressed when it has been found closed for at least 20 msec, equals to 4 successive scannings.

The correspondences between the matrix keyboard lines and the digital I/O lines on CN3 are below reported:

| PA.5   | Col 1 | PC.4   | Row 1 |
| PA.4   | Col 2 | PC.5   | Row 2 |
| PA.3   | Col 3 | PC.6   | Row 3 |
| PA.2   | Col 4 | PC.7   | Row 4 |
| PA.1   | Col 5 |
| PA.0   | Col 6 |
FIGURE 25: LEDs MAP
DISPLAY

The intelligent display management is based on a parallel communication performed through an 8 bit data BUS and 3 control signals. The software must drive all these lines according with display specifications, in order to send commands and/or data to be displayed.

The correspondences between the display lines and the digital I/O lines on CN3 are below reported, both for standard display, FUTABA display:

<table>
<thead>
<tr>
<th>PA.n</th>
<th>DBn, DBn</th>
<th>PC.0</th>
<th>RS</th>
<th>----</th>
</tr>
</thead>
<tbody>
<tr>
<td>PC.1</td>
<td>R/W, /WR</td>
<td>PC.2</td>
<td>E</td>
<td>/SEL</td>
</tr>
</tbody>
</table>

When the software busy status of the display must be acquired, PA.n lines must be bidirectional, viceversa if proper delays are inserted in the software the 11 signals can be simple output lines.

In normal applications the following operations must be executed to correctly use any type of display:

a) Defines the digital I/O lines functionalty according with signals direction.
b) Initialize the display by sending proper commands.
c) Send characters to display or command to be executed (i.e. clear, cursor shift, set addresses) according to application requirements.

A complete description of control signals waveforms, display commands, initialization sequence, characters locations and characters fonts are available in APPENDIX C of this manual.

LEDs

The LEDs driver is the M5480 manufactured by STM. The driver generates a constant current, in addition M5480 driving ability exceeds the requirements of QTP 24P, so not all its signals are connected to LEDs.

Correspondance between LEDs and M5480 signals can be seen in the electric diagram in the appendix A.

Correspondance between LEDs names and their position can be seen in figure 25.

FIGURE 26: AVAILABLE CONNECTIONS DIAGRAM
BIBLIOGRAPHY

In this chapter there is a complete list of technical books, where the user can find all the necessary documentations on the components mounted on QTP 24P.

Manual TEXAS INSTRUMENTS: The TTL Data Book - SN54/74 Families
Data sheets NORITAKE-ITRON: Vacuum Fluorescent Display module specification
Manual SDEC: LCD MODULE
Manual TECDIS: Liquid Crystal Display Modules
Data sheets ST Microelectronics: M5480 - LED display driver

The described manual can be requested directly to manufacturer or local dealers. Alternatively this information and/or upgrades can be found in specific internet web pages, of the listed companies.
FIGURE A1: ELECTRIC DIAGRAM (PART 1)
FIGURE A2: ELECTRIC DIAGRAM (PART 2)
APPENDIX B: DISPLAY CHARACTERS

The following tables shows the characters sets displayed on QTP 24P for all the possible received characters, according with ordered display and model.

Even the not ASCII characters (or special characters) change when the display type changes and if the user requires a character set different from those described in the following figures, he can take a direct contact with grifo®.

**Figure B1: QTP 24P-F2, F4, F24, GF2, GF4 CHARACTERS TABLE IN ALPHANUMERIC MODE**

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<th>L</th>
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<th>10</th>
<th>20</th>
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<th>40</th>
<th>50</th>
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<th>70</th>
<th>80</th>
<th>90</th>
<th>A0</th>
<th>B0</th>
<th>C0</th>
<th>D0</th>
<th>E0</th>
<th>F0</th>
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</thead>
<tbody>
<tr>
<td>00</td>
<td>User chr 0</td>
<td>0@P`RÆE – 3QP</td>
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<tr>
<td>01</td>
<td>User chr 1</td>
<td>1!AQa<em>g</em>#*7p4ã</td>
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<td>02</td>
<td>User chr 2</td>
<td>2BRbrÆ£&quot;Yw`p8</td>
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<tr>
<td>03</td>
<td>User chr 3</td>
<td>#3Cs6CsâNwT3s</td>
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<td>04</td>
<td>User chr 4</td>
<td>$4Dtta]%·IwR</td>
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<td>05</td>
<td>User chr 5</td>
<td>%5EUeuEo·o+16w</td>
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<td>User chr 6</td>
<td>86Fvuo3ano3P</td>
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<td>07</td>
<td>User chr 7</td>
<td>7GW9w34Ftr9G</td>
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<td>08</td>
<td>User chr 0</td>
<td>(8Hxhx@i4)heuJx</td>
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<td>(9Iyiy@5j3j</td>
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<td>0A</td>
<td>User chr 2</td>
<td>c*Jzjzu4e[</td>
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<td>0B</td>
<td>User chr 3</td>
<td>+KkCk&lt;3</td>
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<td>Upper 4-bit (D4 to D7) of Character Code (Hexadecimal)</td>
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**Figure B3:** QTP 24P-GF2, GF4 Characters Table with Minifont Graphic Mode
FIGURE B4: QTP 24P-GF2, GF4 CHARACTERS TABLE WITH KATAKANA GRAPHIC FONT
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**Figure B5: QTP 24P-GF2,GF4 Characters Table with European Graphic Font**
APPENDIX C: ON BOARDS COMPONENTS DESCRIPTION

grifo® provides a free technical documentation service through its manuals and/or web site, where on board components data sheet can be found. In this chapter are reported the information about display management.

DISPLAY

PAGE 1 (LMC-SSC2A20-01 Serial)

1. Mechanical Specification

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LMC-SSC2A20DRG-01 STN, Gray, 1/16 Duty, 6 O’clock
LMC-SSC2A20DRY-01 STN, Yellow Green, 1/16 Duty, 6 O’clock
LMC-SSC2A20DEGB-01 STN, Gray, 1/16 Duty, 6 O’clock, EL Backlight (color is Blue)
LMC-SSC2A20DEYW-01 STN, Yellow Green, 1/16 Duty, 6 O’clock, EL Backlight (color is White)
LMC-SSC2A20DELY-01 STN, Gray, 1/16 Duty, 6 O’clock, LED Backlight
LMC-SSC2A20DELY-01 STN, Yellow Green, 1/16 Duty, 6 O’clock, LED Backlight

EL Use Inverter Type: SDEC-I002A
Inverter Input: DC +5V V 40 mA
Inverter Output: AC 90 ~ 110 V 400 ~ 700 Hz
Backlight Half-Lift Time: 3,000 HR.
LED Backlight Color: Yellow Green
Backlight Input: DC +5.0 V V 140 mA
Backlight Half-Lift Time: 50,000 HR.

2. Mechanical Diagram

3. Interface Pin Connections

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<td>VO</td>
<td>H/L</td>
<td>Contrast Adjust</td>
</tr>
<tr>
<td>4</td>
<td>R/S</td>
<td>H/L</td>
<td>Register select</td>
</tr>
<tr>
<td>5</td>
<td>R/W</td>
<td>H/L</td>
<td>Read/Write</td>
</tr>
<tr>
<td>6</td>
<td>E</td>
<td>H,H→L</td>
<td>Enable signal</td>
</tr>
<tr>
<td>7</td>
<td>DB0</td>
<td>H/L</td>
<td>Data Bit 0</td>
</tr>
<tr>
<td>8</td>
<td>DB1</td>
<td>H/L</td>
<td>Data Bit 1</td>
</tr>
<tr>
<td>9</td>
<td>DB2</td>
<td>H/L</td>
<td>Data Bit 2</td>
</tr>
<tr>
<td>10</td>
<td>DB3</td>
<td>H/L</td>
<td>Data Bit 3</td>
</tr>
<tr>
<td>11</td>
<td>DB4</td>
<td>H/L</td>
<td>Data Bit 4</td>
</tr>
<tr>
<td>12</td>
<td>DB5</td>
<td>H/L</td>
<td>Data Bit 5</td>
</tr>
<tr>
<td>13</td>
<td>DB6</td>
<td>H/L</td>
<td>Data Bit 6</td>
</tr>
<tr>
<td>14</td>
<td>DB7</td>
<td>H/L</td>
<td>Data Bit 7</td>
</tr>
<tr>
<td>15</td>
<td>A/+</td>
<td>DC+5V</td>
<td>LED Backlight +</td>
</tr>
<tr>
<td>16</td>
<td>K/+</td>
<td>0V</td>
<td>LED Backlight -</td>
</tr>
</tbody>
</table>

4. Black Diagram
### 7. Functional Descriptions

#### 7.1 Instruction Table

<table>
<thead>
<tr>
<th>Instruction</th>
<th>CODE</th>
<th>Cycle Time</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Display clear</td>
<td></td>
<td>2.3 ms Max.</td>
<td>Clears all display and sets DD RAM address 0 in the address counter.</td>
</tr>
<tr>
<td>Cursor home</td>
<td></td>
<td>1CYC</td>
<td>Sets DD RAM address 0 in the address counter. Also returns the display being shifted to the original position. DD RAM contents remain unchanged.</td>
</tr>
<tr>
<td>Entry mode set</td>
<td></td>
<td>1CYC</td>
<td>Sets the cursor direction and specifies display shift. These operations are performed during writing/reading data.</td>
</tr>
<tr>
<td>Display ON/OFF control</td>
<td></td>
<td>1CYC</td>
<td>Sets all display ON/OFF(0), cursor ON/OFF(0), cursor blink of character position (B).</td>
</tr>
<tr>
<td>Cursor or display shift</td>
<td></td>
<td>1CYC</td>
<td>Shifts display or cursor, keeping DD RAM contents.</td>
</tr>
<tr>
<td>Function set</td>
<td></td>
<td>1CYC</td>
<td>Sets data length (1F).</td>
</tr>
<tr>
<td>Brightness control</td>
<td></td>
<td>1CYC</td>
<td>Accepts 1 byte data of just after &quot;Function set&quot; as brightness control data.</td>
</tr>
</tbody>
</table>

#### CODE

<table>
<thead>
<tr>
<th>Instruction</th>
<th>RS</th>
<th>RW</th>
<th>DB7</th>
<th>DB6</th>
<th>DB5</th>
<th>DB4</th>
<th>DB3</th>
<th>DB2</th>
<th>DB1</th>
<th>DB0</th>
<th>Time</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CG RAM</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1CYC</td>
<td>Sets the CG RAM address.</td>
</tr>
<tr>
<td>RAM address</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1CYC</td>
<td>Sets the DD RAM address.</td>
</tr>
<tr>
<td>Busy flag</td>
<td>0</td>
<td>1</td>
<td>BF</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1CYC</td>
<td>Reads busy flag (BF) and address counter.</td>
</tr>
<tr>
<td>&amp; address reading</td>
<td>1</td>
<td>0</td>
<td>Data writing</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1CYC</td>
<td>Writes data into CG RAM or DD RAM.</td>
</tr>
<tr>
<td>Data reading from CG or DD RAM</td>
<td>1</td>
<td>1</td>
<td>Data reading</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1CYC</td>
<td>Reads data from CG RAM or DD RAM.</td>
</tr>
</tbody>
</table>

**Note:**
- *: don't care
- CYC: 1CYC is read/write cycle (Min. us) of HOST SYSTEM.
- (): IF RAM read, it is a next operation, needs execution time indicated by ‘(1)’. 

---

[Image] ITALIAN TECHNOLOGY
7.2 Display Clear

This instruction clears all locations in the display data (DD) RAM with 20H (Blank character).
2. Clears the contents of the address counter to 0H.
3. Sets the display counter to zero character shift.
4. Sets the address counter to point to the DD RAM.
5. If the cursor is displayed, moves the cursor to the leftmost character in the top line (line 1).
6. Sets the address counter to increment on each access of DD RAM or CG RAM.

7.3 Cursor Home

This instruction:
1. Clears the contents of the address counter to 0H.
2. Sets the address counter to point to the DDRAM.
3. Sets the display for zero character shift.
4. If the cursor is displayed, moves the leftmost character in the top line (line 1).

7.4 Entry Mode Set

The ID bit selects the way in which the contents of the address counter are modified after a write to DDRAM or CGRAM.
ID=1: The address counter is incremented.
ID=0: The address counter is decremented.

The S bit enables display shift, instead of cursor shift, after each write to or read from the DDRAM.
S=1: Display shift enabled.
S=0: Cursor shift enabled.

The direction in which the display is shifted is opposite in sense to that of the cursor. For example if S=0 and ID=1, the cursor would shift one character to the right after a CPU writes to DD RAM. However if S=1 and ID=1, the display would shift one character to the left and the cursor would maintain its position on the panel.

The cursor will already be shifted in the direction selected by ID during reads of the DD RAM, irrespective of the value of S. Similarly reading and writing the CG RAM always shifts the cursor. Also both lines are shifted simultaneously.

Cursor move and display shift by the "Entry Mode Set"

<table>
<thead>
<tr>
<th>I/D</th>
<th>S</th>
<th>After writing DD RAM data</th>
<th>After reading DD RAM data</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>The cursor moves one character to the left.</td>
<td>The cursor moves one character to the left.</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>The cursor moves one character to the right.</td>
<td>The cursor moves one character to the right.</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>The display shifts one character to the right, without cursor's move.</td>
<td>The cursor moves one character to the right.</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>The display shifts one character to the left, without cursor's move.</td>
<td>The cursor moves one character to the left.</td>
</tr>
</tbody>
</table>

7.5 Display ON/OFF

The D bit turns the entire display on or off.
D=1: Display on
D=0: Display off
Note: When display is turned off, power converter is inhibited and reduce a power consumption.

The C bit turns the cursor on or off.
C=1: Cursor on
C=0: Cursor off

The B bit enables blinking of the character the cursor coincides with.
B=1: Blinking on
B=0: Blinking off

Blinking is achieved by alternating between a normal and all on display of a character. The cursor blinks with a frequency of about 1.1 Hz and DUTY 50%.
7.6 Cursor/Display Shift

DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0

\[ \begin{array}{ccccccc}
0 & 0 & 0 & 1 & S/C & R/L & * \\
10H & \rightarrow & 1FH
\end{array} \]

RS=0  
*: don't care

This instruction shifts the display and/or moves the cursor, on character to the left or right, without reading or writing DD RAM. The S/C bit selects movement of the cursor or movement of both the cursor and the display.

S/C = 1: Shift both cursor and display

S/C = 0: Shift cursor only

The R/L bit selects leftward or rightward movement of the display and/or cursor.

R/L = 1: Shift one character right

R/L = 0: Shift one character left

Cursor move and Display shift by the "Cursor/Display Shift"

<table>
<thead>
<tr>
<th>S/C</th>
<th>R/L</th>
<th>Cursor shift</th>
<th>Display shift</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Move one character to the left</td>
<td>No shift</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Move one character to the right</td>
<td>No shift</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Shift one character to left with display</td>
<td>Shift one character to the left</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Shift one character to right with display</td>
<td>Shift one character to the right</td>
</tr>
</tbody>
</table>

7.7 Function Set

This command sets width of data bus line by itself, and sets screen brightness by following one byte data.

7.7.1 Function Set Command

DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0

\[ \begin{array}{ccccccc}
0 & 0 & 1 & IF & * & * & * \\
20H & \rightarrow & 3FH
\end{array} \]

*: don't care

This instruction initializes the system, and must be the first instruction executed after power-on. The IF bit selects between an 8-bit or a 4-bit bus width interface.

IF = 1: 8-bit CPU interface using DB7 to DB0

IF = 0: 4-bit CPU interface using DB7 to DB4

7.7.2 Brightness Control

DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0

\[ \begin{array}{ccccccc}
* & * & * & * & * & * & * \\
RS=1
\end{array} \]

*: don't care

One byte data (RS = 1) which follows the 'Function Set Command' is considered as brightness data. When a command (RS=0) is written after the 'Function Set Command', the brightness control function is not initiated. Screen brightness is as follows:

<table>
<thead>
<tr>
<th>BR1</th>
<th>BR0</th>
<th>Brightness</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>100% (Default)</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>75%</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>50%</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>25%</td>
</tr>
</tbody>
</table>

7.8 Set CG RAM Address

DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0

\[ \begin{array}{ccccccc}
0 & 0 & 1 & ACG \\
40H & \rightarrow & 7FH
\end{array} \]

RS=0

This instruction:
1. Loads a new 8-bit address into the address counter.
2. Sets the address counter to address CG RAM.

Once 'Set CG RAM Address' has been executed, the contents of the address counter will be automatically modified after every access of CG RAM, as determined by the '7.4 Entry Mode Set' instruction. The active width of the address counter, when it is addressing CG RAM, is 6-bits so the counter will wrap around to 00H from 3FH if more than 64 bytes of data are written to CG RAM.

7.9 Set DD RAM Address

DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0

\[ \begin{array}{ccccccc}
1 & ADD \\
80H & \rightarrow & A7H(1 line)
\end{array} \]

RS=0

This instruction:
1. Loads a new 7-bit address into the address counter.
2. Sets the address counter to point to the DD RAM.
Once the "Set DD RAM Address" instruction has been executed, the contents of the address counter will be automatically modified after each access of DD RAM, as selected by the "7.4 Entry Mode Set" instruction.

Valid DDRAM Address Ranges

<table>
<thead>
<tr>
<th>Number of Characters</th>
<th>ADR</th>
</tr>
</thead>
<tbody>
<tr>
<td>1st line</td>
<td>40</td>
</tr>
<tr>
<td>2nd line</td>
<td>40</td>
</tr>
</tbody>
</table>

7.10 Write Data

<table>
<thead>
<tr>
<th>DATA WRITE</th>
<th>00H to FFH</th>
</tr>
</thead>
<tbody>
<tr>
<td>RS=1</td>
<td></td>
</tr>
</tbody>
</table>

This instruction writes the data in DB7 to DB0 into either the CG RAM or the DD RAM. The RAM space (CG or DD), and the address in that space, that is accessed depends on whether a "Set CG RAM Address" or a "Set DD RAM Address" instruction was last executed, and on the parameters of that instruction. The contents of the address counter will be automatically modified after each "Write Data", as determined by the "7.4 Entry Mode Set". When data is written to the CG RAM, the DB7, DB6 and DB5 bits are not displayed as characters.

7.11 Read Data

<table>
<thead>
<tr>
<th>DATA READ</th>
</tr>
</thead>
<tbody>
<tr>
<td>RS=1</td>
</tr>
</tbody>
</table>

This instruction reads data from either CG RAM or DD RAM, depending on the type of "Set RAM Address" instructions last sent. The address in that space depends on the "Set RAM Address" instructions parameters. Immediately before executing "Read Data", "Set CG RAM Address" or "Set DD RAM Address" must be executed. The contents of the address counter are modified after each "Read Data", as determined by the "7.4 Entry Mode Set". Display shift is not executed, as described at the "7.4 Entry Mode Set".

7.12 Read Busy Flag/Address Counter

<table>
<thead>
<tr>
<th>BF</th>
<th>ACC</th>
</tr>
</thead>
<tbody>
<tr>
<td>RS=0</td>
<td></td>
</tr>
</tbody>
</table>

Reading the instruction register yields the current value of the address counter and the

### CG RAM

<table>
<thead>
<tr>
<th>Character code</th>
<th>CG RAM address</th>
<th>CG RAM data (character pattern)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0</td>
<td>DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0</td>
</tr>
<tr>
<td>00H or (0BH)</td>
<td>0 0 0 0 0 0 * * *</td>
<td>1 2 3 4 5</td>
</tr>
<tr>
<td></td>
<td>0 0 0 0 0 1 * * *</td>
<td>6 7 8 9 10</td>
</tr>
<tr>
<td></td>
<td>0 0 0 0 1 0 * * *</td>
<td>11 12 13 14 15</td>
</tr>
<tr>
<td></td>
<td>0 0 0 1 1 1 * * *</td>
<td>16 17 18 19 20</td>
</tr>
<tr>
<td></td>
<td>0 0 1 0 0 0 * * *</td>
<td>21 22 23 24 25</td>
</tr>
<tr>
<td></td>
<td>0 0 1 0 1 0 * * *</td>
<td>26 27 28 29 30</td>
</tr>
<tr>
<td></td>
<td>0 0 1 1 1 0 * * *</td>
<td>31 32 33 34 35</td>
</tr>
<tr>
<td></td>
<td>0 0 1 1 1 1 * * *</td>
<td>36 0 0 0 0</td>
</tr>
<tr>
<td>01H or (0BH)</td>
<td>0 0 1 0 0 0 * * *</td>
<td>1 2 3 4 5</td>
</tr>
<tr>
<td></td>
<td>0 0 1 0 0 1 * * *</td>
<td>6 7 8 9 10</td>
</tr>
<tr>
<td></td>
<td>0 0 1 0 1 0 * * *</td>
<td>11 12 13 14 15</td>
</tr>
<tr>
<td></td>
<td>0 0 1 0 1 1 * * *</td>
<td>16 17 18 19 20</td>
</tr>
<tr>
<td></td>
<td>0 0 1 1 0 0 * * *</td>
<td>21 22 23 24 25</td>
</tr>
<tr>
<td></td>
<td>0 0 1 1 0 1 * * *</td>
<td>26 27 28 29 30</td>
</tr>
<tr>
<td></td>
<td>0 0 1 1 1 0 * * *</td>
<td>31 32 33 34 35</td>
</tr>
<tr>
<td></td>
<td>0 0 1 1 1 1 * * *</td>
<td>36 0 0 0 0</td>
</tr>
</tbody>
</table>

### REMARKS

*: Don't care  "O": Turned off  "1": Turned on.
Relationship between character code (DDR AM) and character pattern (CGRAM)

<table>
<thead>
<tr>
<th>DDR AM</th>
<th>CGRAM</th>
<th>DDR AM</th>
<th>CGRAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>3</td>
<td>3</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>4</td>
<td>4</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>5</td>
<td>5</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>6</td>
<td>6</td>
<td>6</td>
<td>6</td>
</tr>
<tr>
<td>7</td>
<td>7</td>
<td>7</td>
<td>7</td>
</tr>
<tr>
<td>8</td>
<td>8</td>
<td>8</td>
<td>8</td>
</tr>
<tr>
<td>9</td>
<td>9</td>
<td>9</td>
<td>9</td>
</tr>
</tbody>
</table>

8.2 Power-on reset

- Internal status of the module is initialized, when controller detects rising power supply.

1. Display-clear RAM with 0000 (Square code)
2. Set the address counter to 00
3. During execution of *Display Clear* function (Max. 10 internal clock), the busy flag (BF) is 1
4. Error Mode Set
5. No display shut
6. Brightness 0% - 100%
7. 8-bit interface

*Remarks:
- The bus interface might not work by slow start power supply causes.
- Therefore the initializing by commands needs.
1. Initialization of LCM

The LCM automatically initializes (reset) when power is turned on using the internal reset circuit. If the power supply conditions for correctly operating of the internal reset circuit are not met, initialization by instruction is required. Use the procedure in next page for initialization.

Internal Power Supply reset

- Vcc
- Vdd
- toff
- trcc

(Note 1) 10 ms
(Note 2) toff stipulates the time of power OFF for momentary power supply dip or when power supply cycles ON and OFF.

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Test condition</th>
<th>Limit (Min.)</th>
<th>Limit (Max.)</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power supply rise time</td>
<td>trcc</td>
<td>--</td>
<td>0.1</td>
<td>10</td>
<td>ms</td>
</tr>
<tr>
<td>Power supply off time</td>
<td>toff</td>
<td>--</td>
<td>1</td>
<td>100</td>
<td>µs</td>
</tr>
</tbody>
</table>

(Note 1) 10 ms
(Note 2) toff stipulates the time of power OFF for momentary power supply dip or when power supply cycles ON and OFF.

- Power supply rise time
- Power supply off time

- Busy flag can't be checked.

- Function set : 8 bits
- Function set : 4 bits

- Data Set-Up Time (RS, R/W, E )
- Data Set-Up Time

10. Characters addresses

<table>
<thead>
<tr>
<th>Page</th>
<th>Symbol</th>
<th>Limit (Min.)</th>
<th>Limit (Max.)</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>RS</td>
<td>10</td>
<td>100</td>
<td>µs</td>
</tr>
<tr>
<td>2</td>
<td>R/W</td>
<td>100</td>
<td>250</td>
<td>µs</td>
</tr>
<tr>
<td>3</td>
<td>Address Set-Up Time (RS, R/W, E )</td>
<td>100</td>
<td>250</td>
<td>µs</td>
</tr>
<tr>
<td>4</td>
<td>Data Set-Up Time</td>
<td>100</td>
<td>250</td>
<td>µs</td>
</tr>
</tbody>
</table>

11. Timing Control

11.1 Write and Read Operation

Read Operation

- Enable Cycle Time
- Enable Rise Fall Time
- Address Set-Up Time (RS, R/W, E )
- Data Hold Time

11.2 Busy flag check timing

* Busy flag is checked after instructions are completed. If busy flag isn’t checked, the waiting time between instructions should be longer than execution time of these instructions.
IMPORTANT PRECAUTIONS

* All VFD Modules contain MOS LSI. Anti-Static handling procedures are always required.
  Tools required for assembly, such as soldering irons, must be properly grounded.

* VF Display consists of Soda-lime glass. Heavy shock more than 100G, thermal shock
  greater than 10°C/minute, direct hit with hard material to the glass surface --especially to
  the EXHAUST PIPE -- may CRACK the glass.

* Do not PUSH the display strongly. At mounting to the system frame, slight gap between
  display glass face and front panel is necessary to avoid a contact failure of lead pins of
  display. Twisting or warp mounting will make a glass CRACK around the lead pin of display.

* Neither DATA CONNECTOR or POWER CONNECTOR should be connected or
  disconnected while power is applied. As is often the case with most subsystems, caution
  should be exercised in selectively disconnecting power within a computer based system.
  The modules receive high logic on strobe lines as random signals on all data ports.
  Removal of primary power with logic signals applied may damage input circuitry.

* Stress more than specification listed under the Absolute Maximum Ratings may cause
  PERMANENT DAMAGE of the modules.

* +5 volts power line must be regulated completely since all control logics depend on this
  line. Do not apply slow-start power. Provide sufficient output current power source to
  avoid trouble of RUSH CURRENT at power on. (At least output current of double figure
  of Icc, listed on the specification of each module, is required.)

* Data cable length between module and host system is recommended within 300 mm to be
  free from a miss-operation caused by noise.

* Do not place the module on the conductive plate just after the power off. Due to big
  capacitors on the module, more than 1 min. of discharging time is required to avoid
  the failure caused by shorting of power line.

* 2 hours pre-running with the test mode operation may help the stability of the brightness
  of the VFD when power was not applied more than 2 months.

* Steady repeating of a fixed (static) message displaying, longer than 5 hours in a day may
  cause the phosphor burn-out problem. An automatic shut down Programming, scrolling
  message using DC2 mode or 2 hours test mode operation during the idling of the host is
  recommended.
LED DISPLAY DRIVER

- 3 1/2 DIGIT LED DRIVER (23 segments)
- CURRENT GENERATOR OUTPUTS (no resistors required)
- CONTINUOUS BRIGHTNESS CONTROL
- SERIAL DATA INPUT
- NO LOAD SIGNAL REQUIRED
- WIDE SUPPLY VOLTAGE OPERATION
- TTL COMPATIBILITY

Applications examples
- MICROPROCESSOR DISPLAYS
- INDUSTRIAL CONTROL INDICATION
- RELAY DRIVER
- INSTRUMENTATION READOUTS

DESCRIPTION
The M5480 is a monolithic MOS integrated circuit produced with a N-channel silicon gate technology. It utilizes the M5451 die packaged in a 28-pin plastic package making it ideal for a 3 1/2 digit display. A single pin controls the LED display brightness by setting a reference current through a variable resistor connected either to VDD or to a separate supply of 13.2V maximum.

The M5480 is a pin-to-pin replacement of the NS MM 5480.

PIN CONNECTIONS

ORDER CODE : M5480B7

May 1993
STATIC ELECTRICAL CHARACTERISTICS

(Tamb within operating range, \(V_{CC} = 4.75\) V to 13.2 V, \(V_{DD} = 0\) V unless otherwise specified)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{CC})</td>
<td>Supply Voltage</td>
<td>(V_{CC} = 13.2) V</td>
<td>7 V</td>
<td>7 mA</td>
<td>7 mA</td>
<td>V</td>
</tr>
<tr>
<td>(V_{IL})</td>
<td>Input Voltages</td>
<td>-10 (\mu) A, Input Bias</td>
<td>-0.3 V</td>
<td>-0.8 V</td>
<td>-0.8 V</td>
<td>V</td>
</tr>
<tr>
<td>(V_{IH})</td>
<td>Input Voltages</td>
<td>+5.25 (\mu) A, Input Bias</td>
<td>2.2 V</td>
<td>2.2 V</td>
<td>2.2 V</td>
<td>V</td>
</tr>
<tr>
<td>(I_{L})</td>
<td>Brightness Input Current (note 2)</td>
<td>Input Current = 750 (\mu) A, (T_{Amb} = -25^\circ) C</td>
<td>0.75 mA</td>
<td>0.75 mA</td>
<td>0.75 mA</td>
<td>mA</td>
</tr>
<tr>
<td>(I_{L})</td>
<td>Brightness Input Voltage (pin 13)</td>
<td>Input Current = 750 (\mu) A, (T_{Amb} = -25^\circ) C</td>
<td>4.3 V</td>
<td>4.3 V</td>
<td>4.3 V</td>
<td>V</td>
</tr>
<tr>
<td>(V_{OUT})</td>
<td>Output State Output Voltage</td>
<td>13.2 V</td>
<td>18 V</td>
<td>18 V</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>(I_{O})</td>
<td>Output Sink Current (note 3)</td>
<td>(V_{O} = 3) V</td>
<td>10 (\mu) A</td>
<td>10 (\mu) A</td>
<td>10 (\mu) A</td>
<td>mA</td>
</tr>
<tr>
<td>(I_{O})</td>
<td>Segment OFF</td>
<td>(V_{O} = 1) V (note 4)</td>
<td>10 (\mu) A</td>
<td>10 (\mu) A</td>
<td>10 (\mu) A</td>
<td>mA</td>
</tr>
<tr>
<td>(I_{O})</td>
<td>Brightness In</td>
<td>Brightness In = 0 mA</td>
<td>0 mA</td>
<td>0 mA</td>
<td>0 mA</td>
<td>mA</td>
</tr>
<tr>
<td>(I_{O})</td>
<td>Brightness In</td>
<td>Brightness In = 100 mA</td>
<td>2 (\mu) A</td>
<td>2 (\mu) A</td>
<td>2 (\mu) A</td>
<td>mA</td>
</tr>
<tr>
<td>(I_{O})</td>
<td>Brightness In</td>
<td>Brightness In = 750 mA</td>
<td>15 (\mu) A</td>
<td>15 (\mu) A</td>
<td>15 (\mu) A</td>
<td>mA</td>
</tr>
<tr>
<td>(f_{O})</td>
<td>Input Clock Frequency</td>
<td>0.5 MHz</td>
<td>0.5 MHz</td>
<td>0.5 MHz</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>(I_{O})</td>
<td>Output Matching (note 1)</td>
<td>(\pm 20%)</td>
<td>(\pm 20%)</td>
<td>(\pm 20%)</td>
<td>%</td>
<td></td>
</tr>
</tbody>
</table>

Notes:
1. Output mismatching is calculated as the percent variation from \(\pm 20\%\).
2. The \(V_{DD}\) voltage should be regulated by the user.

FUNCTIONAL DESCRIPTION

The M5480 is specifically designed to operate 3 1/2 digit alphanumeric displays with minimal interface with the display and the data source. Serial data transfer from the data source to the display driver is accomplished with 2 signals, serial data and clock. Using a format of a leading “1” followed by the 35 data bits allows data transfer without an additional load signal. The 35 data bits are latched after the 36th bit is complete, thus providing non-multiplexed, direct drive to the display. Outputs change only if the serial data bits differ from the previous time.

The display brightness is determined by control of the output current for LED displays. A 1nF capacitor should be connected to brightness control, pin 13, to prevent possible oscillations.

A block diagram is shown in Figure 1. The output current is typically 20 times greater than the current into pin 13, which is set by an external variable resistor.

There is an internal limiting resistor of 400 ohm nominal value.

Figure 2 shows the input data format. A start bit of logical “1” precedes the 35 bits of data. At the 36th clock a LOAD signal is generated synchronously with the high state of the clock, which loads the 35 bits of the shift registers into the latches. At the low state of the clock a RESET signal is generated which clears all the shift registers for the next set of data. The shift registers are static master-slave configurations. There is no clear for the master portion of the first register, thus allowing continuous operation.

Figure 3 shows the timing relationships between Data, and Clock. A maximum clock frequency of 0.5 MHz is assumed.

Figure 4 shows the Output Data Format for the M5480. Because it uses only 2 of the possible 35 outputs, 12 of the bits are “Don’t Care.”

For applications where a lesser number of outputs are used, it is possible to increase the current per output, or operate the part at higher than 132°C/W.

The following equation can be used for calculations:

\[ T_{J} = \left( V_{OUT} \right) \left( \text{VDD} \right) / T_{A} \]

where:

- \( T_J \) = junction temperature (150°C max)
- \( V_{OUT} \) = the voltage at the LED driver outputs
- \( L_{LED} \) = the LED current
- 132°C/W = thermal coefficient of the package
- \( T_{A} \) = ambient temperature

TYPICAL APPLICATION

BASIC 3 1/2 Digit Interface.

In this application R must be chosen taking into account the worst operating conditions. R is determined by the maximum number of segments activated.

\[ R = \frac{V_{CC} - V_{MAX} - V_{OUT} \text{MIN}}{N_{MAX} \cdot I_{O}} \]
APPENDIX D: QTP 24P LABELS INSERTION

Operator panels QTP 24P feature several personalization labels, where the user can show one's logo and the functions of keys and LEDs, for the specific application. Here follows the operations to perform to insert the labels.

LABELS INSERTION QTP 24P

The operations to perform to insert the personalization labels in the operator panel QTP 24P are:

1) Unscrew the four black screws from the front panel.
2) Take the panel out.
3) Unscrew the eight screw and their plastic spacers which are places in the back.
4) Separate the set keyboard+printed circuit and the black plastic frame.
5) Now the keyboard is ready for getting the five personalization labels, as shown in the image.
6) Remount QTP 24P, following the previous instructions but on the back-way.

Figure D1: Labels insertion in QTP 24P
APPENDIX E: ALPHABETICAL INDEX

A
ALPHANUMERIC  6, 24
APPLICATIONS  4

B
BACKLIGH  6
BACKLIGHT  19, 22
BASIC LANGUAGE  26
BIBLIOGRAPHY  32
BLOCKS DIAGRAM  5

C
C LANGUAGE  26
COLUMN  14, 28
COMMANDS  30
COMPONENTS MAP  17
CONNECTIONS  12, 31
CONNECTORS  8
  CN1  12
  CN2  14
  CN3  16
  CN4  18
  CN5  20
  CN6  22
CONSOLE  26
CONSUMPTION  9, 10, 11
CONTRAST REGULATION  25
CONTROL SIGNALS  19, 20, 22, 30
CURRENT  10

D
DATA BUS  19, 20, 22, 30
DEFAULT  24
DIMENSION  8
DISPLAY  6, 10, 18, 20, 22, 24, 30, 32
DRIVERS  26

E
ELECTRIC FEATURES  10
F
FEATURES
   ELECTRIC  10
   GENERAL  8
   PHYSICAL  8
   TECHNICAL  8
FIRMWARE  26
FUTABA  30

G
GENERAL FEATURES  8
GENERAL INFORMATION  4
GRAPHIC  6, 24

H
HIGH LEVEL  26
HUMIDITY  8

I
I/O ABACO®  16
I/O CONNECTION  25
I/O LINES  16, 28
INITIALIZATION  30
INSTALLATION  12

J
J1  24
JUMPERS  24

K
KEYBOARD  6, 14, 28

L
LCD  6, 10, 18, 22, 25, 32
LENGTH OF CONNECTIONS  25
LIBRARIES  26
LOW LEVEL  28

M
MATRIX KEYBOARD  6, 14, 28
MODELS  4
MOUNTING  8
P
PASCAL LANGUAGE 26
PHYSICAL FEATURES 8
PORT 16, 30
POWER CONSUMPTION 10
POWER SUPPLY 12, 16, 24, 25
POWER VOLTAGE 10
PRINTED CIRCUIT 3

R
RESOURCES 8
ROW 14, 28
RV1 25

S
SIZE 8
SOFTWARE 26

T
TECHNICAL FEATURES 8
TEMPERATURE 8
TRIMMER 25
TTL 16, 25, 32

V
VERSION 3
VFD 6, 10, 18, 20, 22

W
WEIGHT 8