PIO 01
Peripheral Input Output TTL

TECHNICAL MANUAL
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Standard Eurocard format 100x160 mm; interface to ABACO® Industrial BUS; 96 TTL I/O signals; twelve 8 signals parallel ports managed by four PPI 82C55; 6 standard ABACO® I/O 20 pins connectors; watch dog circuitry capable to work in astable and monostable mode and intervent time settable between 1 msec and 16,50 sec through jumper and trimmer; LED to signal watch dog circuitry activation; wait circuitry to introduce 3, 5 or 8 wait cycles in I/O operations; selection of I/O mapping through 2 dip switches on board; addressing space taken as low as 16 contiguous bytes; management of address BUS 8 or 16÷20 bits wide, selectable through jumpers; direct interface to the field modules type FBC, OBI, RBO, TBO or XBI; direct interface to the parallel operator panels QTP 24P and QTP 16P; unique power supply +5Vdc
IMPORTANT

Although all the information contained herein have been carefully verified, grifo\textsuperscript{®} assumes no responsability for errors that might appear in this document, or for damage to things or persons resulting from technical errors, omission and improper use of this manual and of the related software and hardware. grifo\textsuperscript{®} reserves the right to change the contents and form of this document, as well as the features and specification of its products at any time, without prior notice, to obtain always the best product.

For specific informations on the components mounted on the card, please refer to the Data Book of the builder or second sources.

SYMBOLS DESCRIPTION

In the manual could appear the following symbols:

![Attention symbol] Attention: Generic danger

![Attention symbol] Attention: High voltage

Trade Marks

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Other Product and Company names listed, are trade marks of their respective companies.
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INTRODUCTION

The use of these devices has turned - IN EXCLUSIVE WAY - to specialized personnel.

The purpose of this handbook is to give the necessary information to the cognizant and sure use of the products. They are the result of a continual and systematic elaboration of data and technical tests saved and validated from the manufacturer, related to the inside modes of certainty and quality of the information.

The reported data are destined- IN EXCLUSIVE WAY- to specialized users, that can interact with the devices in safety conditions for the persons, for the machine and for the enviroment, impersonating an elementary diagnostic of breakdowns and of malfunction conditions by performing simple functional verify operations, in the height respect of the actual safety and health norms.

The informations for the installation, the assemblage, the dismantlement, the handling, the adjustment, the reparation and the contingent accessories, devices etc. installation are destined - and then executable - always and in exclusive way from specialized warned and educated personnel, or directly from the TECHNICAL AUTHORIZED ASSISTANCE, in the height respect of the manufacturer recommendations and the actual safety and health norms.

The devices can't be used outside a box. The user must always insert the cards in a container that respect the actual safety normative. The protection of this container is not threshold to the only atmospheric agents, but specially to mechanic, electric, magnetic, etc. ones.

To be on good terms with the products, is necessary guarantee legibility and conservation of the manual, also for future references. In case of deterioration or more easily for technical updates, consult the AUTHORIZED TECHNICAL ASSISTANCE directly.

To prevent problems during card utilization, it is a good practice to read carefully all the informations of this manual. After this reading, the user can use the general index and the alphabetical index, respectly at the begining and at the end of the manual, to find information in a faster and more easy way.

CARD VERSION

This handbook makes reference to boards version 030392 and following ones. The validity of the information contained in this manual is subordinated to the card version, so the user must always verify the correct correspondence between the notations. On the card the release number is present in more points both on printed diagram (serigraph) and printed circuit (for example near connector CN3 on the component side).
PIO 01 (Peripheral Input Output TTL) is a powerful peripheral card featuring the standard Eurocard format and interface to ABACO® industrial BUS. This digital peripheral card implements 96 TTL I/O lines and can be driven through one of the numerous GPC® serie intelligent cards produced by grifo®.

On board are installed four section each of which manages 24 TTL I/O lines, such lines are available on six comfortable standard ABACO® I/O 20 pins connectors.

The on board hardware provides TTL I/O lines; should the user need a different modality of interfacement then he/she can take advantage of a complete serie of signals adaptation modules, such the RBO, TBO, OBI or XBI series modules. These BLOCK family modules can realize most of the common interfacement combinations used in industrial environment.

The intelligent control board (GPC® serie) is charged with setting the employ mode of all the lines so it must decide also their directionality. To read the inputs and to set the outputs it is enough to perform simple read and write operations to bytes.

The 96 I/O lines can be managed simply as parallel ports or can be programmed to work in more sophisticated ways. The four PPI 82C55, that perform the hardware management of the lines, can be programmed to work in many different modalities, allowing the user to deal with several kinds of problematics.

The board also features a Watch Dog circuitry which can reach the intelligent control board directly through the ABACO® BUS. An opportune management of this section allows to increase the security of all the system.

When a Power-On or a Reset occurs PIO 01, by means of a specific cirucitry, configures all the 96 lines as inputs, to warrant the absence of uncertainty about the initial status.

The board takes only 16 bytes of addressing space and can operate on a BUS that features 8 or 16÷20 bits of address word; configuration is made through comfortable jumers.

PIO 01 is the ideal component to employ for all the system automation problems where it is required to manage a high number of logical inputs and outputs or wherever a very high number of TTL lines is needed.

Overall features of PIO 01 are:

- Standard Eurocard format 100x160 mm
- Interface to ABACO® Industrial BUS
- 96 TTL I/O signals
- Twelve 8 signals parallel ports managed by four PPI 82C55
- 6 standard ABACO® I/O 20 pins connectors
- Watch dog circuitry capable to work in astable and monostable mode and intervent time settable between 1 msec and 16,50 sec through jumper and trimmer
- LED to signal watch dog circuitry activation
- Wait circuitry to introduce 3, 5 or 8 wait cycles in I/O operations
- Selection of I/O mapping through 2 dip switches on board
- Addressing space taken as low as 16 contiguous bytes
- Management of address BUS 8 or 16÷20 bits wide, selectable through jumpers
- Direct interface to the field modules type FBC, OBI, RBO, TBO or XBI
- Direct interface to the parallel operator panels QTP 24P and QTP 16P
- Unique power supply +5Vdc
FIGURE 1: BLOCK DIAGRAM

K1 - ABACO® BUS

INTERFACE AND ADDRESSING SECTION

8 or 16÷20 bit Address BUS

DIP1

DIP2

CONTROL LOGIC

WATCH DOG

WAIT STATES GENERATOR

PPI 82C55 1

PPI 82C55 2

PPI 82C55 3

PPI 82C55 4

CN5

CN1

CN3

CN6

CN2

CN4

FIGURE 1: BLOCK DIAGRAM
Here follows a description of the board's functional blocks, with an indication of the operations performed by each one.
To easily locate the blocks and their interconnection please refer to figure 1.

**ADDRESSING AND INTERFACEMENT**

This section manages the information interchange between control logic and external GPC® control cards through ABACO® BUS. In detail, each byte read or written passes through this section, that also provides the I/O board mapping two dip switchces called DIP1 and DIP2. Please remark that this section can be configured to address PIO 01 in a 256 bytes or 64÷1024 Kbytes I/O addressing range. The ABACO® Industrial BUS interfacement has been designed anticipating an 8 bits data path. For further information please refer to the chapters dedicated to hardware and software description.

**CONTROL LOGIC**

This section generates all the chip select signals essential to access the PIO 01 on board peripherals. It allows the programmer to reach the board devices and check their status, read the digital inputs and outputs, etc.
The control logic interfaces to ABACO® Industrial BUS through the addressing and interfacement section, the BUS connection allows an easy software management of all the sections. For further information please refer to the chapter dedicated to software description.

**WATCH DOG**

PIO 01 is provided with one sophisticated watch dog circuit that acts directly to the ABACO® BUS and can reset the intelligent control card at programmable time intervals, if not retriggered. Watch dog circuit is used when the user wants to exit from endless loops or to reset anomalous conditions not estimated by application program. The watch dog can be astable or monostable, with intervention time selectable between 1msec up to 16.50 sec through jumper and trimmer. By software the user can perform a complete management of the device, using specific registers. This circuitery gives to the board an extremely high degree of safety. For further information please refer to the chapters dedicated to hardware and software description.

**WAIT STATE GENERATOR**

The sophisticated wait state generator installed on PIO 01 intervenes directly to ABACO® BUS and allows to insert a programmable number of wait states whenever PIO 01 performs an I/O operation.
A set of comfortable jumpers allow to decide the configuration of this circuitry (number of wait states and activation or deactivation).
The main purpose of this section is to allow to use PIO 01 also matched with very fast CPU boards, and so to increase its versatility.
TTL I/O LINES

This section, based on four PPI 82C55, manages 96 TTL I/O lines divided in twelve 8 bit parallel ports. The lines direction is software settable at byte or nibble level. The software management is performed through 16 registers that control directly the four devices. The 96 I/O lines are available on six standard ABACO I/O 20 pins connectors for the direct connection to the several modules, provided with the same kind of connector, which allow to manage transistor or relay outputs, optocoupled inputs, operator interface devices like keyboards or displays, printers, etc. The four PPI 82C55 can also be programmed to implement sophisticated parallel high speed data transfer protocols, to connect to systems provided with compatible interfaces.

For further informations about the above described device, please refer to the manufacturer documentations or to appendix B of this manual.
TECHNICAL FEATURES

GENERAL FEATURES

On board resources:
- 96 programmable Input/Output TTL (4 PPI 82C55)
- 1 Watch dog (astable or monostable)
- 1 Wait state generator
- 2 Dip-switches with 8 pins to set I/O address

BUS implemented:
- ABACO® industrial
- 8 bits wide data path.

Bytes of addressing space:
- Selectable between 256 bytes and 64÷1024 Kbytes

Bytes taken:
- 16

Watch dog intervent time:
- Settable between 1 msec and 16.50 sec
- Set to about 1 sec in test phase

Number of wait state insertable:
- Selectable amongst 3, 5 or 8

On board peripherals:
- PPI 82C55

PHYSICAL FEATURES

Size:
- Standard EUROCARD format 100x160 mm

Weight:
- 160 g

Connectors:
- K1: DIN 41612 64 pins M 90° A+C type C
- CN1: Low profile 20 pins vertical M
- CN2: Low profile 20 pins vertical M
- CN3: Low profile 20 pins vertical M
- CN4: Low profile 20 pins vertical M
- CN5: Low profile 20 pins 90° M
- CN6: Low profile 20 pins 90° M

Temperature range:
- from 0°C to 70°C

Relative humidity:
- 20% up to 90% (without condensate)
ELECTRIC FEATURES

Power supply voltage: +5 Vdc ± 5%

Current consumption: 140 mA

Current for TTL lines driving: Max 2,5 mA each line

Voltage level of TTL lines: 0 V (low level); +5 Vdc (high level)

FIGURE 2: COMPONENTS MAP
INSTALLATION

In this chapter there are the information for a right installation and correct use of the board. The user can find the location and functions of each connectors, trimmers, jumpers and some explanatory diagrams.

CONNECTIONS

The board has seven connectors that can be linkeded to other devices or directly to the field, according to system requirements. In this paragraph there are connectors pin outs, a short signals description (including the signals direction) and connectors location, plus some figures that describe how the interface signals are connected on the card.

To easily locate the connectors please refer to figure 6.

CN1 - PORT B OF PPI 82C55 SECTIONS 1 AND 2 CONNECTOR

CN1 is a 20 pins low profile vertical male 2.54 mm pitch connector. On connector CN1 are available the 16 I/O digital lines managed through port B of PPI 82C55 belonging to sections 1 and 2. Any parameter of this device (like signals direction, data management mode, etc.) is completely software definible by programming the device itself. All signals are at TTL level and follow the standard I/O ABACO® pin-out.

<table>
<thead>
<tr>
<th>PPI 2 PB.1</th>
<th>PPI 2 PB.3</th>
<th>PPI 2 PB.5</th>
</tr>
</thead>
<tbody>
<tr>
<td>PPI 2 PB.4</td>
<td>PPI 2 PB.6</td>
<td>PPI 2 PB.7</td>
</tr>
<tr>
<td>PPI 2 PB.2</td>
<td>PPI 2 PB.0</td>
<td>+5 Vdc</td>
</tr>
<tr>
<td>GND</td>
<td>GND</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>PPI 1 PB.1</th>
<th>PPI 1 PB.3</th>
<th>PPI 1 PB.5</th>
</tr>
</thead>
<tbody>
<tr>
<td>PPI 1 PB.7</td>
<td>PPI 1 PB.6</td>
<td></td>
</tr>
<tr>
<td>PPI 1 PB.4</td>
<td>PPI 1 PB.0</td>
<td>N.C.</td>
</tr>
</tbody>
</table>

**FIGURE 3: CN1 - PORT B OF PPI 82C55 SECTIONS 1 AND 2 CONNECTOR**
Signals description:

- **PPI 1 PB.n** = I/O - n-th digital TTL signal of section 1 PPI 82C55 port B
- **PPI 2 PB.n** = I/O - n-th digital TTL signal of section 2 PPI 82C55 port B
- **+5 Vdc** = O - +5 Vdc power supply
- **GND** = - Digital ground
- **N.C.** = - Not connected

**Figure 4: PPI 82C55 sections 1 and 2 block diagram**
CN5 - PORTS A AND C OF PPI 82C55 SECTION 1 CONNECTOR

CN5 is a 20 pins low profile 90° male 2.54 mm pitch connector. On connector CN5 are available the 16 I/O digital lines managed through port A and C of PPI 82C55 belonging to section 1. Any parameter of this device (like signals direction, data management mode, etc.) is completely software definable by programming the device itself. All signals are at TTL level and follow the standard I/O ABACO® pin-out.

**Figure 5: CN5 - Ports A and C of PPI 82C55 section 1 connector**

Signals description:

- **PPI 1 PA.n** = I/O - n-th digital TTL signal of section 1 PPI 82C55 port A
- **PPI 1 PC.n** = I/O - n-th digital TTL signal of section 1 PPI 82C55 port C
- **+5 Vdc** = O - +5 Vdc power supply
- **GND** = - Digital ground
- **N.C.** = - Not connected
Figure 6: Connectors, Dip switches, LED and trimmer locations
CN3 - PORTS A AND C OF PPI 82C55 SECTION 2 CONNECTOR

CN3 is a 20 pins low profile 90° male 2.54 mm pitch connector. On connector CN3 are available the 16 I/O digital lines managed through port A and C of PPI 82C55 belonging to section 2. Any parameter of this device (like signals direction, data management mode, etc.) is completely software definable by programming the device itself. All signals are at TTL level and follow the standard I/O ABACO® pin-out.

FIGURE 7: CN3 - PORTS A AND C OF PPI 82C55 SECTION 2 CONNECTOR

Signals description:

<table>
<thead>
<tr>
<th>PPI 2 PA.n</th>
<th>PPI 2 PC.n</th>
<th>+5 Vdc</th>
<th>GND</th>
<th>N.C.</th>
</tr>
</thead>
<tbody>
<tr>
<td>= I/O - n-th digital TTL signal of section 2 PPI 82C55 port A</td>
<td>= I/O - n-th digital TTL signal of section 2 PPI 82C55 port C</td>
<td>= O - +5 Vdc power supply</td>
<td>= - Digital ground</td>
<td>= - Not connected</td>
</tr>
</tbody>
</table>
Figure 8: Card photo
CN2 - PORT B OF PPI 82C55 SECTIONS 3 AND 4 CONNECTOR

CN2 is a 20 pins low profile vertical male 2.54 mm pitch connector. On connector CN2 are available the 16 I/O digital lines managed through port B of PPI 82C55 belonging to sections 3 and 4. Any parameter of this device (like signals direction, data management mode, etc.) is completely software definable by programming the device itself. All signals are at TTL level and follow the standard I/O ABACO® pin-out.

**Figure 9: CN2 - Port B of PPI 82C55 sections 3 and 4 connector**

Signals description:

- **PPI 3 PB.n** = I/O - n-th digital TTL signal of section 3 PPI 82C55 port B
- **PPI 4 PB.n** = I/O - n-th digital TTL signal of section 4 PPI 82C55 port B
- **+5 Vdc** = 0 - +5 Vdc power supply
- **GND** = Digital ground
- **N.C.** = Not connected
**Figure 10: PPI 82C55 Sections 3 and 4 Block Diagram**
CN6 - PORTS A AND C OF PPI 82C55 SECTION 3 CONNECTOR

CN6 is a 20 pins low profile 90° male 2.54 mm pitch connector. On connector CN6 are available the 16 I/O digital lines managed through port A and C of PPI 82C55 belonging to section 3. Any parameter of this device (like signals direction, data management mode, etc.) is completely software definable by programming the device itself. All signals are at TTL level and follow the standard I/O ABACO® pin-out.

![CN6 - Ports A and C of PPI 82C55 Section 3 Connector](image)

**Figure 11: CN6 - Ports A and C of PPI 82C55 Section 3 Connector**

Signals description:

- **PPI 3 PA.n** = I/O - n-th digital TTL signal of section 3 PPI 82C55 port A
- **PPI 3 PC.n** = I/O - n-th digital TTL signal of section 3 PPI 82C55 port C
- **+5 Vdc** = O - +5 Vdc power supply
- **GND** = - Digital ground
- **N.C.** = - Not connected
CN4 - PORTS A AND C OF PPI 82C55 SECTION 4 CONNECTOR

CN4 is a 20 pins low profile vertical male 2.54 mm pitch connector. On connector CN4 are available the 16 I/O digital lines managed through port A and C of PPI 82C55 belonging to section 4. Any parameter of this device (like signals direction, data management mode, etc.) is completely software definable by programming the device itself. All signals are at TTL level and follow the standard I/O ABACO® pin-out.

**Figure 12: CN4 - Ports A and C of PPI 82C55 Section 4 Connector**

 Signals description:

- **PPI 4 PA.n** = I/O - n-th digital TTL signal of section 4 PPI 82C55 port A
- **PPI 4 PC.n** = I/O - n-th digital TTL signal of section 4 PPI 82C55 port C
- **+5 Vdc** = O - +5 Vdc power supply
- **GND** = - Digital ground
- **N.C.** = - Not connected
**K1 - ABACO® BUS CONNECTOR**

K1 is a 64 pins, male, 90°, DIN 41612 connector with 2.54 pitch. On K1 are available all the industrial **ABACO® BUS signals** and it can be used for connections to many other peripheral cards. In the table below there are the standard pin outs both for 8 bits and 16 bits CPU and the signal connected on **PIO 01**. All signals, except power supplies, are compliant to TTL standard.

<table>
<thead>
<tr>
<th>A 16 bit BUS</th>
<th>A 8 bit BUS</th>
<th>A GPC 150</th>
<th>PIN</th>
<th>C GPC 150</th>
<th>C 8 bit BUS</th>
<th>C 16 bit BUS</th>
</tr>
</thead>
<tbody>
<tr>
<td>GND</td>
<td>GND</td>
<td>GND</td>
<td>1</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
</tr>
<tr>
<td>+5 Vdc</td>
<td>+5 Vdc</td>
<td>+5 Vdc</td>
<td>2</td>
<td>+5 Vdc</td>
<td>+5 Vdc</td>
<td>+5 Vdc</td>
</tr>
<tr>
<td>D0</td>
<td>D0</td>
<td>D0</td>
<td>3</td>
<td>N.C.</td>
<td>D8</td>
<td></td>
</tr>
<tr>
<td>D1</td>
<td>D1</td>
<td>D1</td>
<td>4</td>
<td>N.C.</td>
<td>D9</td>
<td></td>
</tr>
<tr>
<td>D2</td>
<td>D2</td>
<td>D2</td>
<td>5</td>
<td>N.C.</td>
<td>D10</td>
<td></td>
</tr>
<tr>
<td>D3</td>
<td>D3</td>
<td>D3</td>
<td>6</td>
<td>/INT</td>
<td>/INT</td>
<td>/INT</td>
</tr>
<tr>
<td>D4</td>
<td>D4</td>
<td>D4</td>
<td>7</td>
<td>/NMI</td>
<td>/NMI</td>
<td>/NMI</td>
</tr>
<tr>
<td>D5</td>
<td>D5</td>
<td>D5</td>
<td>8</td>
<td>N.C.</td>
<td>/HALT</td>
<td>D11</td>
</tr>
<tr>
<td>D6</td>
<td>D6</td>
<td>D6</td>
<td>9</td>
<td>N.C.</td>
<td>/MREQ</td>
<td>/MREQ</td>
</tr>
<tr>
<td>D7</td>
<td>D7</td>
<td>D7</td>
<td>10</td>
<td>/IORQ</td>
<td>/IORQ</td>
<td>/IORQ</td>
</tr>
<tr>
<td>A0</td>
<td>A0</td>
<td>A0</td>
<td>11</td>
<td>/RD</td>
<td>/RD</td>
<td>/RDLDS</td>
</tr>
<tr>
<td>A1</td>
<td>A1</td>
<td>A1</td>
<td>12</td>
<td>/WR</td>
<td>/WR</td>
<td>/WRLDS</td>
</tr>
<tr>
<td>A2</td>
<td>A2</td>
<td>A2</td>
<td>13</td>
<td>N.C.</td>
<td>/BUSAK</td>
<td>D12</td>
</tr>
<tr>
<td>A3</td>
<td>A3</td>
<td>A3</td>
<td>14</td>
<td>N.C.</td>
<td>/WAIT</td>
<td>/WAIT</td>
</tr>
<tr>
<td>A4</td>
<td>A4</td>
<td>A4</td>
<td>15</td>
<td>N.C.</td>
<td>/BUSRQ</td>
<td>D13</td>
</tr>
<tr>
<td>A5</td>
<td>A5</td>
<td>A5</td>
<td>16</td>
<td>/RESET</td>
<td>/RESET</td>
<td>/RESET</td>
</tr>
<tr>
<td>A6</td>
<td>A6</td>
<td>A6</td>
<td>17</td>
<td>N.C.</td>
<td>/M1</td>
<td>IACK</td>
</tr>
<tr>
<td>A7</td>
<td>A7</td>
<td>A7</td>
<td>18</td>
<td>N.C.</td>
<td>/RFSH</td>
<td>D14</td>
</tr>
<tr>
<td>A8</td>
<td>A8</td>
<td>N.C.</td>
<td>19</td>
<td>N.C.</td>
<td>/MEMDIS</td>
<td>/MEMDIS</td>
</tr>
<tr>
<td>A9</td>
<td>A9</td>
<td>N.C.</td>
<td>20</td>
<td>N.C.</td>
<td>VDUSEL</td>
<td>A22</td>
</tr>
<tr>
<td>A10</td>
<td>A10</td>
<td>N.C.</td>
<td>21</td>
<td>N.C.</td>
<td>/IEI</td>
<td>D15</td>
</tr>
<tr>
<td>A11</td>
<td>A11</td>
<td>N.C.</td>
<td>22</td>
<td>N.C.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>A12</td>
<td>A12</td>
<td>N.C.</td>
<td>23</td>
<td>N.C.</td>
<td>CLK</td>
<td>CLK</td>
</tr>
<tr>
<td>A13</td>
<td>A13</td>
<td>N.C.</td>
<td>24</td>
<td>N.C.</td>
<td>/RDUDS</td>
<td></td>
</tr>
<tr>
<td>A14</td>
<td>A14</td>
<td>N.C.</td>
<td>25</td>
<td>N.C.</td>
<td>/WRUDS</td>
<td></td>
</tr>
<tr>
<td>A15</td>
<td>A15</td>
<td>N.C.</td>
<td>26</td>
<td>N.C.</td>
<td>A21</td>
<td></td>
</tr>
<tr>
<td>A16</td>
<td>N.C.</td>
<td></td>
<td>27</td>
<td>N.C.</td>
<td>A20</td>
<td></td>
</tr>
<tr>
<td>A17</td>
<td>N.C.</td>
<td></td>
<td>28</td>
<td>N.C.</td>
<td>A19</td>
<td></td>
</tr>
<tr>
<td>+12 Vdc</td>
<td>+12 Vdc</td>
<td>N.C.</td>
<td>30</td>
<td>N.C.</td>
<td>-12 Vdc</td>
<td>-12 Vdc</td>
</tr>
<tr>
<td>+5 Vdc</td>
<td>+5 Vdc</td>
<td>+5 Vdc</td>
<td>31</td>
<td>+5 Vdc</td>
<td>+5 Vdc</td>
<td>+5 Vdc</td>
</tr>
<tr>
<td>GND</td>
<td>GND</td>
<td>GND</td>
<td>32</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
</tr>
</tbody>
</table>

**Figure 13: K1 - ABACO® BUS Connector**
Signals description:

8 bits CPU

A0-A15 = O - Address BUS  
D0-D7 = I/O - Data BUS  
/INT = I - Interrupt request  
/NMI = I - Non Maskable Interrupt  
/HALT = O - Halt state  
/MREQ = O - Memory Request  
/IORQ = O - Input Output Request  
/RD = O - Read cycle status  
/WR = O - Write cycle status  
/BUSAK = O - BUS Acknowledge  
/WAIT = I - Wait  
/BUSRQ = I - BUS Request  
/RESET = O - Reset  
/M1 = O - Machine cycle one  
/RFSH = O - Refresh for dynamic RAM  
/MEMDIS = I - Memory Display  
/VDUSEL = O - VDU Selection  
/IEI = I - Interrupt Enable Input  
/CLK = O - System clock  
/R.B. = I - Reset button  
/+5 Vdc = I - Power supply at +5 Vdc  
/+12 Vdc = I - Power supply at +12 Vdc  
/-12 Vdc = I - Power supply at -12 Vdc  
/GND = - Ground signal

16 bits CPU

A16-A22 = O - Address BUS  
D8-D15 = I/O - Data BUS  
RD UDS = O - Read Upper Data Strobe  
WR UDS = O - Write Upper Data Strobe  
IACK = O - Interrupt Acknowledge  
RD LDS = O - Read Lower Data Strobe  
WR LDS = O - Write Lower Data Strobe

NOTE
Directionality indications as above stated are referred to a master (GPC®) board and have been kept untouched to avoid ambiguity in case of multi-boards systems.
VISUAL FEEDBACK

PIO 01 board is provided with one LED to signal status conditions, as described in the following table:

<table>
<thead>
<tr>
<th>LED</th>
<th>COLOUR</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>LD1</td>
<td>Red</td>
<td>Indicates the watch dog circuitry activation.</td>
</tr>
</tbody>
</table>

*Figure 14: Visual feedback table*

The main purpose of this LED is to give a visual indication of the board status, making easier the operations of system working verify. To easily locate this LED on the board, please refer to figure 6.

POWER SUPPLY

PIO 01 is provided with an efficient circuitry that solves in a comfortable and simple way the problem of the board's supply, under any condition of use. Here follow the voltages needed:

+5 Vdc: Supplies the on board logic; must be in the range +5 Vdc ± 5% and must be provided through the specific pins of connector K1 (ABACO® BUS).

To warrant great immunity to external noise and so a correct working of the board, it is essential that +5Vdc tension is galvanically isolated from any other supply tensions available in the system.

BOARD CONNECTIONS

To prevent possible connecting problems between PIO 01 board and the external systems, the user has to read carefully the information of the previous paragraphs and he must follow these instructions:

- The TTL signals can be connected directly only to a device featuring the same type of interface. About the correspondance between logic signals and TTL output status, remember that a logic 0 generates a TTL 0 Vdc, while a logic 1 generates a TTL +5 Vdc.

RESET CIRCUITRY

PIO 01 features an efficient reset circuitry that, whenever a reset signal comes from ABACO® BUS or a Power On occours, resets all the 96 I/O signals to their initial status, that is all the signals are configured as inputs. This is done to avoid random settings and/or undesired variations of the outputs and to warrant a safe status of the signals during this critical phase.
JUMPERS

On PIO 01 there are 8 jumpers for card configuration. Connecting these jumpers, the user can define the board working parameters, the peripheral devices functionality and so on. Below there is the jumpers list, location and function:

<table>
<thead>
<tr>
<th>JUMPERS</th>
<th>N. PINS</th>
<th>PURPOSE</th>
</tr>
</thead>
<tbody>
<tr>
<td>J1</td>
<td>2</td>
<td>Selects the connection of the /WAIT signal, generated by the on board circuity, to ABACO® BUS.</td>
</tr>
<tr>
<td>J2</td>
<td>2</td>
<td>Selects the connection of the /M1 signal, from ABACO® BUS, to the on board circuity.</td>
</tr>
<tr>
<td>J3</td>
<td>8</td>
<td>Defines the addressing space for extended addressing mode, between 64 Kbytes and 1 Mbytes.</td>
</tr>
<tr>
<td>J4</td>
<td>3</td>
<td>Selects between normal 256 bytes addressing mode and extended 64÷1024 Kbytes addressing mode.</td>
</tr>
<tr>
<td>J5</td>
<td>2</td>
<td>Selects the watch dog working mode.</td>
</tr>
<tr>
<td>J6</td>
<td>6</td>
<td>Selects the number of wait states generated by the proper circuity.</td>
</tr>
<tr>
<td>J7</td>
<td>3</td>
<td>Selects the connection of the /R.T. signal, generated by the onboard watchdog, to ABACO® BUS.</td>
</tr>
<tr>
<td>J8</td>
<td>3</td>
<td>Defines the watch dog intervent time.</td>
</tr>
</tbody>
</table>

**FIGURE 15: JUMPERS SUMMARIZING TABLE**

The following tables describe all the right connections of PIO 01 jumpers with their relative functions. To recognize these valid connections, please refer to the board printed diagram (serigraph) or to figure 2 of this manual, where the pins numeration is listed; for recognizing jumpers location, please refer to figure 19. The "*" used in the following tables, denotes the default connection, or on the other hand the connection set up at the end of testing phase, that is the configuration the User receives.

**6 PINS JUMPER**

<table>
<thead>
<tr>
<th>JUMPER</th>
<th>CONNECTION</th>
<th>PURPOSE</th>
<th>DEF.</th>
</tr>
</thead>
<tbody>
<tr>
<td>J6</td>
<td>position 1-2</td>
<td>Configures the board for introducing 3 Wait states in the I/O operations.</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>position 3-4</td>
<td>Configures the board for introducing 5 Wait states in the I/O operations.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>position 5-6</td>
<td>Configures the board for introducing 8 Wait states in the I/O operations.</td>
<td></td>
</tr>
</tbody>
</table>

**FIGURE 16: 6 PINS JUMPERS TABLE**
## 2 PINS JUMPERS

<table>
<thead>
<tr>
<th>JUMPER</th>
<th>CONNECTION</th>
<th>PURPOSE</th>
<th>DEF.</th>
</tr>
</thead>
<tbody>
<tr>
<td>J1</td>
<td>not connected</td>
<td>It does not connect the /WAIT signal generated by the on board circuitry to ABACO® BUS.</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>connected</td>
<td>It connects the /WAIT signal generated by the on board circuitry to ABACO® BUS.</td>
<td></td>
</tr>
<tr>
<td>J2</td>
<td>not connected</td>
<td>The interfacement and addressing section does not take care of managing the /M1 signal coming from ABACO® BUS.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>connected</td>
<td>The interfacement and addressing section takes care of managing the /M1 signal that is coming from ABACO® BUS.</td>
<td>*</td>
</tr>
<tr>
<td>J5</td>
<td>not connected</td>
<td>Selects monostable working mode for on board watch dog circuitry.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>connected</td>
<td>Selects astable working mode for on board watch dog circuitry.</td>
<td>*</td>
</tr>
</tbody>
</table>

**Figure 17: 2 pins jumpers table**

## 3 PINS JUMPERS

<table>
<thead>
<tr>
<th>JUMPER</th>
<th>CONNECTION</th>
<th>PURPOSE</th>
<th>DEF.</th>
</tr>
</thead>
<tbody>
<tr>
<td>J4</td>
<td>position 1-2</td>
<td>It selects 256 bytes normal addressing mode.</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>position 2-3</td>
<td>It selects 64÷1024 Kbytes extended addressing mode.</td>
<td></td>
</tr>
<tr>
<td>J7</td>
<td>position 1-2</td>
<td>It connects the output of watch dog circuitry to pin /R.T. of ABACO® BUS.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>position 2-3</td>
<td>It does not connect the output of watch dog circuitry to pin /R.T. of ABACO® BUS.</td>
<td>*</td>
</tr>
<tr>
<td>J8</td>
<td>not connected</td>
<td>It selects low intervent time (1÷72 msec) for on board watch dog circuitry.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>position 1-2</td>
<td>It selects average intervent time (30 msec÷1,76 sec) for on board watch dog circuitry.</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>position 2-3</td>
<td>It selects long intervent time (295 msec÷16,50 sec) for on board watch dog circuitry.</td>
<td></td>
</tr>
</tbody>
</table>

**Figure 18: 3 pins jumpers table**
FIGURE 19: JUMPERS LOCATION
8 PINS JUMPERS

<table>
<thead>
<tr>
<th>JUMPER</th>
<th>CONNECTION</th>
<th>PURPOSE</th>
<th>DEF.</th>
</tr>
</thead>
<tbody>
<tr>
<td>J3</td>
<td>not connected</td>
<td>If normal addressing mode has been selected, then this jumper must be in this position. If extended addressing mode has been selected, it defines 64 Kbytes of addressing space.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>position 7-8</td>
<td>If extended addressing mode has been selected, it defines 128 Kbytes of addressing space, connecting also address signal A16 to the proper circuitry.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>positions 5-6 and 7-8</td>
<td>If extended addressing mode has been selected, it defines 256 Kbytes of addressing space, connecting also address signals A16 and A17 to the proper circuitry.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>positions 3-4, 5-6 and 7-8</td>
<td>If extended addressing mode has been selected, it defines 512 Kbytes of addressing space, connecting also address signals A16, A17 and A18 to the proper circuitry.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>positions 1-2, 3-4, 5-6 and 7-8</td>
<td>If extended addressing mode has been selected, it defines 1 Mbyte of addressing space, connecting also address signals A16, A17, A18 and A19 to the proper circuitry.</td>
<td></td>
</tr>
</tbody>
</table>

**FIGURE 20: 8 PINS JUMPERS TABLE**

WAIT STATE GENERATOR

PIO 01 board is provided with a sophisticated Wait State generator designed to act directly to ABACO® BUS and, if enabled, capable to insert a configurable number of wait states in the I/O operations of PIO 01 board.

The previously described jumper J6 is used to set the number of wait states to introduce (3, 5 or 8); while jumper J1 allows to enable the circuitry by connecting its output to the /WAIT signal of ABACO® BUS.

To easily locate the above mentioned components, please refer to figure 19.

NOTE
The correct working of on board wait state generator depends on the presence of CLK signal from ABACO® BUS. Please refer to the technical manual of the intelligent control card being used (GPC® serie) to check its effective presence.
For further information please contact grifo® directly.
RESET AND WATCH DOG

PIO 01 is provided with one Watch Dog circuitry that is really efficient and easy to use. The most important features of the Watch Dog circuitry are:

- astable or monostable mode;
- intervention time settable from 1 msec to 16.50 sec (modifiable by hardware);
- enable function by hardware;
- retrigger by software;

Watch Dog intervent is signaled by the lighting of LED LD1.

The previously described jumper J5 selects the working modality of the circuitry:

- **Monostable:** In monostable mode when intervention time is elapsed the circuit becomes active and it stays active as far as a reset or power on occour.
- **Astable:** In astable mode when intervention time is elapsed the circuit becomes active, it stays active for about 8 msec then it is again deactivated.

Jumper J7 selects whether to connect or not the output of this circuitry to the signal /R.T. of ABACO® BUS. This would cause the following events:

- Intervent of PIO 01 watch dog circuitry.
- Activation of signal /R.T. of ABACO® BUS (reset request).
- Activation of reset circuitry on GPC® serie intelligent control card.
- Activation of /RESET signal of ABACO® BUS by control card.
- Overall system reset.

Intervent time can be set through jumper J8 and trimmer TR1; table in figure 18 shows the jumper connections to set short, average or long time interval; setting the exact intervent time within the selected interval is done through trimmer TR1.

Please remark that default setting for these components, that is the intervent time set during the test phase of production, is about 1 sec.

About retrigger operation of internal and external watch dog circuits, please refer to paragraph "WATCH DOG" in chapter "PERIPHERAL DEVICES SOFTWARE DESCRIPTION".

To easily locate the above mentioned components please refer to figures 6 and 19, in the previous pages.

**NOTE**

The correct working of on board watch dog circuitry depends on the presence of CLK signal from ABACO® BUS. Please refer to the technical manual of the control card being used (GPC® serie) to check its effective presence.

For further information please contact grifo® directly.
DIGITAL I/O INTERFACES

Through CN3, CN4, CN5 and CN6 (I/O Abaco® standard connector) the PIO 01 card can be connected to all of the numerous grifo® boards featuring the same standard pin out. Installation of these interfaces is very easy; in fact only a 20 pins flat cable (code FLT.20+20) is required, while the software management of these interfaces is as easy; in fact most of the software packages available for PIO 01 card are provided with the necessary procedures. Remarkable modules are:

- **QTP 16P, QTP 24P, KDL x24, KDF 224, DEB 01**, etc. that solve all the local operator interfacing problems. These modules are provided with all the resources needed to obtain a high-level human-machine interface (they feature alphanumeric displays, matrix keyboard and visualization LEDs) at a short distance from PIO 01 card. The available software drivers allow to manage the operator interface resources directly through the high-level instructions for console management. These procedures are software features added to the ones the language already provides and allow to drive the operator interface directly through instructions like PRINT and INPUT in BASIC or PRINTF and SCAND in C. This drastically simplifies the write operations to the display and the input operations from the keyboard.

- **IAC 01, DEB 01**: it is an interface for CENTRONICS parallel printer that can be connected with a standard printer cable. The printer is managed by software through the high level instructions of the selected programming language (LPRINT for BASIC, PRINTF for C, etc.).

- **MCI 64**: it is a large mass memory support that can directly manage the PCMCIA memory cards (RAM, FLASH, ROM, etc.) in their available sizes. About software the developed drivers provide a complete file system interfacing allowing to access the informations stored in the memory card directly through the high-level file management instructions.

- **RBO xx, TBO xx, XBI xx, OBI xx**: these are buffer interfaces for I/O TTL signals. With these modules the TTL input signals are converted in NPN or PNP optoisolated inputs and the TTL output signals are converted in relays or transistor optoisolated outputs. Some of the above mentioned interfaces can be connected directly to CN4.

For more information refer to "EXTERNAL CARDS" chapter and the software tools documentation.
This chapter provides all the hardware informations needed to use PIO 01 board. Here the user will find informations about I/O card mapping and on board peripheral devices addressing.

BOARD MAPPING

PIO 01 board is mapped into a 16 consecutive bytes I/O addressing space that can be based starting from different base addresses according to how the board is configured. This feature allows to use several PIO 01 cards on the same ABACO® BUS, or to install them on a BUS where other peripheral modules are installed obtaining a structure that can be expanded without any difficulty or modifications to the application software.

The base address can be defined through the specific BUS interface circuitry on the board itself; this circuitry uses two dip switches, both featuring 8 pins, called DIP1 and DIP2, from which it reads the address set by the user. Here follows the correspondence between dip switches configuration and address signals.

### Normal addressing (J4 in 1-2)

| DIP2.1 | -> | OFF |
| DIP2.2 | -> | OFF |
| DIP2.3 | -> | OFF |
| DIP2.4 | -> | OFF |
| DIP2.5 | -> | Address BUS signal A4 |
| DIP2.6 | -> | Address BUS signal A5 |
| DIP2.7 | -> | Address BUS signal A6 |
| DIP2.8 | -> | Address BUS signal A7 |

### Extended addressing (J4 in 2-3)

| DIP2.1 | -> | OFF |
| DIP2.2 | -> | OFF |
| DIP2.3 | -> | OFF |
| DIP2.4 | -> | OFF |
| DIP2.5 | -> | Address BUS signal A4 |
| DIP2.6 | -> | Address BUS signal A5 |
| DIP2.7 | -> | Address BUS signal A6 |
| DIP2.8 | -> | Address BUS signal A7 |

DIP1.1 -> Don’t care Address BUS signal A8
DIP1.2 -> Don’t care Address BUS signal A9
DIP1.3 -> Don’t care Address BUS signal A10
DIP1.4 -> Don’t care Address BUS signal A11
DIP1.5 -> Don’t care Address BUS signal A12
DIP1.6 -> Don’t care Address BUS signal A13
DIP1.7 -> Don’t care Address BUS signal A14
DIP1.8 -> Don’t care Address BUS signal A15

These dip switches are driven in complemented logic, this means that if a switch is ON it generates a logic zero, viceversa if a switch is OFF it generates a logic one.

Previously described jumper J4 selects the range of addressing space where the base address of the board can be selected.

If a 256 bytes addressing space (from 00H to FFH) is selected, then only DIP2 is used to allocate the board (the first 4 switches must be OFF) while DIP1 is indifferent.

When normal addressing mode is selected, jumper J3 must be not connected.

When extended addressing mode (64÷1024 Kbytes) is selected, both DIP1 and DIP2 must be set correctly.

Jumper J3 affects the total amount of addressing space bytes, so only dip switches whose address
signal is connected to the addressing circuitry, amongst the ones indicated by (*), must be set (refer to table in figure 20); vice versa the unused switches must be OFF.

Please remark that jumper J2 affects the addressing section and must be set according to the type of master control board (GPC®) used to drive the PIO 01. In detail if the master control board is provided with signal /M1 on ABACO® BUS connector, then jumper J2 must be connected and vice versa.

**NOTE**
If using several boards on the same ABACO® BUS, when setting the boards mapping address the user should be careful not to allocate more than one board in the same addressing space (consider the base address plus the bytes taken by the board addressing). If this condition is not satisfied a BUS conflict situation will occur, prejudicing the correct working of the whole system.

To ease the board use here follow some examples of mapping.

1) Address where mapping PIO 01: 1490H in a 64 Kbytes addressing space.
   Control card used: 16 bits address bus; not provided with signal /M1.
   J2 -> Not connected
   J3 -> Not connected
   J4 -> 2-3
   DIP2.1 -> OFF because address A16 is not connected through J3
   DIP2.2 -> OFF because address A17 is not connected through J3
   DIP2.3 -> OFF because address A18 is not connected through J3
   DIP2.4 -> OFF because address A19 is not connected through J3
   DIP2.5 -> OFF
   DIP2.6 -> ON
   DIP2.7 -> ON
   DIP2.8 -> OFF
   DIP1.1 -> ON
   DIP1.2 -> ON
   DIP1.3 -> OFF
   DIP1.4 -> ON
   DIP1.5 -> OFF
   DIP1.6 -> ON
   DIP1.7 -> ON
   DIP1.8 -> ON
2) Address where mapping **PIO 01**: 40H in a 256 bytes addressing space.
Control card used: 8 bits address bus; provided with signal /M1.

- J2 -> Connected
- J3 -> Not connected
- J4 -> 1-2

- DIP2.1 -> OFF
- DIP2.2 -> OFF
- DIP2.3 -> OFF
- DIP2.4 -> OFF
- DIP2.5 -> ON
- DIP2.6 -> ON
- DIP2.7 -> OFF
- DIP2.8 -> ON

- DIP1 -> Indifferent

3) Address where mapping **PIO 01**: 2F680H in a 256 Kbytes addressing space.
Control card used: 20 bits address bus; Not provided with signal /M1.

- J2 -> Not connected
- J3 -> 5-6 and 7-8
- J4 -> 2-3

- DIP2.1 -> ON
- DIP2.2 -> OFF
- DIP2.3 -> OFF because address A18 is not connected through J3
- DIP2.4 -> OFF because address A19 is not connected through J3
- DIP2.5 -> ON
- DIP2.6 -> ON
- DIP2.7 -> ON
- DIP2.8 -> OFF

- DIP1.1 -> ON
- DIP1.2 -> OFF
- DIP1.3 -> OFF
- DIP1.4 -> ON
- DIP1.5 -> OFF
- DIP1.6 -> OFF
- DIP1.7 -> OFF
- DIP1.8 -> OFF

To easily locate the above mentioned components, please refer to figures 2, 6 and 19 in the previous pages.
INTERNAL REGISTERS ADDRESSING

Indicating the board base address with `<baseaddr>`, that is the address set using DIP1 and DIP2, as indicated in the previous paragraph, **PIO 01** internal registers are addressable as explained in the following table.

<table>
<thead>
<tr>
<th>DEVICE</th>
<th>REG.</th>
<th>ADDRESS</th>
<th>R/W</th>
<th>PURPOSE</th>
</tr>
</thead>
<tbody>
<tr>
<td>PPI 82C55 1</td>
<td>PPI1A</td>
<td>&lt;baseaddr&gt;+00H</td>
<td>R/W</td>
<td>Port A data register, PPI 82C55 section 1.</td>
</tr>
<tr>
<td></td>
<td>PPI1B</td>
<td>&lt;baseaddr&gt;+01H</td>
<td>R/W</td>
<td>Port B data register, PPI 82C55 section 1.</td>
</tr>
<tr>
<td></td>
<td>PPI1C</td>
<td>&lt;baseaddr&gt;+02H</td>
<td>R/W</td>
<td>Port C data register, PPI 82C55 section 1.</td>
</tr>
<tr>
<td></td>
<td>PPI1RC</td>
<td>&lt;baseaddr&gt;+03H</td>
<td>R/W</td>
<td>Command and control register, PPI 82C55 section 1.</td>
</tr>
<tr>
<td>PPI 82C55 2</td>
<td>PPI2A</td>
<td>&lt;baseaddr&gt;+04H</td>
<td>R/W</td>
<td>Port A data register, PPI 82C55 section 2.</td>
</tr>
<tr>
<td></td>
<td>PPI2B</td>
<td>&lt;baseaddr&gt;+05H</td>
<td>R/W</td>
<td>Port B data register, PPI 82C55 section 2.</td>
</tr>
<tr>
<td></td>
<td>PPI2C</td>
<td>&lt;baseaddr&gt;+06H</td>
<td>R/W</td>
<td>Port C data register, PPI 82C55 section 2.</td>
</tr>
<tr>
<td></td>
<td>PPI2RC</td>
<td>&lt;baseaddr&gt;+07H</td>
<td>R/W</td>
<td>Command and control register, PPI 82C55 section 2.</td>
</tr>
<tr>
<td>PPI 82C55 3</td>
<td>PPI3A</td>
<td>&lt;baseaddr&gt;+08H</td>
<td>R/W</td>
<td>Port A data register, PPI 82C55 section 3.</td>
</tr>
<tr>
<td></td>
<td>PPI3B</td>
<td>&lt;baseaddr&gt;+09H</td>
<td>R/W</td>
<td>Port B data register, PPI 82C55 section 3.</td>
</tr>
<tr>
<td></td>
<td>PPI3C</td>
<td>&lt;baseaddr&gt;+0AH</td>
<td>R/W</td>
<td>Port C data register, PPI 82C55 section 3.</td>
</tr>
<tr>
<td></td>
<td>PPI3RC</td>
<td>&lt;baseaddr&gt;+0BH</td>
<td>R/W</td>
<td>Command and control register, PPI 82C55 section 3.</td>
</tr>
<tr>
<td>PPI 82C55 4</td>
<td>PPI4A</td>
<td>&lt;baseaddr&gt;+0CH</td>
<td>R/W</td>
<td>Port A data register, PPI 82C55 section 4.</td>
</tr>
<tr>
<td></td>
<td>PPI4B</td>
<td>&lt;baseaddr&gt;+0DH</td>
<td>R/W</td>
<td>Port B data register, PPI 82C55 section 4.</td>
</tr>
<tr>
<td></td>
<td>PPI4C</td>
<td>&lt;baseaddr&gt;+0EH</td>
<td>R/W</td>
<td>Port C data register, PPI 82C55 section 4.</td>
</tr>
<tr>
<td></td>
<td>PPI4RC</td>
<td>&lt;baseaddr&gt;+0FH</td>
<td>R/W</td>
<td>Command and control register, PPI 82C55 section 4.</td>
</tr>
<tr>
<td>WATCH DOG</td>
<td>WD</td>
<td>&lt;baseaddr&gt;+00H</td>
<td>R</td>
<td>Watch Dog circuitery retrigger register.</td>
</tr>
</tbody>
</table>

**FIGURE 21: INTERNAL REGISTERS ADDRESSING TABLE**
PERIPHERAL DEVICES SOFTWARE DESCRIPTION

In the previous paragraphs are described the external registers addresses, while in this one there is a specific description of registers meaning and function (please refer to I/O addresses table, for the registers names and addresses values). For a more detailed description of the devices, please refer to manufacturing company documentation.
In the following paragraphs the $D_7$-$D_0$ and $.0$-$7$ indications denote the eight bits of the combination used in I/O operations.

WATCH DOG

The retrigger operation for the watch dog circuitry installed on PIO 01 is performed through a simple read operation from anyone of the addresses of register WD. This register shares the same addresses of PPI 82C55 command and control registers but this doesn't create conflicts because the retrigger requires only a read operation and the data read is meaningless.
To prevent the watch dog circuitry from interventing it is essential to retrigger it at regular intervals whose duration must be lower than the intervent time set through jumper J8 and trimmer TR1. If this is not done and jumper J7 connects the circuitry to ABACO® BUS, when the intervent time is elapsed the system is reset.
Please remark that the default intervent time is about 1 sec.

NOTE

The correct working of on board watch dog circuitry depends on the presence of CLK singnal from ABACO® BUS. Please refer to the technical manual of the control card being used (GPC® serie) to check its effective presence.
For further information please contact grifo® directly.

PPI 82C55

This external peripheral device is managed through 4 registers: one status register (PPI nRC) and three data registers (PPI nA, PPI nB, PPI nC). The data registers are available both for input operation (to obtain signal status) and for output operation (to set signal status) with the correspondence described in figure 21. The PPI 82C55 can work in three different modes:

MODE 0 = it provides two 8 bits bidirectional ports (A,B) and two 4 bits bidirectional ports (C LOW, C HIGH); output signals are latched and input signals are not latched; no handshake signals are provided.

MODE 1 = it provides two 12 bits ports (A+C LOW and B+C HIGH) where ports A and B are used as 8 I/O lines and port C are used as 4 handshake lines. Both inputs and outputs are latched.

MODE 2 = it provides a 13 bits port (A+C3÷7) where port A is used as 8 I/O lines and the 5 bits of port C are used as handshake, and a 11 bits port (B+C0÷2) where port B is used as 8 I/O lines and the 3 bits of port C are used as handshakes. Both inputs and outputs are latched.
The device is programmed writing an 8 bits word in the status register CNT, with the following bits meaning:

\[
\text{PPIInRC} = SF \ M1 \ M2 \ A \ CH \ M3 \ B \ CL
\]

where:
- \(SF\) = mode Set Flag: if actived (1) the device is enabled for standard I/O operation
- \(M1\) \(M2\) = mode selection:
  - 0 0 = mode 0
  - 0 1 = mode 1
  - 1 X = mode 2
- \(A\) = port A direction: 1=input; 0=output
- \(CH\) = port C HIGH direction: 1=input; 0=output
- \(M3\) = mode selection: 1=mode 1; 0=mode 0
- \(B\) = port B direction: 1=input; 0=output
- \(CL\) = port C LOW direction: 1=input; 0=output

After Reset or power on the four PPI 82C55 are programmed in mode 0 with all three ports in input; in this way any connection of PPI 82C55 signals can be used without conflict problems.

For further information please refer to the manufacturer technical documentation or to appendix B of this manual.
EXTERNAL CARDS

PIO 01 can be connected to a wide range of block modules and operator interface system produced by grifo®, or to many system of other companies. The on board resources can be expanded with a simple connection to the numerous peripheral grifo® boards, both intelligent and not, thanks to its standard ABACO® BUS connector. Even cards with ABACO® I/O BUS can be connected, by using the proper mother boards. Hereunder some of these cards are briefly described; ask the detailed information directly to grifo®, if required.

MB3 01-MB4 01-MB8 01
Mother Board 3, 4, 8 slots
Motherboard featuring 3, 4 or 8 slots of ABACO® industrial BUS; pitch 4 TE; standard power supply connectors; LEDs for visual feed-back of power supply; holes for rack docking.

SPB 04-SPB 08
Switch Power BUS 4-8 slots
Motherboard featuring 4-8 slots of ABACO® industrial BUS; pitch 4 TE; standard power supply connectors; termination resistances; connector type F for SPC xxx supply; holes for rack docking.

ABB 03
ABACO® Block BUS 3 slots
3 slots ABACO® mother board; 4 TE pitch connectors; ABACO® I/O BUS connector; screw terminal for power supply; connection for DIN C type and Ω rails.

ABB 05
ABACO® Block BUS 5 slots
5 slots ABACO® mother board with power supply. Double power supply built in; 5Vdc 2.5A section for powering the on board logic; second section at 24Vdc 400mA galvanically coupled, for the optocoupled input lines. Auxiliary connector for ABACO® I/O BUS. Connection for DIN Ω rails.

SPC 03.5S
Switch Power Card +5 Vdc
Europe format switching power supply capable to provide +5 Vdc to a load of 4 A; input voltage 12÷24 Vac; power-failure; connector for back-up battery; standard connector for mother board SPB 0x.

SPC 512
Switch Power Card +5 Vdc +12 Vdc
Europe format switching power supply capable to provide +5 Vdc 5A and +12 Vdc 2.5 A; input voltage 12÷24 Vac; power-failure; connector for back-up battery; standard connector for mother board SPB 0x.

FBC 20-120
Flat Block Contact 20 vie
Interface for 2 or 1 mounting cable connectors (low profile 20 pins male) and quick release screw terminal connectors; Plastic mount for rails DIN 46277-1 and 3.
**GPC® 51**
General Purpose Controller fam. 51
Microprocessor family 51 INTEL including the masked BASIC chip; the board features: 16 I/O TTL lines; dip switch; 3 timer/counter; RS 232; 4 A/D converter signals resolution 11 bit; buzzer; on board EPROM programmer; RTC and 32K SRAM with Lithium battery back up; controller for display and keyboard.

**GPC® 188F**
General Purpose Controller 80C188
80C188 μP 20MHz; 1 RS 232 line; 1 RS 232, RS 422-485 or Current Loop line; 24 TTL I/O lines; 1M EPROM or 512K FLASH; 1M RAM Lithium battery backed; 8K serial EEPROM; RTC; Watch Dog; 8 Dip switch; 3 Timer Counter; 8 13 bit A/D lines; Power failure; activity LEDs; single power supply +5Vdc.

**GPC® 150**
General Purpose Controller 84C15
Microprocessor Z80 at 16 MHz; implementation completely CMOS; 512K EPROM or FLASH; 512K SRAM; RTC; Back-Up through external Lithium battery; 4M serial FLASH; 1 serial line RS 232 plus 1 RS 232 or RS 422-485 or current loop; 40 I/O TTL; 2 timer/counter; 2 watch dog; dip switch; EEPROM; A/D converter with resolution 12 bit; activity LED.

**GPC® 15R**
General Purpose Controller 84C15
84C15 μP, 10÷16 MHz; 1 RS 232 line; 1 RS 232 or RS 422-485 or C. L. line; 16÷24 TTL I/O lines; 16 Opto-in; 8 Relays; 4 Opto Coupled Timers Counters; 512K EPROM or FLASH; 512K RAM and RTC backed; 8K serial EEPROM; 8K Backed RAM modul; Buzzer; 1 Activity LED; Watch dog; 4÷12 readable DIPs; LCD Interface.

**GPC® 15A**
General Purpose Controller 84C15
Full CMOS card, 10÷20 MHz 84C15 CPU; 512K EPROM or FLASH; 128K RAM; 8K RAM and RTC backed; 8K serial EEPROM; 1 RS 232 line; 1 RS 232 line or RS 422-485 or Current Loop line; 32 or 40 TTL I/O lines; CTC; Watch dog; 2 Dip switches; Buzzer.

**GPC® 323**
General Purpose Controller 51 family
80C32 μP, 14 MHz; Full CMOS; 1 RS 232 line (software); 1 RS 232 or RS 422-485 or Current Loop line; 24 TTL I/O lines; 11 A/D 12 bits lines; 3 Timers Counters; 64K EPROM; 64K RAM; 32K RAM and RTC backed; 32K DIL EEPROM; 8K serial EEPROM; Buzzer; 2 Activity LED; Watch dog; 5 readable DIPs; LCD Interface.

**GPC® 553**
General Purpose Controller 80C552
80C552 μP, 22÷33 MHz; 1 RS 232 line (software); 1 RS 232 or RS 422-485 or Current Loop line; 16 TTL I/O lines; 8 A/D 10 bits lines; 3 Timers Counters; 64K EPROM; 64K RAM; 32K RAM and RTC backed; 32K DIL EEPROM; 8K serial EEPROM; 2 PWM lines; 1 Activity LED; Watch dog; 5 readable DIPs; LCD Interface.
Figure 22: Possible connections diagram

- **POWER SUPPLY**: +5Vdc only (SPC 03.5S or SPC 512)
- **ALL TYPE CPU**
  - GPC® 150
  - GPC® 15A
  - GPC® 188F
  - GPC® 51
- **ANY MOTHERBOARD TYPE WITH ABACO® BUS**
- **16 DIGITAL TTL I/O**
  - direct to OBI xx, XBI xx ...
  - TRANSISTOR INPUT

- **16 DIGITAL TTL I/O**
  - direct to RBO xx, TBO xx ...
  - TRANSISTOR RELAY

- **16 DIGITAL TTL I/O**
  - direct to video terminal
  - QTP 16P or QTP 24P

- **16 DIGITAL TTL I/O**
  - direct to IAC 01 or DEB 01
  - PRINTER

- **16 DIGITAL TTL I/O LINES**
  - STEPPER MOTOR
  - SMART CARD

- **16 DIGITAL TTL I/O**
  - direct to MCI 64
  - MEMORY CARD

- **FBC 20 or FBC 120**

- **20 pins Flat-cable** (FLT 20+20)
GPC® 153
General Purpose Controller Z80
84C15 μP, 10÷16 MHz; Full CMOS; 1 RS 232 line; 1 RS 232 or RS 422-485 or Current Loop line; 16 TTL I/O lines; 8 A/D 12 bits lines; 2÷4 Timers Counters; 512K EPROM or FLASH; 512K RAM and RTC backed; 8K serial EEPROM; Buzzer; 1 Activity LED; Watch dog; 8 readable DIPs; LCD Interface.

GPC® 183
General Purpose Controller Z180
Z180 μP, 10÷16 MHz; Full CMOS; 1 RS 232 line; 1 RS 232 or RS 422-485 or Current Loop line; 24 TTL I/O lines; 11 A/D 12 bits lines; 2 Timers Counters; 512K EPROM or FLASH; 512K RAM and RTC backed; 8K serial EEPROM; Buzzer; 2 Activity LED; Watch dog; 4 readable DIPs; LCD Interface.

GPC® 324/D
“4” Type General Purpose Controller 80C32/320
80C32 or 80C320 μP, 14÷22 MHz; Full CMOS; 1 RS 232 line; 1 RS 232 or RS 422-485 or Current Loop line; 4÷16 TTL I/O lines; 3 Timers Counters; 64K EPROM; 64K RAM; 32K RAM backed; 32K DIL E2; 8K serial EEPROM; Watch dog; 1 readable DIP; LCD Interface; Abaco® I/O BUS; 5Vdc Power supply; Size: 100x50 mm.

GPC® 554
General Purpose Controller 80C552
Microprocessor 80C552 at 22 MHz; implementation completely CMOS; 32K EPROM; 32 K SRAM; 32 K EEPROM or SRAM; EEPROM; 2 RS 232 serial lines; 16 I/O TTL; 2 PWM lines; 16 bits Timer/Counter; Watch Dog; 6 signals A/D converter with resolution 10 bit; interface for ABACO® I/O BUS.

GPC® 154
“4” Type General Purpose Controller Z80
84C15 μP, 10÷16 MHz; Full CMOS; 1 RS 232 line; 1 RS 232 or RS 422-485 line; 16 TTL I/O lines; 2÷4 Timers Counters; 512K EPROM or FLASH; 512K RAM and RTC backed; 8K serial EEPROM; Watch dog; 2 readable DIPs; LCD Interface; Abaco® I/O BUS; 5Vdc Power supply; Size: 100x50 mm.

GPC® 884
General Purpose Controller Am188ES
Microprocessor AMD Am188ES up to 40 MHz 16 bits; implementation completely CMOS; serie 4 format; 512K EPROM or FLASH; 512K SRAM backed with Lithium battery; RTC; 1 RS 232 serial line + 1 RS 232 or RS 422-485 or current loop; 16 I/O TTL; 3 timer/counter; watch dog; EEPROM; 11 signals A/D converter with 12 bit resolution; interface for ABACO® I/O BUS.

GPC® 114
General Purpose Controller 68HC11
Microprocessor 68HC11A1 at 8 MHz; implementation completely CMOS; serie 4 format; 32K EPROM; 32K SRAM backed with Lithium battery; 32K EPROM, SRAM, EEPROM; RTC; 1 serial line RS 232 or RS 422-485; 10 I/O TTL; 3 timer/counter; watch dog; 8 signals A/D converter with resolution 8 bit; 1 asynchronous serial line; extremly low power consumption; interface for ABACO® I/O BUS.
**KDL X24 - KDF 224**
Keyboard Display LCD 2,4 rows 24 keys
Interface with Fluorescent or LCD display, LEDs backlit, 20x2 or 20x4 characters; up to 24 keys matrix keyboard connector. It is directly driven by a 20 pins ABACO® I/O standard connector; High level languages supported; standard pinout for telephone keyboard.

**QTP 16P**
Quick Terminal Panel 16 keys with Parallel interface
Operator interface equipped with fluorescent alphanumeric display 20x 2 or LCD 20x2, 20x4 LEDs backlit; 16 keys keyboard; on board power supply capable to supply also external loads; parallel interface based on 16 I/O TTL available from a 20 pins I/O ABACO® standard connector; metal frame.

**QTP 24P**
Quick Terminal Panel 24 keys with Parallel interface
Intelligent user panel equipped with Fluorescent or LCD display, LEDs backlit, 20x2 or 20x4 characters; 24 Keys and 16 LEDs with blinking attribute manageable by software; built in power supply; directly driven from 16 TTL I/O lines; high level languages supported.

**IAC 01**
Interface Adapter Centronics
Interface between ABACO® standard I/O 20 pins connector and D 25 pins connector with Centronics standard pin out.

**OBI N8 - OBI P8**
Opto BLOCK Input NPN-PNP
Interface between 8 NPN, PNP optocoupled and displayed input lines, with screw terminal and ABACO® standard I/O 20 pins connector; power supply section; connection for DIN Ω rails.

**TBO 01 - TBO 08**
Transistor BLOCK Output
Interface for ABACO® standard I/O 20 pins connector; 16 or 8 transistor output lines 45 Vdc 3 A open collector; screw terminal; optocoupled and displayed lines; connection for DIN 247277-1 and 3 rails.

**RBO 08 - RBO 16**
Relé BLOCK Output
Interface for ABACO® standard I/O 20 pins connector; 8 or 16 displayed Relays 3A with MOV; screw terminal; connection for DIN Ctype and Ω rails.

**DEB 01**
Didactic Experimental Board
Supporting card for 16 TTL I/O lines use. It includes: 16 keys, 16 LEDs, 4 digits, 16 keys matrix keyboard, Centronics printer interface, LCD display and fluorescent display interface, GPC® 68 I/O connector, field connection with screw terminal.
IAL 42
Interface Adapter LCD
Interface between 16 I/O TTL available on I/O ABACO® standard connector and 14 pins lowprofile male connector featuring standard pin-out for fluorescent LCD displays management.

XBI 01
miXed BLOCK Input Output
Interface for ABACO® standard I/O 20 pins connector; 8 transistor output lines 45 Vdc 3A; 8 input lines; screw terminal; optocoupled and displayed I/O lines; connection for DIN 247277-1 and 3 rails.

XBI R4 - XBI T4
miXed BLOCK Input-Output
Interface for ABACO® standard I/O 20 pins connector; 4 Relays 3A with MOV or 4 optocoupled Transistors 3A open collectors; 4 input lines optocoupled; screw terminal; connection for DIN Ctype and Ω rails.

XBI T4 - XBI R4
miXed BLOCK 4 Input 4 Output relé o transistor
Interfaccia tra 4 input + 4 output TTL (connettore normalizzato I/O ABACO® a 20 vie), con 4 output a transistor in Open Collector da 45 Vcc 3 A oppure a relé da 3A con MOV + 8 input con filtro a Pi-Greco (connettore a morsettiera). I/O optoisolati e visualizzati; attacco rapido per guide DIN 46277-1 e 3.

MCI 64
Memory Cards Interfaces 64 MBytes
Interfacing card for managing 68 pins PCMCIA memory cards, it is directly driven from any ABACO® I/O standard connector; High level languages GDOS supported.
BIBLIOGRAPHY

Here follows a list of manuals that can be a source of further information about the devices installed on PIO 01.

Manual NEC: *Microprocessor and Peripherals - Volume 3*

Manual TEXAS INSTRUMENTS: *The TTL data Book - SN54/74 Families*

Manual TEXAS INSTRUMENTS: *Linear Circuits Data Book - Volume 1*

Please connect to the manufacturer's Web sites to get the latest version of all manuals and data sheets.
APPENDIX A: ELECTRIC DIAGRAMS

This appendix reports the electric diagrams of the most common interfaces used with PIO 01. The user can build in autonomy all these interfaces while only some of them are standard grifo® cards and can be purchased.

**Figure A1: IAC 01 Electric Diagram**

![Electric Diagram](image)
Title: KDL/F-2/424
Date: 22-07-1998
Rel. 1.2
Page: 1 of 1

**Figure A2: KDX x24 Electric Diagram**

- **Components:**
  - LCD20x2 LCD20x4 Futaba VFD
  - R1 = 0Ω N.M. N.M.
  - R2 = N.M. N.M. N.M.
  - R3 = 18Ω 12Ω N.M.
  - R4 = 18Ω 12Ω N.M.
  - R5 = N.M. N.M. N.M.
  - R6 = 470Ω
  - R7 = 470Ω
  - R8 = 470Ω
  - R9 = 470Ω
  - R10 = 22kΩ 9+1 SIP
  - R11 = 22kΩ 9+1 SIP
  - R12 = 10kΩ trimmer
  - C1 = 100μF
  - C2 = 22μF 6.3V Tantalium
  - C3 = 100μF
  - C4 = 100μF
  - C5 = 22μF 6.3V Tantalium
  - CN1 = 2 pins mini male connector
  - CN2 = 10 pins male strip
  - CN3 = 20 pins male low profile connector
  - CN4 = LCD L214 (20x4)
  - CN5 = Futaba VFD20x2
  - CN6 = LCD L2012 (20x2)
  - IC1 = 7407
  - J1 = 2 pins female jumper

- **Connectors:**
  - CN1: 2 pins mini male connector
  - CN2: 10 pins male strip
  - CN3: 20 pins male low profile connector
  - CN4: LCD L214 (20x4)
  - CN5: Futaba VFD20x2
  - CN6: LCD L2012 (20x2)
  - IC1: 7407
  - J1: 2 pins female jumper

**Legend:**
- +5V
- GND
- +VLED
- /BUSY
- R/W
- /SEL
- TEST
- RS
- E
- CONTRAST
- 4x6 External Keyboard
- PA.0 to PA.7
- PC.0 to PC.7
- CN1 to CN6
FIGURE A3: QTP 16P ELECTRIC DIAGRAM
FIGURE A4: QTP 24P ELECTRIC DIAGRAM - PART 1
Figure A5: QTP 24P electric diagram - part 2
APPENDIX B: ON BOARD COMPONENTS DESCRIPTION

OKI semiconductor
MSM82C55A-2RS/GS/VJS
CMOS PROGRAMMABLE PERIPHERAL INTERFACE

GENERAL DESCRIPTION

The MSM82C55A is a programmable universal I/O interface device which operates as high speed and on low power consumption due to 3 μ silicon gate CMOS technology. It is the best fit for an I/O port in a system which employs the 8-bit parallel processing MSM68C05A CPU. This device has 24-bit I/O pins equivalent to three 8-bit I/O ports and all inputs/outputs are TTL interface compatible.

FEATURES

- High speed and low power consumption due to 3 μ silicon gate CMOS technology
- 3 V to 6 V single power supply
- Full static operation
- Programmable 24-bit I/O ports
- Bidirectional bus operation (Port A)
- Bit set/reset function (Port C)
- TTL compatible
- Compatible with 8255A-5
- 40 pin Plastic DIP (OP40-P-800)
- 44 pin PLCC (GFP44-P-9650)
- 44 pin-V Plastic QFP (GFP44-P-910-VK)
- 44 pin-VI Plastic QFP (GFP44-P-910-VIK)

CIRCUIT CONFIGURATION
FUNCTIONAL DESCRIPTION OF PIN

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Item</th>
<th>Input/Output</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>D7 – D0</td>
<td>Bidirectional data bus</td>
<td>Input and output</td>
<td>These are three-state 8 bit bidirectional buses used to write and read data upon receipt of the WR and RD signals from CPU. They can also be used when control words and bits are selected from dB1 to dB8. These signals are transmitted from CPU to MSB and from MSB to CPU.</td>
</tr>
<tr>
<td>RESET</td>
<td>Reset Input</td>
<td>Input</td>
<td>This signal is used to reset the control register and all internal registers when the CPU is in a high level. At this time, the ports are all in the Input mode (high impedance state). After this, the ports are in the Output mode.</td>
</tr>
<tr>
<td>CS</td>
<td>Chip select Input</td>
<td>Input</td>
<td>When the CS is in low level, data transmission is enabled with CPU. When in high level, the data bus is made to the high impedance state, and no data transmission operation is performed.</td>
</tr>
<tr>
<td>RD</td>
<td>Read Input</td>
<td>Input</td>
<td>When RD is in low level, data is transferred from MSB to CPU.</td>
</tr>
<tr>
<td>WR</td>
<td>Write Input</td>
<td>Input</td>
<td>When WR is in low level, data is transferred from CPU to MSB.</td>
</tr>
<tr>
<td>A0, A1</td>
<td>Port select</td>
<td>Input</td>
<td>By combination of A0 and A1, one is selected from among port A, port B, and port C.</td>
</tr>
<tr>
<td>PA7 – PA0</td>
<td>Port A</td>
<td>Input and output</td>
<td>These are universal 8-bit I/O ports. The direction of input/output ports can be determined by writing a control word. When port A is set to mode 2, it becomes an output port.</td>
</tr>
<tr>
<td>PB7 – PB0</td>
<td>Port B</td>
<td>Input and output</td>
<td>These are universal 8-bit I/O ports. The direction of input/output ports can be determined by writing a control word with 4 bits each. When port B is set to mode 1, it becomes a control port.</td>
</tr>
<tr>
<td>PC7 – PC0</td>
<td>Port C</td>
<td>Input and output</td>
<td>These are universal 8-bit I/O ports. The direction of input/output ports can be determined by writing a control word with 4 bits each. When port C is set to mode 1, it becomes a control port.</td>
</tr>
</tbody>
</table>

VCC +5 V power supply.

GROUND

BASIC FUNCTIONAL DESCRIPTION

Group A and Group B

When setting a mode to a port, specific bits are set by dividing it into two groups of 12 bits each.

Group A: Port A (3 bits) and high order 4 bits of port C (PC7 – PC4)

Group B: Port B (3 bits) and low order 4 bits of port C (PC3 – PC0)

Mode 0, 1, 2

There are 3 types of modes to be set by grouping as follows:

Mode 0: Basic input/output operation (Available for both groups A and B)

Mode 1: Strobe input/output operation (Available for both groups A and B)

Mode 2: Bidirectional bus operation (Available for group A only)

When used in mode 1 or mode 2, however, port C has bits to be defined as ports for control signals for operation ports (Port A for group A and Port B for group B) of their respective groups:

Port A, B, C

The internal structure of Port A is as follows:

Port A: One 8-bit data input latch/buffer and one input latch

Port B: One 8-bit data output latch/buffer and one input latch

Port C: One 8-bit data output latch/buffer and one input latch

Single-bit set/reset function for Port C

When Port C is defined as an output port, it is possible to set the high level (in high level) or reset the low level (in low level) by any one of 8 bits individually without affecting other bits.
ITALIAN TECHNOLOGY

OPERATIONAL DESCRIPTION

Control Logic
Operations by addresses and control signals, e.g., read and write, etc., are as shown in the table below:

<table>
<thead>
<tr>
<th>Operation</th>
<th>A1</th>
<th>A0</th>
<th>ZE</th>
<th>WR</th>
<th>RD</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Port A → Data Bus</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>Port B → Data Bus</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Port C → Data Bus</td>
</tr>
<tr>
<td>Output</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Data Bus → Port A</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Data Bus → Port B</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Data Bus → Port C</td>
</tr>
<tr>
<td>Control</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>Data Bus → Control Register</td>
</tr>
<tr>
<td>Others</td>
<td>x</td>
<td>x</td>
<td>1</td>
<td>x</td>
<td>Data bus is in the high impedance status</td>
</tr>
</tbody>
</table>

Setting of Control Word
The control word is composed of 7-bit latch circuit and 1-bit flag as shown below.

Preparation for mode selection
The output registers for ports A and C are cleared to 0 each time data is written in the command register and the mode is changed, but the port B state is undefined.

Bit Set/Reset Function
When port C is defined as output port, it is possible to set last output to 1 or reset last output to 0 any one of 8 bits without affecting other bits as shown next page.

Interrupt Control Function
When the MSM8255A is used in mode 1 or mode 2, the interrupt signal for the CPU is provided. The interrupt request signal is output from port C. When the internal flip-flop INT INTERRUPT REQUEST SIGNAL is set before this time, the desired interrupt request signal is output. When it is reset beforehand, however, the interrupt request signal is not output. The address of the internal flip-flop is made by the bit set/reset function for port C virtually.

Bit set = INTE is set, *Interrupt allowed
Bit reset = INTE is reset => *Interrupt inhibited

Operational Description by Mode
1. Mode 0 (Basic input/output operation)
Mode 0 makes the MSM8255A operate as a basic input/output port. No control signals such as interrupt request, etc., are required in this mode. All 24 bits can be used as one 24-bit ports and two 4-bit ports. Sixteen combinations are then possible for inputs/outputs. The inputs are not latched, but the outputs are.
2. Mode 1 (Strobe input/output operation)

In mode 1, the strobe, interrupt and other control signals are used when input/output operations are made from the specified port. If this mode is available for both groups A and B, in group A at this time, port A is used as the data line and port C as the control signal.

Following is a description of the input operation in mode 1.

**STB (Strobe input)**
- When this signal is low level, the data output from terminal to port C is fetched into the internal latch of the port. This can be made independent from the CPU, and the data is not output to the data bus until the RD signal arrives from the CPU.

**IBF (Input buffer full flag output)**
- This is the response signal for the STB. This signal, when turned to high level indicates that data is fetched into the input latch. This signal turns to high level at the falling edge of STB and to low level at the falling edge of RD.

**INTR (Interrupt request output)**
- This is the interrupt request signal for the CPU of the data fetched into the input latch. It is indicated by high level only when the internal INT flag is set. This signal turns to high level at the rising edge of the STB (DF = 1) at this time.

The mode low level at the falling edge of the STB when the INTE is set.

**INTE**

- Group A is set when the bit for PC4 is set, while Group B is set when the bit for PC5 is set.

Following is a description of the output operation of mode 1.

**OBF (Output buffer full flag output)**
- This signal when turned to low level indicates that data is written to the specified port when receipt of the WR signal from the CPU. This signal turns to low level at the rising edge of the WR and high level at the falling edge of the ACK.

**ACK (Acknowledgment input)**
- This signal when turned to low level indicates that the terminal has received data.

**INTA (Interrupt request output)**
- This is the signal used to interrupt the CPU when a terminal receives data from the CPU via the modes. If the interrupt is high level only when the internal INT flag is set, the signal turns to high level at the rising edge of the ACK (DF = 1) at this time.

**INTE**
- Group A is set when the bit for PC4 is set, while Group B is set when the bit for PC5 is set.

Examples of the relation between the control words and pins when used in mode 1 are shown below:

a) When group A is mode 1 output and group B is mode 1 input.
3. Mode 2 (Strobe bidirectional bus I/O operation)

In mode 2, it is possible to transfer data in 2 directions through a single 8-bit port. This operation is possible in combination with input and output operations. Port C waits for the control signal in this case, too. Mode 2 is available only for group A, however.

Next, a description is made on mode 2.

**RS (Output buffer full flag input)**
- This signal is high when the mode 2 signal is low level and indicates that data has been written to the internal output port latch upon receipt of the WR signal from the CPU. At this time, port A is still in the high impedance state and the data is not yet output to the outside. The signal turns to low level at the rising edge of the WR and high level at the falling edge of the RD.

**ACK (Acknowledge input)**
- When the low level signal is input to this pin, the high impedance status of port A is cleared, the buffer is enabled, and the data written to the internal output latch is output to port A. When the input returns to high level, port A is made into the high impedance state.

**STB (Strobe input)**
- When this signal turns to low level, the data output to the port from the pin is fetched into the internal input latch. The data is output to the data bus upon receipt of the RD signal from the CPU, but it remains in the high impedance status until then.

**OBF (Output buffer full flag output)**
- This signal is high when the mode 2 signal is low level and indicates that data has been written to the input latch. The signal turns to low level at the falling edge of the STB and low level at the rising edge of the RD.

**INTR (Interrupt request output)**
- This signal is used to interrupt the CPU and its operation in the same way as in mode 1. There are two INTB flip-flops internally available for input and output to select either interrupt of input or output operation. The INTB is used to control the interrupt request for output operation and it can be reset by the bit set for PCB. INTB is used to control the interrupt request for the input operation and it can be set by the bit set for PCB.

Following is an example of the relation between the control word and the pin when used in mode 2.

When input in mode 2 for group A and in mode 1 for group B.
### Mode combinations that define no control bit at port C

<table>
<thead>
<tr>
<th>Group A</th>
<th>Group B</th>
<th>Port C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mode 1 input</td>
<td>Mode 0</td>
<td>PC2, PC3, PC4, PC5, PC6, PC7, PC8, PC9</td>
</tr>
<tr>
<td>Mode 0 output</td>
<td>Mode 1 input</td>
<td>I/O, I/O, I/O, I/O, I/O, I/O, I/O, I/O</td>
</tr>
<tr>
<td>Mode 0 output</td>
<td>Mode 1 output</td>
<td>I/O, I/O, I/O, I/O, I/O, I/O, I/O, I/O</td>
</tr>
<tr>
<td>Mode 1 input</td>
<td>Mode 1 input</td>
<td>I/O, I/O, I/O, I/O, I/O, I/O, I/O, I/O</td>
</tr>
<tr>
<td>Mode 1 input</td>
<td>Mode 1 output</td>
<td>I/O, I/O, I/O, I/O, I/O, I/O, I/O, I/O</td>
</tr>
</tbody>
</table>

When the I/O bit is set to input in this case, it is possible to access data by the normal port C read operation. When set to output, PC7 – PC4 bits can be accessed by the OE set/reset function only. Meanwhile, 3 bits from PC2 to PC0 can be accessed by normal write operation.

The bit set/reset function can be used for all of PC3 – PC6 bits. Note that the status of port C varies according to the combination of modes like this.

---

**6. Port C Status Read**

When port C is used for the control signal, that is, in either mode 1 or mode 2, each control signal and bus status signal can be read out by reading the contents of port C. The status read out is as follows:

<table>
<thead>
<tr>
<th>Group A</th>
<th>Group B</th>
<th>Status read on the data bus</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mode 1 input</td>
<td>Mode 0</td>
<td>D1, D2, D3, D4, D5, D6, D7, D8</td>
</tr>
<tr>
<td>Mode 0 output</td>
<td>Mode 0</td>
<td>I/O, I/O, I/O, I/O, I/O, I/O, I/O, I/O</td>
</tr>
<tr>
<td>Mode 0 output</td>
<td>Mode 0</td>
<td>I/O, I/O, I/O, I/O, I/O, I/O, I/O, I/O</td>
</tr>
<tr>
<td>Mode 1 input</td>
<td>Mode 0</td>
<td>I/O, I/O, I/O, I/O, I/O, I/O, I/O, I/O</td>
</tr>
<tr>
<td>Mode 1 input</td>
<td>Mode 0</td>
<td>I/O, I/O, I/O, I/O, I/O, I/O, I/O, I/O</td>
</tr>
<tr>
<td>Mode 1 input</td>
<td>Mode 0</td>
<td>I/O, I/O, I/O, I/O, I/O, I/O, I/O, I/O</td>
</tr>
<tr>
<td>Mode 1 input</td>
<td>Mode 0</td>
<td>I/O, I/O, I/O, I/O, I/O, I/O, I/O, I/O</td>
</tr>
<tr>
<td>Mode 1 input</td>
<td>Mode 0</td>
<td>I/O, I/O, I/O, I/O, I/O, I/O, I/O, I/O</td>
</tr>
<tr>
<td>Mode 1 input</td>
<td>Mode 0</td>
<td>I/O, I/O, I/O, I/O, I/O, I/O, I/O, I/O</td>
</tr>
<tr>
<td>Mode 1 input</td>
<td>Mode 0</td>
<td>I/O, I/O, I/O, I/O, I/O, I/O, I/O, I/O</td>
</tr>
</tbody>
</table>

**6. Reset of MSM82C55A**

Be sure to keep the RESET signal at power ON in the high level at least for 50 μs. Subsequently, it becomes the input mode at a high level pulse above 500 ns.

**Note:** Comparison of MSM82C55A-6 and MSM82C55A-2

**MSM82C55A-6**
- After a write command is executed to the command register, the internal latch is cleared in PORTA, PORTB, PORTC.
- PORTS is the output of the beginning of a write command when the output port is assigned. However, if PORTB is not cleared at this time, PORTS is unaccessible. In other words, PORTS only outputs the reset data (I/O value) according to the device during the period from after a write command is executed till the first data is written to PORTB.

**MSM82C55A-2**
- After a write command is executed to the command register, the internal latch is cleared in MS82PI0A, MS82PI0B, MS82PI0C.
- PORTS is the output of the beginning of a write command when the output port is assigned.
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<td><strong>N</strong></td>
<td>NORMAL ADDRESSING MODE</td>
<td>27</td>
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<td>PERIPHERAL DEVICES SOFTWARE DESCRIPTION</td>
<td>31</td>
</tr>
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<td></td>
<td>PERIPHERALS</td>
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<td>PORT B OF SECTIONS 1 AND 2</td>
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<td></td>
<td>PORTS A AND C OF SECTION 2</td>
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