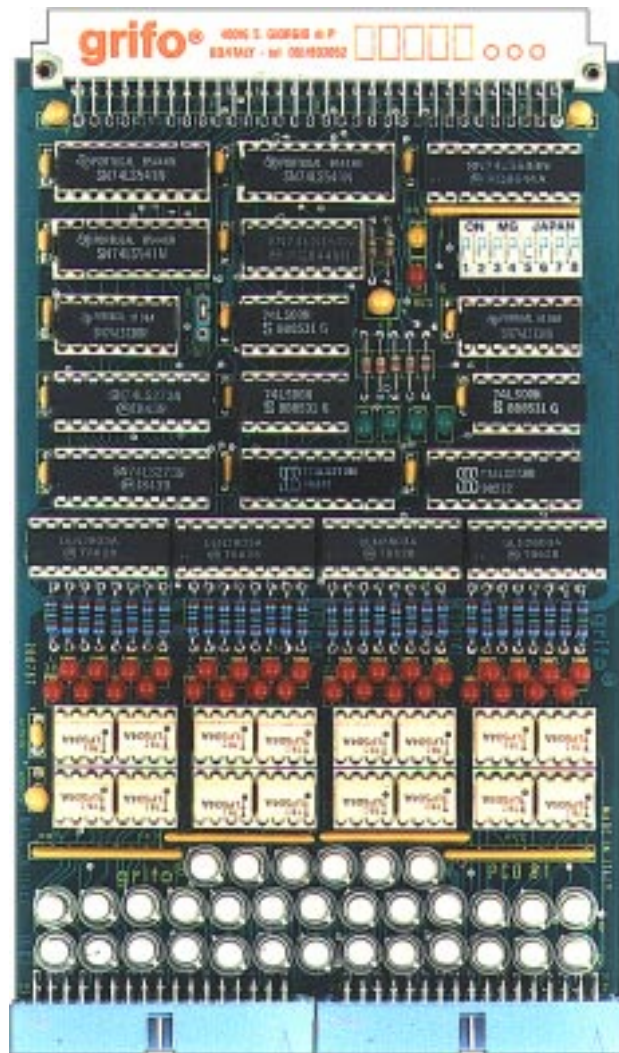


PCO 01

Peripheral Coupled Output NPN Transistors

TECHNICAL MANUAL



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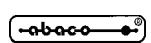


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PCO 01

Edition 5.00

Rel. 02 March 2001

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PCO 01

Peripheral Coupled Output NPN Transistors

TECHNICAL MANUAL

Peripheral card in Eurocard format size 100x160 mm; interface to **ABACO**[®] Industrial BUS; 32 optocoupled open collector NPN 500 mA 30 Vdc transistor digital output lines, without heat sink; visualization through LED of the logic status of each output line; circuitry to prevent lines activation during power on; two standard 34 pins output connectors; I/O mapping space selection through on board dip switch; I/O room taken as low as 4 Byte; data BUS width selectable between 8 or 16 bits through jumper; 2 LEDs to visualize BUS interface configuration; possibility to connect or not the /RESET signal; interfacement to the external world through **FBC 324** modules; unique power supply +5 Vdc

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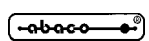
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For specific informations on the components mounted on the card, please refer to the Data Book of the builder or second sources.

SYMBOLS DESCRIPTION

In the manual could appear the following symbols:

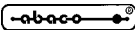


Attention: Generic danger



Attention: High voltage

Trade Marks

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GENERAL INDEX

INTRODUCTION	1
CARD VERSION	1
GENERAL INFORMATION	2
INTERFACING AND ADDRESSING	4
CONTROL LOGIC	4
OUTPUT	4
TECHNICAL FEATURES	6
GENERAL FEATURES	6
PHYSICAL FEATURES	6
ELECTRIC FEATURES	6
INSTALLATION	8
POWER SUPPLY	8
BOARD CONNECTIONS	8
CONNECTIONS	8
CN1 - TRANSISTOR OUTPUT SECTIONS A AND B CONNECTOR	9
CN2 - TRANSISTOR OUTPUT SECTIONS C AND D CONNECTOR	10
K1 - CONNECTOR FOR ABACO® BUS	12
VISUAL SIGNALATIONS	14
JUMPERS	16
RESET CIRCUITRY CONFIGURATION	16
HARDWARE DESCRIPTION	17
BOARD MAPPING	17
INTERNAL REGISTERS ADDRESSING	19
INTERNAL REGISTERS ADDRESSING FOR 8 BIT ADDRESSING MODE	19
INTERNAL REGISTERS ADDRESSING FOR 16 BIT ADDRESSING MODE	19
PERIPHERAL DEVICES SOFTWARE DESCRIPTION	20
TRANSISTOR OUTPUTS	20
EXTERNAL CARDS	22
BIBLIOGRAPHY	27
APPENDIX A: ALPHABETICAL INDEX	A-1

FIGURES INDEX

FIGURE 1: BLOCK DIAGRAM	3
FIGURE 2: COMPONENTS MAP	5
FIGURE 3: CARD PHOTO	7
FIGURE 4: CN1 - TRANSISTOR OUTPUT SECTIONS A AND B CONNECTOR	9
FIGURE 5: CN2 - TRANSISTOR OUTPUT SECTIONS C AND D CONNECTOR	10
FIGURE 6: TRANSISTOR OUTPUTS BLOCK DIAGRAM	11
FIGURE 7: K1 - CONNECTOR FOR ABACO® BUS	12
FIGURE 8: VISUAL SIGNALATIONS TABLE	14
FIGURE 9: CONNECTORS, DIP SWITCH, LEDs AND JUMPERS LOCATION	15
FIGURE 10: JUMPERS SUMMARIZING TABLE	16
FIGURE 11: INTERNAL REGISTERS ADDRESSING TABLE FOR 8 BIT ADDRESSING MODE	19
FIGURE 12: INTERNAL REGISTERS ADDRESSING TABLE FOR 16 BIT ADDRESSING MODE	19
FIGURE 13: POSSIBLE CONNECTIONS DIAGRAM	25

INTRODUCTION

The use of these devices has turned - IN EXCLUSIVE WAY - to specialized personnel.

The purpose of this handbook is to give the necessary information to the cognizant and sure use of the products. They are the result of a continual and systematic elaboration of data and technical tests saved and validated from the manufacturer, related to the inside modes of certainty and quality of the information.

The reported data are destined- IN EXCLUSIVE WAY- to specialized users, that can interact with the devices in safety conditions for the persons, for the machine and for the environment, impersonating an elementary diagnostic of breakdowns and of malfunction conditions by performing simple functional verify operations , in the height respect of the actual safety and health norms.

The informations for the installation, the assemblage, the dismantlement, the handling, the adjustment, the reparation and the contingent accessories, devices etc. installation are destined - and then executable - always and in exclusive way from specialized warned and educated personnel, or directly from the TECHNICAL AUTHORIZED ASSISTANCE, in the height respect of the manufacturer recommendations and the actual safety and health norms.

The devices can't be used outside a box. The user must always insert the cards in a container that respect the actual safety normative. The protection of this container is not threshold to the only atmospheric agents, but specially to mechanic, electric, magnetic, etc. ones.

To be on good terms with the products, is necessary guarantee legibility and conservation of the manual, also for future references. In case of deterioration or more easily for technical updates, consult the AUTHORIZED TECHNICAL ASSISTANCE directly.

To prevent problems during card utilization, it is a good practice to read carefully all the informations of this manual. After this reading, the user can use the general index and the alphabetical index, respectly at the begining and at the end of the manual, to find information in a faster and more easy way.

CARD VERSION

The present manual is reported to the **PCO 01** version **040788**.

The validity of the bring informations is subordinate to the number of the card release. The user must always verify the correct correspondence among the two denotations. Version number is printed on the boards in several positions both in serigraph and in printed circuit (for example near LED L38 on the component side).

GENERAL INFORMATION

PCO 01 (Peripheral Coupled Output **32** transistors NPN) board is a very powerful I/O module capable to drive 32 output lines on a standard connector. This extreme compactness marks all **grifo**[®] boards and allows to optimize room and final cost of the applications.

Output section is optocoupled so that to warrant the galvanic separation between the external world and the on board electronic. Each output line is provided with an open collector NPN transistor and its own LED that visualizes the logic status of the line itself. A LED turns on when the respective output signal is activated. There is also a special circuitry that warrants the Reset condition for all the outputs during the power on. It is also possible to unmatch the outputs Reset from the CPU card Reset acting on Dip-Switch DIP1. By unmatching the **PCO 01** Reset from the Master Reset, it is possible to keep the output signals in a Latch condition even when the main CPU is reset.

To warrant with the maximum security the outputs status, especially during the delicate phase of power on, a specific circuitry keeps all the outputs deactivated until, section by section, it receives the specific write abilitation command and the board responds turning ON the LED of the section enabled. This prevents the possibility of undesired oscillations on the output signals when power supply is not reliable.

PCO 01 is connected to the external world through two Standard **ABACO**[®] connectors. This warrants a correct I/O interchange amongst the peripherals available in the **ABACO**[®] listing.

To ease the operations of cable mounting and connection of wires from the external world, a set of modules capable of mounting on DIN rack has been created; these modules belong to **FBC xxx** family. In detail these modules allow to unravel the wires coming from the external Flat-Cables making them available on comfortable quick release screw terminal connectors. There are also **FBC** modules designed specifically for connections of output cards. Remarkable is **FBC 234**.

PCO 01 peripheral board can work both matching with 8 bit CPU's and 16 bit CPU's, taking only 4 bytes in the I/O addressing space. The choice between the 8 or 16 bit BUS interface is made by a specific Dip-switch. The condition set is visualized through two specific LEDs located near the selection Dip-switch.

- Peripheral card in Eurocard format size 100x160 mm
- Interface to **ABACO**[®] Industrial BUS
- 32 output signals, optocoupled and buffered, provided with open collector transistors, **500 mA, 30 Vdc**, without heat sink
- Visualization through LED of the logic status of each input line
- Circuitry to prevent lines activation during power on
- **Two** standard **32** pins output connectors
- Connection to the external world through **FBC 324**, etc.
- BUS data width selectable between **8** or **16** bits through jumper
- Two LEDs to visualize BUS interface configuration
- Possibility to connect or disconnect BUS /RESET signal
- I/O mapping through **dip switch**, in 256 Byte mapping space
- I/O room taken as low as 4 Byte
- Unique power supply **+5 Vdc**

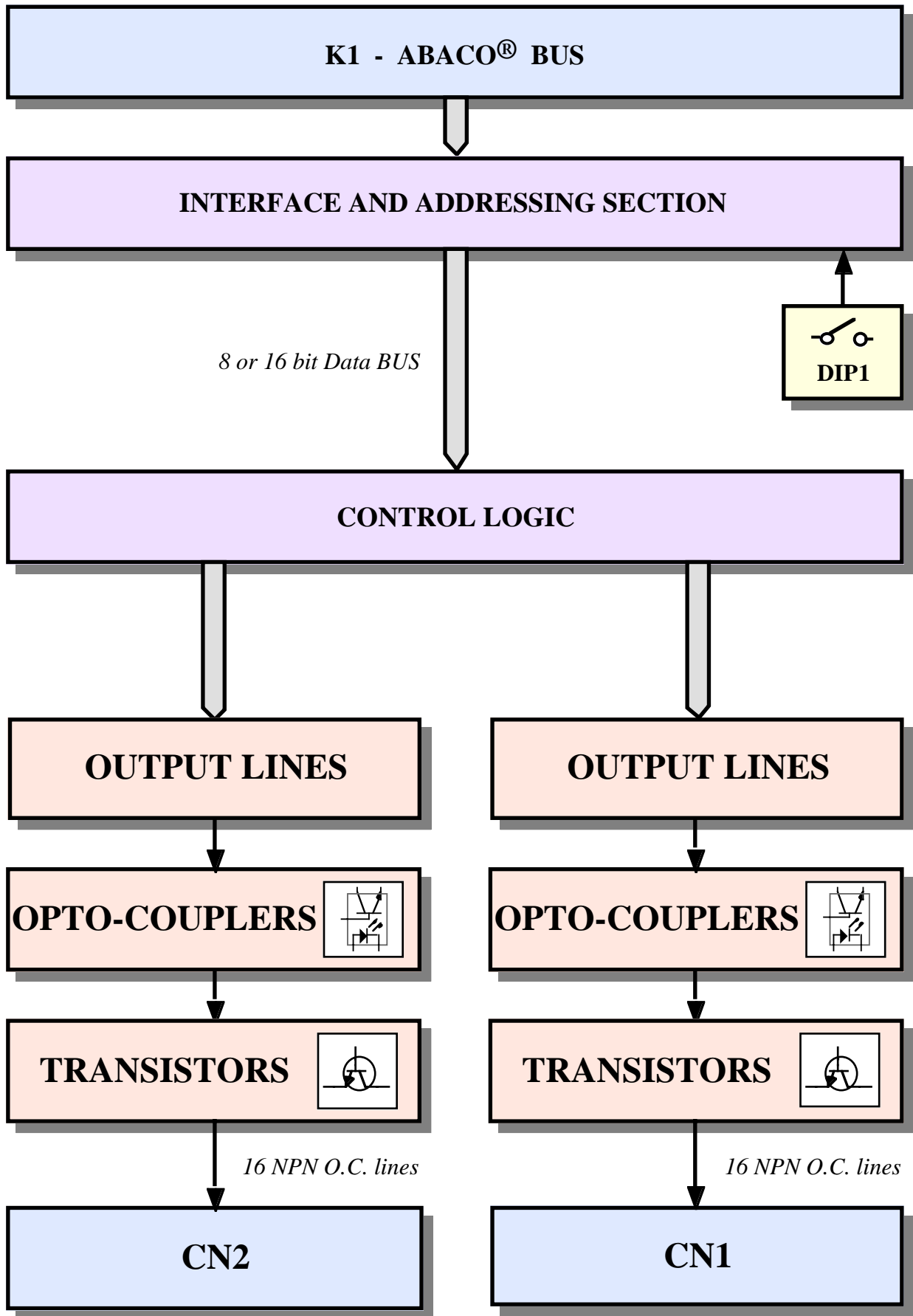


FIGURE 1: BLOCK DIAGRAM

Here follows a description of **PCO 01** board's functional blocks, with an indication of the operations performed by each one. To easily locate these blocks and verify their connections please refer to figure 1.

INTERFACING AND ADDRESSING

This section manages the data exchange between control logic and command board through **ABACO® BUS**. In particular, all written data transit across this section that, in addition, provides the board I/O management, by setting the dip switch **DIP1**. Please remark that this section can be configured to make **PCO 01** addressable in a physical space of 256 bytes.

ABACO® industrial BUS supports both 8 bits and 16 bits addressing mode.

For further information please refer to the chapter dedicated to board's software description.

CONTROL LOGIC

This section generates all the chip select signals needed to access the several peripherals on **PCO 01** boards. Using this section the programmer can interact to the board's several sections, verifying their status, setting digital input configurations, etc.

All this can be done through a simple software management based on **ABACO® BUS**, to which the control logic connects through the interfacing and addressing section. For further information please refer to the chapter dedicated to board's software description.

OUTPUT

It features two sections with 16 output signals driven by one or more latches. These components are managed through specific write registers, according to the information contained in the chapters dedicated to board's hardware and software description. Any Output signal, optocoupled and visualized through its own LED, controls a 500 mA, 30 Vdc open collector NPN transistor without heat sink.

The power supply is +5 Vdc, which supplies the on board logic circuits. This solution allows to have an unique stabilized voltage to supply the whole system.

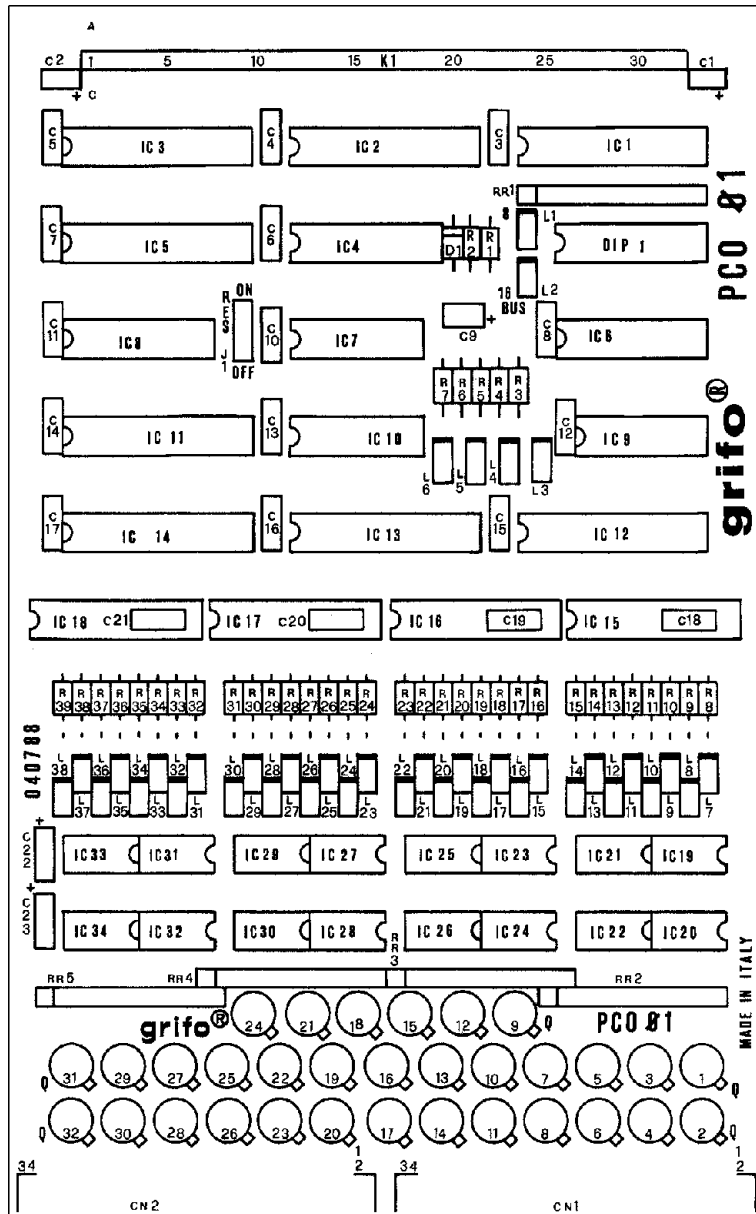


FIGURE 2: COMPONENTS MAP

TECHNICAL FEATURES

GENERAL FEATURES

On board resources:	32 Output open collector NPN transistor 1 dip switch with 8 pins to set the I/O address
BUS type:	ABACO® Industrial 8 or 16 bits data and addresses
N. addressable bytes:	256 bytes
N. bytes / words occupied:	4 / 2

PHYSICAL FEATURES

Size:	Standard EUROCARD format 100x160 mm
Weight:	164 g
Connectors:	K1: DIN 41612 64 pins M 90° A+C type C CN2: Low profile 34 pins M 90° CN1: Low profile 34 pins M 90°
Temperature range:	from 0 to 70 centigrad degrees
Relative humidity:	20% up to 90% (without condensing)

ELECTRIC FEATURES

Power supply:	+5 Vdc ± 5%
Current consumption:	570 mA
Max current on transistor:	500 mA (*)
Max voltage on transistors:	30 Vdc (*)
Max power each transistor:	500 mW (*)

(*) Values referred to a working temperature of 20 °C

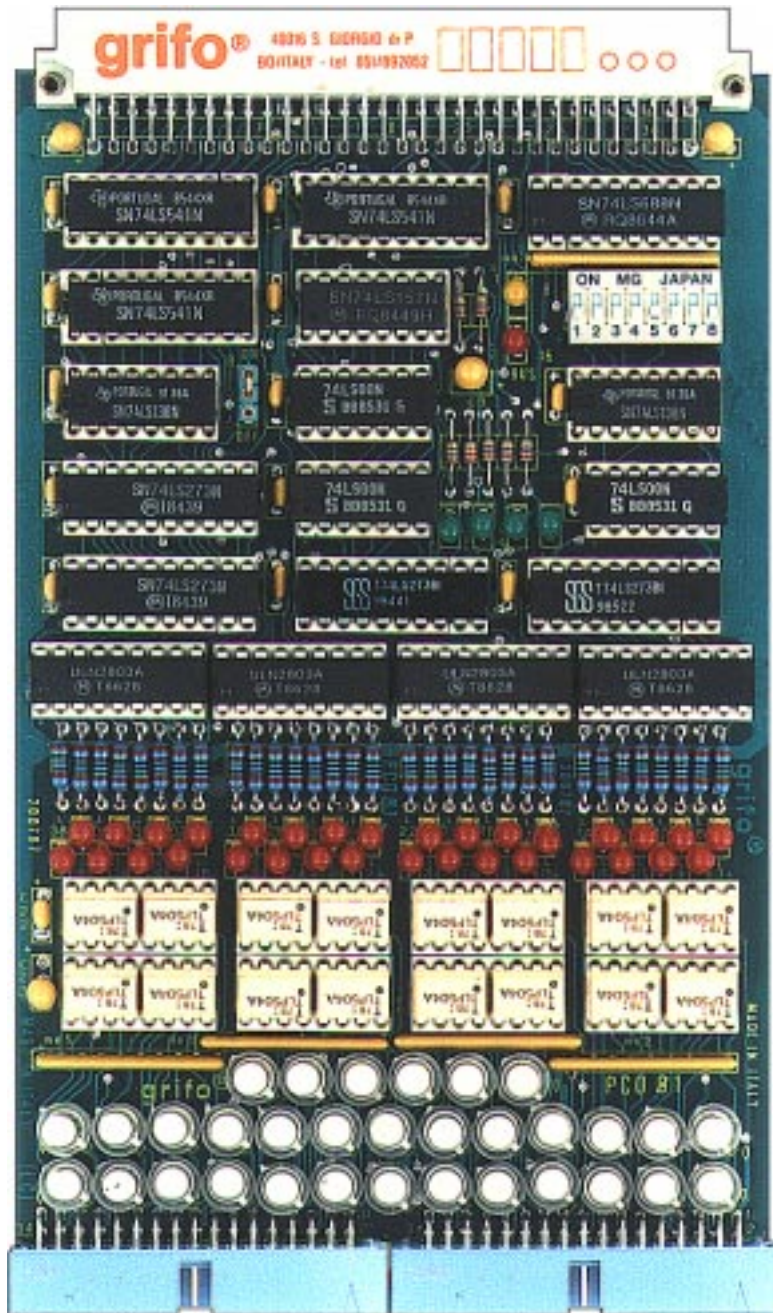


FIGURE 3: CARD PHOTO

INSTALLATION

In this chapter there are the information for a right installation and correct use of **PCO 01** card. The user can find the location and functions of each connectors, jumpers, dip switch, LEDs and some explanatory diagrams.

POWER SUPPLY

PCO 01 is provided with an efficient circuitry that solves in a comfortable and simple way the problem of the board's supply, under any condition of use.

Here follow the voltages needed:

+5 Vdc: Supplies the on board logic; must be in the range $+5 \text{ Vdc} \pm 5\%$ and must be provided through the specific pins of connector K1 (**ABACO® BUS**).

To warrant great immunity to external noise and so a correct working of the board, it is essential that **+5 Vdc** tension is galvanically isolated from any other supply in the system.

BOARD CONNECTIONS

To prevent possible connecting problems between **PCO 01** board and the external systems, the user has to read carefully the information of the previous paragraphs and he must follow these instructions:

- The NPN transistors output signals must be connected directly to the load to drive (power relays, etc.). The board provides the open collector outputs called OC OUTx.y, capable to bear a maximum current of **500 mA** with a tension that can be **+30 Vdc**. Being without heat sink, they can dissipate at most **500 mW** at a working temperature of 20 centigrad degrees.
A COMMON terminal connected to all the transistors is available.
- The TTL output signals can be connected directly only to a device featuring the same type of interface. About the correspondance between logic signals and TTL output status, remember that a logic **0** generates a TTL 0 Vdc, while a logic **1** generates a TTL +5 Vdc.

CONNECTIONS

The **PCO 01** card has 3 connectors that can be linkeded to other devices or directly to the field, according to system requirements. In this paragraph there are connectors pin outs, a short signals description (including the signals direction) and connectors location (please see figure 9), plus some figures that describe how the interface signals are connected on the card.

CN1 - TRANSISTOR OUTPUT SECTIONS A AND B CONNECTOR

The connector for NPN transistor outputs of sections A and B, called CN1, is a low profile, 2.54 mm pitch, 90 degrees, 34 pins connector. Open collector contacts of each output transistor of sections A and B and one common terminal (emitter) are present; please remark that the maximum current for each transistor is 500 mA, maximum voltage is +30 Vdc.

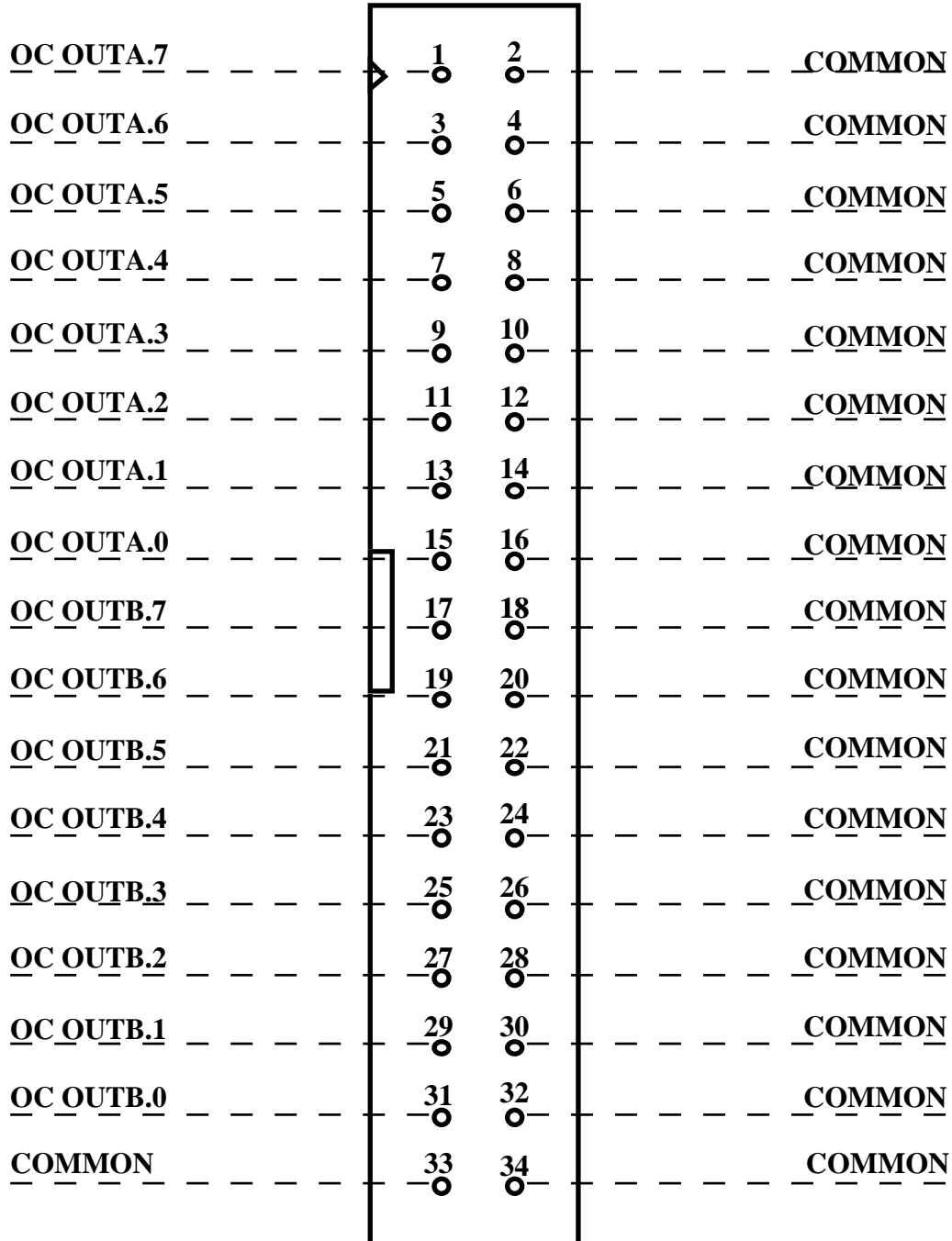


FIGURE 4: CN1 - TRANSISTOR OUTPUT SECTIONS A AND B CONNECTOR

Signals description:

- OC OUTA.n** = O - Contact of n-th open collector output in section A.
- OC OUTB.n** = O - Contact of n-th open collector output in section B.
- COMMON** = - Common contact of the 32 transistors of sections A, B, C and D.

CN2 - TRANSISTOR OUTPUT SECTIONS C AND D CONNECTOR

The connector for NPN transistor outputs of sections C and D, called CN2, is a low profile, 2.54 mm pitch, 90 degrees, 34 pins connector. Open collector contacts of each output transistor of sections A and B and one common terminal (emitter) are present; please remark that the maximum current for each transistor is 500 mA, maximum voltage is +30 Vdc.

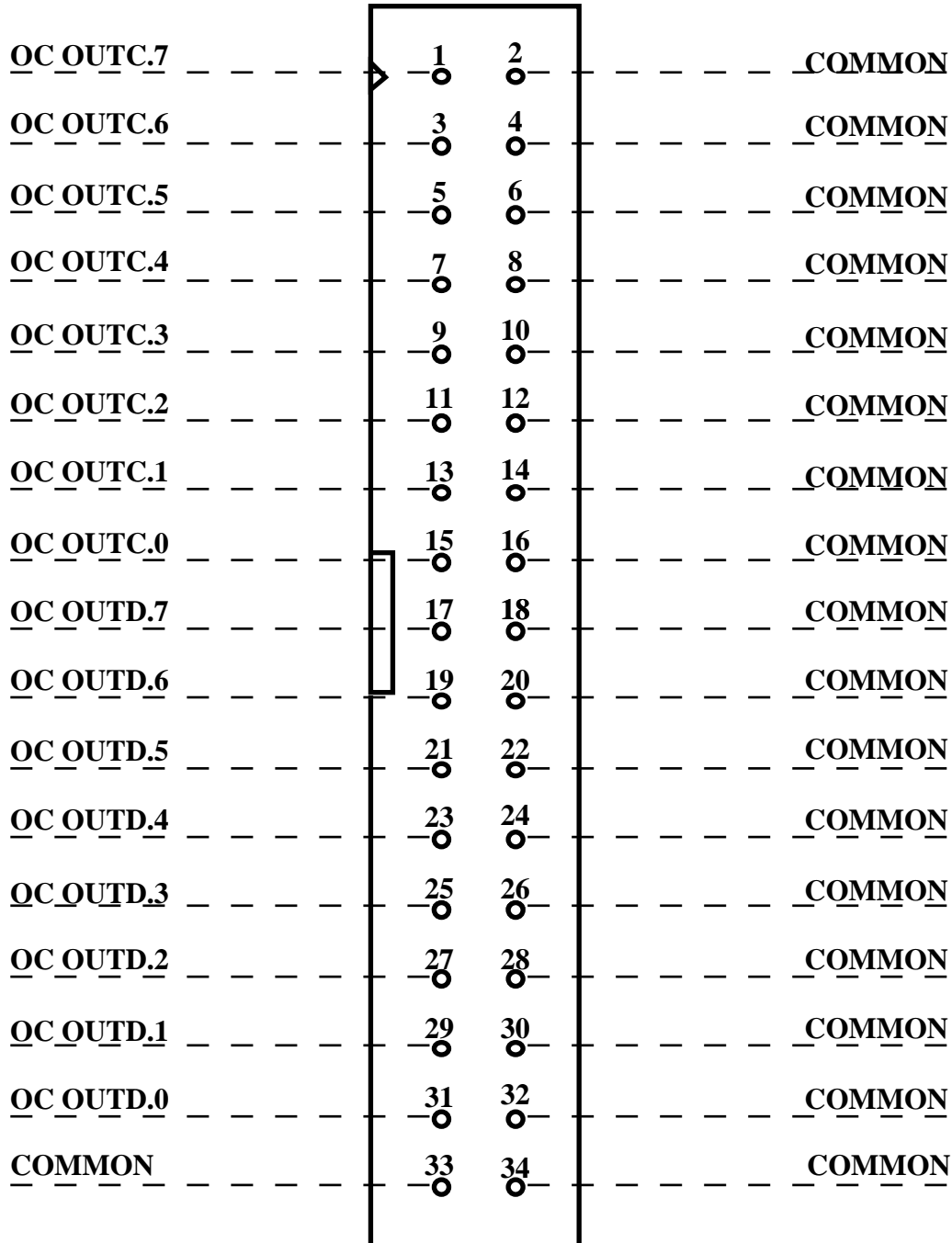


FIGURE 5: CN2 - TRANSISTOR OUTPUT SECTIONS C AND D CONNECTOR

Signals description:

- OC OUTC.n** = O - Contact of n-th open collector output in section C.
- OC OUTD.n** = O - Contact of n-th open collector output in section D.
- COMMON** = - Common contact of the 32 transistors of sections A, B, C and D.

The transistor output signals available on **PCO 01** are provided with a LED for visual feed back (the LED will light whenever the transistor is conducting); in addition they are optocoupled, to warrant galvanic separation between internal electronics and external world.

The final stage of the outputs is made by a **NPN** open collector transistor, capable to bear a maximum current of **500 mA** with a tension that can be as high as **+30 Vdc**, at a working temperature of 20 centigrad degrees.

The interface circuitry for these 32 transistors output section is shown in the following diagram.

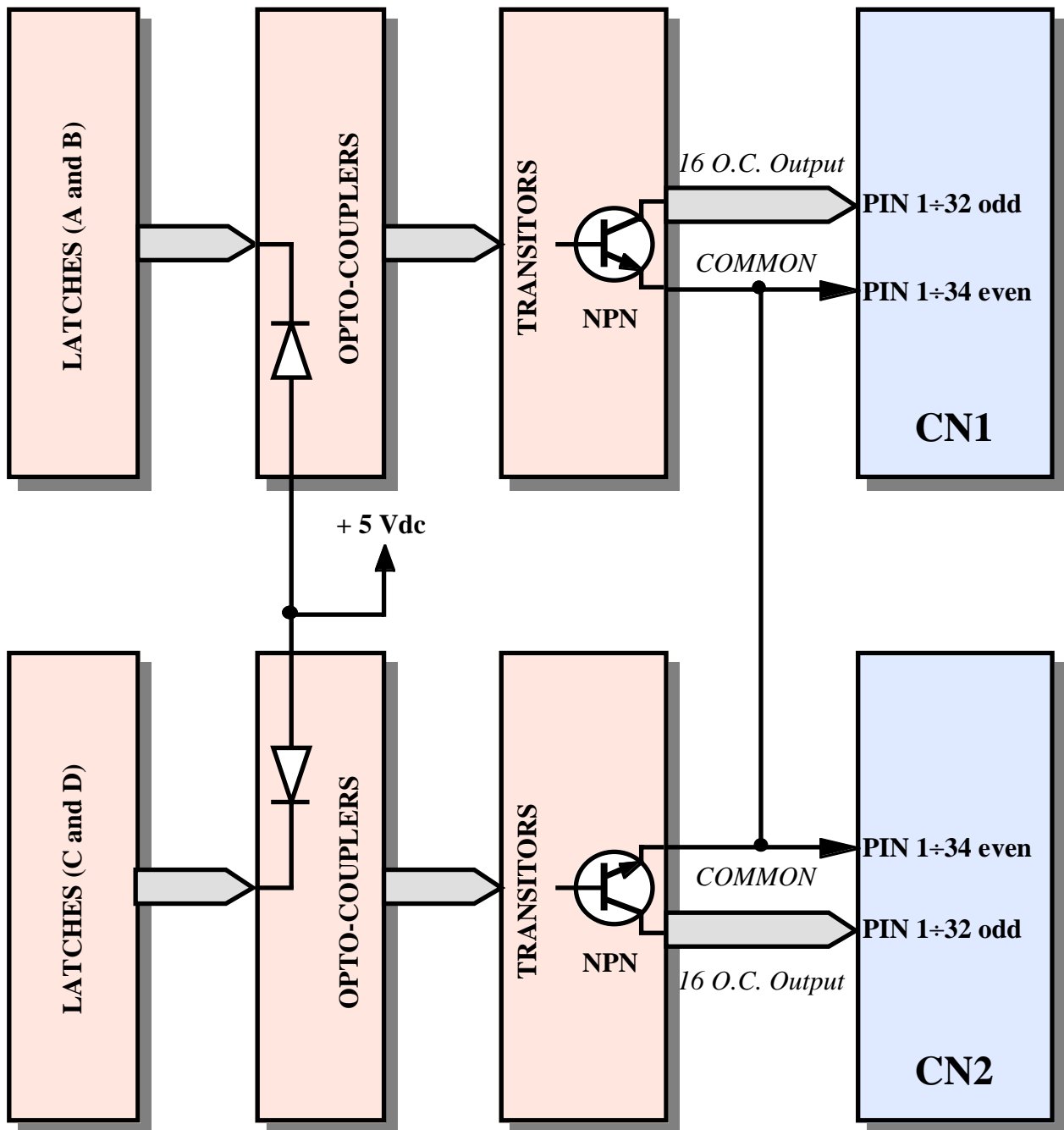


FIGURE 6: TRANSISTOR OUTPUTS BLOCK DIAGRAM

K1 - CONNECTOR FOR ABACO® BUS

The connector for ABACO® BUS, called K1 on the board, is a DIN 41612, male, 90°, type C, A+C. Here follows the pin-out of the connector installed on **PCO 01**, in addition there is the standard 8 bits and 16 bits ABACO® BUS pin-out.

Please remark that all the signals here described are TTL, except for the power supplies.

A 16 bit BUS	A 8 bit BUS	A PCO 01	PIN	C PCO 01	C 8 bit BUS	C 16 bit BUS
GND	GND	GND	1	GND	GND	GND
+5 Vdc	+5 Vdc	+5 Vdc	2	+5 Vdc	+5 Vdc	+5 Vdc
D0	D0	D0	3	D8		D8
D1	D1	D1	4	D9		D9
D2	D2	D2	5	D10		D10
D3	D3	D3	6	N.C.	/INT	/INT
D4	D4	D4	7	N.C.	/NMI	/NMI
D5	D5	D5	8	D11	/HALT	D11
D6	D6	D6	9	N.C.	/MREQ	/MREQ
D7	D7	D7	10	/IORQ	/IORQ	/IORQ
A0	A0	A0	11	N.C.	/RD	/RD LDS
A1	A1	A1	12	/WR	/WR	/WR LDS
A2	A2	A2	13	D12	/BUSAK	D12
A3	A3	A3	14	N.C.	/WAIT	/WAIT
A4	A4	A4	15	D13	/BUSRQ	D13
A5	A5	A5	16	N.C.	/RESET	/RESET
A6	A6	A6	17	/M1	/M1	/IACK
A7	A7	A7	18	D14	/RFSH	D14
A8	A8	N.C.	19	N.C.	/MEMDIS	/MEMDIS
A9	A9	N.C.	20	N.C.	VDUSEL	A22
A10	A10	N.C.	21	D15	/IEI	D15
A11	A11	N.C.	22	N.C.		
A12	A12	N.C.	23	N.C.	CLK	CLK
A13	A13	N.C.	24	N.C.		/RD UDS
A14	A14	N.C.	25	/WR UDS		/WR UDS
A15	A15	N.C.	26	N.C.		A21
A16		N.C.	27	N.C.		A20
A17		N.C.	28	N.C.		A19
A18		N.C.	29	N.C.	/R.T.	/R.T.
+12 Vdc	+12 Vdc	N.C.	30	N.C.	-12 Vdc	-12 Vdc
+5 Vdc	+5 Vdc	+5 Vdc	31	+5 Vdc	+5 Vdc	+5 Vdc
GND	GND	GND	32	GND	GND	GND

FIGURE 7: K1 - CONNECTOR FOR ABACO® BUS

Signals description:

8 bits CPU

A0-A15	=	O	- Address BUS
D0-D7	=	I/O	- Data BUS
/INT	=	I	- Interrupt request
/NMI	=	I	- Non Maskable Interrupt
/HALT	=	O	- Halt state
/MREQ	=	O	- Memory Request
/IORQ	=	O	- Input Output Request
/RD	=	O	- Read cycle status
/WR	=	O	- Write cycle status
/BUSAK	=	O	- BUS Acknowledge
/WAIT	=	I	- Wait
/BUSRQ	=	I	- BUS Request
/RESET	=	O	- Reset
/M1	=	O	- Machine cycle one
/RFSH	=	O	- Refresh for dynamic RAM
/MEMDIS	=	I	- Memory Display
/VDUSEL	=	O	- VDU Selection
/IEI	=	I	- Interrupt Enable Input
CLK	=	O	- System clock
/R.T.	=	I	- Reset button
+5 Vdc	=	I	- Power supply at +5 Vdc
+12 Vdc	=	I	- Power supply at +12 Vdc
-12 Vdc	=	I	- Power supply at -12 Vdc
GND	=		- Ground signal
N. C.	=		- Not connected

16 bits CPU

A0-A22	=	O	- Address BUS
D0-D15	=	I/O	- Data BUS
/RD UDS	=	O	- Read Upper Data Strobe
/WR UDS	=	O	- Write Upper Data Strobe
/IACK	=	O	- Interrupt Acknowledge
/RD LDS	=	O	- Read Lower Data Strobe
/WR LDS	=	O	- Write Lower Data Strobe

NOTE

Directionality indications as above stated are referred to a master (GPC®) board and have been kept untouched to avoid ambiguity in case of multi-boards systems.

VISUAL SIGNALATIONS

PCO 01 card is provided with signalation LEDs to show several status informations, as described in the following table:

LED	COLOUR	PURPOSE
L1	Yellow	If ON, indicates 8 bits data BUS selection.
L2	Red	If ON, indicates 16 bits data BUS selection.
L3	Green	If ON, indicates that at least one write operation to section A outputs has been performed since a reset or a Power On occurred.
L4	Green	If ON, indicates that at least one write operation to section B outputs has been performed since a reset or a Power On occurred.
L5	Green	If ON, indicates that at least one write operation to section C outputs has been performed since a reset or a Power On occurred.
L6	Green	If ON, indicates that at least one write operation to section D outputs has been performed since a reset or a Power On occurred.
L7÷L14	Red	Visualize the status of the eight section A NPN transistor output lines, respectively OC OUTA.7÷OC OUTA.0. A LED ON means open collector transistor conducting.
L15÷L22	Red	Visualize the status of the eight section B NPN transistor output lines, respectively OC OUTB.7÷OC OUTB.0. A LED ON means open collector transistor conducting.
L23÷L30	Red	Visualize the status of the eight section C NPN transistor output lines, respectively OC OUTC.7÷OC OUTC.0. A LED ON means open collector transistor conducting.
L31÷L38	Red	Visualize the status of the eight section D NPN transistor output lines, respectively OC OUTD.7÷OC OUTD.0. A LED ON means open collector transistor conducting.

FIGURE 8: VISUAL SIGNALATIONS TABLE

The main purpose of LEDs is to show a visual indication about the card's status, making so easier debug and verify operations. To easily locate these visual signalations please refer to the figure 9.

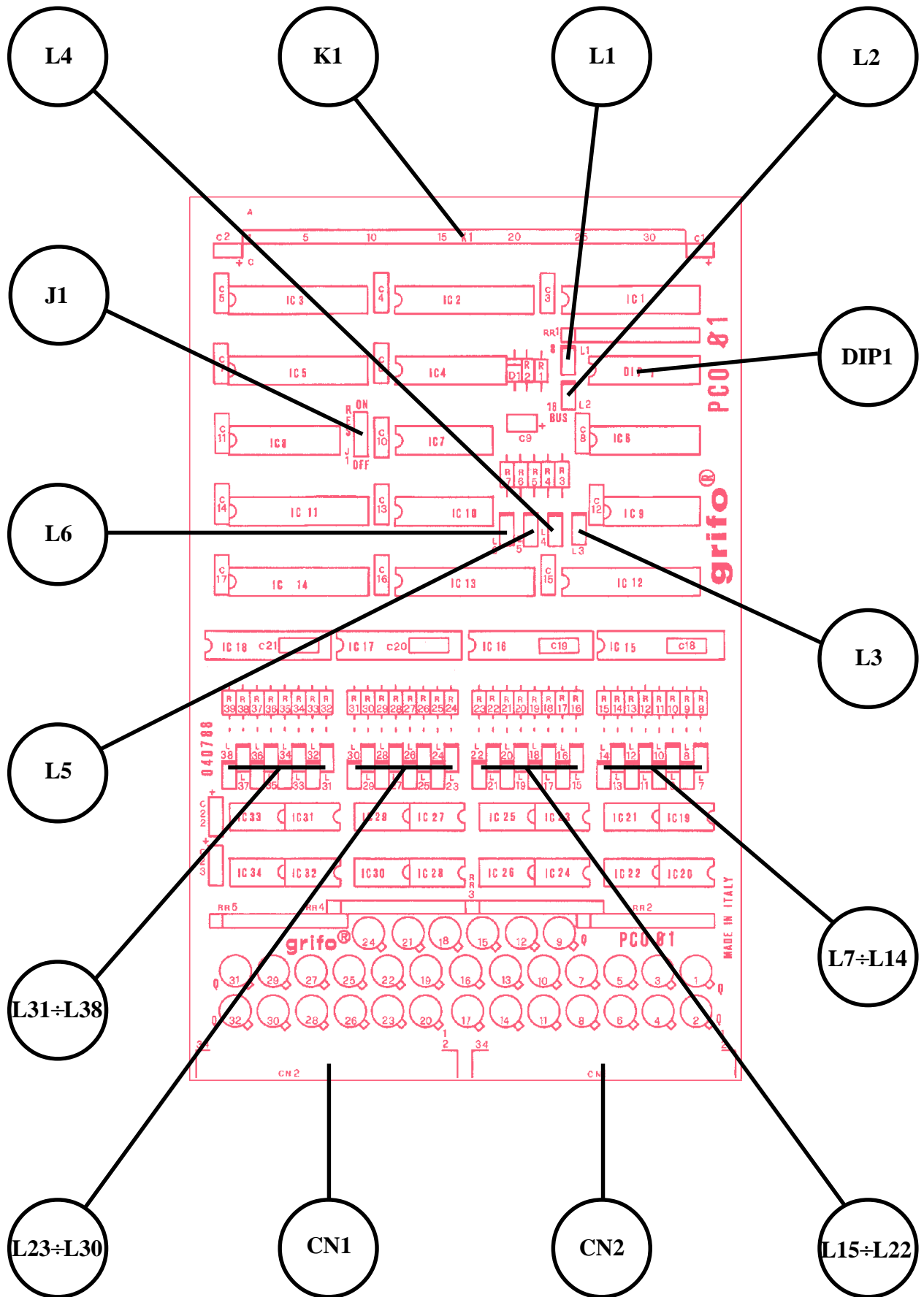


FIGURE 9: CONNECTORS, DIP SWITCH, LEDs AND JUMPERS LOCATION

JUMPERS

On **PCO 01** board there are two jumpers to configure the card. Below there is the jumpers list, location and function.

The following tables describe all the right connections of **PCO 01** jumpers with their relative functions. To recognize these valid connections, please refer to the board printed diagram (serigraph) or to figure 2 of this manual, where the pins numeration is listed; for recognizing jumpers location, please refer to figure 9.

The "*" used in the following tables, denotes the default connection, or on the other hand the connection set up at the end of testing phase, that is the configuration the user receives.

JUMPER	CONNECTIONS	PURPOSE	DEF.
DIP1.1	OFF	Configures the board to be managed through a 16 bits data BUS.	*
	ON	Configures the board to be managed through an 8 bits data BUS.	
J1	OFF	It does not connect /RESET signal coming from ABACO [®] BUS to on board circuitry.	
	ON	It connects /RESET signal coming from ABACO [®] BUS to on board circuitry.	

FIGURE 10: JUMPERS SUMMARIZING TABLE

RESET CIRCUITRY CONFIGURATION

Through jumper **J1**, as described in the next paragraph, the user may select whether to connect or not the /RESET signal coming from **ABACO**[®] BUS to the specific circuitry on the board **PCO 01**; if the jumper is **connected in position ON**, when the /RESET is active the board's outputs are **disabled**. Viceversa if the jumper is **connected in position OFF**, /RESET signal **doesn't affect** the status of the outputs, that are disabled whenever a Power-On occurs. This feature is essential when, for example, the outputs must not change status for a control board's reset due to, for example, an intervent of its on board Watch Dog circuitry.

HARDWARE DESCRIPTION

This chapter provides all the hardware information needed to use **PCO 01** board. Here the user will find information about I/O card mapping and on board peripheral devices addressing.

BOARD MAPPING

PCO 01 board is mapped into a **4** bytes I/O addressing space (or two words in 16 bits addressing mode), that can be mapped starting from different base addresses according to how the board is configured. This feature allows to use several **PCO 01** cards on the same **ABACO®** BUS, or to install them on a BUS where other peripheral modules are installed obtaining a structure that can be expanded without any difficulty or modifications to the application software.

The base address can be defined through the specific BUS interface circuitry on the board itself; this circuitry uses the eight pins dip switch called **DIP1**, from which it reads the address set by the user. Here follows the corrispondance between dips configuration and address signals.

DIP1.1	->	<i>Please see paragraph "JUMPERS"</i>
DIP1.2	->	<i>Don't care</i> <u>8 bits BUS data path (DIP1.1 ON)</u> <i>Address A1</i> <u>16 bits BUS data path (DIP1.1 OFF)</u>
DIP1.3	->	Address A2
DIP1.4	->	Address A3
DIP1.5	->	Address A4
DIP1.6	->	Address A5
DIP1.7	->	Address A6
DIP1.8	->	Address A7

These dips are driven in complemented logic, this means that if a switch is **ON** generates a **logic zero**, viceversa if a switch is **OFF** generates a **logic one**.

When the board is configured for 16 bits data BUS management, DIP1.2 must be ON, so the board can be mapped only from addresses where **A1=0**.

NOTE

When allocating the mapping address of the boards, please be careful not to allocate more than one device in the same addressing space (count also the number of bytes occupied by the card). If this condition will not be respected, a BUS conflict will happen; such conflict will compromise the correct working of the whole system.

As an example, possible mappings are reported here.

- 1) Address used to map **PCO 01**: 048H.
Control board used: featuring 8 bits addressing mode.

DIP1.1	->	ON
DIP1.2	->	Don't care
DIP1.3	->	ON
DIP1.4	->	OFF
DIP1.5	->	ON
DIP1.6	->	ON
DIP1.7	->	OFF
DIP1.8	->	ON

- 2) Address used to map **PCO 01**: A4H.
Control board used: featuring 8 bits addressing mode.

DIP1.1	->	OFF
DIP1.2	->	ON
DIP1.3	->	OFF
DIP1.4	->	ON
DIP1.5	->	ON
DIP1.6	->	OFF
DIP1.7	->	ON
DIP1.8	->	OFF

To easily locate the above mentioned components please refer to figure 9.

INTERNAL REGISTERS ADDRESSING

Indicating the board base address with <baseaddr>, that is the address set using dip switch DIP1, as indicated in the previous paragraph, **PCO 01** internal registers are addressable as explained in the following tables, respectively when addressing mode is 8 bit and 16 bit.

INTERNAL REGISTERS ADDRESSING FOR 8 BIT ADDRESSING MODE

DEVICE	REG.	ADDRESS	R/W	MEANING
OUTPUT A	OUTA	<baseaddr>+00H	W	Register to set the 8 transistor NPN output lines of section A.
OUTPUT B	OUTB	<baseaddr>+01H	W	Register to set the 8 transistor NPN output lines of section B.
OUTPUT C	OUTC	<baseaddr>+02H	W	Register to set the 8 transistor NPN output lines of section C.
OUTPUT D	OUTD	<baseaddr>+03H	W	Register to set the 8 transistor NPN output lines of section D.

FIGURE 11: INTERNAL REGISTERS ADDRESSING TABLE FOR 8 BIT ADDRESSING MODE

INTERNAL REGISTERS ADDRESSING FOR 16 BIT ADDRESSING MODE

DEVICE	REG.	ADDRESS	R/W	PURPOSE
OUTPUT C, A	OUTCA	<baseaddr>+00H	W	Register to set the 16 NPN transistor output lines of section C (byte H) and section A (byte L).
OUTPUT D, B	OUTDB	<baseaddr>+02H	W	Register to set the 16 NPN transistor output lines of section D (byte H) and section B (byte L).

FIGURE 12: INTERNAL REGISTERS ADDRESSING TABLE FOR 16 BIT ADDRESSING MODE

PERIPHERAL DEVICES SOFTWARE DESCRIPTION

In the previous paragraph allocation addresses of all the peripherals have been reported, here follows a detailed description of function and meaning of internal registers (please always refer to the peripheral mapping tables to understand completely the following informations). Should the present documentaion be inadequate please refer to the component's manufacturer documentation.

In the following paragraphs the indications **D0÷D7** or **D0÷D15** are used to refer the bits of the byte or word involved in the I/O operations.

TRANSISTOR OUTPUTS

Input registers (called OUTA, OUTB, OUTC and OUTD when using an 8 bit data BUS or OUTCA and OUTDB when using an 16 bit data BUS) perform the input management on **PCO 01** board. The bits of these registers have the following meaning:

8 bits data BUS

OUTC.D7 -> OC OUTC.7
 OUTC.D6 -> OC OUTC.6
 OUTC.D5 -> OC OUTC.5
 OUTC.D4 -> OC OUTC.4
 OUTC.D3 -> OC OUTC.3
 OUTC.D2 -> OC OUTC.2
 OUTC.D1 -> OC OUTC.1
 OUTC.D0 -> OC OUTC.0

OUTA.D7 -> OC OUTA.7
 OUTA.D6 -> OC OUTA.6
 OUTA.D5 -> OC OUTA.5
 OUTA.D4 -> OC OUTA.4
 OUTA.D3 -> OC OUTA.3
 OUTA.D2 -> OC OUTA.2
 OUTA.D1 -> OC OUTA.1
 OUTA.D0 -> OC OUTA.0

OUTD.D7 -> OC OUTD.7
 OUTD.D6 -> OC OUTD.6
 OUTD.D5 -> OC OUTD.5
 OUTD.D4 -> OC OUTD.4
 OUTD.D3 -> OC OUTD.3
 OUTD.D2 -> OC OUTD.2
 OUTD.D1 -> OC OUTD.1
 OUTD.D0 -> OC OUTD.0

16 bits data BUS

OUTCA.D15 -> OC OUTC.7
 OUTCA.D14 -> OC OUTC.6
 OUTCA.D13 -> OC OUTC.5
 OUTCA.D12 -> OC OUTC.4
 OUTCA.D11 -> OC OUTC.3
 OUTCA.D10 -> OC OUTC.2
 OUTCA.D9 -> OC OUTC.1
 OUTCA.D8 -> OC OUTC.0

OUTCA.D7 -> OC OUTA.7
 OUTCA.D6 -> OC OUTA.6
 OUTCA.D5 -> OC OUTA.5
 OUTCA.D4 -> OC OUTA.4
 OUTCA.D3 -> OC OUTA.3
 OUTCA.D2 -> OC OUTA.2
 OUTCA.D1 -> OC OUTA.1
 OUTCA.D0 -> OC OUTA.0

OUTDB.D15 -> OC OUTD.7
 OUTDB.D14 -> OC OUTD.6
 OUTDB.D13 -> OC OUTD.5
 OUTDB.D12 -> OC OUTD.4
 OUTDB.D11 -> OC OUTD.3
 OUTDB.D10 -> OC OUTD.2
 OUTDB.D9 -> OC OUTD.1
 OUTDB.D8 -> OC OUTD.0

8 bits data BUS

OUTB.D7 -> OC OUTB.7
 OUTB.D6 -> OC OUTB.6
 OUTB.D5 -> OC OUTB.5
 OUTB.D4 -> OC OUTB.4
 OUTB.D3 -> OC OUTB.3
 OUTB.D2 -> OC OUTB.2
 OUTB.D1 -> OC OUTB.1
 OUTB.D0 -> OC OUTB.0

16 bits data BUS

OUTDB.D7 -> OC OUTB.7
 OUTDB.D6 -> OC OUTB.6
 OUTDB.D5 -> OC OUTB.5
 OUTDB.D4 -> OC OUTB.4
 OUTDB.D3 -> OC OUTB.3
 OUTDB.D2 -> OC OUTB.2
 OUTDB.D1 -> OC OUTB.1
 OUTDB.D0 -> OC OUTB.0

The indication **OC OUTx.y** stands for sections A, B, C and D. Their input signals are available on connectors CN1 and CN2.

Performing an input operation at the address of the above mentioned registers the corresponding optocoupled input signals are acquired.

The correspondance between status of an input and value of a bit is:

Bit at logic 0 -> Output disabled = NPN open collector transistor disengaged
 Bit at logic 1 -> Output enabled = NPN open collector transistor conducting

All registers are reset (all bits are 0) when a Reset or a Power On occur if **J1** is connected in position ON, this disables all the outputs and so disables all the open collector transistors.

EXTERNAL CARDS

PCO 01 board can interface to most of **grifo**[®] industrial boards. Their main purpose is to perform a digital Inpu/Output interfacement between CPU (**GPC**[®]) cards and the external world.

Here is reported an illustrative list of cards capable to interact with **PCO 01** board with a short description of their features; for further informations please request the specific documentation.

MB3 01-MB4 01-MB8 01

Mother Board 3, 4, 8 slots

Motherboard featuring 3, 4 or 8 slots of **ABACO**[®] industrial BUS; pitch 4 TE; standard power supply connectors; LEDs for visual feed-back of power supply; holes for rack docking.

SPB 04-SPB 08

Switch Power BUS 4-8 slots

Motherboard featuring 4-8 slots of **ABACO**[®] industrial BUS; pitch 4 TE; standard power supply connectors; termination resistances; connector type F for **SPC xxx** supply ; holes for rack docking.

ABB 03

ABACO[®] Block BUS 3 slots

3 slots **ABACO**[®] mother board; 4 TE pitch connectors; **ABACO**[®] I/O BUS connector; screw terminal for power supply; connection for DIN C type and Ω rails.

ABB 05

ABACO[®] Block BUS 5 slots

5 slots **ABACO**[®] mother board with power supply. Double power supply built in; 5Vdc 2,5A section for powering the on board logic; second section at 24Vdc 400mA galvanically coupled, for the optocoupled input lines. Auxiliary connector for **ABACO**[®] I/O BUS. Connection for DIN Ω rails.

SBP 02-xx

Switch BLOCK Power xx version

Low cost switching power supply able to generate voltage from +5 to +40 Vdc and current up to 2.5 A; Input from 12 to 24 Vac; Connection for DIN C Type and Ω rails.

SPC 03.5S

Switch Power Card +5 Vdc

Europe format switching power supply capable to provide +5 Vdc to a load of 4 A; input voltage 12÷24 Vac; power-failure; connector for back-up battery; standard connector for mother board **SPB 0x**.

SPC 512

Switch Power Card +5 Vdc +12 Vdc

Europe format switching power supply capable to provide +5 Vdc 5A and +12 Vdc 2.5 A; input voltage 12÷24 Vac; power-failure; connector for back-up battery; standard connector for mother board **SPB 0x**.

GPC® 153

General Purpose Controller Z80

84C15 μ P, 10÷16 MHz; Full CMOS; 1 RS 232 line; 1 RS 232 or RS 422-485 or Current Loop line; 16 TTL I/O lines; 8 A/D 12 bits lines; 2÷4 Timers Counters; 512K EPROM or FLASH; 512K RAM and RTC backed; 8K serial EEPROM; Buzzer; 1 Activity LED; Watch dog; 8 readable DIPs; LCD Interface.

GPC® 183

General Purpose Controller Z180

Z180 μ P, 10÷16 MHz; Full CMOS; 1 RS 232 line; 1 RS 232 or RS 422-485 or Current Loop line; 24 TTL I/O lines; 11 A/D 12 bits lines; 2 Timers Counters; 512K EPROM or FLASH; 512K RAM and RTC backed; 8K serial EEPROM; Buzzer; 2 Activity LED; Watch dog; 4 readable DIPs; LCD Interface.

GPC® 324/D

“4” Type General Purpose Controller 80C32/320

80C32 or 80C320 μ P, 14÷22 MHz; Full CMOS; 1 RS 232 line; 1 RS 232 or RS 422-485 or Current Loop line; 4÷16 TTL I/O lines; 3 Timers Counters; 64K EPROM; 64K RAM; 32K RAM backed; 32K DIL E2; 8K serial EEPROM; Watch dog; 1 readable DIP; LCD Interface; Abaco® I/O BUS; 5Vdc Power supply; Size: 100x50 mm.

GPC® 554

General Purpose Controller 80C552

Microprocessor 80C552 at 22 MHz; implementation completely CMOS; 32K EPROM; 32 K SRAM; 32 K EEPROM or SRAM; EEPROM; 2 RS 232 serial lines; 16 I/O TTL; 2 PWM lines; 16 bits Timer/Counter; Watch Dog; 6 signals A/D converter with resolution 10 bit; interface for **ABACO®** I/O BUS.

GPC® 154

“4” Type General Purpose Controller Z80

84C15 μ P, 10÷16 MHz; Full CMOS; 1 RS 232 line; 1 RS 232 or RS 422-485 line; 16 TTL I/O lines; 2÷4 Timers Counters; 512K EPROM or FLASH; 512K RAM and RTC backed; 8K serial EEPROM; Watch dog; 2 readable DIPs; LCD Interface; Abaco® I/O BUS; 5Vdc Power supply; Size: 100x50 mm.

GPC® 884

General Purpose Controller Am188ES

Microprocessor AMD Am188ES up to 40 MHz 16 bits; implementation completely CMOS; serie 4 format; 512K EPROM or FLASH; 512K SRAM backed with Lithium battery; RTC; 1 RS 232 serial line + 1 RS 232 or RS 422-485 or current loop; 16 I/O TTL; 3 timer/counter; watch dog; EEPROM; 11 signals A/D converter with 12 bit resolution; interface for **ABACO®** I/O BUS.

GPC® 114

General Purpose Controller 68HC11

Microprocessor 68HC11A1 at 8 MHz; implementation completely CMOS; serie 4 format; 32K EPROM; 32K SRAM backed with Lithium battery; 32K EPROM, SRAM, EEPROM; RTC; 1 serial line RS 232 or RS 422-485; 10 I/O TTL; 3 timer/counter; watch dog; 8 signals A/D converter with resolution 8 bit; 1 asynchronous serial line; extremely low power consumption; interface for **ABACO®** I/O BUS.

GPC® 51

General Purpose Controller fam. 51

Microprocessor family 51 INTEL including the masked BASIC chip; the board features: 16 I/O TTL lines; dip switch; 3 timer/counter; RS 232; 4 A/D converter signals resolution 11 bit; buzzer; on board EPROM programmer; RTC and 32K SRAM with Lithium battery back up; controller for display and keyboard.

GPC® 188F

General Purpose Controller 80C188

80C188 μ P 20MHz; 1 RS 232 line; 1 RS 232, RS 422-485 or Current Loop line; 24 TTL I/O lines; 1MEPROM or 512K FLASH; 1MRAMLithium battery backed; 8K serial EEPROM; RTC; Watch Dog; 8 Dip switch; 3 Timer Counter; 8 13 bit A/D lines; Power failure; activity LEDs; single power supply +5Vdc.

GPC® 15A

General Purpose Controller 84C15

Full CMOS card, 10÷20 MHz 84C15 CPU; 512K EPROM or FLASH; 128K RAM; 8K RAM and RTC backed; 8K serial EEPROM; 1 RS 232 line; 1 RS 232 line or RS 422-485 or Current Loop line; 32 or 40 TTL I/O lines; CTC; Watch dog; 2 Dip switches; Buzzer.

GPC® 150

General Purpose Controller 84C15

Microprocessor Z80 at 16 MHz; implementation completely CMOS; 512K EPROM or FLASH; 512K SRAM; RTC; Back-Up through external Lithium battery; 4M serial FLASH; 1 serial line RS 232 plus 1 RS 232 or RS 422-485 or current loop; 40 I/O TTL; 2 timer/counter; 2 watch dog; dip switch; EEPROM; A/D converter with resolution 12 bit; activity LED.

GPC® 15R

General Purpose Controller 84C15

84C15 μ P, 10÷16 MHz; 1 RS 232 line; 1 RS 232 or RS 422-485 or C. L. line; 16÷24 TTL I/O lines; 16 Opto-in; 8 Relays; 4 Opto Coupled Timers Counters; 512K EPROM or FLASH; 512K RAM and RTC backed; 8K serial EEPROM; 8K Backed RAM modul; Buzzer; 1 Activity LED; Watch dog; 4÷12 readable DIPs; LCD Interface.

GPC® 323

General Purpose Controller 51 family

80C32 μ P, 14 MHz; Full CMOS; 1 RS 232 line (software); 1 RS 232 or RS 422-485 or Current Loop line; 24 TTL I/O lines; 11 A/D 12 bits lines; 3 Timers Counters; 64K EPROM; 64K RAM; 32K RAM and RTC backed; 32K DIL EEPROM; 8K serial EEPROM; Buzzer; 2 Activity LED; Watch dog; 5 readable DIPs; LCD Interface.

GPC® 553

General Purpose Controller 80C552

80C552 μ P, 22÷33 MHz; 1 RS 232 line (software); 1 RS 232 or RS 422-485 or Current Loop line; 16 TTL I/O lines; 8 A/D 10 bits lines; 3 Timers Counters; 64K EPROM; 64K RAM; 32K RAM and RTC backed; 32K DIL EEPROM; 8K serial EEPROM; 2 PWM lines; 1 Activity LED; Watch dog; 5 readable DIPs; LCD Interface.

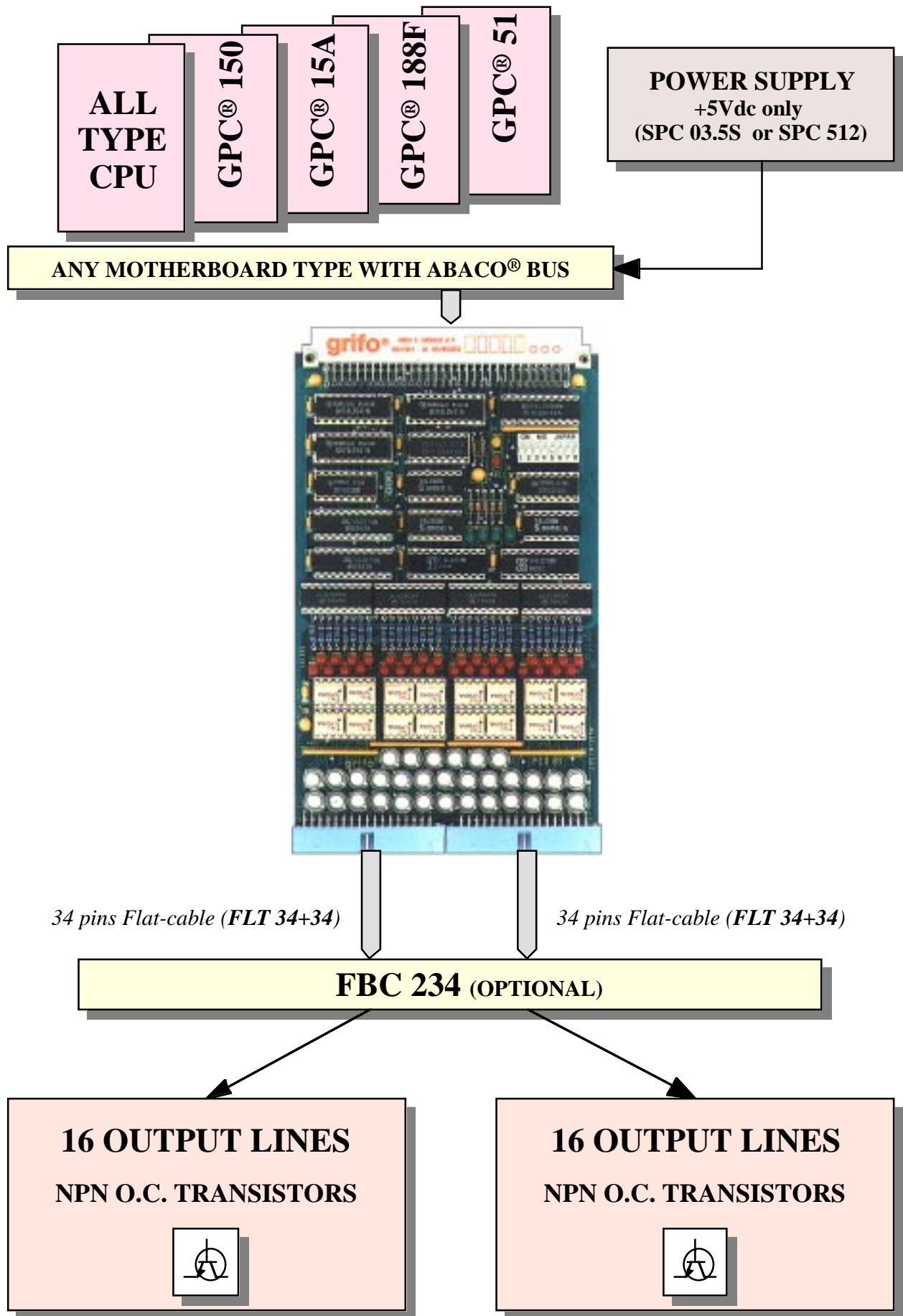


FIGURE 13: POSSIBLE CONNECTIONS DIAGRAM

PBI 01

PNP BLOCK Input

Interface for PNP drivers through NPN inputs; 16 inputs for driver PNP, visualized by LEDs; 16 NPN outputs on **ABACO**[®] standard input connector; Plastic mount for rails DIN 46277-1 and 3.

FBC 20-120

Flat Block Contact 20 vie

Interface for 2 or 1 mounting cable connectors (low profile 20 pins male) and quick release screw terminal connectors; Plastic mount for rails DIN 46277-1 and 3.

FBC 34

Flat Block Contact 34 vie

Interface for 2 mounting cable connector (low profile 34 pins male) and quick release screw terminal connectors; Plastic mount for rails DIN 46277-1 and 3.

FBC L20

Flat Block Contact LED 20 vie

Interface for 1 mounting cable connector (low profile 20 pins male, featuring **ABACO**[®] standard Input pin out, and quick release screw terminal connectors; All the signals are visualized through LEDs; Plastic mount for rails DIN 46277-1 and 3.

FBC L34

Flat Block Contact LED 34 vie

Interface for 2 mounting cable connectors (low profile 34 and 20 pins male) and quick release screw terminal connectors; featuring **ABACO**[®] standard Input and Output pin out; All the signals are visualized through LEDs; Plastic mount for rails DIN 46277-1 and 3.

BIBLIOGRAPHY

Here follows a list of manuals and technical notes that the User can read to acquire more informations about **PCO 01** board.

Manual SGS-THOMSON: *Industrial and Computer Peripheral ICs - Data Book*

Manual SGS-THOMSON: *Small Signal Transistors - Data Book*

Manual TEXAS INSTRUMENTS: *The TTL data Book - SN54/74 Families*

Manual TOSHIBA: *Photo Couplers - Data Book*

Please connect to the manufactures Web sites to get the latest version of all manuals and data sheets.



APPENDIX A: ALPHABETICAL INDEX

A

ABACO® BUS 4, 6, 8, 12, 17
ADDRESSABLE BYTES 6
ADDRESSING 4, 19
ADDRESSING SPACE 17

B

BIBLIOGRAPHY 27
BOARD CONNECTIONS 8
BOARD MAPPING 17
BYTES / WORDS OCCUPIED 6

C

CARD VERSION 1
CONNECTIONS 8
CONNECTORS 6
 CN1 9
 CN2 10
 K1 12
CONTROL LOGIC 4
CURRENT CONSUMPTION 6

D

DIP SWITCH 6
DIP1 4, 17, 19

E

ELECTRIC FEATURES 6
EXTERNAL CARDS 22

G

GENERAL FEATURES 6
GENERAL INFORMATION 2

I

INSTALLATION 8
INTERFACING 4
INTERNAL REGISTERS ADDRESSING 19
INTRODUCTION 1

L

LEDS 4, 14

M

MAX CURRENT ON TRANSISTOR 6

MAX POWER EACH TRANSISTOR 6

MAX VOLTAGE ON TRANSISTOR 6

N

NPN OUTPUT 21

O

OUTPUT 20

P

PERIPHERAL DEVICES SOFTWARE DESCRIPTION 20

PHYSICAL FEATURES 6

POWER SUPPLY 6, 8

R

REGISTERS 19

RELATIVE HUMIDITY 6

RESET 16

RESET CIRCUITRY CONFIGURATION 16

S

SIZE 6

T

TECHNICAL FEATURES 6

TEMPERATURE RANGE 6

TRANSISTOR NPN DIGITAL OUTPUTS 9, 6, 10

TTL 8

V

VISUAL SIGNALATIONS 14

W

WEIGHT 6