MCI 64

Memory Card Interface 64 MBytes

TECHNICAL MANUAL

PRELIMINARY

grifo®
ITALIAN TECHNOLOGY

Via dell' Artigiano, 8/6
40016 San Giorgio di Piano
(Bologna) ITALY
E-mail: grifo@grifo.it
http://www.grifo.it http://www.grifo.com
Tel. +39 051 892.052 (a. r.) FAX: +39 051 893.661

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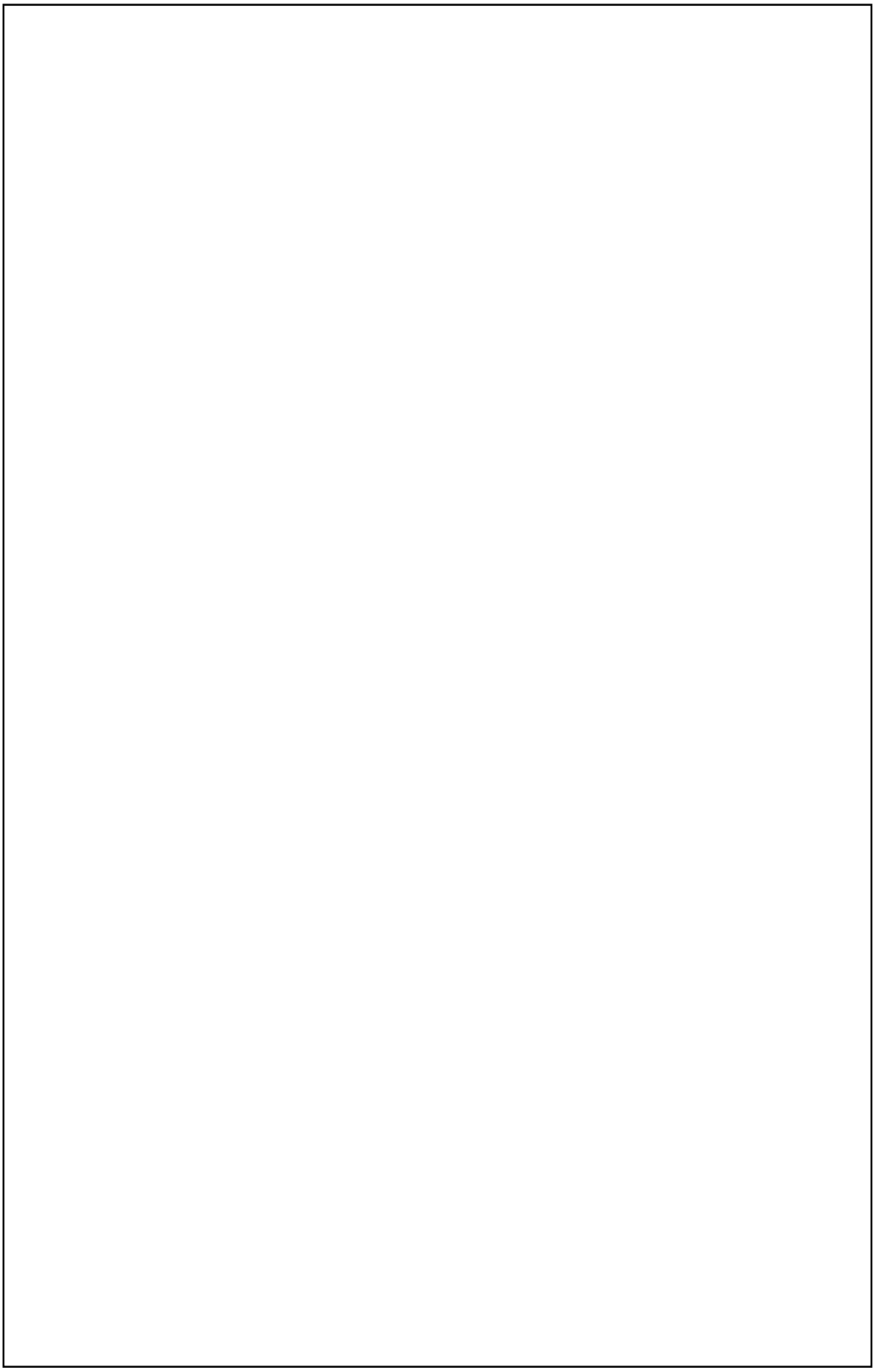

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EUROCARD format size 150x100 mm; provided with a standard I/O ABACO® 20 pins connector; front 68 pins connector for PCMCIA type 1 cards with extractor; 4 frontal LEDs for signalations; back up circuitery with Lithium battery; addressing space 64 MBytes; capable to read and write PCMCIA type 1 RAM Memory Cards; CENTRONICS parallel interface to connect to a PC; can be driven by any structure provided with two TTL I/O ports divided in 12 bits as outputs and 4 bits as inputs.

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For specific informations on the components mounted on the card, please refer to the Data Book of the builder or second sources.

SYMBOLS DESCRIPTION

In the manual could appear the following symbols:

Attention: Generic danger

Attention: High voltage

Trade Marks

abaco, **GPC®**, **grifo®** : are trade marks of **grifo®**.

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PRELIMINARY MCI 64

FIGURE ?: CARD PHOTO

GENERAL FEATURES

MCI 64 is a peripheral card, in standard EUROCARD format, that allows to manage RAM Memory Card **PCMCIA** type 1 through 16 TTL I/O signals.
It is provided with two standard **I/O ABACO®** and **CENTRONICS** P.C. connectors for a direct connection to several contol systems.
Overall features are:

- **EUROCARD** format size 150x100 mm
- Provided with a standard **I/O ABACO®** 20 pins connector
- Front 68 pins connector for **PCMCIA** type 1 cards with extractor
- **4 frontal LEDs** for signalations
- **Back up** circuitery with **Lithium** battery
- Addressing space **64 MBytes**
- Capable to read and write PCMCIA type 1 **RAM Memory Cards**
- **CENTRONICS** parallel interface to connect to a PC
- Can be driven by any structure provided with two TTL I/O ports divided in 12 bits as outputs and 4 bits as inputs

Specific applications of this card are the ones that require a big amount of memory, easily removable in modules, like data login systems, on board operating systems (**MCI 64** will provide them abig mass memory device), every insustrial environmental data storage system, etc.

INSTALLATION

In this chapter there are the information for a right installation and correct use of the card. The user can find the location and functions of each connectors and LEDs and some explanatory diagrams.

FRONT PANEL

MCI 64 can be provided with an optional metallic front panel.
The panel must be used in the applications where electronics has to be installed in a metallic rack. Visualization LEDs, PCMCIA card slot and its explusion button remain however accessible.
Connecting this panel to GND warrants a good shielding, and so a better safety, to the overall system.
Please refer to next paragraph for informatio about connecting panel to GND.

JUMPER

On **MCI 64** there is one 2 pins jumper, called J2.
Its purpose is to connect or disconnect the ground from the eventual front panel of the card:

Jumper Connected:	Eventual front panel is connected to GND
Jumper not Connected:	Eventual front panel is not connected to GND

By default, **MCI 64** is delivered with J2 disconnected.

CONNECTIONS

The **MCI 64** card is with 5 connectors that can be linkeded to control system cards or directly to the field, according to system requirements. In this paragraph there are connectors pin out, a short signals description (including the signals direction) and connectors location (please refer to figure ?).
Following figures show the frontal view of connectors; they can be easily recognized because they reproduce exactly the shape of the connectors and also thanks to the serigraph on the board.

CN3 - CONNECTOR FOR BUS ABACO®

The connector for **ABACO® industrial BUS**, called CN3 on board,is a DIN 41612, male, a 90 °, type C, A+C.
Here follows the pin-out of the connector installed on **MCI 64**, the connector is used only to supply the card.

A 16 bit BUS	A 8 bit BUS	A MCI 64	PIN	C MCI 64	C 8 bit BUS	C 16 bit BUS
GND	GND	GND	1	GND	GND	GND
+5 Vdc	+5 Vdc	+5 Vdc	2	+5 Vdc	+5 Vdc	+5 Vdc
D0	D0	-	3	-	-	D8
D1	D1	-	4	-	-	D9
D2	D2	-	5	-	-	D10
D3	D3	-	6	-	/INT	/INT
D4	D4	-	7	-	/NMI	/NMI
D5	D5	-	8	-	/HALT	D11
D6	D6	-	9	-	/MREQ	/MREQ
D7	D7	-	10	-	/IORQ	/IORQ
A0	A0	-	11	-	/RD	/RDLDS
A1	A1	-	12	-	/WR	/WRLDS
A2	A2	-	13	-	/BUSAK	D12
A3	A3	-	14	-	/WAIT	/WAIT
A4	A4	-	15	-	/BUSRQ	D13
A5	A5	-	16	-	/RESET	/RESET
A6	A6	-	17	-	/M1	/IACK
A7	A7	-	18	-	/RFSH	D14
A8	A8	-	19	-	/MEMDIS	/MEMDIS
A9	A9	-	20	-	VDUSEL	A22
A10	A10	-	21	-	/IEI	D15
A11	A11	-	22	-	-	-
A12	A12	-	23	-	CLK	CLK
A13	A13	-	24	-	-	/RDUDS
A14	A14	-	25	-	-	/WRUDS
A15	A15	-	26	-	-	A21
A16	-	-	27	-	-	A20
A17	-	-	28	-	-	A19
A18	-	-	29	-	/R.T.	/R.T.
+12 Vdc	+12 Vdc	-	30	-	-12 Vdc	-12 Vdc
+5 Vdc	+5 Vdc	+5 Vdc	31	+5 Vdc	+5 Vdc	+5 Vdc
GND	GND	GND	32	GND	GND	GND

FIGURE ?: CN3 - BUS ABACO® CONNECTOR

Signals description:

8 bits CPU

A0-A15	=	O	- Address BUS
D0-D7	=	I/O	- Data BUS
/INT	=	I	- Interrupt request
/NMI	=	I	- Non Maskable Interrupt
/HALT	=	O	- Halt state
/MREQ	=	O	- Memory Request
/IORQ	=	O	- Input Output Request
/RD	=	O	- Read cycle status
/WR	=	O	- Write cycle status
/BUSAK	=	O	- BUS Acknowledge
/WAIT	=	I	- Wait
/BUSRQ	=	I	- BUS Request
/RESET	=	O	- Reset
/M1	=	O	- Machine cycle one
/RFSH	=	O	- Refresh for dynamic RAM
/MEMDIS	=	I	- Memory Display
VDUSEL	=	O	- VDU Selection
/IEI	=	I	- Interrupt Enable Input
CLK	=	O	- System clock
R.B.	=	I	- Reset button
+5 Vdc	=	I	- Power supply at +5 Vdc
+12 Vdc	=	I	- Power supply at +12 Vdc
-12 Vdc	=	I	- Power supply at -12 Vdc
GND	=		- Ground signal

16 bits CPU

A16-A22	=	O	- Address BUS
D8-D15	=	I/O	- Data BUS
/RD UDS	=	O	- Read Upper Data Strobe
/WR UDS	=	O	- Write Upper Data Strobe
/IACK	=	O	- Interrupt Acknowledge
/RD LDS	=	O	- Read Lower Data Strobe
/WR LDS	=	O	- Write Lower Data Strobe

NOTE
Directionality indications as above stated are referred to a master (**GPC®**) board and have been kept untouched to avoid ambiguity in case of multi-boards systems.

CN2 - I/O ABACO® CONNECTOR

CN2 is a 20 pins, male, vertical, low profile connector with 2.54mm pitch.
This connector allows to connect MCI 64 to its management card through a 20 pins flat cable.
All these signals follow TTL standard and I/O **ABACO®** standard pin out.

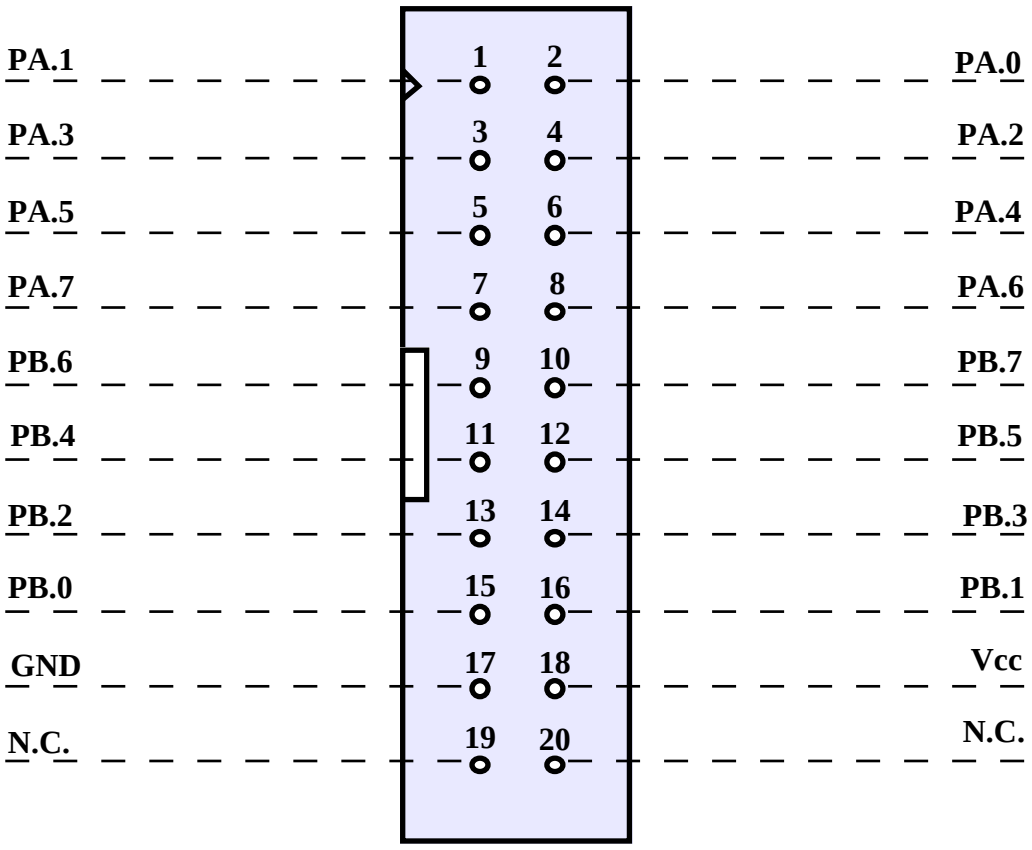


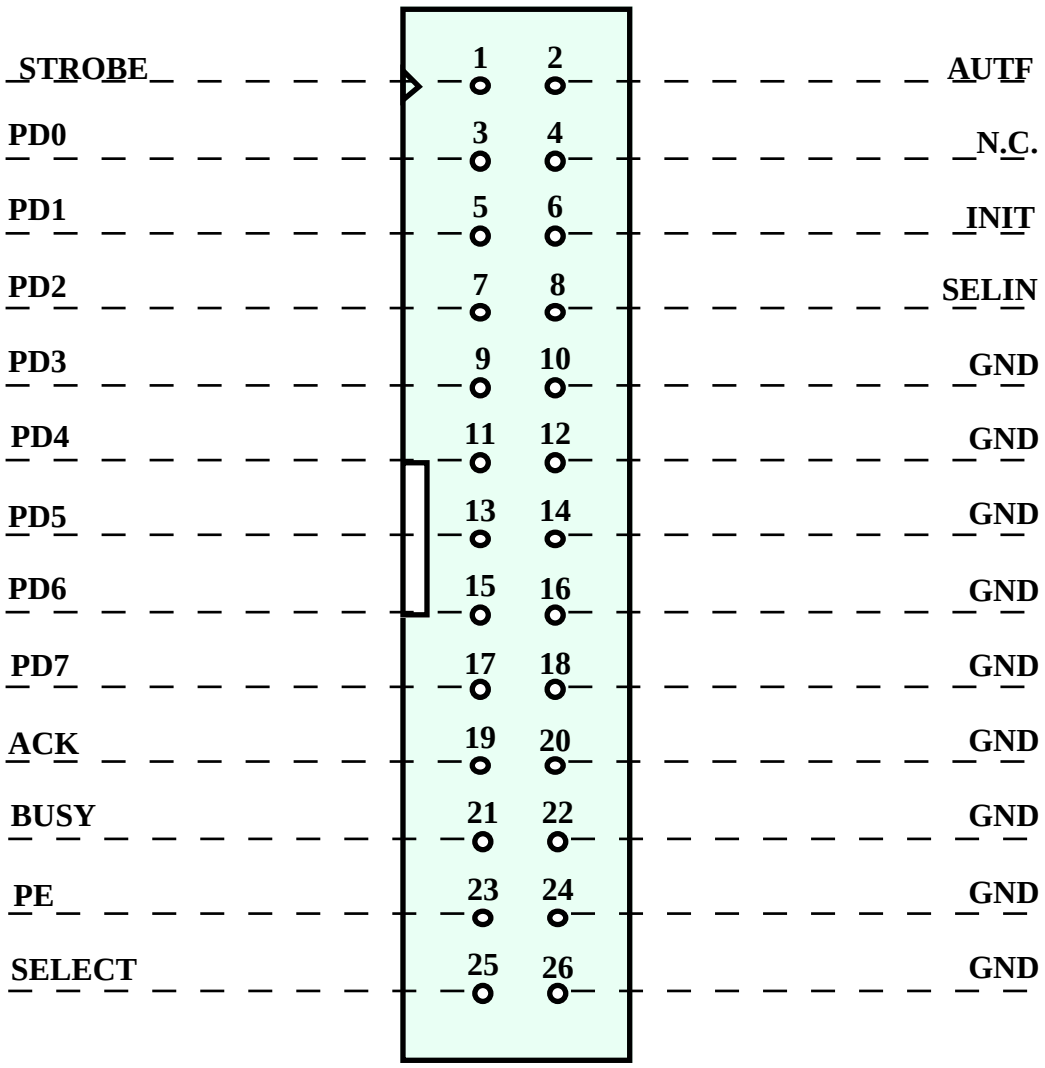
FIGURE ?: CN2 - I/O ABACO® CONNECTOR

Signals description:

PA.n	=	I/O - n-th digital line of PPI 82C55 port A.
PB.n	=	I/O - n-th digital line of PPI 82C55 port B.
PC.n	=	I/O - n-th digital line of PPI 82C55 port C.
+5 Vdc	=	O - Unique +5 Vdc power supply.
GND	=	- Ground.
N.C.	=	- Not connected.

CN4 - CENTRONICS COMPATIBLE CONNECTOR

CN4 is a 26 pins, low profile, male, vertical connector, pitch 2.54 mm.
It features **CENTRONICS** compatible pin out, that allows to connect MCI 64 to PC parallel port through a flat cable with a 26 pins connector on one side and a 25 pins D type connrctor on the other side.



Signal description:

PD0÷7	=	I	- Printer data 0÷7
AUTF	=	I	- Automatic line feed
INIT	=	I	- Printer initialization
SELIN	=	I	- Printer work mode selection
STROBE	=	I	- Valid data for printer
ACK	=	O	- Acknowledge
BUSY	=	O	- Printer busy
PE	=	O	- Paper ready test
SELECT	=	O	- Printer selection verify
GND	=		- Ground
N.C.	=		- Not connected

To avoid working problems with **MCI 64** connecti it to the PC with a cable not longer than 100 cm, a flat cable is better because it shields each signsl for the ground.

Correspondance between signals of CN4 and CN2 (and so between the 16 I/O signals used to manage **MCI 64**) is reported here:

PD0÷7	->	PA0÷7
AUTF	->	PB.1
INIT	->	PB.2
SELIN	->	PB.3
STROBE	->	PB.0
ACK	->	PB.6
BUSY	->	PB.7
PE	->	PB.5
SELECT	->	PB.4

CN6 - BACK UP EXTERNAL BATTERY CONNECTOR

CN6 is a 2 pins, male, vertical connector with 2.54mm pitch.
Through CN6 the user must connect an external battery for RAM when the power supply is switched off or even when on board battery is not present.

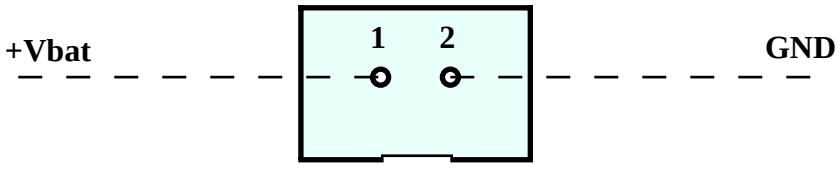


FIGURE ?: CN6 - BACK UP EXTERNAL BATTERY CONNECTOR

Signals description:

+Vbat	=	I	-	Back up external battery positive pin
GND	=		-	Back up external battery negative pin

CN1 - PCMCIA CARD TYPE 1 CONNECTOR

CN1 is a 68 pin standard PCMCIA type 1 connector, where the memory card must be inserted.
For further information please refer to specific hardware and electronic documentation about PCMCIA standard.

USE EXAMPLE

Following paragraphs are intended for expert technician with specific knowledge about PCMCIA standard and its use.
Less experienced users can take advantage of the several examples, written in many high level languages, that allow to use completely the card.
These examples are delivered with the card or are availabe on our web site.

MCI 64 AND GDOS 80

In addition to the above mentioned examples of use, our ROMmed operating system for Zilog CPU's, **GDOS 80**, allows to use the memory card as if it was a filesystem. This is the easiest way to access the features of 64 MBytes of space using the high level instructions that manage files.

I/O PORT MANAGEMENT

To use correctly **MCI 64** it is essential to configure the I/O port, or, more in general, the management signals, like this:

Port A (bit 0÷7)	as	Output
Port B (bit 0÷3)	as	Output
Port B (bit 4÷7)	as	Input

Port A send data and addresses to memory card, while Port B performs the read operation and addresses the several latches of MCI 64. For this latter operation, bit 0÷2 are used; in detail:

PB.2	PB.1	PB.0	
0	0	0	Allows to read least significant nibble of data addressed
0	0	1	Read: allows to read most significant nibble of data addressed Write: allows to latch address of DATA (A0÷A7) with data on Port A
0	1	0	Allows to latch the address of SECTOR (A8÷A15) with data on Port A
0	1	1	Allows to latch the address of TRACK (A16÷A23) with data on Port A
1	0	0	Allows to latch the address of CYLINDER (A24÷A25) with data on Port A and the memory card management signals
1	0	1	Allows to read the **MCI 64** status nibble
1	0	1	Allows to set /WR signal to logic level low, so to write data on Port A to the previously latched address
1	0	1	No new operation, complete operation in progess

Bit PB.3 is used to activate the management logic of **MCI 64**, so it must be always kept at logic level low, otherwise the card is not enabled.
In this latter case the remaining 15 management signals can be used for different purposes, but mantaining the same directionality.
To latch an address or a data with one of on board lathces, it is essential to activate the device by setting opportunely PB.2÷PB.0, then write to Port A the data.
The value will be physically latched only when a new data will be written to PB.2÷PB.0, that is the previously selected latch is disabled.
In other words, data on Port A is latched only when next setting of PB.2÷PB.0 is performed.
Management circuitery of **MCI 64** has been designed to make extermly safe access to every kind of memory card.
For this reason if the card in not inserted correctly, no data can be latched.

STATUS NIBBLE

It is possible to know whether memory card has been inserted correctly or not, it is write protected or not and on board back up battery charge status by reading the status nibble:

BIT 4: 0 - Memory card write protection enabled
1 - Memory card write protection disabled

BIT 5: 0 - Power supply of memory present
1 - Power supply of memory not present

BIT 6: 0 - Eventual on board back up battery discharged
1 - Eventual on board back up battery charged

BIT 7: 0 - Memory card not present or not correctly inserted
1 - Memory card present and correctly inserted

STATUS NIBBLE

It is possible to latch CYLINDER address, memory card management signals and turn ON and OFF LEDs LD3 and LD4 by writing to this byte:

BIT 0: - Bit 0 of CYLINDER address (A24 of memory card)

BIT 1: - Bit 1 of CYLINDER address (A25 of memory card)

BIT 2: 1 - Engage the line that generates /WR signal for memory card; it is essential to set this bit to 1 to be able to activate /WR signals by setting PB2÷PB0
0 - /WR signal always disabled

BIT 3: 1 - Sets to logic level 0 signal /CE of memory card
0 - Sets to logic level 1 signal /CE of memory card

BIT 4: 1 - Supplies memory card
0 - Removes powet supply of memory card

BIT 5: 1 - Sets to logic level 1 signal REG of memory card
0 - Sets to logic level 0 signal REG of memory card

BIT 6: 1 - Turns ON the red LED LD4
0 - Turns OFF the red LED LD4

BIT 7: 1 - Turns ON the green LED LD3
0 - Turns OFF the green LED LD3

WRITING DATA THROUGH I/O ABACO® SIGNALS

To write correctly a data into memory card through standard **I/O ABACO®** signals, it is essential the perform the following operations in sequence:

1 - Set PB.0÷PB.3 with value 5, to read status nibble.

2 - Wait for memory card to be present, testing bit 7 of status nibble, and for write protection to be disabled, testing bit 4. Status nibble is read by simply reading Port B.

3 - Set PB.0÷PB.3 with value 4, to write the management signals.

4 - Set the desired CYLINDER address in Port A (bit 0 and 1), engage the /WR signal (bit 2 set to 1), set signal /CE to 0 (bit 3 set to 1), supply memory card (set bit 4 to 1) and set REG to 1 (set bit 5 to 1).

5 - Set PB.0÷PB.3 with value 3, to activate the latch ad TRACK address; this operation latches the value on Port A written at step 4.

6 - Set TRACK address into Port A.

7 - Set PB.0÷PB.3 with value 2, to activate the latch ad SECTOR address; this operation latches the value on Port 4 written at step 6.

8 - Set SECTOR address into Port A.

9 - Set PB.0÷PB.3 with value 1, to activate the latch ad DATA address; this operation latches the value on Port 4 written at step 8.

10 - Set DATA address into Port A.

11 - Set PB.0÷PB.3 with value 6, to activate (logic status 0) signal /WR on memory card; this operation latches the value on Port 4 written at step 10.

12 - Set data to be written into Port A.

13 - Set PB.0÷PB.3 with value 4, to write the byte with management signals; by this operation /WR signal returns to logic level 1 and data on Port A is stored into memory card at the previously latched address.

14 - Set Port A with a value that disengages /WR signal (bit 2 set to 0), sets signal /CE to 1 (bit 3 set to 0), turns off supply of memory card (set bit 4 to 0) and set REG to 0 (set bit 5 to 0).

15 - Set PB.0÷PB.3 with value 7, to latch the data on Port A written at step 14.

READING DATA THROUGH I/O ABACO® SIGNALS

To read correctly a data from memory card through standard **I/O ABACO®** signals, it is essential the perform the following operations in sequence:

1 - Set PB.0÷PB.3 with value 5, to read status nibble.

2 - Wait for memory card to be present, testing bit 7 of status nibble, and for write protection to be disabled, testing bit 4. Status nibble is read by simply reading Port B.

3 - Set PB.0÷PB.3 with value 4, to write the management signals.

4 - Set the desired CYLINDER address in Port A (bit 0 and 1), disengage the /WR signal (bit 2 set to 0), set signal /CE to 0 (bit 3 set to 1), supply memory card (set bit 4 to 1) and set REG to 1 (set bit 5 to 1).

5 - Set PB.0÷PB.3 with value 3, to activate the latch ad TRACK address; this operation latches the value on Port A written at step 4.

6 - Set TRACK address into Port A.

7 - Set PB.0÷PB.3 with value 2, to activate the latch ad SECTOR address; this operation latches the value on Port 4 written at step 6.

8 - Set SECTOR address into Port A.

9 - Set PB.0÷PB.3 with value 1, to activate the latch ad DATA address; this operation latches the value on Port 4 written at step 8.

10 - Set DATA address into Port A.

11 - Set PB.0÷PB.3 with value 0, to read least significant nibble on memory card; this operation latches the value on Port 4 written at step 10.

12 - Read least significant nibble on the memory card through PB.4÷PB.7 from the previously latched address.

13 - Set PB.0÷PB.3 with value 1, to read most significant nibble on memory card.

14 - Read most significant nibble on memory card through PB.4÷PB.7 from the previously latched address.

15 - Set PB.0÷PB.3 with value 4, to write the management signals.

16 - Set Port A with a value that sets signal /CE to 1 (bit 3 set to 0), turns off supply of memory card (set bit 4 to 0) and set REG to 0 (set bit 5 to 0).

17 - Set PB.0÷PB.3 with value 7, to latch the data on Port A written at step 16.

WRITING DATA THROUGH PC COMPATIBLE CENTRONICS INTERFACE

To write correctly a data into memory card through compatible CENTRONICS interface signals, it is essential the perform the following operations in sequence:

1 - Set PB.0÷PB.3 with values 13 and 5 in sequence, to read status nibble.

2 - Wait for memory card to be present, testing bit 7 of status nibble, and for write protection to be disabled, testing bit 4. Status nibble is read by simply reading Port B.

3 - Set the desired CYLINDER address in Port A (bit 0 and 1), engage the /WR signal (bit 2 set to 1), set signal /CE to 0 (bit 3 set to 1), supply memory card (set bit 4 to 1) and set REG to 1 (set bit 5 to 1).

4 - Set PB.0÷PB.3 with values 12, 4 and 12 in sequence to latche the management signals written at step 3.

5 - Set TRACK address into Port A.

6 - Set PB.0÷PB.3 with values 11, 3 and 11 in sequence to latche the TRACK address written at step 5.

7 - Set SECTOR address into Port A.

8 - Set PB.0÷PB.3 with values 10, 2 and 10 in sequence to latche the SECTOR address written at step 7.

9 - Set DATA address into Port A.

10 - Set PB.0÷PB.3 with values 9, 1 and 9 in sequence to latche the DATA address written at step 9.

11 - Set data to be written into Port A.

12 - Set PB.0÷PB.3 with values 14, 6 and 14 in sequence to write the byte with management signals; this operation generates an impilse on /WR signal and data on Port A is stored into memory card at the previously latched address.

13 - Set Port A with a value that disengages /WR signal (bit 2 set to 0), sets signal /CE to 1 (bit 3 set to 0), turns off supply of memory card (set bit 4 to 0) and set REG to 0 (set bit 5 to 0).

14 - Set PB.0÷PB.3 with values 12, 4 and 12 to latch the data on Port A written at step 13.

READING DATA FROM PC COMPATIBLE CENTRONICS INTERFACE

To read correctly a data from memory card through compatible CENTRONICS interface signals, it is essential the perform the following operations in sequence:

1 - Set PB.0÷PB.3 with values 13 and 5 in sequence, to read status nibble.

2 - Wait for memory card to be present, testing bit 7 of status nibble, and for write protection to be disabled, testing bit 4. Status nibble is read by simply reading Port B.

3 - Set the desired CYLINDER address in Port A (bit 0 and 1), disengage the /WR signal (bit 2 set to 0), set signal /CE to 0 (bit 3 set to 1), supply memory card (set bit 4 to 1) and set REG to 1 (set bit 5 to 1).

4 - Set PB.0÷PB.3 with values 12, 4 and 12 in sequence to latche the management signals written at step 3.

5 - Set TRACK address into Port A.

6 - Set PB.0÷PB.3 with values 11, 3 and 11 in sequence to latche the TRACK address written at step 5.

7 - Set SECTOR address into Port A.

8 - Set PB.0÷PB.3 with values 10, 2 and 10 in sequence to latche the SECTOR address written at step 7.

9 - Set DATA address into Port A.

10 - Set PB.0÷PB.3 with values 9, 1 and 9 in sequence to latche the DATA address written at step 9.

11 - Set PB.0÷PB.3 with values 8 and 0 in sequence, to read least significant nibble on memory card.

12 - Read least significant nibble on the memory card through PB.4÷PB.7 from the previously latched address.

13 - Set PB.0÷PB.3 with values 9 and 1, to read most significant nibble on memory card.

14 - Read most significant nibble on memory card through PB.4÷PB.7 from the previously latched address.

15 - Set PB.0÷PB.3 with value 9, to disable the previosly enabled read operation.

16 - Set Port A with a value that sets signal /CE to 1 (bit 3 set to 0), turns off supply of memory card (set bit 4 to 0) and set REG to 0 (set bit 5 to 0).

17 - Set PB.0÷PB.3 with values 12, 4 and 12 in sequence,to latch the data on Port A written at step 16.

CENTRONICS COMPATIBLE INTERFACE SOFTWARE MANAGEMENT

Previously described operations sequences to read and write bytes from and to memory card use indications Port A and Port B; corresponance with CENTRONICS interface is described in paragraph dedicated to CN4.
By software, the PC (DOS) addresses CENTRONICS interface through three registers:

Data register: address 378H for port LPT1
Control register: address 37AH for port LPT1
Status register: address 379H for port LPT1

correspondance between bits of these registers and signals used is the following:

REGISTER	D7	D6	D5	D4	D3	D2	D1	D0	CN?
DATA	PD.7	PD.6	PD.5	PD.4	PD.3	PD.2	PD.1	PD.0	CN4
	PA.7	PA.6	PA.5	PA.4	PA.3	PA.2	PA.1	PA.0	CN2
CONTROL	N.U.	N.U.	N.U.	N.U.	/SELIN	INIT	/AUTF	/STROBE	CN4
	N.U.	N.U.	N.U.	N.U.	PB.3	PB.2	PB.1	PB.0	CN2
STATUS	BUSY	ACK	PE	SELECT	N.U.	N.U.	N.U.	N.U.	CN4
	PB.7	PB.6	PB.5	PB.4	N.U.	N.U.	N.U.	N.U.	CN2

FIGURE ?: CORRESPONDANCE BETWEEN BITS OF LPT REGISTERS AND CARD SIGNALS

bits indicated with leading '/' are complemented respect to the corresponding signal on the connector so must be managed as complemented logic signals.
For example, if value 9 must be set on signals PB.0÷PB.3 then the software will have to write 02H in control register.

POWER SUPPLY

MCI 64 needs an unique +5 Vdc, 50 mA power supply that must be provided through connector CN2 or connector CN3.