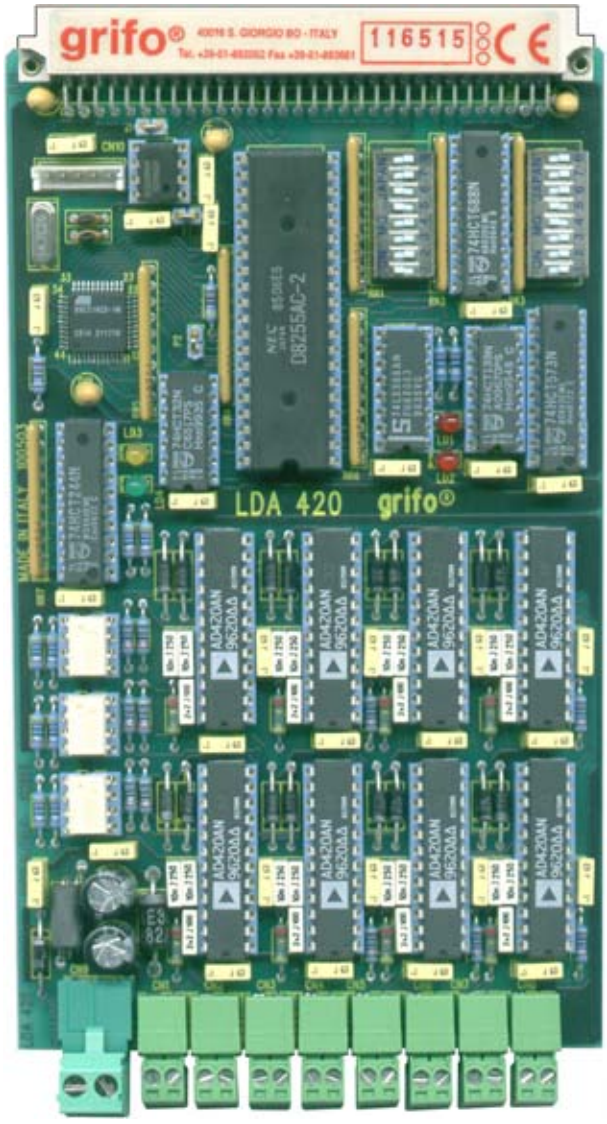
LDA 420

Low cost Digital to Analog converter 4÷20 mA

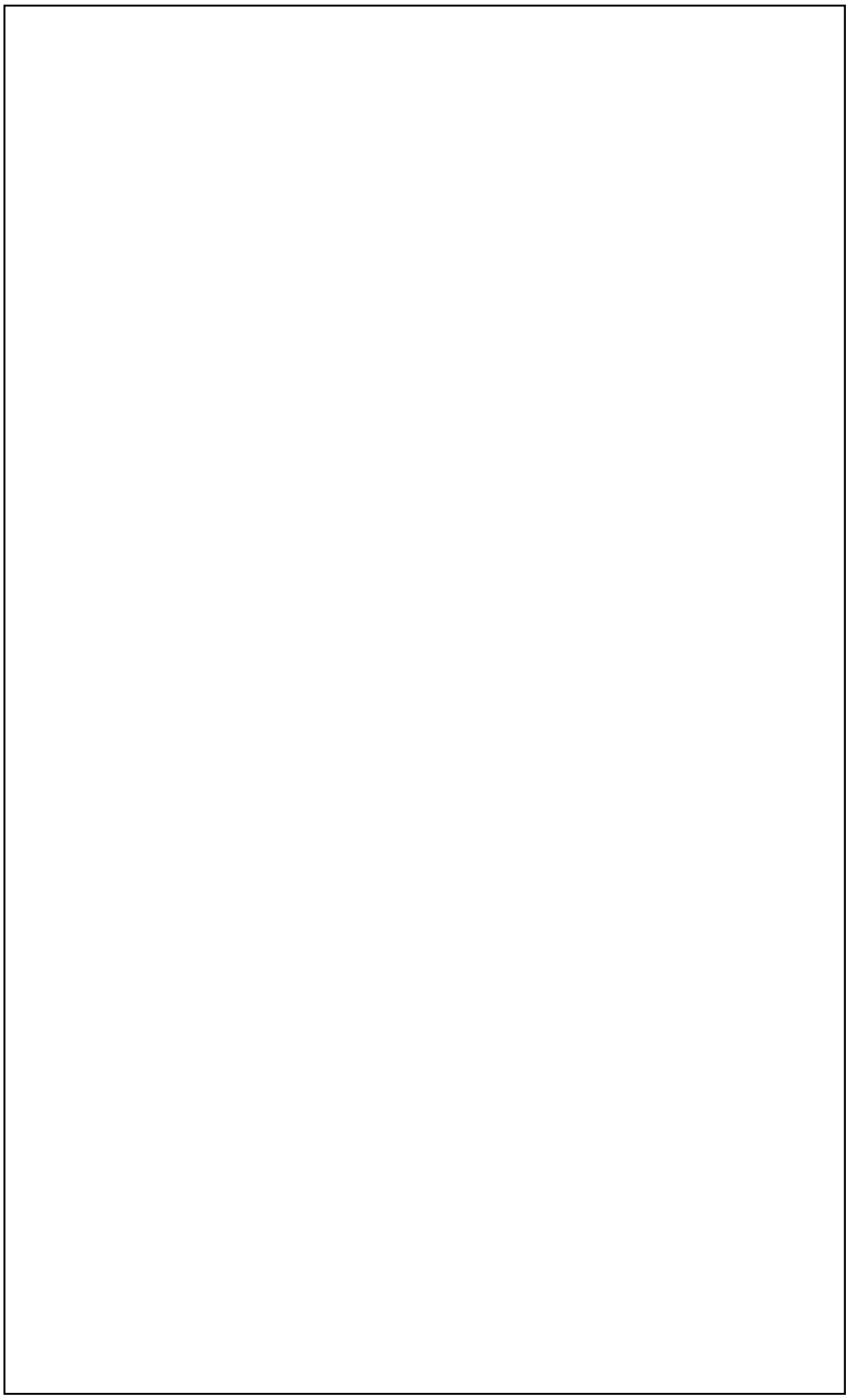
USER MANUAL



grifo®
ITALIAN TECHNOLOGY

Via dell' Artigiano, 8/6
40016 San Giorgio di Piano
(Bologna) ITALY
E-mail: grifo@grifo.it
http://www.grifo.it http://www.grifo.com
Tel. +39 051 892.052 (a.r.) FAX: +39 051 893.661

LDA 420 Rel. 5.00 *Edition 01 June 2004*



LDA 420

Low cost Digital to Analog converter 4÷20 mA

USER MANUAL

Single Euro format, with **100x160 mm** dimension. **8** separated sections of **D/A** conversion, based on **AD 420** component, **16 Bits** resolution, with active **4÷20 mA** output on furnished analog power supply voltage; **8** different **protection** and **filter** circuits. Wide range power **supply** input for **analog section**: **12÷32 V**, **210 mA** max. 8 **screw terminal quick release**, **2 pins** connectors for generated analog signals; 1 **screw terminal quick release**, **2 pins** connector for analog section power supply, not compatible with the analog output ones. **Galvanic separation** between analog section and control logic section. **Four** different **configurations** can be ordered, equipped wit **2**,**4**,**6**,**8** analog outputs. 8 ways **dip switch** for configuration and settings; visualization, through coloured **LEDs**, of the card status. Asynchronous **TTL serial** interface with configurable physic protocol; direct parallel interface to **Abaco**® Industrial BUS. On board CPU that manages the analog sections through commands received from **serial** or **parallel** interface; **GNET** logic communication protocol that allows the use of many units as slave devices connected on a serial line. Management firmware complete of **10** general purpose **commands** and with possibility to add interesting high level functions. 8 ways **dip switch** to set the allocation address of the card; used addressing space: **2 bytes**; nornal addressing range of **256 bytes**. Single power supply for control logic: **+5 Vdc**, **130 mA**. Supplied with **demo programs** that simplify and speed the card use with each programmable external systems

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ITALIAN TECHNOLOGY

Via dell' Artigiano, 8/6
40016 San Giorgio di Piano
(Bologna) ITALY
E-mail: grifo@grifo.it
http://www.grifo.it http://www.grifo.com
Tel. +39 051 892.052 (a.r.) FAX: +39 051 893.661

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IMPORTANT

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grifo® reserves the right to change the contents and form of this document, as well as the features and specification of its products at any time, without prior notice, to obtain always the best product.

For specific informations on the components mounted on the card, please refer to the Data Book of the builder or second sources.

SYMBOLS DESCRIPTION

In the manual could appear the following symbols:

Attention: Generic danger

Attention: High voltage

Attention: ESD sensitive device

Trade Marks

abaco®, **GPC®**, grifo® : are trade marks of grifo®.

Other Product and Company names listed, are trade marks of their respective companies.

GENERAL INDEX

FIGURE INDEX

INTRODUCTION

The use of these devices has turned - IN EXCLUSIVE WAY - to specialized personnel.
This device is not a **safe component** as defined in directive **98-37/CE**.

Pins of Mini Module are not provided with any kind of ESD protection. They are connected directly to their respective pins of microcontroller. Mini Module is affected by electrostatic discharges. Personnel who handles Mini Modules is invited to take all necessary precautions to avoid possible damages caused by electrostatic discharges.

The purpose of this handbook is to give the necessary information to the cognizant and sure use of the products. They are the result of a continual and systematic elaboration of data and technical tests saved and validated from the manufacturer, related to the inside modes of certainty and quality of the information.

The reported data are destined- IN EXCLUSIVE WAY- to specialized users, that can interact with the devices in safety conditions for the persons, for the machine and for the enviroment, impersonating an elementary diagnostic of breakdowns and of malfunction conditions by performing simple functional verify operations , in the height respect of the actual safety and health norms.

The informations for the installation, the assemblage, the dismantlement, the handling, the adjustment, the reparation and the contingent accessories, devices etc. installation are destined - and then executable - always and in exclusive way from specialized warned and educated personnel, or directly from the TECHNICAL AUTHORIZED ASSISTANCE, in the height respect of the manufacturer recommendations and the actual safety and health norms.

The devices can't be used outside a box. The user must always insert the cards in a container that rispect the actual safety normative. The protection of this container is not threshold to the only atmospheric agents, but specially to mechanic, electric, magnetic, etc. ones.

To be on good terms with the products, is necessary guarantee legibility and conservation of the manual, also for future references. In case of deterioration or more easily for technical updates, consult the AUTHORIZED TECHNICAL ASSISTANCE directly.

To prevent problems during card utilization, it is a good practice to read carefully all the informations of this manual. After this reading, the user can use the general index and the alphabetical index, respectly at the begining and at the end of the manual, to find information in a faster and more easy way.

HARDWARE AND FIRMWARE VERSION

The present handbook is reported to the **LDA 420** card release **100503** and to firmware version **1.1**. The validity of the bring informations is subordinate to the number of the card release. The user must always verify the correct correspondence among the two denotations. On the card the release number is present in more points both board printed diagram (serigraph) and printed circuit (for example near resistor network RR7 on the component side) and the firmware version is reported on a label put on the CPU, which is component called IC3. Also, firmware version can be requested directly to the peripheral using a specific serial command.

GENERAL INFORMATION

LDA 420 is an inexpensive and powerful peripheral device, in Eurocard format, featuring BUS **ABACO®** interface.
It belongs to the analog peripherals listing, in detail its purpose is to provide up to 8 Digital to Analog conversion signals, each one can output a current in the range 4÷20 mA, with 16 bits of resolution. Locally generated analog signals are available on a comfortable quick release screw terminal connector, located in the front side, for faster and easier cabling.
Generation of analog signals is made by eight indipendent D/A conversion circuits and as many filtering and protection circuits, to reduce interferences and nois on the signals.
LDA 420 is modulare, that is it can be ordered with the desired number of outputs (up to 8), to allow a further optimization of costs, according to the application to build.
LDA 420 can be ordered in one of these configurations: **LDA 420**, **LDA 420/4**, **LDA 420/6** and **LDA 420/8** featuring respectively two, four, six and eight current outputs in the range 4÷20 mA.
Regardless of the configuration, **LDA 420** is always delivered with an input for analog section power supply, which is also connected to a screw terminal.
The choice to use an external voltage to supply analog section avoids problems of power dissipation and voltage level of current loop controlled on board, increasing the fields of use.
Other remarkable features of **LDA 420** arethe galvanic separation between control logic and analog section, which makes **LDA 420** suitable also for electrically noisy industrial environments, and the presence of a local CPU, to have a software management easier and faster.
Functionalities of **LDA 420** are coded in its firmware, executed on the local CPU, and can be easily expanded on user request, making possible, for example, the generation of ramps, preset analog profiles, repeated and proportional settings, etc.
LDA 420 can be driven through the parallel BUS by any **grifo® GPC® xxx** intelligent module connectable to **BUS ABACO®**, where **LDA 420** takes as low as two contiguous bytes, or it can be driven through serial port by any card provided with a programmable asynchronous line.

- Single Eurocard format, with **100x160 mm** dimension
- **8** separated sections of **D/A** conversion, based on **AD 420** component, **16 Bits** resolution, with active **4÷20 mA** output on furnished analog power supply voltage
- **8** different **protection** and **filter** circuits
- Wide range power **supply** input for **analog section**: **12÷32 V**, **210 mA** max
- 8 **screw terminal quick release**, **2 pins** connectors for generated analog signals

- 1 **screw terminal quick release**, **2 pins** connector for analog section power supply, not compatible with the analog output ones
- **Galvanic separation** between analog section and control logic section
- **Four** different **configurations** can be ordered, equipped wit **2**,**4**,**6**,**8** analog outputs
- 8 ways **dip switch** for configuration and settings
- Visualization, through coloured **LEDs**, of the card status
- Asynchronous **TTL serial** interface with configurable physic protocol
- Direct parallel interface to **Abaco®** Industrial BUS
- On board CPU that manages the analog sections through commands received from **serial** or **parallel** interface
- **GNET** logic communication protocol that allows the use of many units as slave devices connected on a serial line
- Management firmware complete of **10** general purpose **commands** and with possibility to add interesting high level functions
- 8 ways **dip switch** to set the allocation address of the card
- Used addressing space: **2 bytes**; nornal addressing range of **256 bytes**
- Single power supply for control logic: **+5 Vdc**, **130 mA**
- Supplied with **demo programs** that simplify and speed the card use with each programmable external systems
- Possibility of special executions of custom programs, also for small quantities

Here follows a description of the board's functional blocks, with an indication of the operations performed by each one. To easily recognize the blocks, please refer to figure 1.

CPU

LDA 420 uses processor Atmel AT89C51AC2.
This microprocessor manages completely the peripheral, allowing it to operate in autonomy and the master to perform operation control without wasting time for driving the output signals.
In fact, CPU takes care of communication and of signals setting, configuration and control, starting from data ready to use and so easy to manipulate.

MEMORY DEVICES

LDA 420 features three memory devices, inside the CPU:

- FLASH EPROM for management firmware code;
- Work RAM for firmware and parameters;
- EEPROM for storing configurations;

Size of these memories are immutable and have been decided according to peripheral operativity. Their management is made completely by the firmware and the user is not involved at all.

SERIAL COMMUNICATION

Serial communication to the external world is made by an **asynchronous full duplex** TTL serial line that, using specific external converters (like **grifo® MSI 01**) can be buffered as RS 232, RS 485, RS 422 or passive current loop.
Please remark that serial lines RS 422, RS 485 and current loop and the powerful logic communication protocol included in the firmware allow to connect up to 128 **LDA 420** in a network, using only 2 or 4 wires.
This means to be able to have intelligent units located at high distances, capable to drive a great number of signals, remote controlled by only the serial communication cables.
For further information about the physical and logical communication protocol please contact **grifo®** directly.

BUS INTERFACE

It is possible to use a parallel interface, other than the above mentioned serial interface, to communicate faster with **LDA 420**, parallel interface of **LDA 420** is called BUS **ABACO®**.
This section manages the data exchange between control logic and command device (**CPU** or **GPC®**), in detail it manages the peripheral BUS addressing trough a dip switch called DSW2.
BUS **ABACO®** addressing uses 8 bits and allows access to 256 different addresses. For further information please refer to chapter "ADDRESSES AND MAPS".
In addition, using a mother board like **grifo® ABB 03** or **grifo® ABB 05**, it is possible to use BLOCK format control devices for **ABACO® I/O BUS**.
This feature allows to expand the application with a good price/performance rate and so makes it suitable to solve several problems of industrial automation.
Please refer to chapter "EXTERNAL CARDS" for a brief description of control devices.

STATUS AND CONFIGURATION

An 8 pins dip switch has been installed to configure the peripheral and application functions.
Acquiring the status of these 8 signals, the user can manage several working conditions, without having to employ other signals to do that.
The firmware can use this dip switch to select some operating conditions, as described in furthere paragraphs.
All the status and configuration resources are completely managed by firmware through specific commands or can indicate faulty conditions in autonomy.

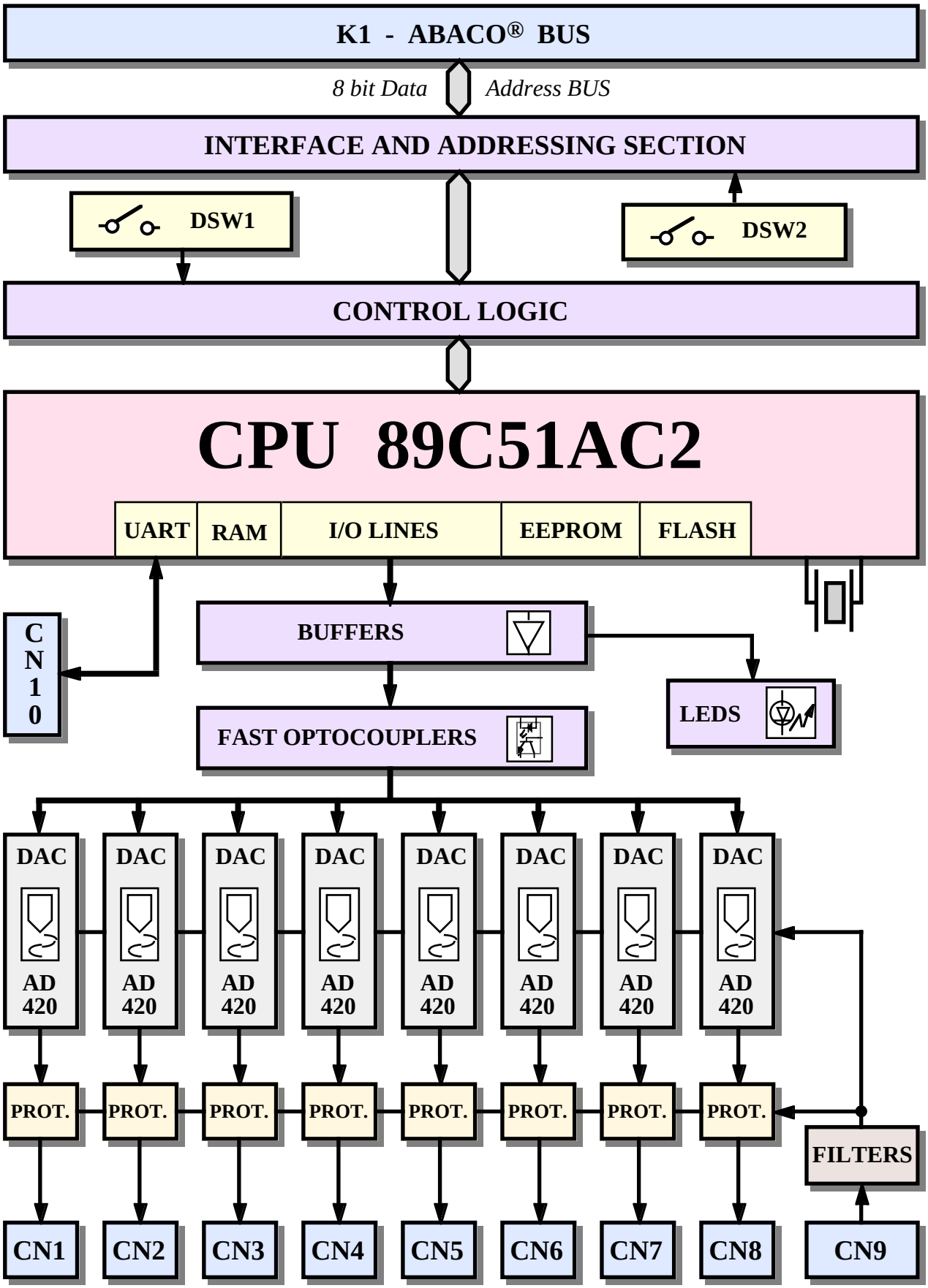

FIGURE 1: BLOCK DIAGRAM

ANALOG SECTION

This section includes the analog signals management and generation circuitery and is based on eight indipendent 16 bits D/A converters (AD420), each one of them provides an output current signal in the range 4÷20 mA.
These outputs are connected to eight protection and filtering circuits and become available to the user on a specific comfortable screw terminal connector.
Opportune buffers and fast optocouplers separate analog section and digital section to cancel any reciprocal interference; this warrants the correct working of the unit under any operative condition and remarkable stability and precision.
Analog output sections number can be configured, in default version only two signals are available and the remaining 6 are optional, that is they are installed only if they are requested in the commercial order.
In detail, **LDA 420** can be delivered in one of the following configurations:

default version	->	2 D/A that is **2** analog outputs in the range 4÷20 mA
version **/4**	->	4 D/A that is **4** analog outputs in the range 4÷20 mA
version **/6**	->	6 D/A that is **6** analog outputs in the range 4÷20 mA
version **/8**	->	8 D/A that is **8** analog outputs in the range 4÷20 mA

Every output is active, that is it can generate the programmed output current starting from a specific external supply and so can be connected directly to passive devices.
For further information about signals type, connection and required power supply please refer to further paragraphs and chapters.
Programming of analog section components is made by local CPU, which can can drive every D/A installed through its I/O signals and the firmware.
A set of firmware commands allow the user to decide the status of generated signals according to the requirements of application to make.

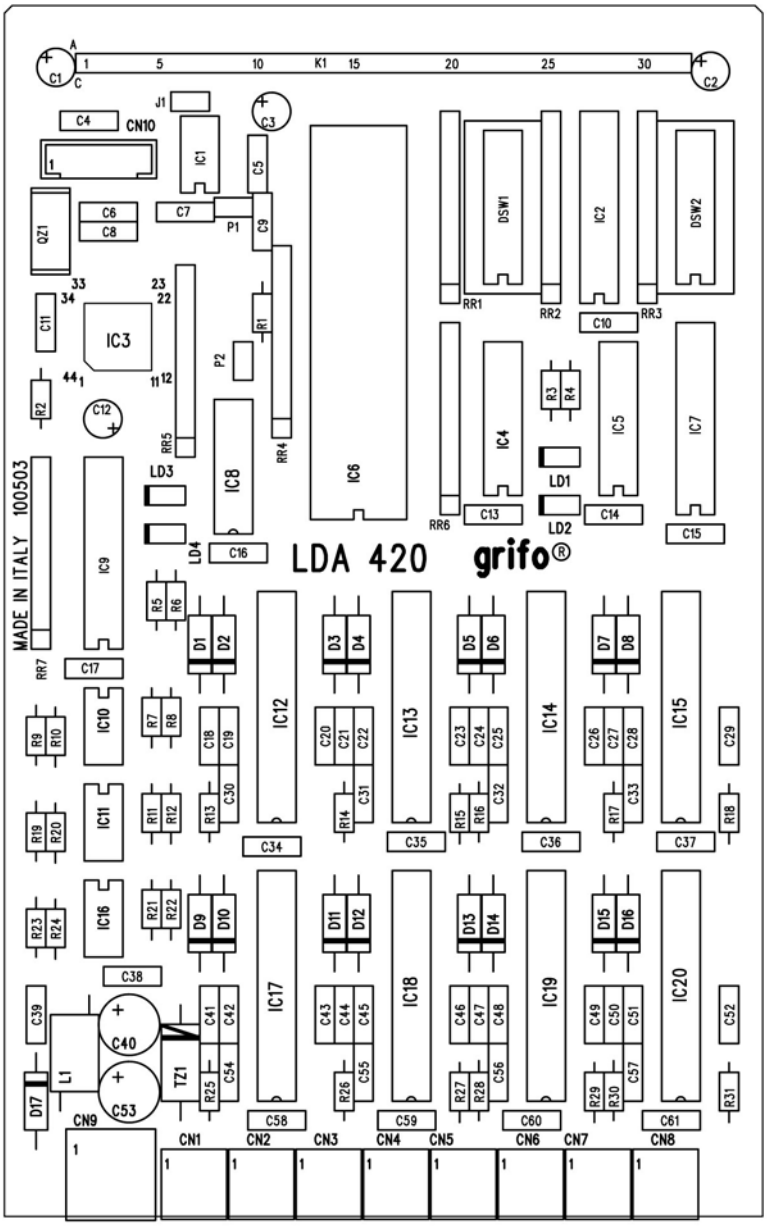

FIGURE 2: COMPONENTS MAP (COMPONENTS SIDE)

TECHNICAL FEATURES

GENERAL FEATURES

BUS type:	**ABACO®**
Addressable Range:	256
Bytes taken:	2
Local resources:	8 analog outputs in the range 4÷20 mA 9 protection and filtering sections 8 D/A converter with resolution 16 bits 1 fast optocoupler section 1 TTL asynchronous serial line 1 configration 8 pins dip switch 1 address setting 8 pins dip switch 4 indication LEDs
Local peripherals:	8 AD420
Local CPU:	ATMEL AT89c51AC2 with quartz 14.7456 MHz
Local memory:	IC3: FLASH EPROM 32KBytes RAM 1280 Bytes EEPROM 2KBytes
Physical serial protocol:	please contact **grifo®**
Analog output resolution:	16 bits
D/A channel settling time:	3.8 msec
Reset time:	80 msec
Interrupt activation time:	5 µsec
Firmware commands:	10

PHYSICAL FEATURES

Size:	Eurocard standard format 100 x 160 mm
Weight:	170 g max
Connectors:	K1: DIN 41612, 64 pins, male, 90 degreeses, A+C type C

CN1: quick release screw terminal, 2 pins, 90 deg, 3.5 mm pitch
CN2: quick release screw terminal, 2 pins, 90 deg, 3.5 mm pitch
CN3: quick release screw terminal, 2 pins, 90 deg, 3.5 mm pitch
CN4: quick release screw terminal, 2 pins, 90 deg, 3.5 mm pitch
CN5: quick release screw terminal, 2 pins, 90 deg, 3.5 mm pitch
CN6: quick release screw terminal, 2 pins, 90 deg, 3.5 mm pitch
CN7: quick release screw terminal, 2 pins, 90 deg, 3.5 mm pitch
CN8: quick release screw terminal, 2 pins, 90 deg, 3.5 mm pitch
CN9: quick release screw terminal, 2 pins, 90 deg, 5 mm pitch
CN10: low profile 5 pins, male, vertical

Temperature range: From 0 to 70 °C

Relative humidity: 20% up to 90% (without condense)

ELECTRIC FEATURES

Power supply:	+5 Vdc ±5%.	
Digital current consumption:	105 mA (default configuration) 130 mA (higest consumption)	
Analog power supply voltage:	12 ÷ 32 Vdc (typical 22 Vdc)	
Analog current consumption:	54 mA (default configuration) 205 mA (higest consumption)	
Output current range of D/A:	4.0000 ÷ 20.0000 mA	
Offset:	±0.0020 mA	(*)
Linearity:	±0.0030 mA	(*)
Repetibility on the same channel:	±0.0010 mA	(*)
Max difference of output current on all channels:	±0.0100 mA	(*)
Total noise:	±0.0001 mA	(*)
Max error due to power supply:	±0.0300 mA	(*)
Max error due to temperature:	±0.0070 mA	(*)
Maximum resistance connectable:	300 Ω	(*)

(*) Data reported here are referred to a typical +Vdcanalog (analog power supply) +22 Vdc

INSTALLATION

In this chapter there are the information for a right installation and correct use of **LDA 420**.
In detail there are the locations and functions of each connector, of the user LEDs,jumpers, dip switches, etc.

CONNECTIONS

LDA 420 has 11 connectors that can be linkeded to other devices or directly to the field, according to system requirements.
In this paragraph there are connectors pin out, a short signals description (including the signals direction) and connectors location (see figure 13 to easily locate them).

CN1÷CN8 - D/A ANALOG OUTPUT CONNECTORS

CN1÷CN8 are eight 2 pins quick release screw terminal connector, 90 degreeses, pitch 3.5 mm.
These connectors feature the eight current analog outputs 4÷20 mA generated by **LDA 420**, ready to be connected to the external world.
Connectors are located in the frontal to easy the connection and signals location is designed to reduce the interferences as much as possible.

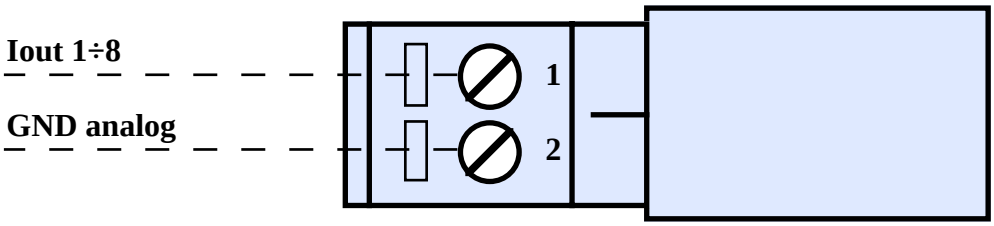

FIGURE 3: CN1÷CN8 - D/A ANALOG OUTPUT CONNECTORS

Signals description:

Iout n = O - D/A n-th current output signal, in the range 4÷20 mA.
D/A GND = - Ground of analog output signals.

Connectors CN1÷CN8 are always present while some of the corresponding analog signals are available only if **LDA 420** is opportunely configured.

Following figures show the connection modalities for all analog outputs both locally and externally; in specific figure 7 allows to locate more easily the positions both of signals and of connectors.

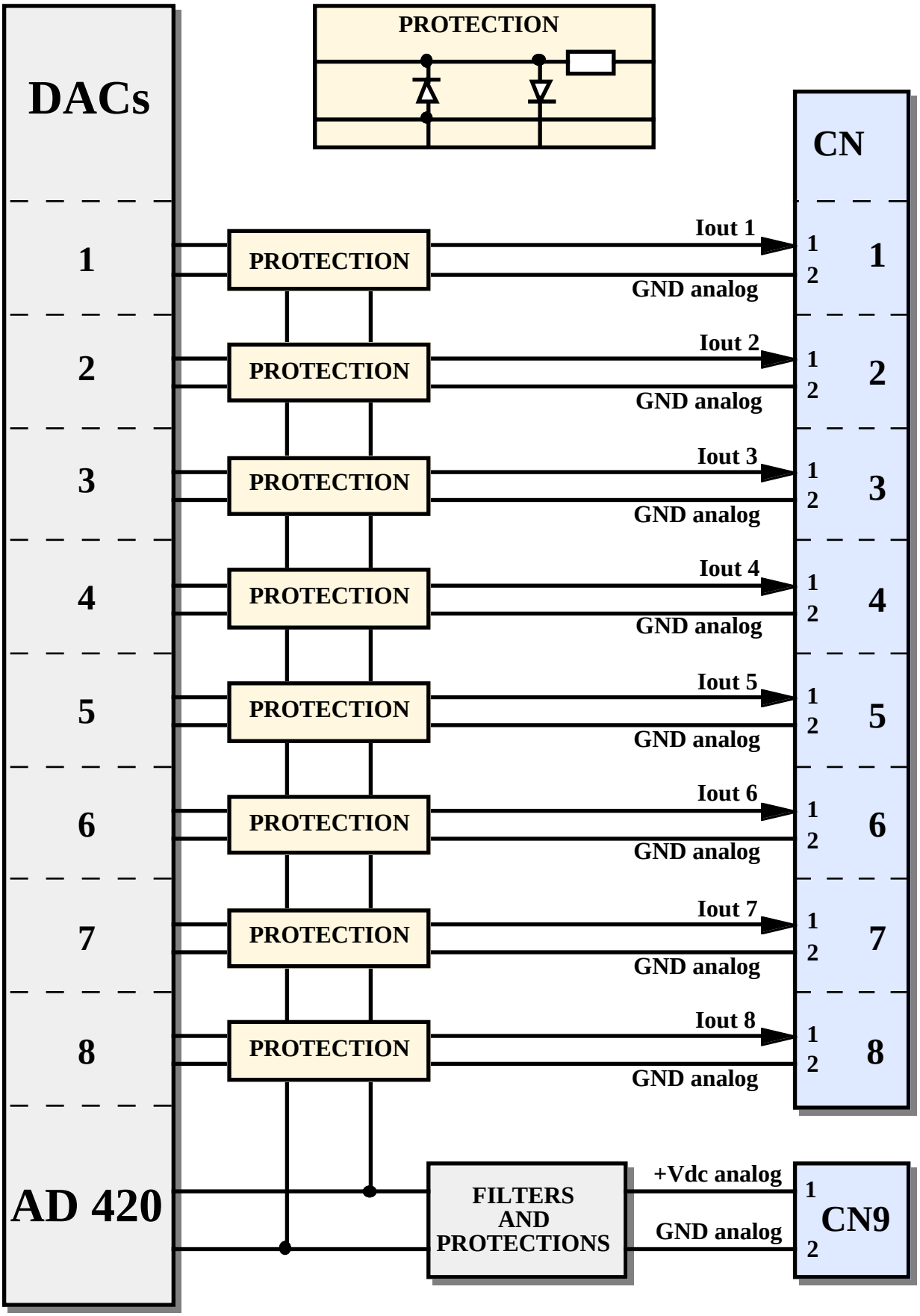

FIGURE 4: D/A SECTION CONNECTIONS BLOCK DIAGRAM

As can be seen on figure 4, every analog output is provided with its own protection circuitery which prevents damages and breakings in case of connection to incompatible devices.
Such circuitery keeps the voltage in the current loop between the limits of analog power supply (+Vdcanalog) through the two clamping diodes and keeps the amount of current circulating in the allowed range (serie resistor).
Anamog power supply (+Vdcanalog) is required to supply the whole section and to proved the current for the outputs installed. These latter are therfore ACTIVE outputs so they must be connected to PASSIVE devices capable to accept a supplied current loop.
Following figure shows the connection modality of external devices with indications about their analog input stage: such stage should be ideal (impedance = 0), but in real applications impedance must be lower than 300 Ω.
For further information about analog outputs please refer to paragraph "ELECTRIC FEATURES".

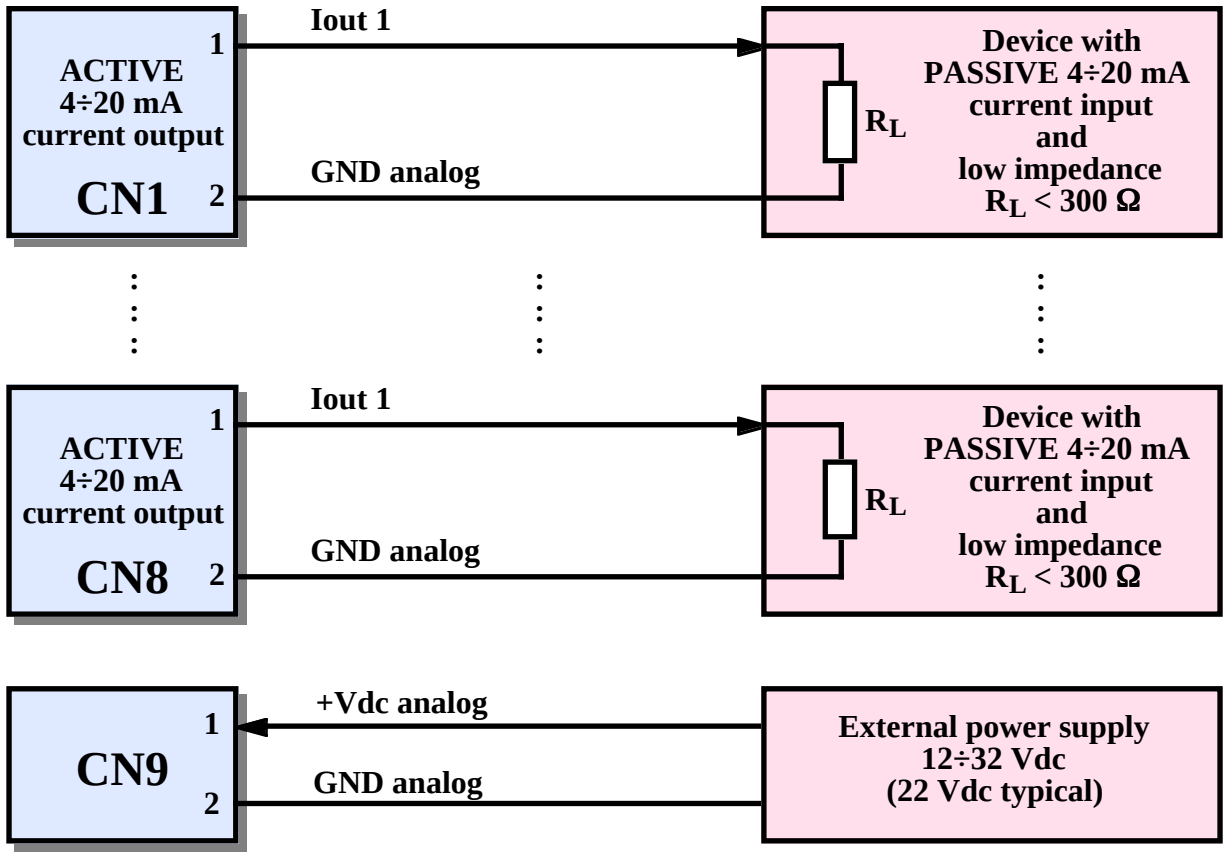

FIGURE 5: CONNECTION OF ANALOG OUTPUTS TO EXTERNAL DEVICES

CN9 - ANALOG POWER SUPPLY CONNECTOR

CN9 is a 2 pins quick release screw terminal connector, 90 degreeses, pitch 5.12 mm.
Power supply for analog section must be connected to CN9, it is required to make the **LDA 420** work correctly.
CN9 is on the frontal side to easy connection.

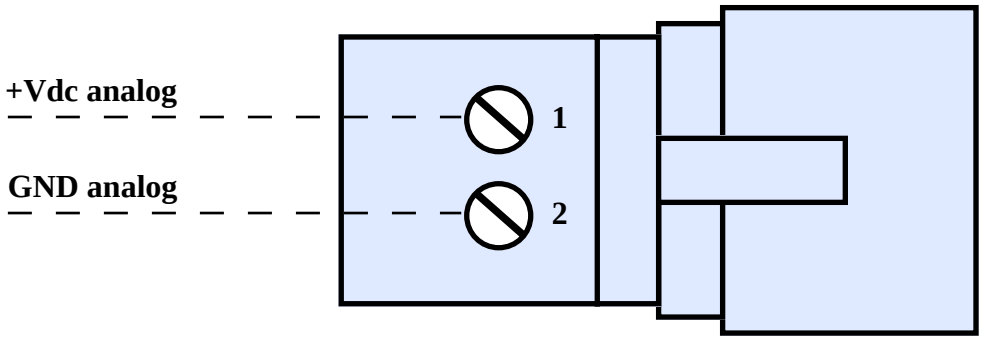

FIGURE 6: CN9 - ANALOG POWER SUPPLY CONNECTOR

Signals description:

+Vdc analog = I - Analog power supply signal: 12 ÷ 32 Vdc (typical is 22 Vdc).
GND analog = - Ground of analog output signals.

For further information about analog power supply please refer to paragraph "POWER SUPPLY".
The figure below shows signals location on the connectes dedicated to analog outputs seen from the component side of **LDA 420**.

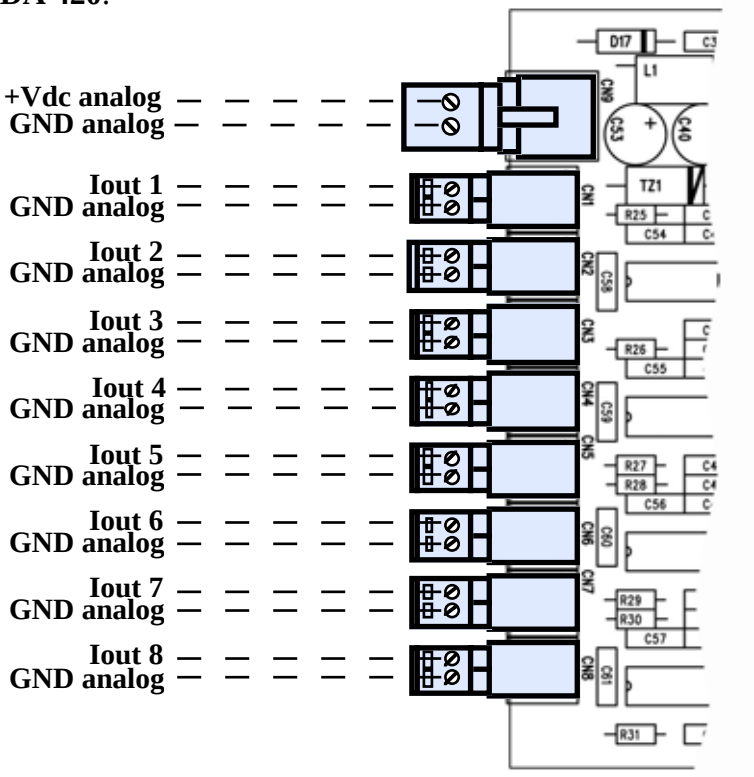

FIGURE 7: ANALOG SIGNALS LOCATION

CN10 - SERIAL LINE CONNECTOR

CN10 is a 5 pins low profile, vertical, male connector pitch 2.54 mm.
CN10 features all the signals for TTL serial communication, that is digital power supply, TX and RX signals plus a third signal (direction) in case of network communication.
Pins location is designed to reduce interferences as much as possible and to easy the connection.
Female connector for CN10 can be ordered to **grifo®** by specifing code CC.RS422 in the order, which corresponds to a set of 5 colored wires one meter long, crimped on a 5 pins female connector.

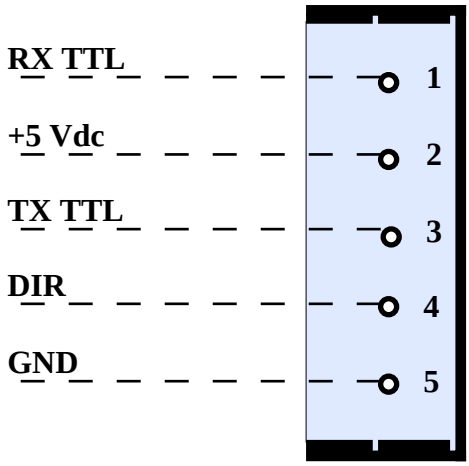

FIGURE 8: CN10 - SERIAL LINE CONNECTOR

Signals description:

RX TTL	=	I	- Receive Data: TTL serial reception signal.
TX TTL	=	O	- Transmit Data: TTL serial transmission signal.
DIR	=	O	- Direction or handshake signal for TTL serial line.
+5 Vdc	=	O	- Positive terminal of +5 Vdc digital power supply.
GND	=		- Ground of analog output signals.

For further information about serial line configuration and its communication modalities, please contact **grifo®** directly, while for further information about how to connect this device both to other TTL devices and to devices with another serial line protocol, please refer to the following figures.

FIGURE 9: TTL SERIAL CONNECTION EXAMPLE

Surely the conversion interface **MSI 01** is the most comfortable solution to convert a TTL serial line of **LDA 420** into a RS 232, RS 422, RS 485 or current loop serial line.
As already indicated in chapter "SERIAL COMMUNICATION" these electric protocols allow to connect **LDA 420** event at remarkable distances, through electrically noisy environments and even making networks at low cost.

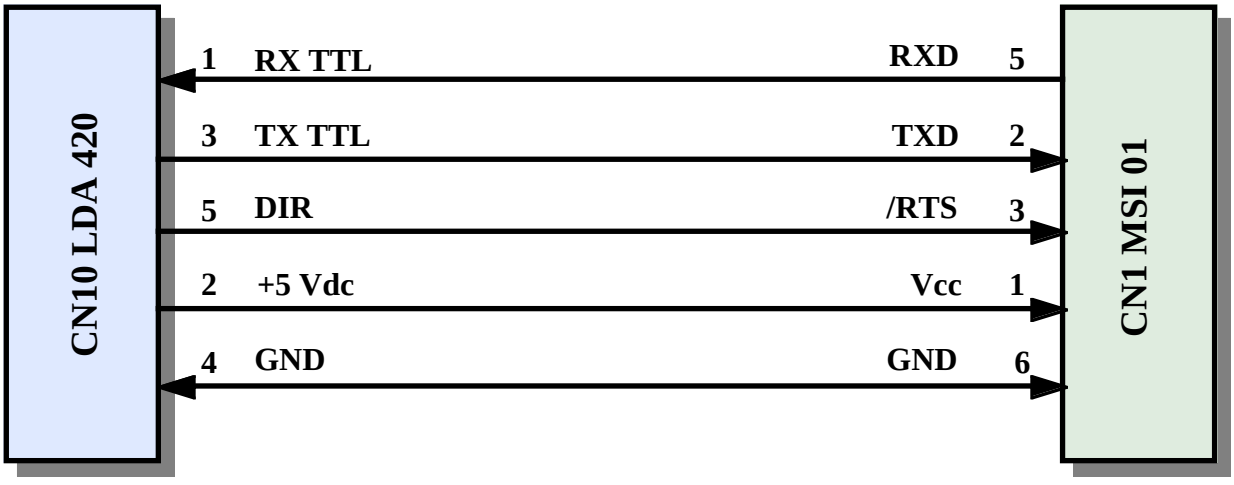

FIGURE 10: CONNECTION THROUGH MSI 01 SERIAL INTERFACE

K1 - CONNECTOR FOR ABACO® BUS

The connector for **ABACO® industrial BUS**, called K1 on the board,is a DIN 41612, male, a 90 °, type C, A+C.
Here follows the pin-out of the connector installed on **LDA 420**, in addition there is the standard 8 bits and 16 bits**ABACO®** BUS pin-out.
Please remark that all the signals here described are TTL, except for the power supplies.

Row A 16 bit BUS	Row A 8 bit BUS	K1 A LDA 420	PIN	K1 C LDA 420	Row C 8 bit BUS	Row C 16 bit BUS
GND	GND	GND	1	GND	GND	GND
+5 Vdc	+5 Vdc	+5 Vdc	2	+5 Vdc	+5 Vdc	+5 Vdc
D0	D0	D0	3	N.C.	-	D8
D1	D1	D1	4	N.C.	-	D9
D2	D2	D2	5	N.C.	-	D10
D3	D3	D3	6	/INT	/INT	/INT
D4	D4	D4	7	N.C.	/NMI	/NMI
D5	D5	D5	8	N.C.	/HALT	D11
D6	D6	D6	9	N.C.	/MREQ	/MREQ
D7	D7	D7	10	/IORQ	/IORQ	/IORQ
A0	A0	A0	11	/RD	/RD	/RDLDS
A1	A1	A1	12	/WR	/WR	/WRLDS
A2	A2	A2	13	N.C.	/BUSAK	D12
A3	A3	A3	14	N.C.	/WAIT	/WAIT
A4	A4	A4	15	N.C.	/BUSRQ	D13
A5	A5	A5	16	N.C.	/RESET	/RESET
A6	A6	A6	17	/M1	/M1	/IACK
A7	A7	A7	18	N.C.	/RFSH	D14
A8	A8	N.C.	19	N.C.	/MEMDIS	/MEMDIS
A9	A9	N.C.	20	N.C.	VDUSEL	A22
A10	A10	N.C.	21	N.C.	/IEI	D15
A11	A11	N.C.	22	N.C.	-	-
A12	A12	N.C.	23	N.C.	CLK	CLK
A13	A13	N.C.	24	N.C.	-	/RDUDS
A14	A14	N.C.	25	N.C.	-	/WRUDS
A15	A15	N.C.	26	N.C.	-	A21
A16	-	N.C.	27	N.C.	-	A20
A17	-	N.C.	28	N.C.	-	A19
A18	-	N.C.	29	N.C.	/R.T.	/R.T.
+12 Vdc	+12 Vdc	N.C.	30	N.C.	-12 Vdc	-12 Vdc
+5 Vdc	+5 Vdc	+5 Vdc	31	+5 Vdc	+5 Vdc	+5 Vdc
GND	GND	GND	32	GND	GND	GND

FIGURE 11: K1 - CONNECTOR FOR ABACO® BUS

Signals description:

8 bits CPU

A0-A15	=	O	- Address BUS
D0-D7	=	I/O	- Data BUS
INT	=	I	- Interrupt request
NMI	=	I	- Non Maskable Interrupt
HALT	=	O	- Halt state
MREQ	=	O	- Memory Request
IORQ	=	O	- Input Output Request
RD	=	O	- Read cycle status
WR	=	O	- Write cycle status
BUSAK	=	O	- BUS Acknowledge
WAIT	=	I	- Wait
BUSRQ	=	I	- BUS Request
RESET	=	O	- Reset
M1	=	O	- Machine cycle one
RFSH	=	O	- Refresh for dynamic RAM
MEMDIS	=	I	- Memory Display
VDUSEL	=	O	- VDU Selection
IEI	=	I	- Interrupt Enable Input
CLK	=	O	- System clock
R.B.	=	I	- Reset button
+5 Vdc	=	I	- Power supply at +5 Vdc
+12 Vdc	=	I	- Power supply at +12 Vdc
-12 Vdc	=	I	- Power supply at -12 Vdc
GND	=		- Ground signal

16 bits CPU

A16-A22	=	O	- Address BUS
D8-D15	=	I/O	- Data BUS
RD UDS	=	O	- Read Upper Data Strobe
WR UDS	=	O	- Write Upper Data Strobe
IACK	=	O	- Interrupt Acknowledge
RD LDS	=	O	- Read Lower Data Strobe
WR LDS	=	O	- Write Lower Data Strobe

NOTE
Directionality indications as above stated are referred to a master (**GPC®**) board and have been kept untouched to avoid ambiguity in case of multi-boards systems.

I/O CONNECTIONS

To prevent possible connecting problems between **LDA 420** and the external systems, the user has to read carefully the previous paragraph information and must follow these instrunctions:

- For RS 232, RS 422, RS 485, current loop and TTL signals the user must follow the standard rules of each one of these protocols;

- For all TTL signals the user must follow the rules of this electric standard. The connected digital signal must be always referred to card digital ground and if an electric insulation is necessary, then an opto coupled interface must be connected. For TTL signals, the 0V level corresponds to logic state 0, while 5V level corrisponds to logic state 1.

- The analog outputs must be connected to low impedance passive inputs: using a shielded cable reduces the electric noise. Eventual connections to power actuators (motors), must be made through a specific power driver circuits, e.g., activation or inverter.

- To take advantage of **LDA 420** galvanic separation, it must be supplied using two separated tensions from two diffrerent sources, that must be galvanically separated too.

- Analog power supply must be proviede by a source that generates no electric noise, perfectly stable and indipendent from any external factor like temperature, radio frequincies, etc.

VISUAL SIGNALATIONS

LDA 420 features 4 LEDs described in the following table:

LED	COLOUR	PURPOSE
LD1	Red	Visualizes parallel communication interrupt activation (interrupt request from **LDA 420** to CPU master on BUS **ABACO®**).
LD2	Red	When parallel communication is used, it turns ON when a data is received.
LD3	Yellow	Activity LED manageable through a specific command and general malfunction indication.
LD4	Green	Activity LED manageable through a specific command.

FIGURE 12: LEDS TABLE

The main function of LEDs is to inform the user about status, with a simple visual indication and in addition to this, LEDs make easier the debug and test operations of the complete system.
Firmware turns LEDs ON and OFF automatically, according to the situation and the conditions and provides further visual indications about status and malfunctioning.
To recognize the LED location on the card, please refer to figure 13.

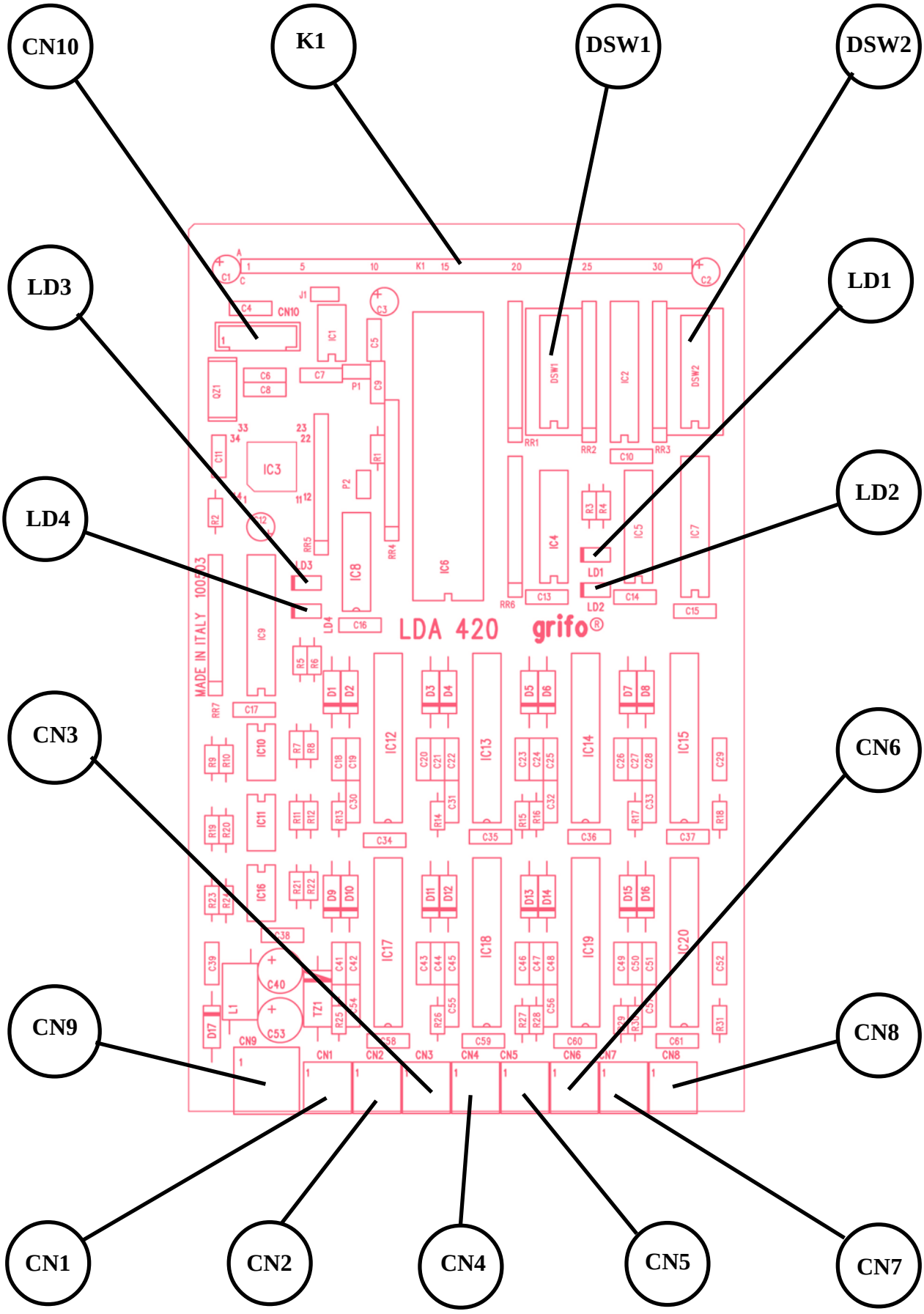

FIGURE 13: LEDS, CONNECTORS, DIP SWITCH, ETC. LOCATION

JUMPERS

On **LDA 420** there are 3 jumpers and two dip switches for working mode configuration.
Here below is the jumpers list, location and function:

JUMPER	N° PINS	PURPOSE
J1	2	Connects parallel communication request signals to interrupt on BUS **ABACO®**.
P1	2	Reset contacts (please see paragraph POWER ON AND RESET).
P2	2	Selects CPU operating mode.
DSW2.1	2	Enables management of signal /M1 coming from BUS **ABACO®**.

FIGURE 14: JUMPERS SUMMARIZING TABLE

The following tables describe all the right connections of **LDA 420** jumpers with their relative functions.
To recognize these valid connections, please refer to the board printed diagram (serigraph) or to figure 2 of this manual, where the pins numeration is listed; for recognizing jumpers location, please refer to figure 16.
The "*" denotes the default connection, or on the other hand the connection set up at the end of testing phase, that is the configuration the user receives.

2 PINS JUMPERS

JUMPER	CONNECTION	PURPOSE	DEF.
J1	not connected	Does not connect parallel communication request signal to interrupt on BUS **ABACO®**.	*
	connected	Connects parallel communication request signal to interrupt on BUS **ABACO®**.	
P1	not connected	On board CPU reset signal, not actived.	*
	connected	On board CPU reset signal kept actived.	
P2	not connected	Selects RUN mode for on board CPU.	*
	connected	Selects DEBUG mode for on board CPU. (reserved to grifo® technicians).	
DSW2.1	not connected	Circuitery to interface BUS **ABACO®** does not manage signal /M1.	*
	connected	Circuitery to interface BUS **ABACO®** manages signal /M1.	

FIGURE 15: 2 PINS JUMPERS TABLE

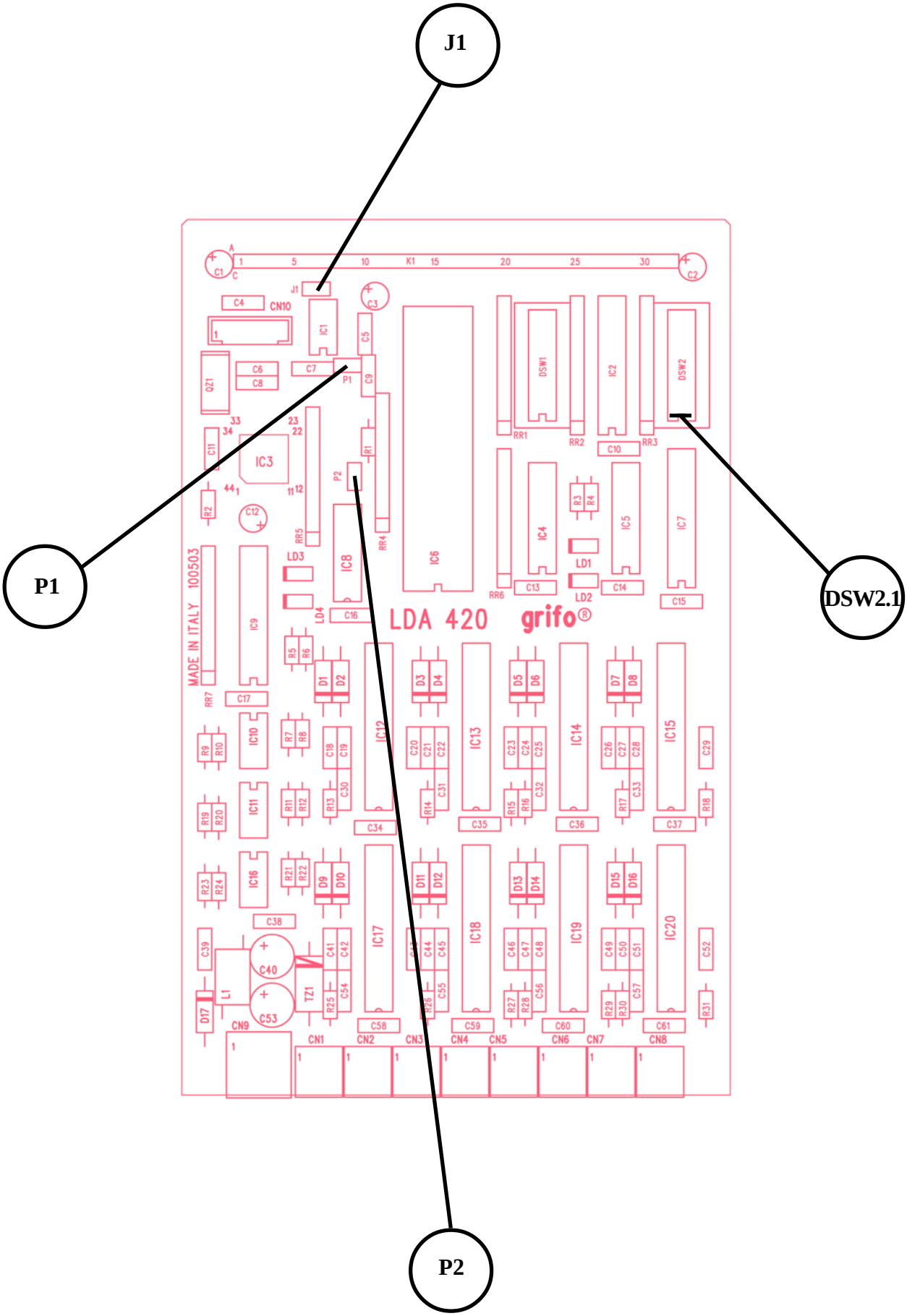

FIGURE 16: JUMPERS LOCATION

RESET AND POWER ON

LDA 420 is provided with a reset circuitery that manages the always critical phase of turining on and at the same time it monitors continuously digital power supply voltage, to avoid problems due to misuse.
After activation and consequent deactivation of reset circuitery, **LDA 420** restart the execution of management firmware in a condition where all outputs are set to the beginning og the scale (4 mA). This circuitery decides also the time elapsed between its activation and firmware restart: 50 msec in case of reset and 80 msec in case of power on.
Possible reset sources are jumper P1 and power supply control circuitery but remarkable is the fact that /RESET signal of BUS **ABACO®** (pin 16 of connector K1) is not connected, so **LDA 420** in NOT aware of reset CPU or GPC® reset signals.
Pins of P1 can be connected to a normally open contact (e.g. a push button) and when the contact is closed (the pins are short-circuited) reset circuitery activates with opportune timings.
Its main purpose is to exit from infinite loop conditions, especially during debug phase, and to execute the application program from the beginning without having to disconnect power supply/
To easily locate reset contact, please refer to figure 16.

INTERRUPT

LDA 420 generates an interrupt request when the local CPU must send a data to the control system on BUS **ABACO®** or when it is in condition to reveice a data from this latter.
By hardware, it is possible to connect this request to /INT signal on BUS **ABACO®** (pin 6C of connector K1), and LED LD1 shows its status.
Main purpose of interrupt signal is to ask the attention of the control system when it is possible a bidirectional data exchange, it is easy to see that this signal allows to optimize management times, in fact control system must not poll for the status of **LDA 420**.
Interrupt signal remains in active status for 5 µsec, to allow a correct management also in case of contemporary interrupts generated by other peripherals.

POWER SUPPLY

LDA 420 requires two power supplies:

- *for digital section* supply must be +5 Vdc ± 5%, that must be provided through the specific pins of connector K1. Tracks lay out has been designed to fetch digital supply from K1 and distribute it to all the point that require it; this explains the directionality reported in the signal descriptions and the connectors, where +5 Vdc is an input only on K1. For special cases the user can provide +5 Vdc also from different entry points, but must make a preventive correct working verification. A filtering circuitery efficent and distributed protects the local sections against disturbs or noise from the external world, to improve the overall working efficence.

- *for analog section* supply must be in the range +12 ÷ +32 Vdc, that must be provided through the pins 1 and 9 of connector CN9 respecting the polarity. This voltage is used to supply the whole analog section including the current outputs, this means that its current consumption changes according to the configuration ordered. Typical voltage for this supply is +22 Vdc, that minimizes offset and linearity errors; **EXPS-1** power supply generates this voltage starting from main power supply. Anolog voltage connected to CN9 passes through a filtering and protection circuitery, which includes also a **TransZorb™**, to prevent damages due to wrong voltages and breaking of supply section and to get a greater stability on the signals generated.

To warrant highest immunity against disturbs and so a correct working of the whole system, it is required that these two voltages are galvanically separated.
In other words the user must assure that signals **GND** and **GNDanalog** are electrically NOT connecrd.
For further information please refer to paragraph "ELECTRIC FEATURES".

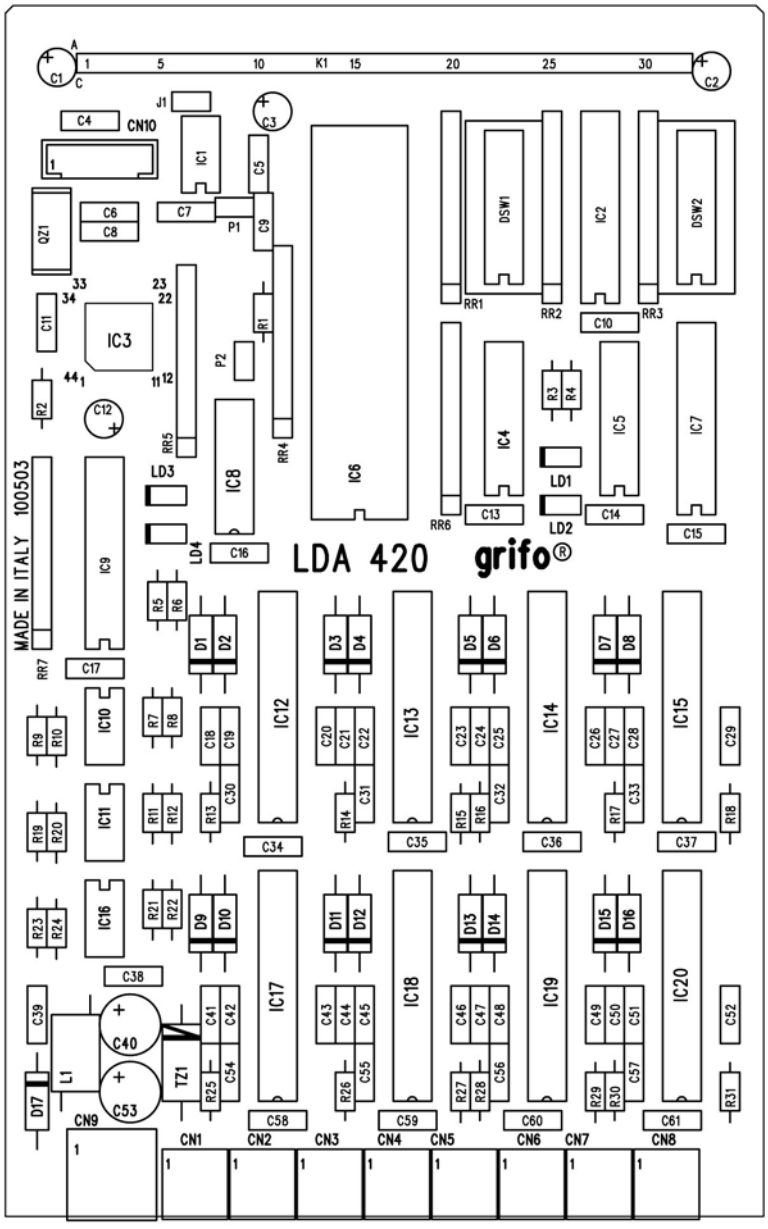

FIGURE 17: COMPONENTS MAP (SOLDER SIDE)

ADDRESSES AND MAPS

This chapter provides all the hardware informations needed to use **LDA 420** board.
Here the user will find informations about I/O space mapping and local peripheral devices addressing.
Of course, if **LDA 420** is configured for serial communication, all the information reported in this chapter are superfluous.

PERIPHERAL MAPPING

LDA 420 is mapped into a **2** contiguous bytes I/O addressing space, that can be mapped starting from different base addresses according to how the board is configured. This feature allows to use several **LDA 420** on the same BUS **ABACO®**, or to install them on a BUS where other peripheral modules are installed obtaining a structure that can be expanded without any difficulty or modifications to the application software.
The base address can be defined through the specific BUS interface circuitry on the board itself; this circuitry uses the eight pins dip switch called **DSW2**, from which it reads the address set by the user.
Here follows the corrispondance between dips configuration and address signals.

DSW2.1	->	Not used (See paragraph "JUMPERS")
DSW2.2	->	Address A1
DSW2.3	->	Address A2
DSW2.4	->	Address A3
DSW2.5	->	Address A4
DSW2.6	->	Address A5
DSW2.7	->	Address A6
DSW2.8	->	Address A7

These dips are driven in complemented logic, this means that if a switch is **ON** generates a **logic zero**, viceversa if a switch is **OFF** generates a **logic one**.
Dips DSW2.2 ÷ DSW2.8 allow to select the mapping address, ranging from 00H to FEH, covering a normal addressing range of 256 bytes where only even addresses (00H, 02H, ... , 0FEH) can be used.
Also DSW2.1, described in the previous chapters, influences addressing logic and must be set according to which control system (**GPC®**) is used.
In detail, if this latter is provided with /M1 signal on BUS **ABACO®** connector, then DSW2.1 must be ON and viceversa.
Do not allocate more than one peripheral in the same addressing space (calculate also number of bytes taken), otherwise the BUS conflicts that may derive could prevent the overall system from working properly.
As an example, here follows a mapping description:

LDA 420 should be mapped at address 192 = 0C0H, the control system is provided with signal /M1, mapping is done as follows:

DSW2.1 -> ON
DSW2.2 -> ON
DSW2.3 -> ON
DSW2.4 -> ON
DSW2.5 -> ON
DSW2.6 -> ON
DSW2.7 -> OFF
DSW2.8 -> OFF

To easily locate the components mentioned here, please refer to figures 13 and 16.

COMMUNICATION REGISTERS ADDRESSING

Indicating the board base address with <**baseaddr**>, that is the address set using dip switch DSW2, as indicated in the previous paragraph **LDA 420** internal registers are addressable as explained in the following table:

REGISTER	ADDRESS	R/W	PURPOSE
STATUS	<baseaddr>+00	R	Status register for parallel communication.
DATA	<baseaddr>+01	R/W	Data register for parallel communication.

FIGURE 18: REGISTERS ADDRESSING TABLE

As described in next paragraph, one register is read only while the other register irs readable and writeable, the first one indicates communication status, the second one is used for data exchange.

PARALLEL COMMUNICATION MANAGEMENT

This paragraph explains the sofware management modalities of the parallel communication between **LDA 420** board and a master control unit.
The read/write DATA register, described in the previous table, allows to receive from and to transmit informations to the board, while the read only STATUS registers must be interpreted as follows:

	bit7	*bit6*	*bit5*	*bit4*	*bit3*	*bit2*	*bit1*	*bit0*
STATUS =	**OBF**	**IBF**	NU	NU	NU	NU	NU	NU

where:

NU = Not Used

IBF = If active (**1**) indicates that the **LDA 420** board is ready to receive a new data; the master control unit can write it to the DATA register.

OBF = If active (**1**) indicates that the **LDA 420** board has written a data into its transmission buffer; the master control unit can read the data performing a read operation of the DATA register.

After a Reset or a Power-On the master control unit must verify that the **LDA 420** board has completed its initialization phase and is ready to receive data.
This condition is indicated by the logic state of the flags IBF and OBF, which must show the values: **IBF=1** and **OBF=0**.
The program running on the control board must start by performing a cycle (eventually timed out for more safety) to test the status of these signals and wait for the **LDA 420** board to be ready for the commmunication.

To show the above described modalities, here follow two examples subroutines written in CBZ 80:

```
"sendtolda"
REM Send to LDA 420 data contained in variable var%
REM Begin
      DO                                  : REM Wait for bit IBF
            st%=INP(stato%)
      UNTIL ((st% AND &040)=&040)
      OUT dati%, var%                     : REM Send data to LDA 420
REM End
RETURN
```

```
"recfromlda"
REM Checks whether LDA 420 has sent a character; in such case character is returned
REM in variable var%, otherwise value -1 is returned
REM Begin
      st%=INP(stato%)                     : REM Check status of bit OBF
      LONG IF ((st% AND &080)=&080)
            var%=INP(dati%)               : REM Get data from LDA 420
          XELSE
            var%=-1                       : REM LDA 420 sent no data
      ENDIF
REM End
RETURN
```

SOFTWARE DESCRIPTION

LDA 420 operativity is completely managed by its firmware which allows data exchange through serial line or BUS **ABACO®** parallel interface.
The firmware can recognize several commands and take actions in consequence: in practice it allows to set a value on the current outputs and to set/report information about peripheral configuration.
Next paragraph reports the description of the possible working modalities: description is mnemonic, ASCII and numeric, both in decimal and in hexadecimal.
Following description is referred to version 1.1; please remark that in case of specific needs, custom firmwares can be developed, so to create the best application.
For this latter evenience, please contact **grifo®** directly.

GENERATED CURRENT AND CORRESPONDING COMBINATIONS

Commands managed by firmware of **LDA 420**, in specific referred to analog outputs, are based on a 16 bit combination, which is the resolution of D/A converters and of the channels.
Such combination has the following correspondance with generated Ioutn:

00000 = 0000H	->	4.0000 mA
65535 = FFFFH	->	20.0000 mA

this is a direct proportionality based on the current formula where the indipendent variable is the current desired in mA:

combination = *Round*(((Iout - 4) / 16) * 65535)

and where *Round* function approximates to the closest integer number. From the above, it is possible to obtain the corresponding inverse formula that returns the currnent in mA from the combination:

Iout = ((combination / 65535) * 16) + 4

Here follw some examples of combinations and corresponding generated currents:

Iout in mA	->	combination
4.0000	->	00000 = 0000H
5.0000	->	04096 = 1000H
5.1000	->	04506 = 119AH
5.1100	->	04546 = 11C2H
5.1110	->	04551 = 11C7H
5.1113	->	04552 = 11C8H
12.0000	->	32768 = 8000H
20.0000	->	65535 = FFFFH

LOGIC PROTOCOL

Logic protocol is the set of rules to code and organize data exchange to and from **LDA 420**, that is the rules that control system must follow to use properly the commands of **LDA 420**.
Logic protocol used by firmware is **GNET**: a grifo® legacy protocol designed and developed to peroform data exchange with any control unit and using both serial communication and parallel communication through BUS **ABACO®**.
For serial communication, as already indicated in this manual, please contact directly grifo®.
This protocol makes **LDA 420** echo each received byte, so to avoid communication errors it is opportune to wait for the echo of the byte just sent before sending another one.
The echo to wait for is the byte just sent.
Logic protocol for sending a command to **LDA 420** is:

1) Send individual IDENTIFICATION NAME (128 ÷ 255).
2) Reception of echo.
3) Command code transmission (16 ÷ 127).
4) Reception of echo.
5) Send most significant nibble (0 ÷ 15) of first parameter required by the command.
6) Reception of echo.
7) Send least significant nibble (0 ÷ 15) of first parameter required by the command.
8) Reception of echo.

: : :

: : :

N-3) Send most significant nibble (0 ÷ 15) of first parameter required by the command.
N-2) Reception of echo.
N-1) Send least significant nibble (0 ÷ 15) of first parameter required by the command.
N) Reception of echo.

The only bytes that the control system must always send are the first and the second (numbers 1 and 3) to specifiy which **LDA 420** in the network has to execute the command and which command must be executed; all other bytes are optional as some commands may even require no parameters at all.
Logic protocol used by **LDA 420** for communication of the eventual answer, after receiving a command, is:

N. BYTES RECEIVED FROM EXTERNAL SYSTEM	MEANING
1	Most significant nibble (0 ÷ 15) of first parameter returned by the command.
2	Least significant nibble (0 ÷ 15) of first parameter returned by the command.
:	: : : : : : : : : :
:	: : : : : : : : : :
N-1	Most significant nibble (0 ÷ 15) of last parameter returned by the command.
N	Least significant nibble (0 ÷ 15) of last parameter returned by the command.

This transmission begins only after **LDA 420** has sent the echo of the last character received.

Interpretation, execution and eventual answer transmission of a command are performed only if IDENTIFICATION NAME sent to the network and the same value stored in non-volatile memory of excactly one **LDA 420** in the same netwark are equal.
So, before sending a command to a **LDA 420** the user must set its name with the specific commands. At first, the commands can be used referring to a name equal to 255, which makes the **LDA 420** always execute a command, regardless the name stored in memory.
Of course, this operation must be executed only once, when the **LDA 420** is installed, or in case of modifications of the application.
IDENTIFICATION NAME that the GNET protocol uses is the main element that allows to connect more than one **LDA 420** in a netword and is stored in a EEPROM memory, which does not lose its content even when power supply is turned off.

To clarify, we remark that in the following paragraphs with PARAMETER we mean the transmission or reception of two bytes corresponding to the two nibbles that make if (first bytes is most significant nibble, second byte is least significant nibble).
The example reported at the end of a command description explains in detail this feature, idicating the operations to perform for a corret working of **LDA 420**.

Here follows a list of all available commands; figure A-1 shows a summary of them.

ACQUISITION OF CURRENT COMBINATION OFAN ANALOGIC CHANNEL

Code:	16
Hex Code:	10H
ASCII Mnemonic:	DLE
N. parameters required:	1
N. parameters returned:	2

Description:
After receiving the echo of command code (16), one parameter must be sent:

N. PARAMETER		MEANING
1	---------->	Number of analog channel to acquire (1÷8)

then 2 parametera are retruned, their meanging is:

N. PARAMETER		MEANING
1	---------->	Most significant byte of 16 bit combination set on the channel (0÷255)
2	---------->	Least significant byte of 16 bit combination set on the channel (0÷255)

SETTING OF CURRENT COMBINATION OFAN ANALOGIC CHANNEL

Code: 17
Hex Code: 11H
ASCII Mnemonic: DC1
N. parameters required: 3
N. parameters returned: 0

Description:
After receiving the echo of command code (17), three parameter must be sent:

N. PARAMETER		MEANING
1	---------->	Number of analog channel to set (1÷8)
2	---------->	Most significant byte of 16 bit combination to set on the channel (0÷255)
3	---------->	Least significant byte of 16 bit combination to set on the channel (0÷255)

SET ALL ANALOG OUTPUTS TO BEGINNING OF SCALE

Code: 18
Hex Code: 12H
ASCII Mnemonic: DC2
N. parameters required: 0
N. parameters returned: 0

Description:
After receiving the echo of command code (18), all analog outputs available are set to the value of the beginning of the scale, that is 4 mA.

ACQUISITION OF CONFIGURATION DIP SWITCH STATUS

Code: 19
Hex Code: 13H
ASCII Mnemonic: DC3
N. parameters required: 0
N. parameters returned: 1

Description:
After receiving the echo of command code (19), one parameter is returned:

N. PARAMETER		MEANING
1	---------->	Byte containing current status of configuration dio switch DSW1 (0÷255)

SET ACTIVITY LEDS STATUS

Code: 20
Hex Code: 14H
ASCII Mnemonic: DC4
N. parameters required: 2
N. parameters returned: 0

Description:
After receiving the echo of command code (10), two parameters must be sent:

N. PARAMETER		MEANING
1	---------->	Status of activity LED LD3, yellow (0 = OFF; 255 = ON)
2	---------->	Status of activity LED LD4, green (0 = OFF; 255 = ON)

OVERALL STATUS ACQUISITION

Code: 21
Hex Code: 15H
ASCII Mnemonic: NAK
N. parameters required: 0
N. parameters returned: 1

Description:
After receiving the echo of command code (21), one parameter is returned:

N. PARAMETER		MEANING
1	---------->	Byte containing overall status of peripheral (0÷7): DATA.0 -> Activity LED LD3 status (0 = OFF; 1 = ON) DATA.1 -> Activity LED LD4 status (0 = OFF; 1 = ON) DATA.2 -> Status of EEPROM configuration (0 = OK; 1 = error) DATA.3 -> Writing to EEPROM (0 = OK; 1 = error) DATA.4 -> Commands of GNET protocol (0 = OK; 1 = error) DATA.5 -> Parameters of GNET protocol (0 = OK; 1 = error) DATA.6 -> Not Used DATA.7 -> Not Used

ACQUISITION OF IDENTIFICATION NAME

Code: 22
Hex Code: 16H
ASCII Mnemonic: SYN
N. parameters required: 0
N. parameters returned: 1

Description:
After receiving the echo of command code (22), one parameter is returned:

N. PARAMETER		MEANING
1	---------->	Byte containing the identification name (128 ÷ 255)

SETTING OF IDENTIFICATION NAME

Code: 23
Hex Code: 17H
ASCII Mnemonic: ETB
N. parameters required: 1
N. parameters returned: 0

Description:
After receiving the echo of command code (23), one parameter is returned:

N. PARAMETER		MEANING
1	---------->	Byte containing the identification name (128 ÷ 255)

ACQUISITION OF ANALOG CHANNELS PRESENCE

Code: 24
Hex Code: 18H
ASCII Mnemonic: CAN
N. parameters required: 0
N. parameters returned: 1

Description:
After receiving the echo of command code (24), one parameter is returned:

N. PARAMETER		MEANING
1	---------->	Byte containing DAC presence configuration (3 ÷ 255): DATA.0 -> Channel 1 (0 = not present; 1 = present) this is always present DATA.1 -> Channel 2 (0 = not present; 1 = present) this is always present DATA.2 -> Channel 3 (0 = not present; 1 = present) DATA.3 -> Channel 4 (0 = not present; 1 = present) DATA.4 -> Channel 5 (0 = not present; 1 = present) DATA.5 -> Channel 6 (0 = not present; 1 = present) DATA.6 -> Channel 7 (0 = not present; 1 = present) DATA.7 -> Channel 8 (0 = not present; 1 = present)

ACQUISITION OF FIRMWARE VERSION

Code: 25
Hex Code: 19H
ASCII Mnemonic: EM
N. parameters required: 0
N. parameters returned: 1

Description:
After receiving the echo of command code (25), one parameter is returned:

N. PARAMETER		MEANING
1	---------->	Byte containing firmware version multiplied by 10, that is if firmware version is 1.1, 11 is returned

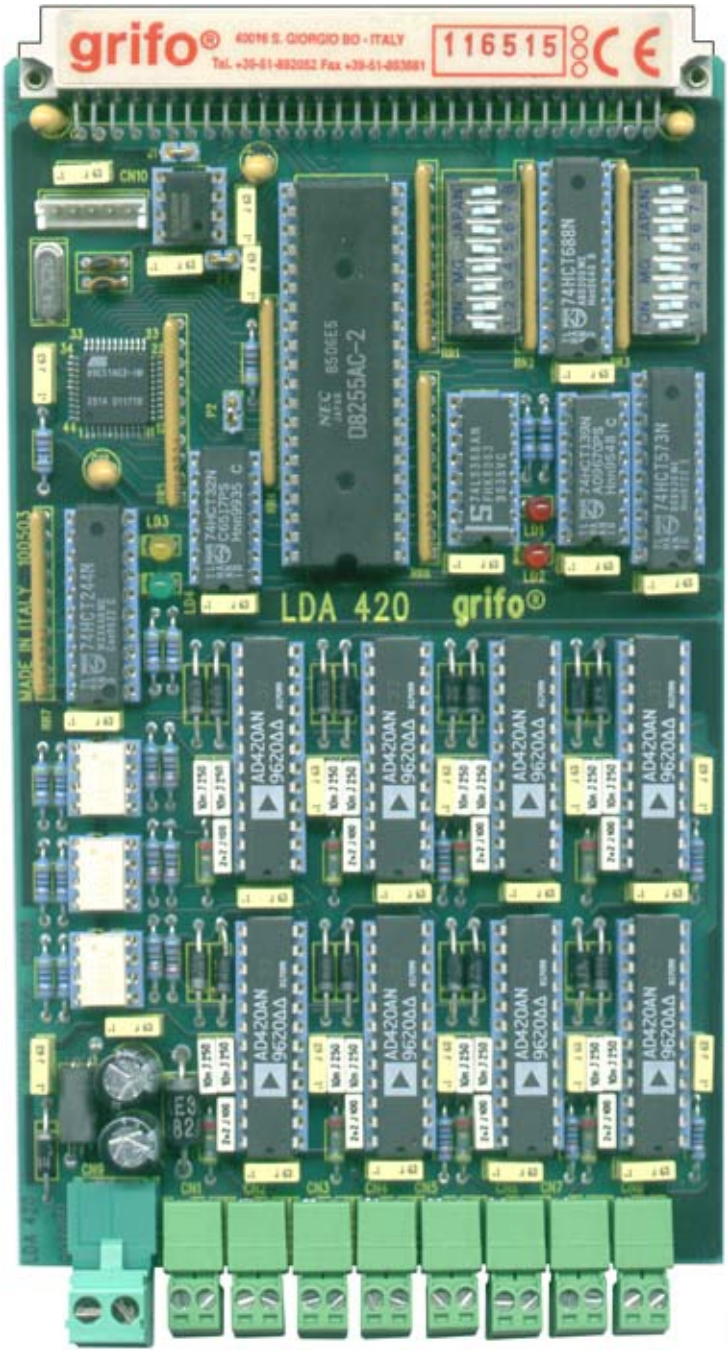

FIGURE 19: PHOTO OF THE PERIPHERAL

COMMUNICATION EXAMPLE

To clarify the communication modalities, here follow the basic operations that control system must perform to execute some commands of **LDA 420**.
The three commands used in this example are respectively: SETTING OF IDENTIFICATION NAME, OVERALL STATUS ACQUISITION and SETTING OF CURRENT COMBINATION OF AN ANALOG CHANNEL.

01) Send byte 255	(255 = identification name always recognized)
02) Wait for byte echo	
03) Send byte 23	(23 = command Setting Of Identification Name)
04) Wait for byte echo	
05) Send byte 08	(08 = Most significant nibble of identification name 128=80H)
06) Wait for byte echo	
07) Send byte 00	(00 = Least significant nibble of identification name 128=80H)
08) Wait for byte echo	
09) Send byte 128	(128 = identification name)
10) Wait for byte echo	
11) Send byte 21	(21 = command Overall Status Acquisition)
12) Wait for byte echo	
13) Wait for one byte reception	(= Most significant nibble of status)
14) Wait for one byte reception	(= Least significant nibble of status)
15) Send byte 128	(128 = identification name)
16) Wait for byte echo	
17) Send byte 17	(17 = command Set Current Combination Of An Analog Channel)
18) Wait for byte echo	
19) Send byte 01	(01 = MS Nibble of MSB Byte of combination to set = 1234H)
20) Wait for byte echo	
21) Send byte 02	(02 = LS Nibble of MSB Byte of combination to set = 1234H)
22) Wait for byte echo	
23) Send byte 03	(03 = MS Nibble of LSB Byte of combination to set = 1234H)
24) Wait for byte echo	
25) Send byte 04	(04 = LS Nibble of LSB Byte of combination to set = 1234H)
26) Wait for byte echo	

Of course, basic operations "Send byte", "Wait for byte reception" and "Wait for byte echo" are different according to the kind of communication selected.
In fact, in case of serial communication system modalities will be used while in case of parallel BUS communications modalities described in chapter "PARALLEL COMMUNICATION MANAGEMENT" will be used.

EXTERNAL CARDS

LDA 420 can be connected to a wide range of block modules and operator interface system produced by **grifo®**, or to many system of other companies.The local resources can be expanded with a simple connection to the numerous peripheral **grifo®**,both intelligent and not, thanks to its standard **ABACO®** BUS connector. Even cards with **ABACO®** I/O BUS can be connected, by using the proper mother boards.
Hereunder some of these cards are briefly described; ask the detailed information directly to **grifo®**, if required.

MB3 01-MB4 01-MB8 01
Mother Board 3, 4, 8 slots
Motherboard featuring 3, 4 or 8 slots of **ABACO®** industrial BUS; pitch 4 TE; standard power supply connectors; LEDs for visual feed-back of power supply; holes for rack docking.

SPB 04-SPB 08
Switch Power BUS 4-8 slots
Motherboard featuring 4-8 slots of **ABACO®** industrial BUS; pitch 4 TE; standard power supply connectors; termination resistances; connector type F for **SPC xxx** supply ; holes for rack docking.

ABB 05
ABACO® Block BUS 5 slots
5 slots **ABACO®** mother board with power supply. Double power supply built in; 5Vdc 2,5A section for powering the on board logic; second section at 24Vdc 400mA galvanically coupled, for the optocoupled input lines. Auxiliary connector for **ABACO®** I/O BUS. Connection for DIN Ω rails.

SBP 02-xx
Switch BLOCK Power xx version
Low cost switching power supply able to generate voltage from +5 to +40 Vdc and current up to 2.5 A; Input from 12 to 24 Vac; Connection for DIN C Type and Ω rails.

SPC 03.5S
Switch Power Card +5 Vdc
Europe format switching power supply capable to provide +5 Vdc to a load of 4 A; input voltage 12÷24 Vac; power-failure; connector for back-up battery; standard connector for mother board **SPB 0x**.

GPC® 188F
General Purpose Controller 80C188
80C188 µP 20 MHz; 256K FLASH; 256K RAM Lithium battery backed; 8K serial EEPROM; 1 RS 232 line; 1 RS 232 or RS 422-485 or Current Loop line; 24 TTL I/O lines; RTC; 8 A/D lines at 12 bits; Watch dog; 8 Dip switch; 3 Timer Counter.

GPC® 15A
General Purpose Controller 84C15
Full CMOS card, 10÷20 MHz 84C15 CPU; 512K EPROM or FLASH; 128K RAM; 8K RAM and RTC backed; 8K serial EEPROM; 1 RS 232 line or RS 422-485 or Current Loop line; 32 or 40 TTL I/O lines; CTC; Watch dog; 2 Dip switches; Buzzer.

GPC® 550

General Purpose Controller 80C552

Microprocessor 80C552 at 22 MHz. 32K EPROM; 32 K RAM; 32 K EEPROM or SRAM; RTC; serial EEPROM; serial lines 1 RS 232 + 1 RS 232 or RS 422-485 or current loop; 40 I/O TTL; 2 lines of PWM; 16 bits timer/counter; watch dog; dip switch; 8 lines 10 bit A/D converter; interface for BUS **ABACO®**; CAN line galvanically isolated. Unique power supply +5 Vdc; EUROCARD format.

IPC 52

Intelligent Peripheral Controller, 24 analogic input

This intelligent peripheral card acquires 24 indipendent analogic input lines: 8 PT 100 or PT 1000 sensors, 8 J,K,S,T termocouples, 8 analog input ±2Vdc or 4÷20mA; 16 bits + sign A/D section; 0.1 °C resolution; 32K RAM for local data logging; buzzer; 16 TTL I/O lines; 5 or 8 conversion per second; facility of networking up to 127 IPC 52 cards using serial line. BUS interfacing or through RS 232, RS 422, RS 485 or current loop line. Only 5Vdc power supply.

JMS 34

Jumbo Multifunction Support for Axis control

Generic peripheral axis control card. 3 optocoupled acquisition channels, with 16 bits bidirectional counter, for incremental encoder. 4 12bits ±10Vdc D/A channels. 8 Opto-in; 8 NPN Opto-output 40Vdc 500 mA. All I/O lines displayed with LEDs.

MSI 01

Multi Serial Interface 1 line

Interface card for TTL serial line that is buffered in RS 232, RS 422, RS 485, or current loop line. The TTL line is on a mini screw connector and the buffered one is on standard plug connector.

CI/O R16

16 Coupled Input Output Relé

16 optocoupled input with π-filter; input voltage 24 Vdc. 16 micro-relays 1 A with disturb suppression by MOV 24 Vac. I/O visualized through LEDs; 8 bit BUS; standard addressing.

EXPS-1

EXternal Power Supply 2 tensioni

Mains power supply 75x55x90 mm with plastic container. Input voltage: 230 Vac, 50 Hz. Output voltage: 24 Vdc, 200 mA. Standard wall plug for input power supply. Quick release screw terminal connector for output voltage. Output voltage LED presence.

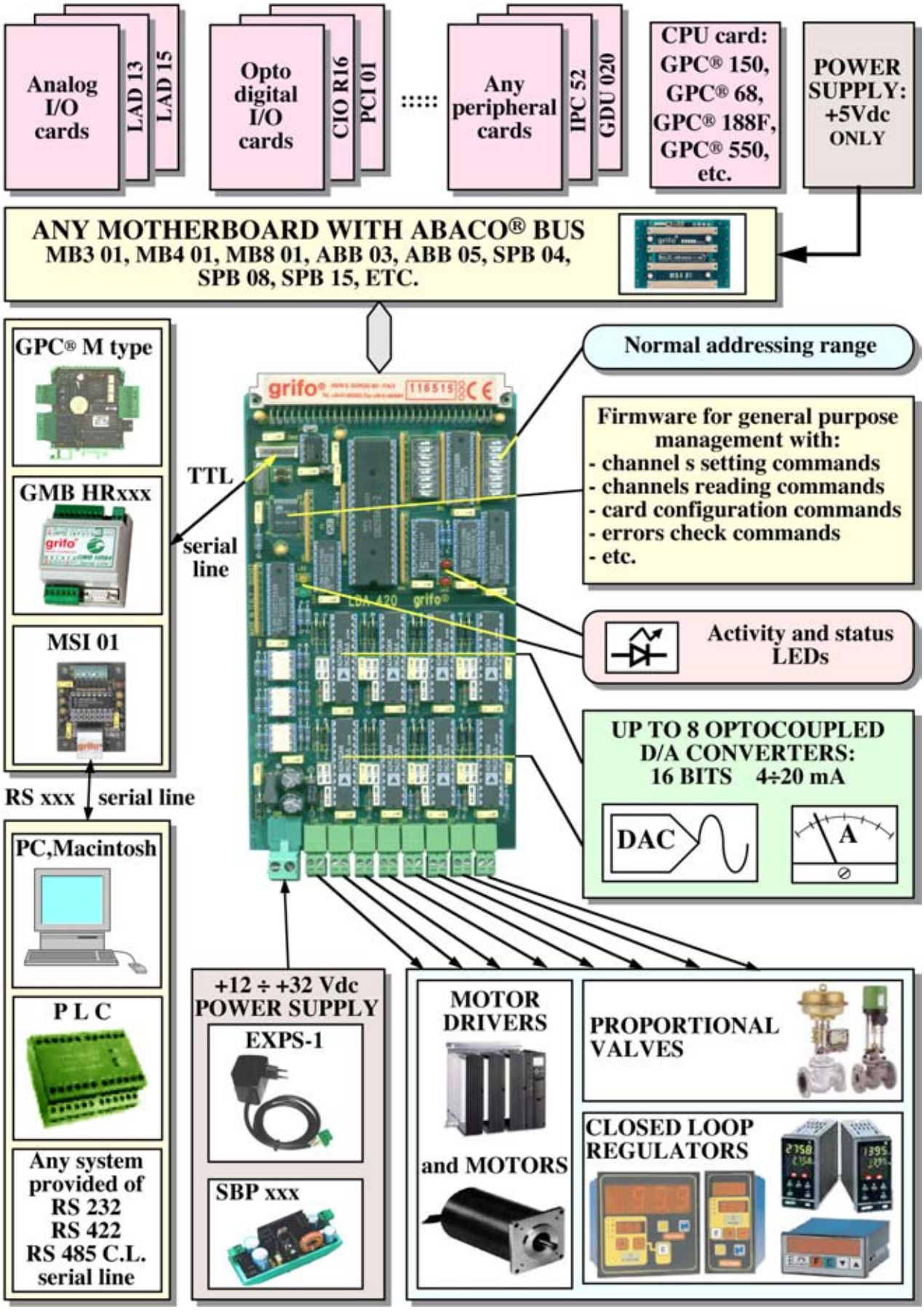

FIGURE 20: POSSIBLE CONNECTIONS DIAGRAM

BIBLIOGRAPHY

In this chapter there is a complete list of technical books, where the user can find all the necessary documentations on the components mounted on **LDA 420.**

Data Sheet ANALOG DEVICE:	*AD420 - Serial input 16 bit 4mA-20 mA DAC*
Data Sheet ATMEL:	*89C51AC2 Enhanced 8 bit MCU*
Manual NEC:	*Microprocessors and Peripherals - Volume 3*
Manual PHILIPS:	*80C51 - Based 8-Bit Microcontrollers*
Manual TEXAS INSTRUMENTES:	*The TTL Data Book - SN54/74 Families*
Manual TEXAS INSTRUMENTES:	*Linear Circuits - Voltage regulators/Supervisors*
Manual TOSHIBA:	*Photo couplers Data Book*

Please connect to the manifactures Web sites to get the latest version of all manuals and data sheets.

APPENDIX A: COMMANDS LIST

To make the search for the commands of **LDA 420** faster, here follows a table that summarizes them, including required and returned parameters.
Please refer to specific paragraphs of this manual for further information.

CODE	N° PARAMETERS REQUIRED	N° PARAMETERS RETURNED	COMMAND PURPOSE
16	1	2	Acquisition of current combination of an analog channel.
17	3	0	Setting of current combination of an analog channel.
18	0	0	Set all analog outputs to beginning of scale.
19	0	1	Acquisition of configuration dip switch status.
20	2	0	Set activity LED status.
21	0	1	Overall status acquisition.
22	0	1	Acquisition of identification name.
23	1	0	Setting of identification name.
24	0	1	Acquisition of analog channels presence.
25	0	1	Acquisition of firmware version.

FIGURE A-1: COMMANDS SUMMARIZING TABLE

APPENDIX B: ALPHABETICAL INDEX

P

R

S

T

V

W