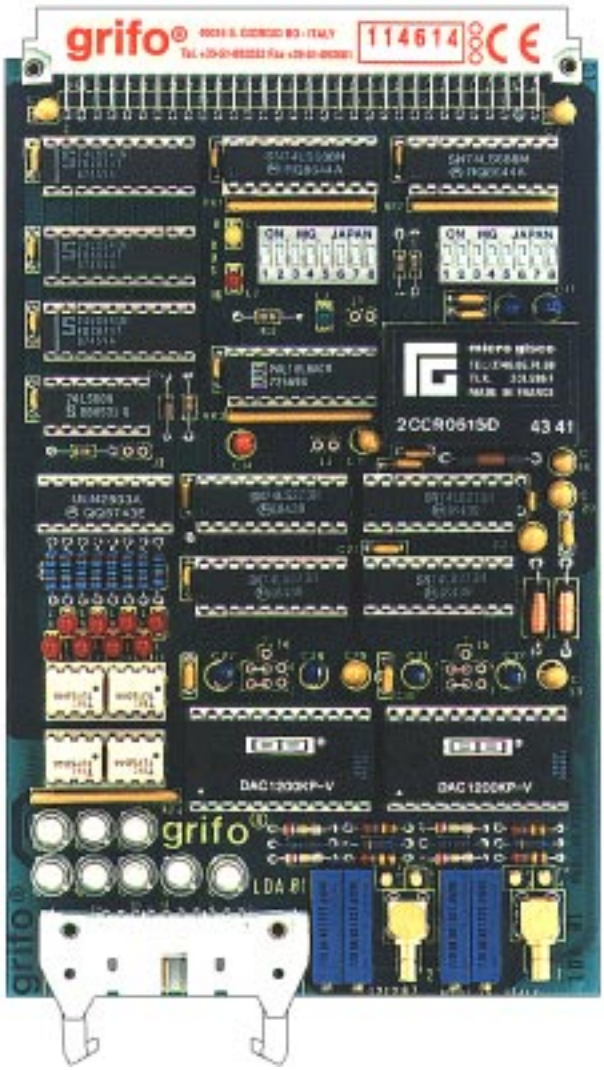
LDA 01

Low cost Digital to Analog converter

TECHNICAL MANUAL



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LDA 01 Edition 5.00 *Rel. 19 February 2001*

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Euroformat size 100x160 mm; direct interface to **ABACO**® Industrial BUS; 2 separated sections of D/A Converter with resolution 12 Bits based on as many DAC80P; output voltage selectable amongst: 0÷+5 Vdc; 0÷+10 Vdc; ±5 Vdc; ±10 Vdc; ±2.5 Vdc; on board DC/DC converter to generate the voltages needed by analog sections; 8 digital output signals, optocoupled, with open collector NPN transistor capable to bear 500 mA at 30 Vdc whithout heat sink; visualization through LEDs of the 8 digital output signals status; anti activation during power on circuit for the output signals; 2 on board dip switches to set the I/O mapping of the card; addressing space as low as 4 contiguous bytes; capable to manage addresses and data BUS 8 or 16 bits wide, selectable by jumper; 3 LEDs to visualize BUS interface configuration; possibility to connect or not to connect the /RESET signal coming from BUS; 2 sub-miniature gold plated UHF connectors for analog voltages output; 20 pins low profile 90° output connector with strain relief clamp; direct interfacement to field modules FBC type; unique power supply +5 Vdc.

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For specific informations on the components mounted on the card, please refer to the Data Book of the builder or second sources.

SYMBOLS DESCRIPTION

In the manual could appear the following symbols:

Attention: Generic danger

Attention: High voltage

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GENERAL INDEX

FIGURES INDEX

INTRODUCTION

The use of these devices has turned - IN EXCLUSIVE WAY - to specialized personnel.

The purpose of this handbook is to give the necessary information to the cognizant and sure use of the products. They are the result of a continual and systematic elaboration of data and technical tests saved and validated from the manufacturer, related to the inside modes of certainty and quality of the information.

The reported data are destined- IN EXCLUSIVE WAY- to specialized users, that can interact with the devices in safety conditions for the persons, for the machine and for the enviroment, impersonating an elementary diagnostic of breakdowns and of malfunction conditions by performing simple functional verify operations , in the height respect of the actual safety and health norms.

The informations for the installation, the assemblage, the dismantlement, the handling, the adjustment, the reparation and the contingent accessories, devices etc. installation are destined - and then executable - always and in exclusive way from specialized warned and educated personnel, or directly from the TECHNICAL AUTHORIZED ASSISTANCE, in the height respect of the manufacturer recommendations and the actual safety and health norms.

The devices can't be used outside a box. The user must always insert the cards in a container that rispect the actual safety normative. The protection of this container is not threshold to the only atmospheric agents, but specially to mechanic, electric, magnetic, etc. ones.

To be on good terms with the products, is necessary guarantee legibility and conservation of the manual, also for future references. In case of deterioration or more easily for technical updates, consult the AUTHORIZED TECHNICAL ASSISTANCE directly.

To prevent problems during card utilization, it is a good practice to read carefully all the informations of this manual. After this reading, the user can use the general index and the alphabetical index, respectly at the begining and at the end of the manual, to find information in a faster and more easy way.

CARD VERSION

The present handbook is reported to the **LDA 01** card release **141197** and later. The validity of the bring informations is subordinate to the number of the card release. The user must always verify the correct correspondence among the two denotations. On the card the release number is present in more points both board printed diagram (serigraph) and printed circuit (for example near connector CN1 on the component side).

GENERAL INFORMATION

LDA 01 (**L**ow cost **D**igital to **A**nalog converter) card is a powerful Eurocard format card, provided with **ABACO®** industrial BUS interface. This card belongs to the analog peripherals units list and, in specific, its purpose is to provide two Digital-Analog conversion lines with **12 bits** of resolution. The analog signal is avalilable on two robust gold plated UHF sub-miniature connectors that assure a strong mechanical connections and a very low contact resistance. Two indipendent D/A Converter circuitries, based on as many **DAC80P**, warrant a complete separation of the signals.
Analog circuitry is capable to generate the signals amongst a wide range of possible choices. The output signal definition range is assured by two separated groups of jumpers, that allow to select amongst the five different output values: 0÷5 Vdc; 0÷10 Vdc; ±2,5 Vdc; ±5 Vdc; ±10 Vdc.
A DC/DC converter is charged to generate all the voltages essential for the correct working from the unique power supply of +5 Vdc.
In addition to the two analog lines, also eight NPN Open-Collector galvanically isolated digital outputs are available. The 20 pins output connector is **ABACO®** standard compliant, this allows an immediate interfacing to several modules for the field, like FBC xxx, that untangle the signals from the flat cable to comfortable quick release screw terminal connectors. These eight auxiliary digital outputs allow to drive directly small external loads or to activate the secondary commands of motor controls without any need to add other cards or electronic interfaces.
LDA 01 card can be driven through any CPU board in the **ABACO®** listing and takes as low as 4 contiguous bytes in the addressing space.
No software initialization is required to starts using the board. When a **Power On** occours or after a **Reset** the **LDA 01** card deactivates the outputs (if not disabled through a specific jumper), to prevent any kind of uncertainty about their initial status.
A remarkable feature of **LDA 01** is the capability to use 8 or 16 bits wide bus data path and 8 or 16 bits wide bus address path. Comfortable jumpers allow to select between Byte or Word modality and the addressing range, these information are visualized through specific LEDs.
Overall features of **LDA 01** are as follows:

- Euroformat size 100x160 mm
- Direct interface to **ABACO®** Industrial BUS
- 2 separated sections of D/A Converter with resolution 12 Bits based on as many **DAC80P**
- Output voltage selectable amongst: 0÷+5 Vdc; 0÷+10 Vdc; ±5 Vdc; ±10 Vdc; ±2.5 Vdc; on board DC/DC converter to generate the voltages needed by analog sections
- 8 digital output signals, optocoupled, with open collector NPN transistor capable to bear 500 mA at 30 Vdc whithout heat sink
- Visualization through LEDs of the 8 digital output signals status
- Anti activation during power on circuit for the output signals
- 2 on board dip switches to set the I/O mapping of the card; addressing space as low as 4 contiguous bytes
- Capable to manage addresses and data BUS 8 or 16 bits wide, selectable by jumper
- 3 LEDs to visualize BUS interface configuration; possibility to connect or not to connect the /RESET signal coming from BUS
- 2 sub-miniature gold plated UHF connectors for analog voltages output
- 20 pins low profile 90° output connector with strain relief clamp
- Direct interfacement to field modules FBC type; unique power supply +5 Vdc

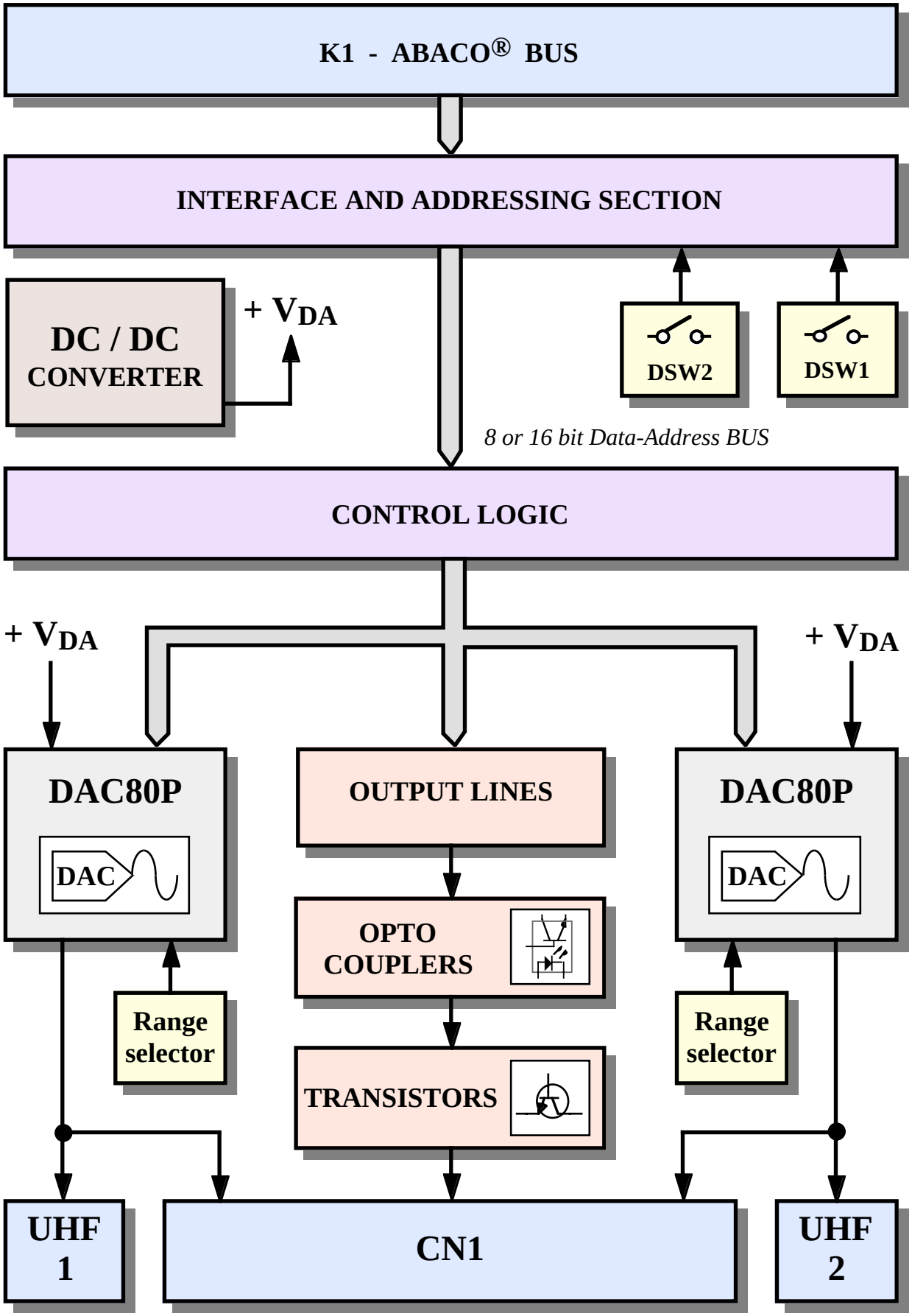

FIGURE 1: BLOCK DIAGRAM

Here follows a description of **LDA 01** board's functional blocks, with an indication of the operations performed by each one. To easily locate these blocks and verify their connections pleare refer to figure 1.

INTERFACING AND ADDRESSING SECTION

This section manages the data exchange between contol logic and command board through **ABACO®** BUS. In particular, all written or read data transit across this section that, in addition, provides the board I/O management, by setting the dip switched **DSW1** and **DSW2**. Please remark that this section can be configured to make **LDA 01** addressable in a phisycal space of 256 or 64 Kbytes.
ABACO® industrial BUS supports both 8 bits and 16 bits addressing mode.
For further informations please refer to the chapter dedicated to board's software description.

CONTROL LOGIC

This section generates all the chip select signals needed to acces the several peripherals on **LDA 01** boards. Using this section the programmer can interact to the board's several sections, verifing their status, reading digital input configurations, setting output signals, etc.
All this can be done through a simple software management based on **ABACO®** BUS, to which the contol logic connects through the interfacing and addressing section. For further informations please refer to the chapter dedicated to board's software description.

OUTPUT SECTION

This section features 8 Output signals driven by latches. These components are managed through specific write registers, according to the information contained in the chapters dedicated to board's hardware and software description. Any Output signal, optocoupled and visualized through its own LED, controls a 500 mA (not continuative), 30 Vdc open collector NPN transistor. The power supply is +5 Vdc, which supplies the on board logic circuits. This solution allows to have an unique stabilized voltage to supply the whole system.

D/A CONVERTER

This section features two indipendent D/A Converter signals, based on as many **DAC80P**, warranting a complete separation of the lines. Analog circuitry is capable to generate the signals amongst a wide range of possible choices. The output signal definition range is assured by two separated groups of 7 pins jumpers, that allow to select amongst the five different output values: 0÷5 Vdc; 0÷10 Vdc; ±2.5 Vdc; ±5 Vdc; ±10 Vdc.
The peripheral is software programmed and takes as low as 4 contiguous bytes in the addressing space.
The two analog voltage outputs are avalilable both on the low profile 20 pins connectora and on two robust gold plated UHF sub-miniature connectors that assure a strong mechanical connections and a very low contact resistance.

DC/DC CONVERTER

A positive booster installed on **LDA 01** board is charged to provide the voltages needed by the digital to analog conversion section. Such DC/DC converter generates two ±15 Vdc voltages starting from the unique +5 Vdc power supply and needs no software management.

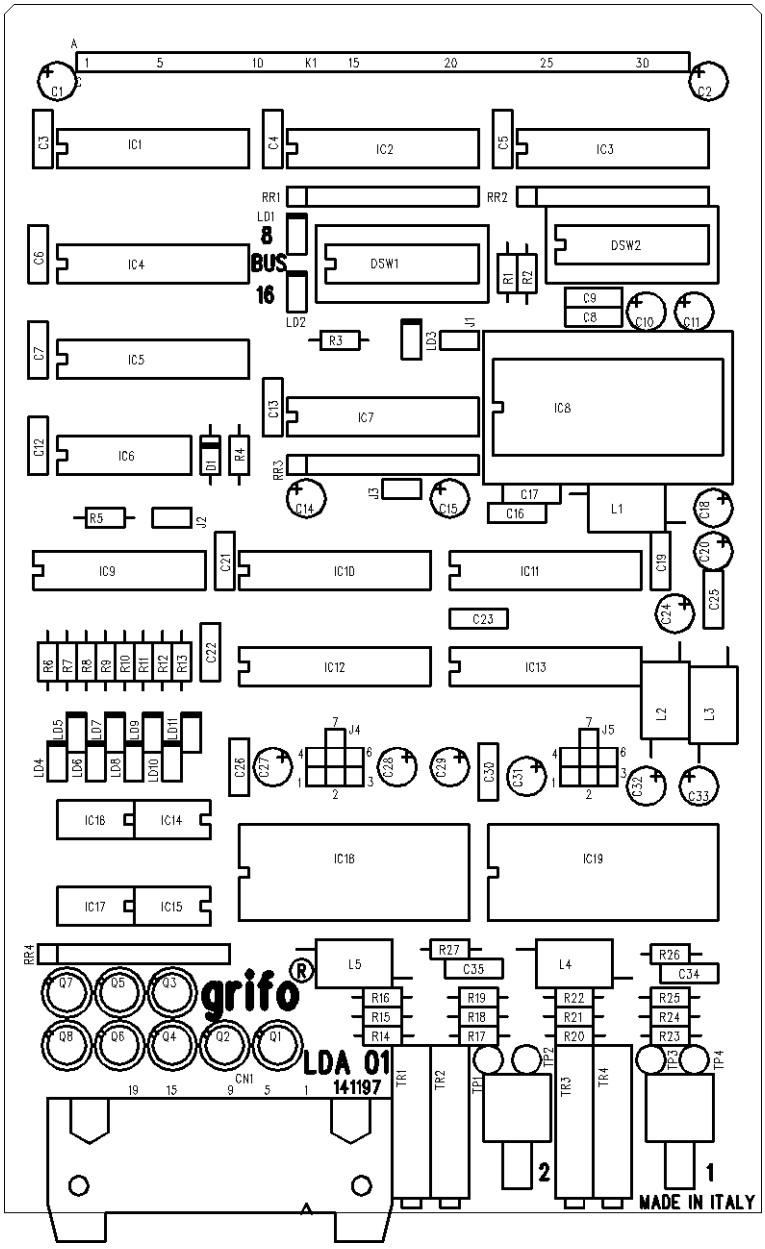

FIGURE 2: COMPONENTS MAP

TECHNICAL FEATURES

GENERAL FEATURES

On board resources:	2 twelve bits D/A converter (2 analog outputs) 8 Outputs NPN transistors open collector 2 eight pins Dip-switches to set I/O address
BUS type:	Industrial **ABACO®** Manageable 8 or 16 bits.
Addressing space:	Selectable between 256 bytes and 64 Kbytes
Byte / word taken:	4 / 2
On board peripherals:	DAC80P

ELECTRIC FEATURES

Power supply:	+5 Vdc ± 5%	
Current consumption:	485 mA	
D/A reference voltage:	6.30 Vdc generated on board	
D/A voltage outputs range:	Each single channel can select amongst 0÷5 Vdc; 0÷10 Vdc; ±2,5 Vdc; ±5 Vdc and ±10 Vdc	
D/A maximum output current:	±5 mA	
Transistor maximum current:	500 mA	(*)
Transistor maximum voltage:	30 Vdc	(*)
Transistor maximum power:	500 mW	(*)

(*) Values referred to a working temperature of 20 °C

PHYSICAL FEATURES

Size:	Standard EUROCARD format 100x160 mm
Weight:	167 g
Connectors:	K1: DIN 41612 64 pins M 90° A+C type C CN1: Low profile 20 pins M 90° strain clamp relief UHF 1: UHF sub miniature M 90° (SMB serie) UHF 2: UHF sub miniature M 90° (SMB serie)
Temperature range:	from 0 to 70° C
Relative humidity:	20% up to 90% (without condensing)

INSTALLATION

In this chapter there are the information for a right installation and correct use of **LDA 01** card.
The User can find the location and functions of each connectors, jumpers, LEDs and some explanatory diagrams.

CONNECTIONS

The **LDA 01** card has 4 connectors that can be linkeded to other devices or directly to the field, according to system requirements. In this paragraph there are connectors pin outs, a short signals description (including the signals direction) and connectors location (please see figure 6), plus some figures that describe how the interface signals are connected on the card.

UHF 1 - D/A ANALOG OUTPUT 1 CONNECTOR

The D/A 1 analog output connector is called UHF 1, it is a coaxial UHF sub miniature gold plated male 90° connector, belonging to **SMB** serie. This kind of connector, matched to its female part, assures a strong mechanical connections and a very low contact resistance.
The connector features D/A 1 analog output and its ground, which acts also as shielding.

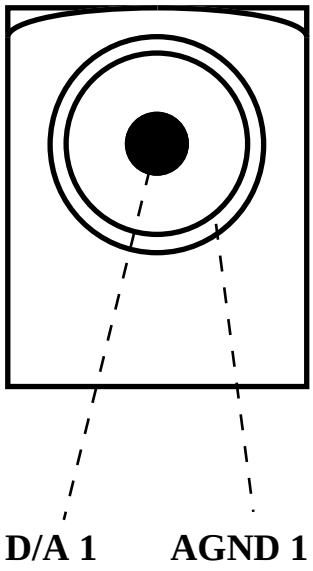

FIGURE 3: UHF 1 - D/A ANALOG OUTPUT 1 CONNECTOR

Signals description:

D/A 1 = O - Section 1 digital to analog converter output signal.
AGND 1 = - Ground and shileding of section 1 analog output signal.

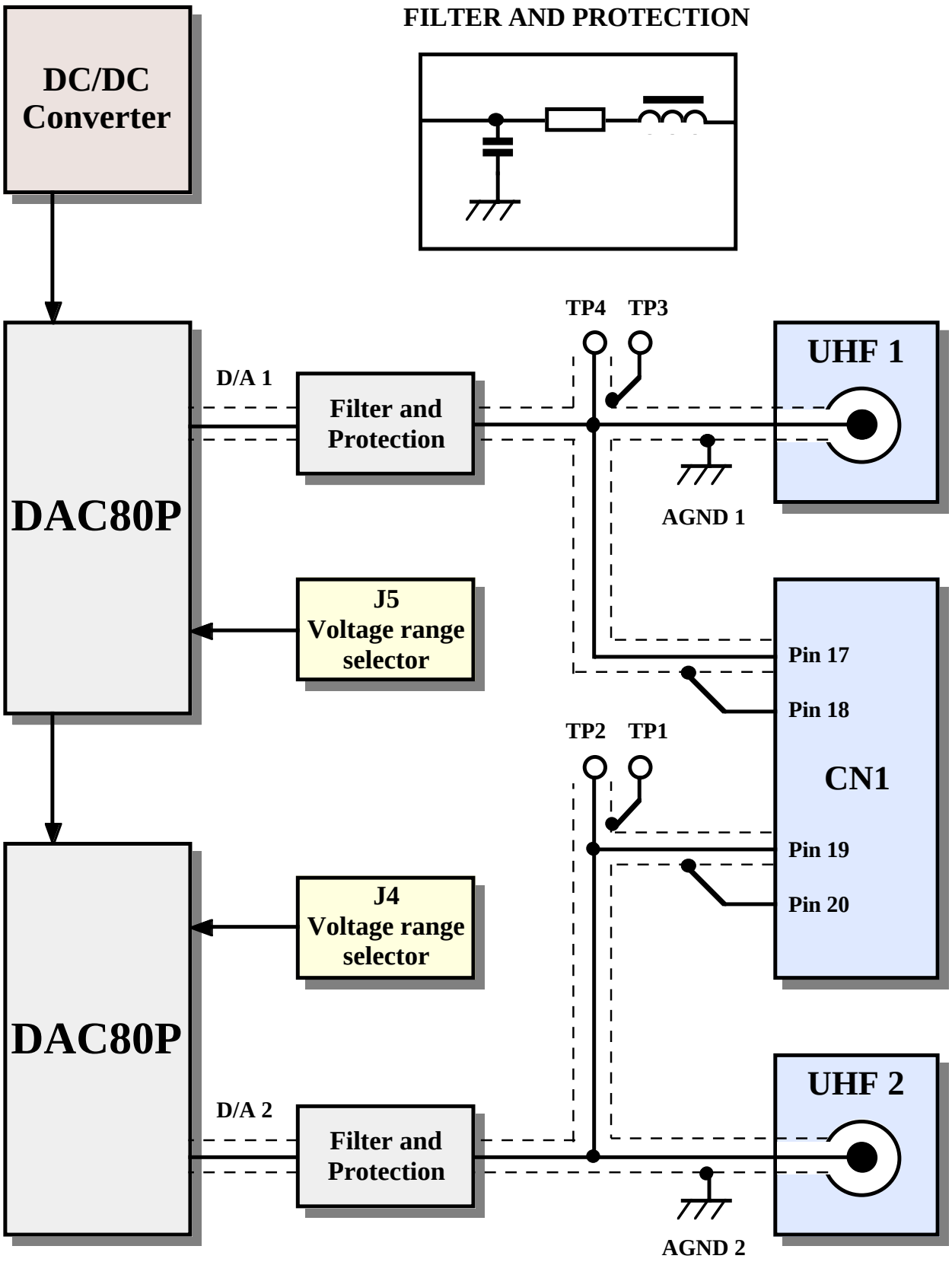

FIGURE 4: DIGITAL TO ANALOG CONVERSION SECTION BLOCK DIAGRAM

UHF 2 - D/A ANALOG OUTPUT 2 CONNECTOR

The D/A 2 analog output connector is called UHF 2, it is a coaxial UHF sub-miniature gold plated male 90° connector, belonging to **SMB** serie.
This kind of connector, matched to its female part, assures a strong mechanical connections and a very low contact resistance.
The connector features D/A 2 analog output and its ground, which acts also as shielding.

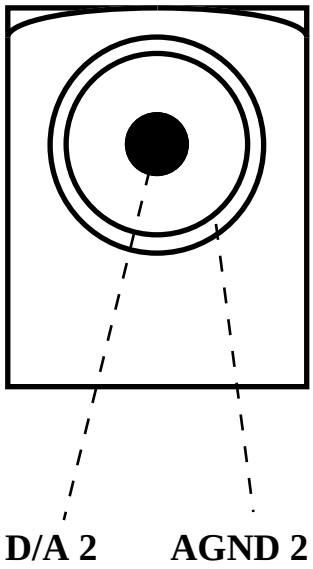

FIGURE 5: UHF 2 - D/A ANALOG OUTPUT 2 CONNECTOR

Signals description:

D/A 2 = O - Section 2 digital to analog converter output signal.
AGND 2 = - Ground and shileding of section 2 analog output signal.

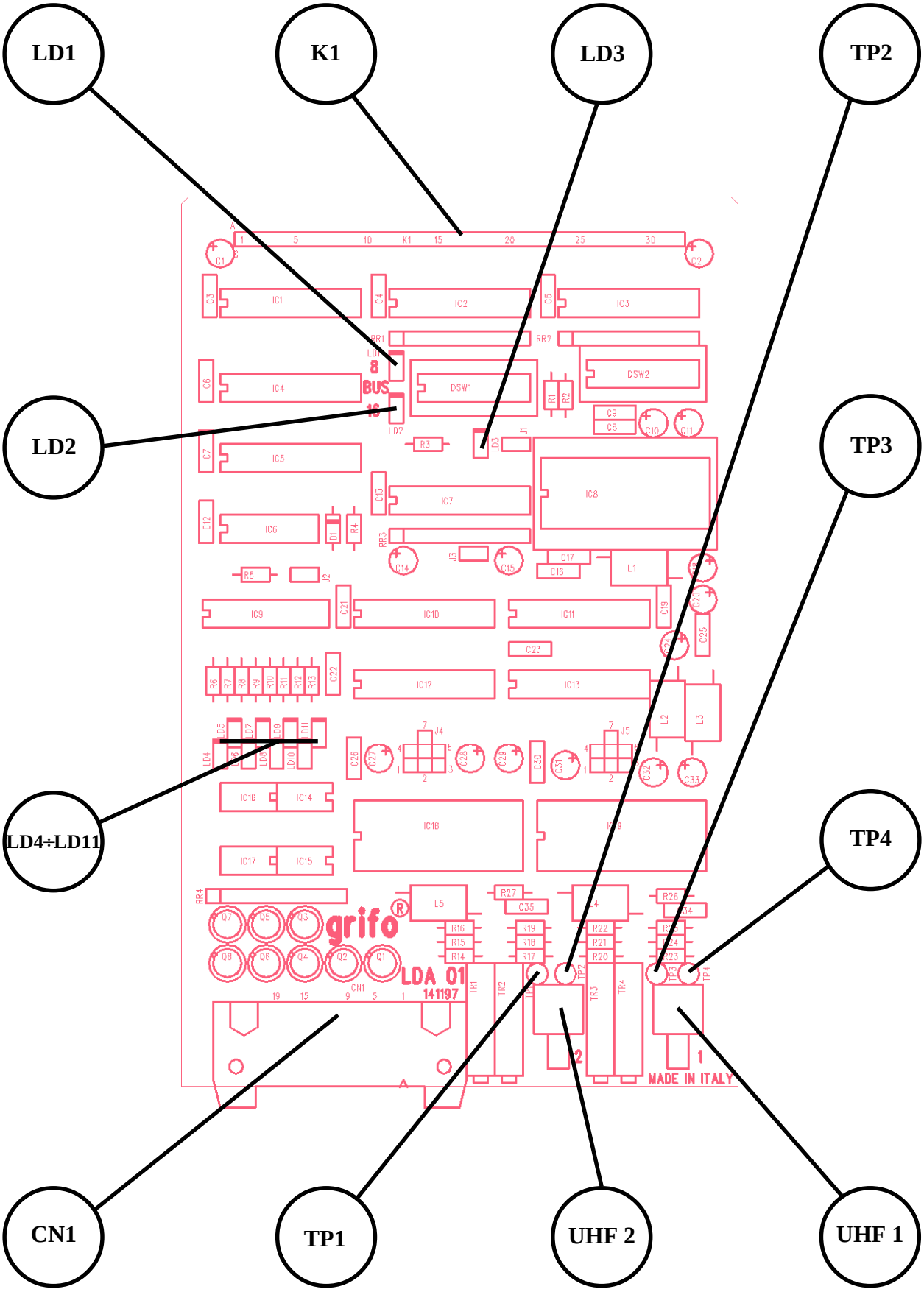

FIGURE 6: CONNECTORS, TEST POINTS, LEDS LOCATION

CN1 - TRANSISTOR AND ANALOG OUTPUTS CONNECTOR

The connector for NPN transistor outputs, called CN1,is a low profile, 2.54 mm pitch, 90 °, 20 pins connector with strain clamp relief.
Open collector contacts of each output transistor and their common (emitter) terminal are present; please remark that the maximun current for each transistor is 500 mA non continuative, maximum voltage is +30 Vdc.
In addition CN1 features also the two digital to analog converters outputs D/A 1 and D/A 2 and their ground/shield lines, as can be seen in figure 4.
This allows to fetch all the **LDA 01** output signals simply through an unique 20 pins flat cable, however the quality of analog signal connection is worse than the quality obtainable using the on board UHF connectors **UHF 1** and **UHF 2**.

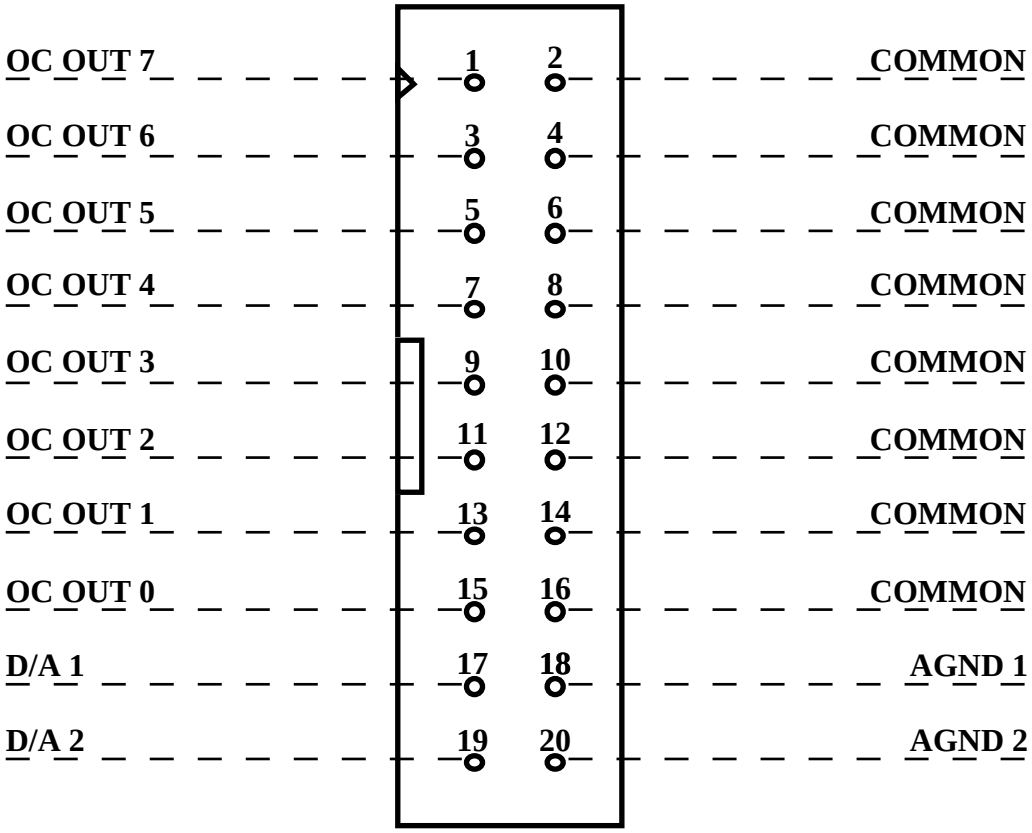

FIGURE 7: CN2 - TRANSISTOR OUTPUTS CONNECTOR

Signals descritpion:

OC OUT n = O - Contact of n-th open collector transistor output.
COMMON = - Common contact of the 8 transistors.
D/A n = O - n-th digital to analog converter output signal.
AGND n = - Ground and shileding of n-th analog output signal.

Each transistor output signals available on **LDA 01** is provided with a LED for visual feed back (the LED will light whenever the transistor is conducting); in addition it is optocoupled, to warrant galvanic separation between internal electronics and external world.
The final stage othe outputs is made by **NPN** open collector transistor, capable to bear a maximum current of **500 mA non continuative** or a tension that can be as high as **+30 Vdc**.
Please remark that this component, being without heat sink, the working temperature must be 20 centigrad degreeses.
The interface circuitry for this 8 transistors output section is shown in the following diagram.

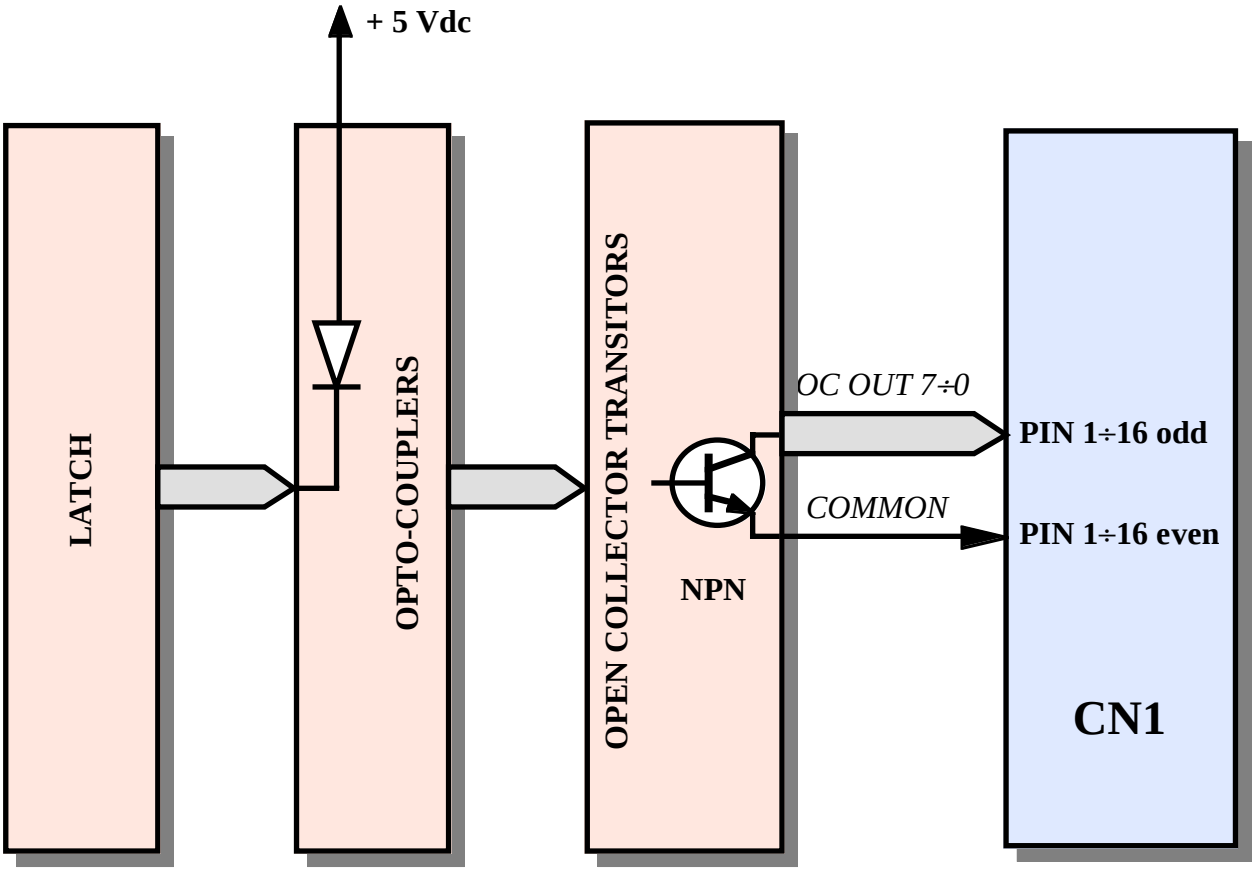

FIGURE 8: TRANSISTOR OUTPUTS BLOCK DIAGRAM

K1 - CONNECTOR FOR ABACO® BUS

The connector for **ABACO® industrial BUS**, called K1 on the board,is a DIN 41612, male, a 90 °, type C, A+C.
Here follows the pin-out of the connector installed on **LDA 01**, in addition there is the standard 8 bits and 16 bits**ABACO®** BUS pin-out.
Please remark that all the signals here described are TTL, except for the power supplies.

A 16 bit BUS	A 8 bit BUS	A LDA 01	PIN	C LDA 01	C 8 bit BUS	C 16 bit BUS
GND	GND	GND	1	GND	GND	GND
+5 Vdc	+5 Vdc	+5 Vdc	2	+5 Vdc	+5 Vdc	+5 Vdc
D0	D0	D0	3	D8		D8
D1	D1	D1	4	D9		D9
D2	D2	D2	5	D10		D10
D3	D3	D3	6	N.C.	/INT	/INT
D4	D4	D4	7	N.C.	/NMI	/NMI
D5	D5	D5	8	D11	/HALT	D11
D6	D6	D6	9	N.C.	/MREQ	/MREQ
D7	D7	D7	10	/IORQ	/IORQ	/IORQ
A0	A0	A0	11	N.C.	/RD	/RDLDS
A1	A1	A1	12	/WR	/WR	/WRLDS
A2	A2	A2	13	D12	/BUSAK	D12
A3	A3	A3	14	N.C.	/WAIT	/WAIT
A4	A4	A4	15	D13	/BUSRQ	D13
A5	A5	A5	16	/RESET	/RESET	/RESET
A6	A6	A6	17	/M1	/M1	/IACK
A7	A7	A7	18	D14	/RFSH	D14
A8	A8	A8	19	N.C.	/MEMDIS	/MEMDIS
A9	A9	A9	20	N.C.	VDUSEL	A22
A10	A10	A10	21	D15	/IEI	D15
A11	A11	A11	22	N.C.		
A12	A12	A12	23	N.C.	CLK	CLK
A13	A13	A13	24	N.C.		/RDUDS
A14	A14	A14	25	/WRUDS		/WRUDS
A15	A15	A15	26	N.C.		A21
A16		N.C.	27	N.C.		A20
A17		N.C.	28	N.C.		A19
A18		N.C.	29	N.C.	/R.T.	/R.T.
+12 Vdc	+12 Vdc	N.C.	30	N.C.	-12 Vdc	-12 Vdc
+5 Vdc	+5 Vdc	+5 Vdc	31	+5 Vdc	+5 Vdc	+5 Vdc
GND	GND	GND	32	GND	GND	GND

FIGURE 9: K1 - CONNECTOR FOR ABACO® BUS

Signals description:

8 bits CPU

A0-A15	=	O	- Address BUS
D0-D7	=	I/O	- Data BUS
INT	=	I	- Interrupt request
NMI	=	I	- Non Maskable Interrupt
HALT	=	O	- Halt state
MREQ	=	O	- Memory Request
IORQ	=	O	- Input Output Request
RD	=	O	- Read cycle status
WR	=	O	- Write cycle status
BUSAK	=	O	- BUS Acknowledge
WAIT	=	I	- Wait
BUSRQ	=	I	- BUS Request
RESET	=	O	- Reset
M1	=	O	- Machine cycle one
RFSH	=	O	- Refresh for dynamic RAM
MEMDIS	=	I	- Memory Display
VDUSEL	=	O	- VDU Selection
IEI	=	I	- Interrupt Enable Input
CLK	=	O	- System clock
R.B.	=	I	- Reset button
+5 Vdc	=	I	- Power supply at +5 Vdc
+12 Vdc	=	I	- Power supply at +12 Vdc
-12 Vdc	=	I	- Power supply at -12 Vdc
GND	=		- Ground signal

16 bits CPU

A16-A22	=	O	- Address BUS
D8-D15	=	I/O	- Data BUS
RD UDS	=	O	- Read Upper Data Strobe
WR UDS	=	O	- Write Upper Data Strobe
IACK	=	O	- Interrupt Acknowledge
RD LDS	=	O	- Read Lower Data Strobe
WR LDS	=	O	- Write Lower Data Strobe

NOTE
Directionality indications as above stated are referred to a master (**GPC®**) board and have been kept untouched to avoid ambiguity in case of multi-boards systems.

VISUAL SIGNALATIONS

LDA 01 card is provided with signalation LEDs to show several status informations, as described in the following table:

LED	COLOUR	PURPOSE
LD1	Yellow	If ON, indicates that 8 bits data BUS has been selected.
LD2	Red	If ON, indicates that 16 bits data BUS has been selected.
LD3	Green	If ON, indicates that 64 KBytes extended addressing mode has been selected.
LD4÷LD11	Red	Visualize the status of the eight transistor NPN outputs, rispectively OC OUT 0÷OC OUT 7. When a LED is ON the output is actived (O. C. transistor conducting).

FIGURE 10: VISUAL SIGNALATIONS TABLE

The main purpose of LEDs is to show a visual indication about the card's status, making so easier debug and verify operations. To easily locate these visual signalations please refer to the figure 6.

POWER SUPPLY

LDA 01 is provided with an efficent circuitery that solves in a comfortable and simple way the problem of the board's supply, under any condition of use.
Here follow the voltages nedded:

+5 Vdc: Supplies the on board logic; must be in the range +5 Vdc ± 5% and must be provided through the specific pins of connector K1 (**ABACO®** BUS).

A positive booster installed on **LDA 01** board is charged to provide the voltages needed by the digital to analog conversion section. Such DC/DC converter generates two ±15 Vdc voltages starting from the unique +5 Vdc power supply and needs no software management.

To warrant great immunity to external noise and so a correct working of the board, it is essential that **+5 Vdc** tension is galvanically isolated.

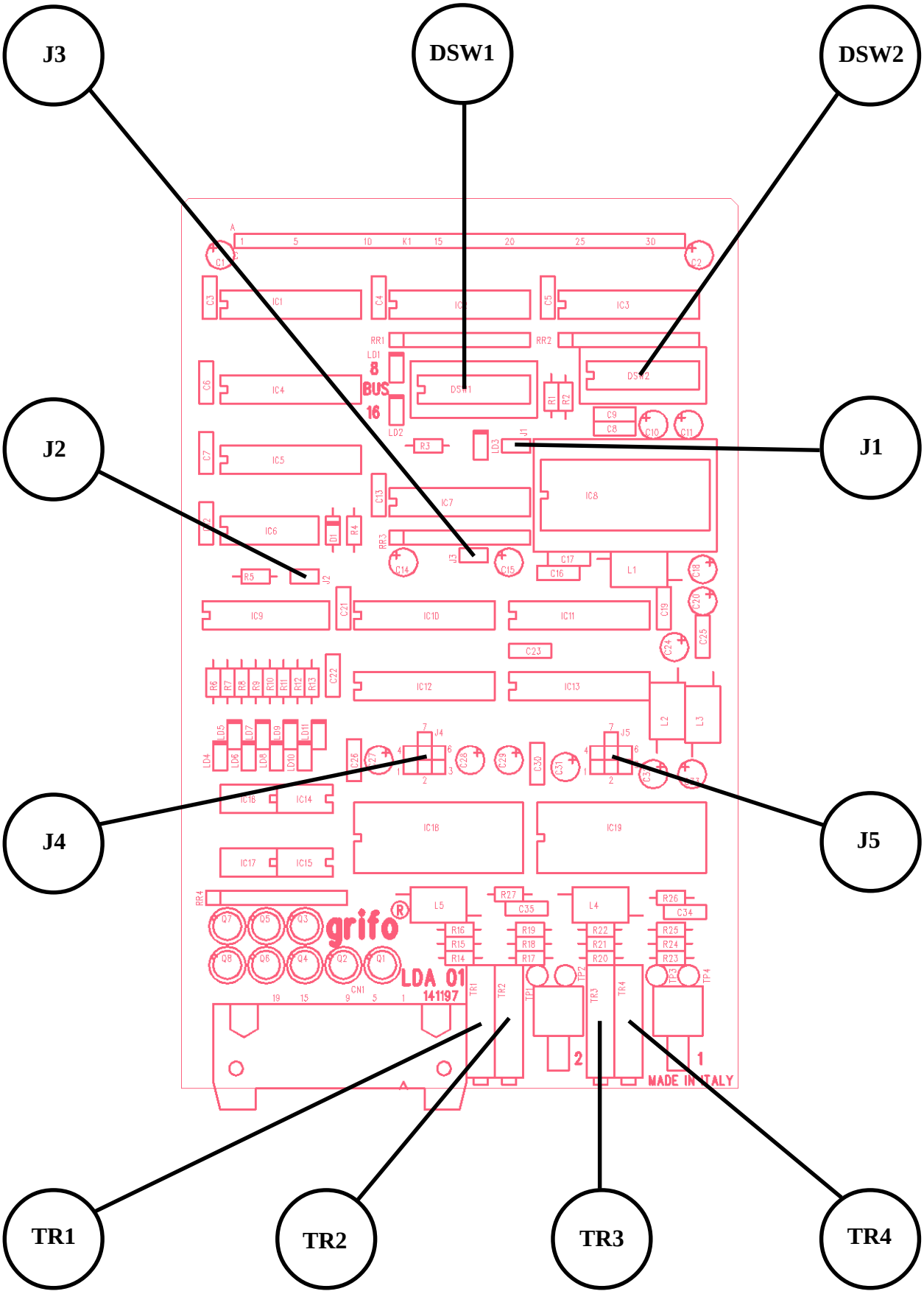

FIGURE 11: DIP SWITCHES, TRIMMERS AND JUMPERS LOCATION

RESET CIRCUITRY CONFIGURATION

As described in the next paragraphs, jumper **J2** allows to select whether to connect or not to connect the /RESET signal coming from **ABACO®** BUS to the **LDA 01** on board circuitery. If the jumper is connected, when the /RESET signal is actived the board outputs will be set to their initial status (transistors disengaged and analog outputs to their maximum value), viceversa if **J2** is not connected such initial status is warranted anyway when a Power On occours, but eventual activations ot the /RESET signal will not affect the outputs status.
This feature is essential when, for example, the outputs status must not change when the intelligent control card activates the reset due to, for example, a watch dog not retriggered.

JUMPERS

On **LDA 01** board there are 6 jumpers for card configuration. Below there is the jumpers list, location and function.

JUMPERS	N. PINS	PURPOSE
J1	2	Selects between normal 256 bytes addressing modality and extended 64 Kbytes addressing modality.
J2	2	Selects the connection of /RESET signal coming from **ABACO®** BUS to the on board devices.
J3	2	Selects the connection of /M1 signal coming from **ABACO®** BUS to the on board devices.
J4	7	Selects the output voltage range of section 2 D/A converter DAC80P (D/A 2).
J5	7	Selects the output voltage range of section 1 D/A converter DAC80P (D/A 1).
DSW1.1	2	Selects between 8 or 16 bits BUS data path width.

FIGURE 12: JUMPERS SUMMARIZING TABLE

The following tables describe all the right connections of **LDA 01** jumpers with their relative functions. To recognize these valid connections, please refer to the board printed diagram (serigraph) or to figure 2 of this manual, where the pins numeration is listed; for recognizing jumpers location, please refer to figure 11.
The "*" used in the following tables, denotes the default connection, or on the other hand the connection set up at the end of testing phase, that is the configuration the User receives.

7 PINS JUMPERS

The two 7 pind jumpers called **J4** and **J5** allow to configure the output voltage range of the digital to analog conversion sections installed on **LDA 01**.
The following figure shows how to connect the jumpers to obtain the desired setting; please remark that the correspondance of jumpers and D/A sections is the following:

J4 -> *Selects the output voltage range of section D/A 2*
J5 -> *Selects the output voltage range of section D/A 1*

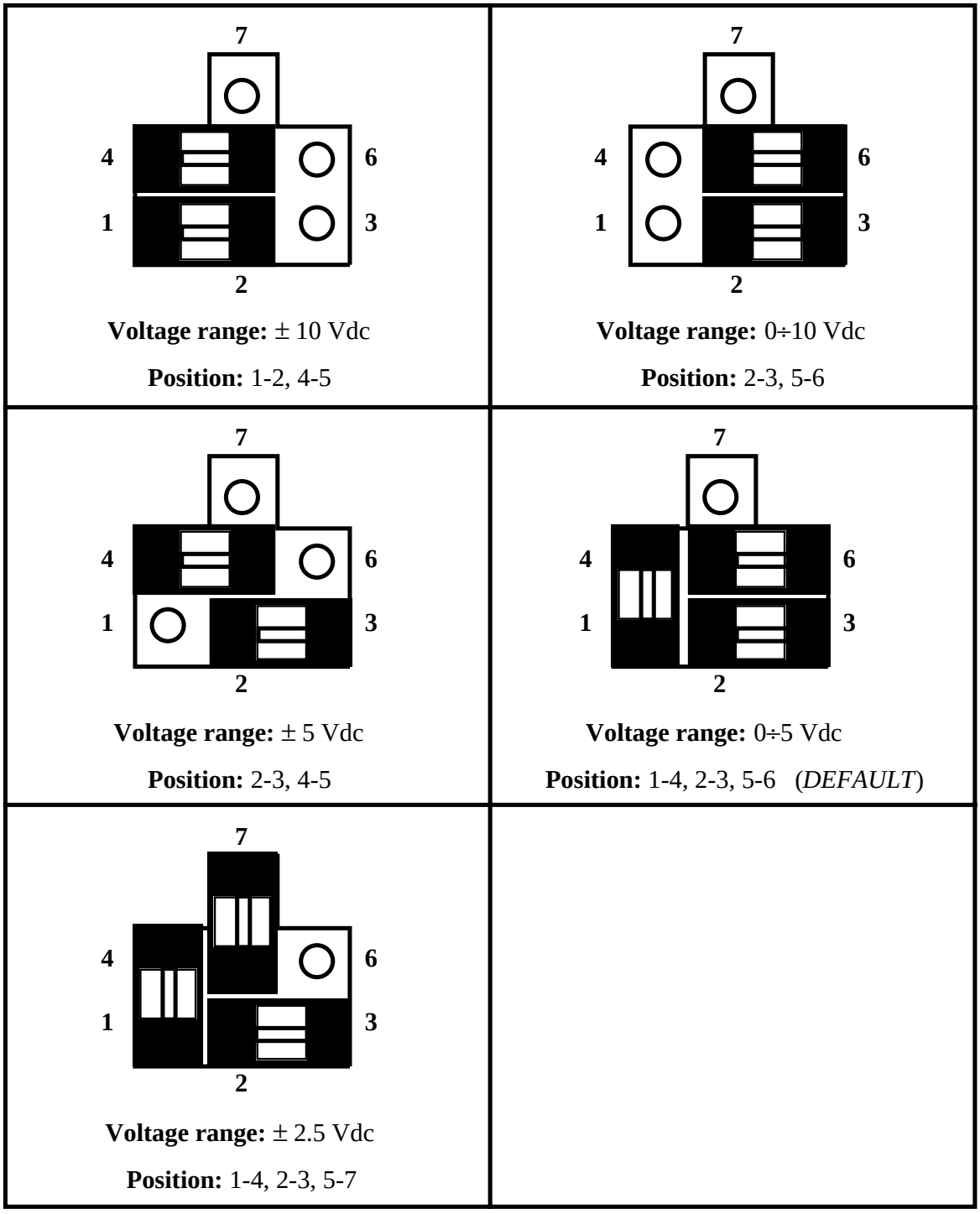

FIGURE 13: 7 PINS JUMPERS CONNECTIONS

2 PINS JUMPERS

JUMPER	CONNECTION	PURPOSE	DEF.
J1	not connected	Selects normal 256 bytes addressing mode.	*
	connected	Selects extended 64 Kbytes addressing mode.	
J2	not connected	It does not connect the /RESET signal, coming from **ABACO** ® BUS, to the specific on board management circuitry.	
	connected	It connects the /RESET signal, coming from **ABACO** ® BUS, to the specific on board management circuitry.	*
J3	not connected	Parallel interface does not manage signal /M1 coming from **ABACO**® BUS.	*
	connected	Parallel interface manages signal /M1 coming from **ABACO**® BUS.	
DSW1.1	OFF	Configures the board to be managed thorugh a 16 bits wide data BUS.	
	ON	Configures the board to be managed thorugh a 8 bits wide data BUS.	*

FIGURE 14: 2 PINS JUMPERS TABLE

TEST POINT

The board is provided with 4 test points called TP?, that allow to read, through a galvanically isolated multimeter, the output voltages of the digital to analog conversion sections. Their purpose is to make possible a monitoring of the analog outputs values during the set up and/or development phases. Correspondance between test points and board signals is:

TP1 -> AGND 2
TP2 -> D/A 2
TP3 -> AGND 1
TP4 -> D/A 1

To easily locate the test points contacts please refer to figure 6, while for further information about the signals they carry please refer to the previous pages that describe the connectors.

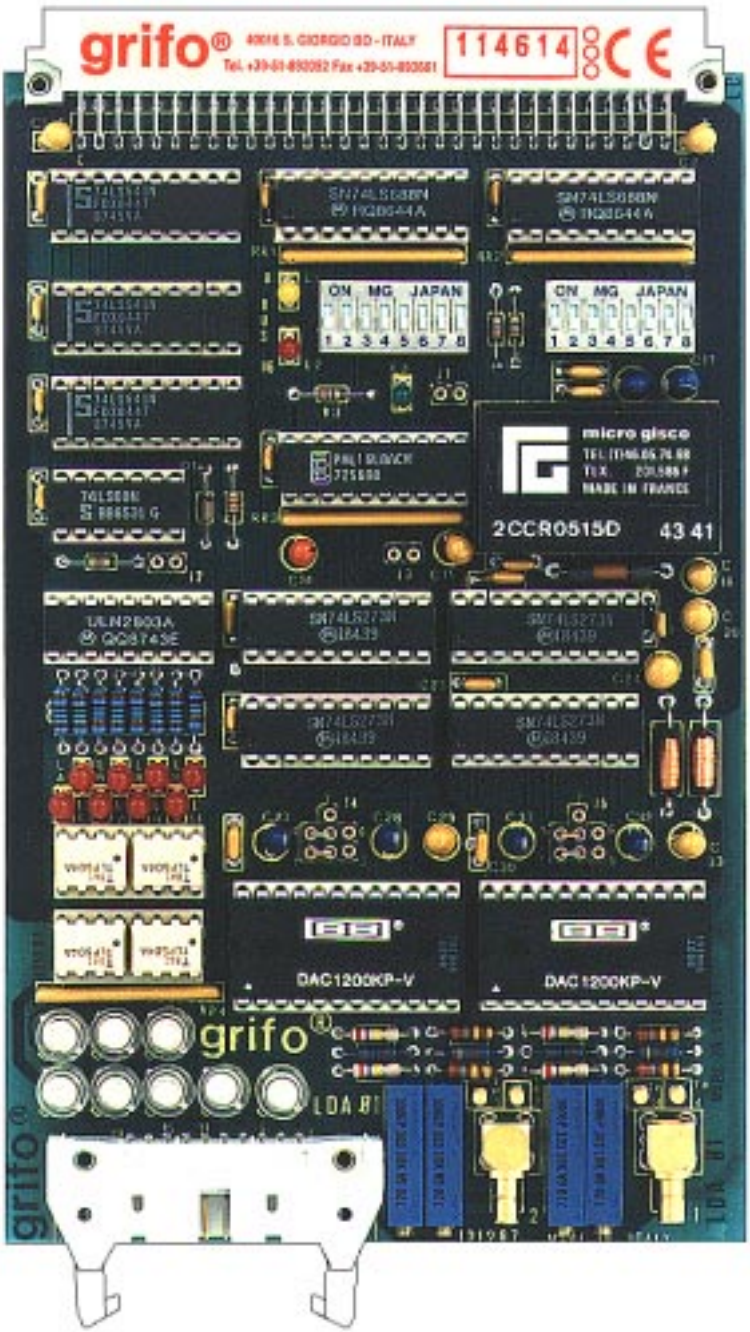

FIGURE 15: CARD PHOTO

TRIMMERS AND CALIBRATION

On **LDA 01** there are four trimmers, called **TR?**, that calibrate the output voltages of the A/D converter sections; in detail they allow to set the maximum and minimum output voltages for each section.
The **LDA 01** is subjected to a careful test that verifies and calibrates all the card sections.
The calibration is executed in laboratory, with a conntrolled +20° C room temperature, following these steps:

- The card is calibrated with analog outputs configured for the range 0÷5 Vdc (default setting).

- The analog output of D/A 1 is programmed for output value of 0 Vdc (all bits set to 1), then trimmer **TR4** is moved to have the voltage 0.000 V on test points **TP3** and **TP4**. The measure is made using a galvanically isolated 5 digits reference multimeter.

- The analog output of D/A 1 is programmed for output value of +5 Vdc (all bits set to 0), then trimmer **TR3** is moved to have the voltage 5.000 V on test points **TP3** and **TP4**.

- Another control of 0 Vdc is performed, eventually correcting the position of **TR4**.

- The analog output of D/A 2 is programmed for output value of 0 Vdc (all bits set to 1), then trimmer **TR2** is moved to have the voltage 0.000 V on test points **TP1** and **TP2**.

- The analog output of D/A 2 is programmed for output value of +5 Vdc (all bits set to 0), then trimmer **TR1** is moved to have the voltage 5.000 V on test points **TP1** and **TP2**.

- Another control of 0 Vdc is performed, eventually correcting the position of **TR2**.

- The trimmers are blocked with paint.

The analog interfaces use high precision components that are selected during mounting phase to avoid complicate and long calibration procedures. After the calibration, the on board trimmers are blocked with paint to mantain calibration also in presence of mechanic stresses (vibrations, movings, delivery, etc.).
The user must not modify the card calibration, but if thermic drifts,time drifts and so on, make necessary a new calibration, the user must strictly follow the previously described procedure.
To easily locate the above mentioned components please refer to figures 2, 6 and 11; for further information about test points please refer to the previous paragraph; for further information about how to set the D/A converters output voltages please refer to chapter “SOFTWARE DESCRIPTION”.

BOARD CONNNECTIONS

To prevent possible connecting problems between **LDA 01** board and the external systems, the user has to read carefully the information of the previous paragraphs and he must follow these instrunctions:

- The NPN transistors output signals must be connected directly to the load to drive (power relays, etc.). The board provides the open collector outputs called OC OUT x, capable to bear a maximum current of **500 mA** with a tension that can be **+30 Vdc**.
  Being without heat sink, they can drive in continuative way a resistive load absorbing a maximum power of **500 mW** at a working temperature of 20 centigrad degreeses.
  There is a COMMON terminal connected to all the eight transistors.

- The analog outputs can erogate a maximum current of ±5 mA; for this reason they must be connected only to external circuits featuring a high impedance, which warrants not to exceed such current limit across the whole output range.
  Eventual connections to power actuators, like power motors, must be made through the specific power driver circuits, like, for exemple, activation or inverter.

- The TTL output signals can be connected directly only to a device featuring the same type of interface. About the correspondance between logic signals and TTL output status, remember that a logic **0** generates a TTL 0 Vdc, while a logic **1** generates a TTL +5 Vdc.

HARDWARE DESCRIPTION

This chapter provides all the hardware informations needed to use **LDA 01** board. Here the User will find informations about I/O card mapping and on board peripheral devices addressing.

BOARD MAPPING

LDA 01 board is mapped into a **4** bytes I/O addressing space (or two words in 16 bits addressing mode), that can be mapped starting from different base addresses according to how the board is configured. This feature allows to use several **LDA 01** cards on the same **ABACO®** BUS, or to install them on a BUS where other peripheral modules are installed obtaining a structure that can be expanded without any difficulty or modifications to the application software.
The base address can be defined through the specific BUS interface circuitry on the board itself; this circuitry uses the 2 eight pins dip switched called **DSW1** and **DSW2**, from which it reads the address set by the user. Here follows the corrispondance between dips configuration and address signals.

DSW1.1	->	*Please see paragraph "2 PINS JUMPERS"*	
DSW1.2	->	*Don't care*	*8 bits BUS data path (**DSW1.1 ON**)*
		Address A1	*16 bits BUS data path (**DSW1.1 OFF**)*
DSW1.3	->	Address A2	
DSW1.4	->	Address A3	
DSW1.5	->	Address A4	
DSW1.6	->	Address A5	
DSW1.7	->	Address A6	
DSW1.8	->	Address A7	
DSW2.1	->	Address A8	
DSW2.2	->	Address A9	
DSW2.3	->	Address A10	
DSW2.4	->	Address A11	
DSW2.5	->	Address A12	
DSW2.6	->	Address A13	
DSW2.7	->	Address A14	
DSW2.8	->	Address A15	

These dips are driven in complemented logic, this means that if a switch is **ON** generates a **logic zero**, viceversa if a switch is **OFF** generates a **logic one**.
Jumper J1, described in the previous chapter, selects the number of bytes addressed amogst which the allocation address can be chosen. If the 256 bytes (from 00H to FFH) normal addressing mode is selected, only DSW1 is significant (switches configuration on DSW2 is indifferent); if the 64Kbytes (from 0000H to FFFFH) extended addresing mode is selected, then both DSW1 and DSW2 must be configured correctly.

Also jumper J3, described in the previous chapter, affectes the addressing logic and must be connected accordind to the type of control card (**GPC**® serie) is used. In detail if the control card is provided with signal /M1 on the **ABACO**® BUS connector, then jumper J3 must be connected and vicecersa.

NOTE
When allocating the mapping address of the boards, plase be careful not to allocate more than one device in the same addressing space (count also the number of bytes occupied by the card). If this condtion will not be respected, a BUS conflict will happen; such conflict will compromise the correct working of the whole system.

As an example, possible mappings are reported here.

1) Address used to map **LDA 01**: 048H with 256 bytes addressing mode.
Control board used: data and addresses bus path are 8 bits wide;
provided with signal /M1.

J1	->	Not connected
J3	->	Connected
DSW1.1	->	ON
DSW1.2	->	Don't care
DSW1.3	->	ON
DSW1.4	->	OFF
DSW1.5	->	ON
DSW1.6	->	ON
DSW1.7	->	OFF
DSW1.8	->	ON
DSW2	->	Don't care

2) Address used to map **LDA 01**: 14F8H with 64Kbytes addressing mode.
Control board used: data bus path is 8 bits wide;
addresses bus path is 16 bits wide;
not provided with signal /M1.

J1	->	Connected
J3	->	Not connected
DSW1.1	->	ON
DSW1.2	->	Don't care
DSW1.3	->	ON
DSW1.4	->	OFF
DSW1.5	->	OFF
DSW1.6	->	OFF
DSW1.7	->	OFF
DSW1.8	->	OFF

DSW2.1 -> ON
DSW2.2 -> ON
DSW2.3 -> OFF
DSW2.4 -> ON
DSW2.5 -> OFF
DSW2.6 -> ON
DSW2.7 -> ON
DSW2.8 -> ON

3) Address used to map **LDA 01**: F680H with 64Kbytes addressing mode.
Control board used: data and addresses bus path are 16 bits wide; not provided with signal /M1.

J1 -> Connected
J3 -> Not connected

DSW1.1 -> OFF
DSW1.2 -> ON
DSW1.3 -> ON
DSW1.4 -> ON
DSW1.5 -> ON
DSW1.6 -> ON
DSW1.7 -> ON
DSW1.8 -> OFF

DSW2.1 -> ON
DSW2.2 -> OFF
DSW2.3 -> OFF
DSW2.4 -> ON
DSW2.5 -> OFF
DSW2.6 -> OFF
DSW2.7 -> OFF
DSW2.8 -> OFF

To easily locate jumpers and dip switches please refer to figures 2 and 11.

INTERNAL REGISTERS ADDRESSING

Indicating the board base address with <**baseaddr**>, that is the address set using Dip Switches DSW1 and DSW2, as indicated in the previous paragraph **LDA 01** internal registers are addressable as explained in the following tables, respectively when addressing mode is 8 bit and 16 bit.

NOTE
If using several boards on the same **ABACO®** BUS, when setting the boards mapping address the user shold be careful not to allocate more than one board in the same addressing space (consider the base address plus the bytes taken by the board addressing). If this condition is not satisfied a BUS conflict situation will occour, prejudicing the correct working of the whole system.

INTERNAL REGISTERS ADDRESSING FOR 8 BIT ADDRESSING MODE

DEVICE	REG.	ADDRESS	R/W	MEANING
DAC80P 2	DA2H	<baseaddr>+00H	W	Register that sets the high byte (bit D11÷D4) of section 2 DAC80P.
	DA2L	<baseaddr>+01H	W	Register that sets the low nibble (bit D3÷D0) of section 2 DAC80P.
DAC80P 1	DA1H	<baseaddr>+02H	W	Register that sets the high byte (bit D11÷D4) of section 1 DAC80P.
	DA1L	<baseaddr>+03H	W	Register that sets the low nibble (bit D3÷D0) of section 1 DAC80P.
OUTPUT	OUTL	<baseaddr>+01H	W	Register that sets the status of 4 transistor outputs OC OUT 0÷OC OUT 3.
	OUTH	<baseaddr>+03H	W	Register that sets the status of 4 transistor outputs OC OUT 4÷OC OUT 7.

FIGURE 16: INTERNAL REGISTERS ADDRESSING TABLE FOR 8 BIT ADDRESSING MODE

INTERNAL REGISTERS ADDRESSING FOR 16 BIT ADDRESSING MODE

DEVICE	REG.	ADDRESS	R/W	MEANING
DAC80P 2	DA2	<baseaddr>+00H	W	Regiser that sets the output voltage value (bit D11÷D0) of section 2 DAC80P.
DAC80P 1	DA1	<baseaddr>+02H	W	Regiser that sets the output voltage value (bit D11÷D0) of section 1 DAC80P.
OUTPUT	OUTL	<baseaddr>+00H	W	Register that sets the status of 4 transistor outputs OC OUT 0÷OC OUT 3.
	OUTH	<baseaddr>+02H	W	Register that sets the status of 4 transistor outputs OC OUT 4÷OC OUT 7.

FIGURE 17: INTERNAL REGISTERS ADDRESSING TABLE FOR 16 BIT ADDRESSING MODE

PERIPHERAL DEVICES SOFTWARE DESCRIPTION

In the previous paragraph allocation addresses of all the peripherals have been reported, here follows a detailed description of function and meaning of internal registers (please always refer to the peripheral mapping tables to understand completely the following informations). Should the present documentaion be inadequate please refer to the component's manufacturer documentation.
In the following paragraphs the indications **D0÷D7** or **D0÷D15** are used to refer the bits of the byte or word involved in the I/O operations.

D/A CONVERTER DAC80P

Management of 12 bits D/A convertes DAC80P is performed through write operations to its specific control registers described in figures 16 and 17.
The meaning of the bits in the write registers is:

8 bits data BUS			*16 bits data BUS*		
DAnH.D7	->	bit D11 of n-th D/A	**DAn.D15**	->	bit D11 of n-th D/A
DAnH.D6	->	bit D10 of n-th D/A	**DAn.D14**	->	bit D10 of n-th D/A
DAnH.D5	->	bit D9 of n-th D/A	**DAn.D13**	->	bit D9 of n-th D/A
DAnH.D4	->	bit D8 of n-th D/A	**DAn.D12**	->	bit D8 of n-th D/A
DAnH.D3	->	bit D7 of n-th D/A	**DAn.D11**	->	bit D7 of n-th D/A
DAnH.D2	->	bit D6 of n-th D/A	**DAn.D10**	->	bit D6 of n-th D/A
DAnH.D1	->	bit D5 of n-th D/A	**DAn.D9**	->	bit D5 of n-th D/A
DAnH.D0	->	bit D4 of n-th D/A	**DAn.D8**	->	bit D4 of n-th D/A
DAnL.D7	->	bit D3 of n-th D/A	**DAn.D7**	->	bit D3 of n-th D/A
DAnL.D6	->	bit D2 of n-th D/A	**DAn.D6**	->	bit D2 of n-th D/A
DAnL.D5	->	bit D1 of n-th D/A	**DAn.D5**	->	bit D1 of n-th D/A
DAnL.D4	->	bit D0 of n-th D/A	**DAn.D4**	->	bit D0 of n-th D/A

The indications DAnH, DAnL and DAn mean the conversion management registers, 8 or 16 bits wide, of digital to analog converters DAC80P called D/A 1 and D/A 2 in the previous pages.

NOTE
Please remark that registers DA2L and DA2 are allocated at hte same I/O address of register OUTL, while registers DA1L and DA1 are allocated at the same I/O address of register OUTH.
For this reason writing to the bits not described above means to change the status of transistor outputs, as stated in the following paragraph; so every operation that involves the registers must also consider the status of such outputs.

The 12 bit data that is written into registers is inversely proportional to the output voltage,according to the relation:

DIGITAL VALUE (Bit D11÷D0)	DAC80P ANALOG OUTPUTS CONFIGURATION				
	0÷5 Vdc	**0÷10 Vdc**	**±2.5 Vdc**	**±5 Vdc**	**±10 Vdc**
4095 = FFF_{HEX}	0 Vdc	0 Vdc	-2.5 Vdc	-5 Vdc	-10 Vdc
2047 = $7FF_{HEX}$	+2.5 Vdc	+5 Vdc	0 Vdc	0 Vdc	0 Vdc
0	+5 Vdc	+10 Vdc	+2.5 Vdc	+5 Vdc	+10 Vdc

FIGURE 18: CORRESPONDANCE BETWEEN DIGITAL VALUE AND ANALOG OUTPUT VALUE

If , for example, the user wants to set the analog output value +6.25 Vdc in section 2 DAC80P, configured for output range 0÷10 Vdc, then he/she must perform the following operations:

- The 12 bit digital value to write into D/A registers is: 1536 (600_{HEX}).
  8 bits data bus
- Write data 96 (60_{HEX}) into register DA2H.
- Write data 0 (00_{HEX}) into register DA2L.
  16 bit data bus
- Write data 24576 (6000_{HEX}) into register DA2.

If , for example, the user wants to set the analog output value -1.25 Vdc in section 1 DAC80P, configured for output range ±10 Vdc, then he/she must perform the following operations:

- The 12 bit digital value to write into D/A registers is: 2303 ($8FF_{HEX}$).
  8 bits data bus
- Write data 143 ($8F_{HEX}$) into register DA1H.
- Write data 240 ($F0_{HEX}$) into register DA2L.
  16 bit data bus
- Write data 36848 ($8FF0_{HEX}$) into register DA2.

Please remark that the above example involve a contemporary disactivation of the transistor outputs (see next paragraph); for such reason to keep unchanged the status of these outputs the registers should be managed opportunely.

NOTE

If jumper J2 is connected, all the registers are reset (all bits to 0) when a power on or a Reset occour; this sets the analog outputs to the **highest positive value**.
All the opportune expedients must be made to avoid damages due to this situation.
One possible solution is to use one of the transistor outputs (normally disactived) to enable the power driver connected to the analog outputs.

TRANSISTOR OUTPUTS

Output registers (called OUTH and OUTL) 8 or 16 bits wide are used to perform the output management on **LDA 01** board. The bits of these registers have the following meaning:

8 or 16 bits data BUS

OUTH.D3	->	OC OUT 4
OUTH.D2	->	OC OUT 5
OUTH.D1	->	OC OUT 6
OUTH.D0	->	OC OUT 7
OUTL.D3	->	OC OUT 0
OUTL.D2	->	OC OUT 1
OUTL.D1	->	OC OUT 2
OUTL.D0	->	OC OUT 3

The indication **OC OUT n** stands for the 8 transistor outputs, whose output signals are available on connector CN1.
Performing an output operation at the address of, OUTL or OUTH the corresponding outputs are set by the output data.
The correspondance between status of an output and value of a bit is:

Bit at logic 0	->	Output disabled	=	Open collector transistor disactived
Bit at logic 1	->	Output enabled	=	Open collector transistor conducting

NOTE
Please remark that registers DA2L and DA2 are allocated at hte same I/O address of register OUTL, while registers DA1L and DA1 are allocated at hte same I/O address of register OUTH.
For this reason writing to the bits not described above means to change the status of analog outputs, as stated in the following paragraph; so every operation that involves the registers must also consider the status of such outputs.

All registers are reset (all bits are 0) when a Reset or a Power On occour if **J2** is connected, this disables all the outputs and disables all the open collector transistor signals.

EXTERNAL CARDS

LDA 01 can be connected to a wide range of block modules and operator interface system produced by **grifo®**, or to many system of other companies.The on board resources can be expanded with a simple connection to the numerous peripheral **grifo®** boards,both intelligent and not, thanks to its standard **ABACO®** BUS connector. Even cards with **ABACO®** I/O BUS can be connected, by using the proper mother boards.
Hereunder some of these cards are briefly described; ask the detailed information directly to **grifo®**, if required.

MB3 01-MB4 01-MB8 01
Mother Board 3, 4, 8 slots
Motherboard featuring 3, 4 or 8 slots of **ABACO®** industrial BUS; pitch 4 TE; standard power supply connectors; LEDs for visual feed-back of power supply; holes for rack docking.

SPB 04-SPB 08
Switch Power BUS 4-8 slots
Motherboard featuring 4-8 slots of **ABACO®** industrial BUS; pitch 4 TE; standard power supply connectors; termination resistances; connector type F for **SPC xxx** supply ; holes for rack docking.

ABB 03
ABACO® Block BUS 3 slots
3 slots **ABACO®** mother board; 4 TE pitch connectors; **ABACO®** I/O BUS connector; screw terminal for power supply; connection for DIN C type and Ω rails.

ABB 05
ABACO® Block BUS 5 slots
5 slots **ABACO®** mother board with power supply. Double power supply built in; 5Vdc 2,5A section for powering the on board logic; second section at 24Vdc 400mA galvanically coupled, for the optocoupled input lines. Auxiliary connector for **ABACO®** I/O BUS. Connection for DIN Ω rails.

SBP 02-xx
Switch BLOCK Power xx version
Low cost switching power supply able to generate voltage from +5 to +40 Vdc and current up to 2.5 A; Input from 12 to 24 Vac; Connection for DIN C Type and Ω rails.

SPC 03.5S
Switch Power Card +5 Vdc
Europe format switching power supply capable to provide +5 Vdc to a load of 4 A; input voltage 12÷24 Vac; power-failure; connector for back-up battery; standard connector for mother board **SPB 0x**.

SPC 512
Switch Power Card +5 Vdc +12 Vdc
Europe format switching power supply capable to provide +5 Vdc 5A and +12 Vdc 2.5 A; input voltage 12÷24 Vac; power-failure; connector for back-up battery; standard connector for mother board **SPB 0x**.

GPC® 51

General Purpose Controller fam. 51

Microprocessor family 51 INTEL including the masked BASIC chip; the board features: 16 I/O TTL lines; dip switch; 3 timer/counter; RS 232; 4 A/D converter signals resolution 11 bit; buzzer; on board EPROM programmer; RTC and 32K SRAM with Lithium battery back up; controlloer for display and keyboard.

GPC® 188F

General Purpose Controller 80C188

80C188 µP 20MHz; 1 RS 232 line; 1 RS 232, RS 422-485 or Current Loop line; 24 TTL I/O lines; 1M EPROM or 512K FLASH; 1M RAM Lithium battery backed; 8K serial EEPROM; RTC; Watch Dog; 8 Dip switch; 3 Timer Counter; 8 13 bit A/D lines; Power failure; activity LEDs; single power supply +5Vdc.

GPC® 15A

General Purpose Controller 84C15

Full CMOS card, 10÷20 MHz 84C15 CPU; 512K EPROM or FLASH; 128K RAM; 8K RAM and RTC backed; 8K serial EEPROM; 1 RS 232 line; 1 RS 232 line or RS 422-485 or Current Loop line; 32 or 40 TTL I/O lines; CTC; Watch dog; 2 Dip switches; Buzzer.

GPC® 150

General Purpose Controller 84C15

Microprocessor Z80 at 16 MHz; implementation completely CMOS; 512K EPROM or FLASH; 512K SRAM; RTC; Back-Up through external Lithium battery; 4M serail FLASH ; 1 serial line RS 232 plus 1 RS 232 or RS 422-485 or current loop; 40 I/O TTL; 2 timer/counter; 2 watch dog; dip switch; EEPROM; A/D converter with resolution 12 bit; activity LED.

GPC® 15R

General Purpose Controller 84C15

84C15 µP, 10÷16 MHz; 1 RS 232 line; 1 RS 232 or RS 422-485 or C. L. line; 16÷24 TTL I/O lines; 16 Opto-in; 8 Relays; 4 Opto Coupled Timers Counters; 512K EPROM or FLASH; 512K RAM and RTC backed; 8K serial EEPROM; 8K Backed RAM modul; Buzzer; 1 Activity LED; Watch dog; 4÷12 readable DIPs; LCD Interface.

GPC® 323

General Purpose Controller 51 family

80C32 µP, 14 MHz; Full CMOS; 1 RS 232 line (software); 1 RS 232 or RS 422-485 or Current Loop line; 24 TTL I/O lines; 11 A/D 12 bits lines; 3 Timers Counters; 64K EPROM; 64K RAM; 32K RAM and RTC backed; 32K DIL EEPROM; 8K serial EEPROM; Buzzer; 2 Activity LED; Watch dog; 5 readable DIPs; LCD Interface.

GPC® 553

General Purpose Controller 80C552

80C552 µP, 22÷33 MHz; 1 RS 232 line (software); 1 RS 232 or RS 422-485 or Current Loop line; 16 TTL I/O lines; 8 A/D 10 bits lines; 3 Timers Counters; 64K EPROM; 64K RAM; 32K RAM and RTC backed; 32K DIL EEPROM; 8K serial EEPROM; 2 PWM lines; 1 Activity LED; Watch dog; 5 readable DIPs; LCD Interface.

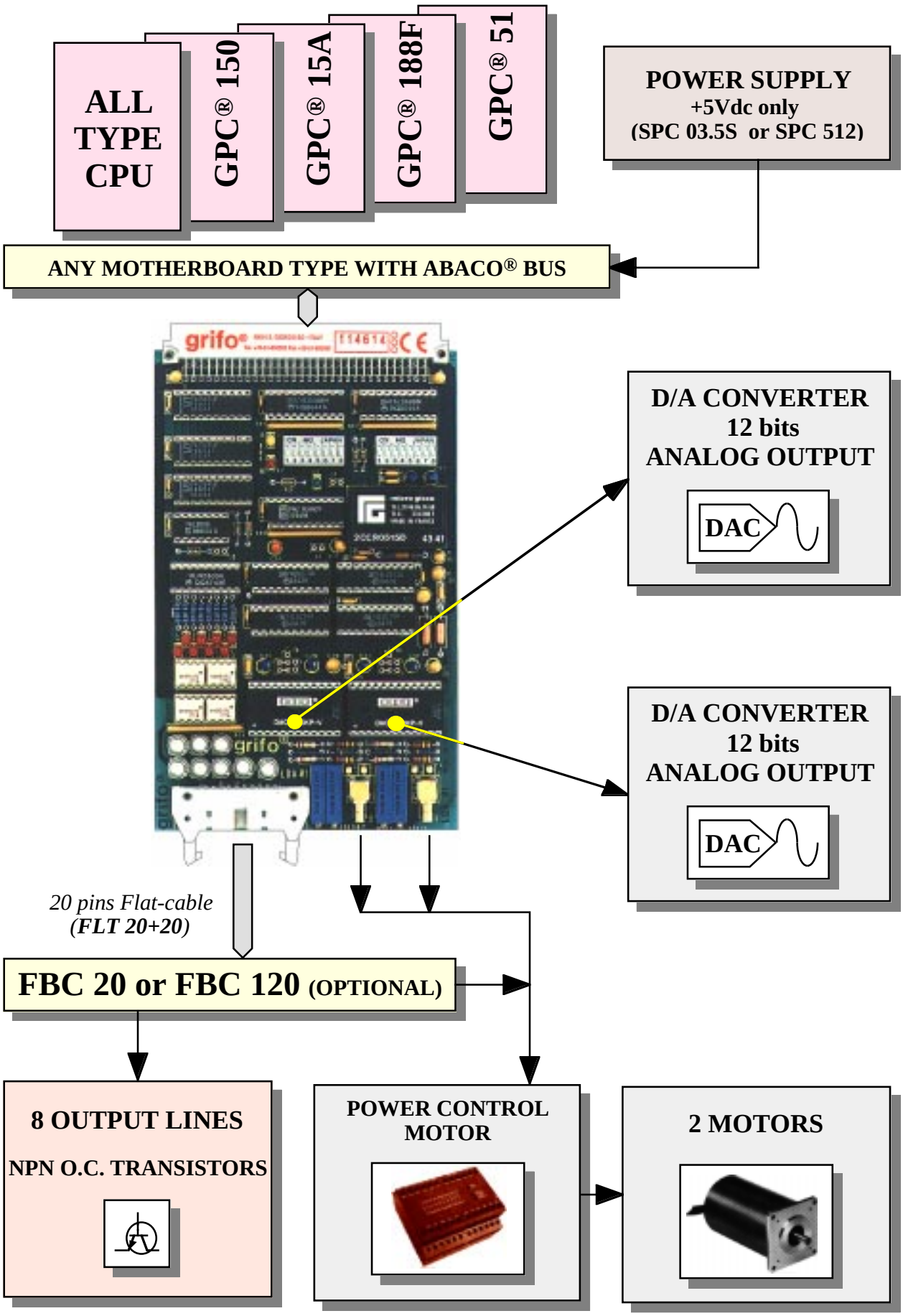

FIGURE 19: POSSIBLE CONNECTIONS DIAGRAM

GPC® 153

General Purpose Controller Z80

84C15 µP, 10÷16 MHz; Full CMOS; 1 RS 232 line; 1 RS 232 or RS 422-485 or Current Loop line; 16 TTL I/O lines; 8 A/D 12 bits lines; 2÷4 Timers Counters; 512K EPROM or FLASH; 512K RAM and RTC backed; 8K serial EEPROM; Buzzer; 1 Activity LED; Watch dog; 8 readable DIPs; LCD Interface.

GPC® 183

General Purpose Controller Z180

Z180 µP, 10÷16 MHz; Full CMOS; 1 RS 232 line; 1 RS 232 or RS 422-485 or Current Loop line; 24 TTL I/O lines; 11 A/D 12 bits lines; 2 Timers Counters; 512K EPROM or FLASH; 512K RAM and RTC backed; 8K serial EEPROM; Buzzer; 2 Activity LED; Watch dog; 4 readable DIPs; LCD Interface.

GPC® 324/D

"4" Type General Purpose Controller 80C32/320

80C32 or 80C320 µP, 14÷22 MHz; Full CMOS; 1 RS 232 line; 1 RS 232 or RS 422-485 or Current Loop line; 4÷16 TTL I/O lines; 3 Timers Counters; 64K EPROM; 64K RAM; 32K RAM backed; 32K DIL E2; 8K serial EEPROM; Watch dog; 1 readable DIP; LCD Interface; Abaco® I/O BUS; 5Vdc Power supply; Size: 100x50 mm.

GPC® 554

General Purpose Controller 80C552

Microprocessor 80C552 at 22 MHz; implementation completely CMOS; 32K EPROM; 32 K SRAM; 32 K EEPROM or SRAM; EEPROM; 2 RS 232 serial lines; 16 I/O TTL; 2 PWM lines; 16 bits Timer/Counter; Watch Dog; 6 signals A/D converter with resolution 10 bit; interface for **ABACO®** I/O BUS.

GPC® 154

"4" Type General Purpose Controller Z80

84C15 µP, 10÷16 MHz; Full CMOS; 1 RS 232 line; 1 RS 232 or RS 422-485 line; 16 TTL I/O lines; 2÷4 Timers Counters; 512K EPROM or FLASH; 512K RAM and RTC backed; 8K serial EEPROM; Watch dog; 2 readable DIPs; LCD Interface; Abaco® I/O BUS; 5Vdc Power supply; Size: 100x50 mm.

GPC® 884

General Purpose Controller Am188ES

Microprocessor AMD Am188ES up to 40 MHz16 bits; implementation completely CMOS; serie 4 format; 512K EPROM or FLASH; 512K SRAM backed with Lithium battery; RTC; 1 RS 232 serial line + 1 RS 232 or RS 422-485 or current loop; 16 I/O TTL; 3 timer/counter; watch dog; EEPROM; 11 signals A/D converter with 12 bit resolution; interface for **ABACO®** I/O BUS.

GPC® 114

General Purpose Controller 68HC11

Microprocessor 68HC11A1 at 8 MHz; implementation completely CMOS; serie 4 format; 32K EPROM; 32K SRAM backed with Lithium battery; 32K EPROM, SRAM, EEPROM; RTC; 1 serial line RS 232 or RS 422-485; 10 I/O TTL; 3 timer/counter; watch dog; 8 signals A/D converter with resolution 8 bit; 1 asunchronous serial line; extremly low power consumption; interface for **ABACO®** I/O BUS.

PBI 01

PNP BLOCK Input

Interface for PNP drivers through NPN inputs; 16 inputs for driver PNP, visualized by LEDs; 16 NPN outputs on **ABACO**® standard input connector; Plastic mount for rails DIN 46277-1 and 3.

FBC 20-120

Flat Block Contact 20 vie

Interface for 2 or 1 mounting cable connectors (low profile 20 pins male) and quick release screw terminal connectors; Plastic mount for rails DIN 46277-1 and 3.

FBC 34

Flat Block Contact 34 vie

Interface for 2 mounting cable connector (low profile 34 pins male) and quick release screw terminal connectors; Plastic mount for rails DIN 46277-1 and 3.

FBC L20

Flat Block Contact LED 20 vie

Interface for 1 mounting cable connector (low profile 20 pins male,featuring **ABACO**® standard Input pin out, and quick release screw terminal connectors; All the signals are visualized through LEDs; Plastic mount for rails DIN 46277-1 and 3.

FBC L34

Flat Block Contact LED 34 vie

Interface for 2 mounting cable connectors (low profile34 and 20 pins male) and quick release screw terminal connectors; featuring **ABACO**® standard Input and Output pin out; All the signals are visualized through LEDs; Plastic mount for rails DIN 46277-1 and 3.

BIBLIOGRAPHY

Here follows a list of manuals and technical notes that the User can read to acquire more informations about **LDA 01** board.

Manual SGS-THOMSON: *Industrial and Computer Peripheral ICs - Data Book*
Manual SGS-THOMSON: *Programmable logic manual - GAL Products*
Manual SGS-THOMSON: *Small Signal Transistors - Data Book*

Manual TEXAS INSTRUMENTS: *The TTL data Book - SN54/74 Families*

Manual TOSHIBA: *Photo Couplers - Data Book*

Manual BURR-BROWN: *Integrated circuits data book - Volume 33*

Technical Note MICRO-GISCO: *DC/DC Converter 2CCR0515D*

Please connect to the manifactures Web sites to get the latest version of all manuals and data sheets.

APPENDIX A: ALPHABETICAL INDEX

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