LAD 415

4 Low cost Analog to Digital 15 bits

TECHNICAL MANUAL

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LAD 415 Edition 5.10 *Rel. 16 March 2001*

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Eurocard format size 100x160 mm; interface to **ABACO®** industrial BUS; 4 analog to digital multislope integration technique with resolution 15 bits plus sign; indipendent conversion speed for the 4 sections selectable amongst **5, 10, 20 or 40** conversions per second; voltage full range and input ranges software selectable amongst **±3.2768 Vdc, ±5 Vdc, ±10 Vdc**; current input 0÷20 mA or 4÷20 mA; 9 indication LEDs on the front panel; 9 pins **D type** connector for input analog signals; circuitry to generate interrupts on **ABACO®** BUS; 8 bits data BUS management; only as low as **4 bytes** taken; **polarity** indication through software; highest noise immunity against **50 Hz** manis frequence; **single conversion** or **automatic conversion** working mode; direct interfacement to **FBC** field modules; unique power supply **+5Vdc**

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IMPORTANT

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For specific informations on the components mounted on the card, please refer to the Data Book of the builder or second sources.

SYMBOLS DESCRIPTION

In the manual could appear the following symbols:

Attention: Generic danger

Attention: High voltage

Trade Marks

abaco®, **GPC**®, **grifo**® : are trade marks of **grifo**®.
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GENERAL INDEX

FIGURES INDEX

INTRODUCTION

The use of these devices has turned - IN EXCLUSIVE WAY - to specialized personnel.

The purpose of this handbook is to give the necessary information to the cognizant and sure use of the products. They are the result of a continual and systematic elaboration of data and technical tests saved and validated from the manufacturer, related to the inside modes of certainty and quality of the information.

The reported data are destined- IN EXCLUSIVE WAY- to specialized users, that can interact with the devices in safety conditions for the persons, for the machine and for the enviroment, impersonating an elementary diagnostic of breakdowns and of malfunction conditions by performing simple functional verify operations , in the height respect of the actual safety and health norms.

The informations for the installation, the assemblage, the dismantlement, the handling, the adjustment, the reparation and the contingent accessories, devices etc. installation are destined - and then executable - always and in exclusive way from specialized warned and educated personnel, or directly from the TECHNICAL AUTHORIZED ASSISTANCE, in the height respect of the manufacturer recommendations and the actual safety and health norms.

The devices can't be used outside a box. The user must always insert the cards in a container that rispect the actual safety normative. The protection of this container is not threshold to the only atmospheric agents, but specially to mechanic, electric, magnetic, etc. ones.

To be on good terms with the products, is necessary guarantee legibility and conservation of the manual, also for future references. In case of deterioration or more easily for technical updates, consult the AUTHORIZED TECHNICAL ASSISTANCE directly.

To prevent problems during card utilization, it is a good practice to read carefully all the informations of this manual. After this reading, the user can use the general index and the alphabetical index, respectly at the begining and at the end of the manual, to find information in a faster and more easy way.

CARD VERSION

The present handbook is reported to the **LAD 415** card release **200292** and later. The validity of the bring informations is subordinate to the number of the card release. The user must always verify the correct correspondence among the two denotations. On the card the release number is present in more points both board printed diagram (serigraph) and printed circuit (for example near jumpers J11 both on the component side and on the solder side).

GENERAL INFORMATION

LAD 415 (**4 L**ow cost **A**nalog to **D**igital 15 bits) card is a powerful Eurocard format card, provided with **ABACO®** industrial BUS interface. This card belongs to the analog peripherals units list and, in specific, its purpose is to provide four high precision Analog to Digital conversion lines.
The analog signals are connected through one 9 pins lD type standard connector. Four indipendent A/D Converter circuitries, based on as many **TSC 850**, warrant a complete separation of the signals. A/D circuitry features **15 bits** of resolution plus sign.
The signal to be acquired can be configured as voltage (**±3.2768 Vdc, ±5 Vdc, ±10 Vdc**) or current (**0÷20 mA** or **4÷20 mA**) indipenndently for each section by moving the opportune jumper for inserting a current-to-voltage conversion.
The 9 pins output connector allows an immediate interfacing to modules for the field, like **FBC D9**x, that untangle the signals from the flat cable to comfortable quick release screw terminal connectors. Remarkable is **FBC D9M** for the specific use with this card and an extension cable .
LAD 415 card can be driven through any CPU board in the **ABACO®** listing and takes as low as 4 contiguous bytes in the addressing space.
A remarkable feature of **LAD 415** is the capability to be Multi-Range and to allows the acquisition of input signal with several different characteristics by a simple hardware setting. On the front of the board one software manageable LED is available, in addition there are two more LEDs for each section that signal the end of a converson and the access to A/D converter.
LAD 415 is the ideal component for all the applications where good conversion speed, very high precision, several lines and low costs are required. It is in fact more convenient to install more cards to increase the number of signals to acquire than installing multiplexing cards that degrade the conversion quality and decrease the sampling rate, vanificating the investiment for an high speed card.
Overall features of **LAD 415** are as follows:

- Eurocard format size 100x160 mm
- Interface to **ABACO®** industrial BUS
- 4 analog to digital multislope integration technique with resolution 15 bits plus sign
- Indipendent conversion speed for the 4 sections selectable amongst **5, 10, 20 or 40** conversions per second
- Voltage full range and input ranges software selectable amongst **±3.2768 Vdc, ±5 Vdc, ±10 Vdc**
- Current input 0÷20 mA or 4÷20 mA
- 9 indication LEDs on the front panel
- 9 pins **D type** connector for input analog signals
- Circuitry to generate interrupts on **ABACO®** BUS
- 8 bits data BUS management
- Only as low as **4 bytes** taken
- **Polarity** indication through software
- Highest noise immunity against **50 Hz** mains frequence
- **Single conversion** or **automatic conversion** working mode
- Direct interfacement to **FBC** field modules
- Unique power supply **+5Vdc**

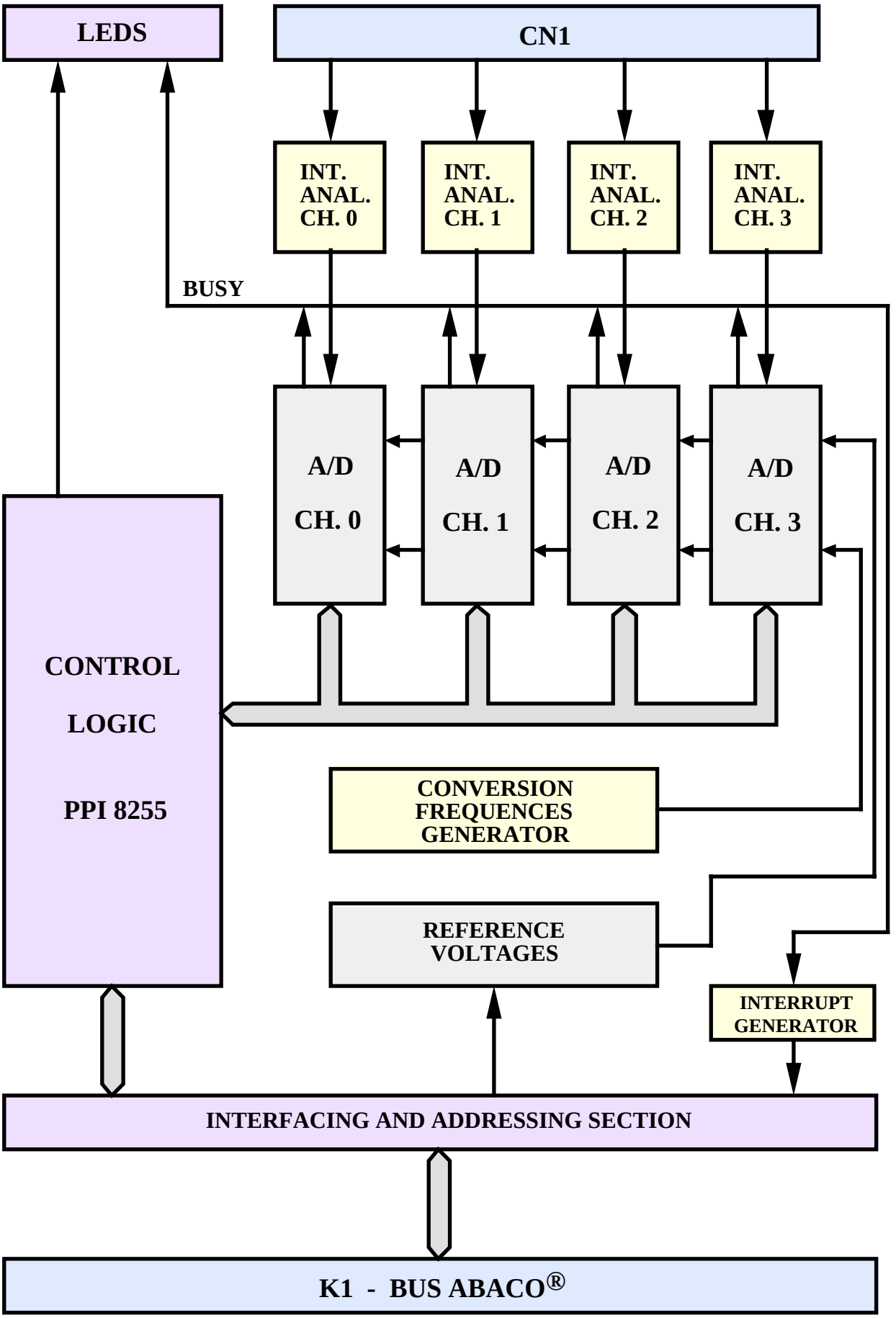

FIGURE 1: BLOCK DIAGRAM

Here follows a description of **LAD 415** board's functional blocks, with an indication of the operations performed by each one. To easily locate these blocks and verify their connections pleare refer to figure 1.

INTERFACING AND ADDRESSING

This section manages the data exchange between contol logic and command board through **ABACO®** BUS. In particular, all written or read data transit across this section that, in addition, provides the board I/O management in a 256 or 512 bytes addressing space, by setting the dip switch **DIP1**.
For further information please refer to the chapter dedicated to board's software description.

CONTROL LOGIC

This section generates all the chip select signals needed to acces the several peripherals on **LAD 415** boards. Using this section the programmer can interact to the board's several sections, verifing their status, setting configuration of A/D converters, etc.
All this can be done through a simple software management based on **ABACO®** BUS, to which the contol logic connects through the interfacing and addressing section. Control logic section is based on a PPI 82C55. For further information please refer to chapter “PERIPHERAL DEVICES SOFTWARE DESCRIPTION”.

CLOCK

LAD 415 is provided with an oscillator circuit to generate the clock signals indipendently needed by the four A/D converter sections. Required frequences are generated from a 3.2768 MHz quartz, each A/D converter section can reveive the needed frequence by simply moving a jumper. Such frequence determines the time succession of the several A/D conversion phases process, its value has been chosen to optimize both conversion time and noise immunity.

INPUT INTERFACES

Each of the 4 analog inputs is provided with an indipendent interfacement circuitery that fits the input signal coming from external world to match the requirement of the A/D converter analog input. Such circuitery is based on precision components selected in laboratory, to provide the boards with the same kind of interfacement.
Should the input interface not fulfil the requirements of user application, please contact **grifo®** directly.
For further information about input circuitery please refer to paragraph “TRIMMERS AND CALIBRATION”.

REFERENCE VOLTAGES

A specific precision circuitery is charged to generate the two reference voltages (**Vref**) required by the A/D converters. Such voltages are perfectly stabilized and indipendent from the board supply and temperature variations, so to increase **LAD 415** precision and reliability.
Each A/D converter has its own indipendent **Vref** setting.
For further information please see paragraph “TRIMMERS AND CALIBRATION”.

A/D CONVERTER

LAD 415 board features four indipendent A/D converter sections based on as many **TSC 850**, these are precision A/D converters that take advantage of the multiple slope technique. This allows to feature the same precision of double slope converters and higher conversion speed.
Overall features are:

- Resolution 15 bits plus sign
- high noise immunity
- Max linearity and offset error ±2 LSB
- Analog internal circuitery requires no calibrations (self zero)
- Conversion in continuous mode or “single shot” mode
- Simple software management

TSC 850 is the ideal component for the typical application of industrial automation, where a good conversion speed and a very high grade of precision are required. For further information about this component please refer to manufacturer documentation.

TECHNICAL FEATURES

GENERAL FEATURES

On board resources:	4 analog inputs (four 1 channel A/D converters) 1 eight pins dip switch to set I/O address
BUS type:	Industrial **ABACO®**
Addressing space:	256 or 512 bytes
Bytes taken:	4
On board peripherals:	TSC 850 PPI 82C55 or PPI 71055
A/D external clock frequence:	3.2768 MHz
A/D conversion speed:	selectable amongst 5, 10, 20 and 40 conversion/sec
A/D resolution:	15 bits + sign
A/D max linearity and offset error:	±2 LSB (*)
A/D max offset error:	±0.5 LSB (*)
A/D differantial input error:	±0.5 LSB (*)

PHYSICAL FEATURES

Size:	Standard EUROCARD format 100x160 mm
Weight:	190 g
Connectors:	K1: DIN 41612 64 pins M 90° A+C type C CN1: 9 pins D type M 90°
Temperature range:	from 0 to 70° C
Relative humidity:	20% up to 90% (without condensing)

(*) Values referred to a working temperature of 20 °C

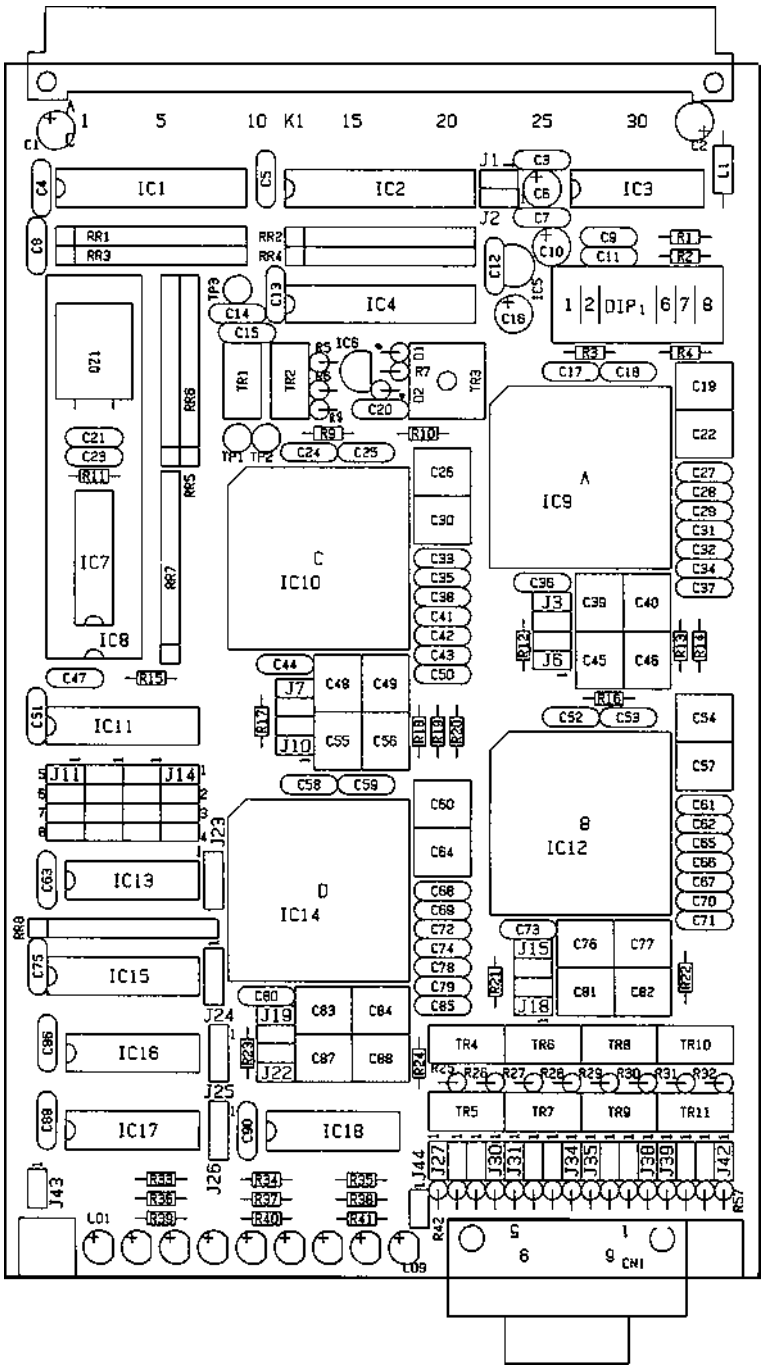

FIGURE 2: COMPONENTS MAP

ELECTRIC FEATURES

Power supply:	+5 Vdc ± 5%
Current consumption:	230 mA
A/D input impedance:	≥ 1 MΩ
Analog inputs:	±3.2768 Vdc, ±5 Vdc, ±10 Vdc 0÷20 mA or 4÷20 mA
A/D reference voltages:	1.6384 Vdc and 25.60 mVdc generated on board
Interface on analog inputs:	analog signal fitting through voltage dividers and drop resistors

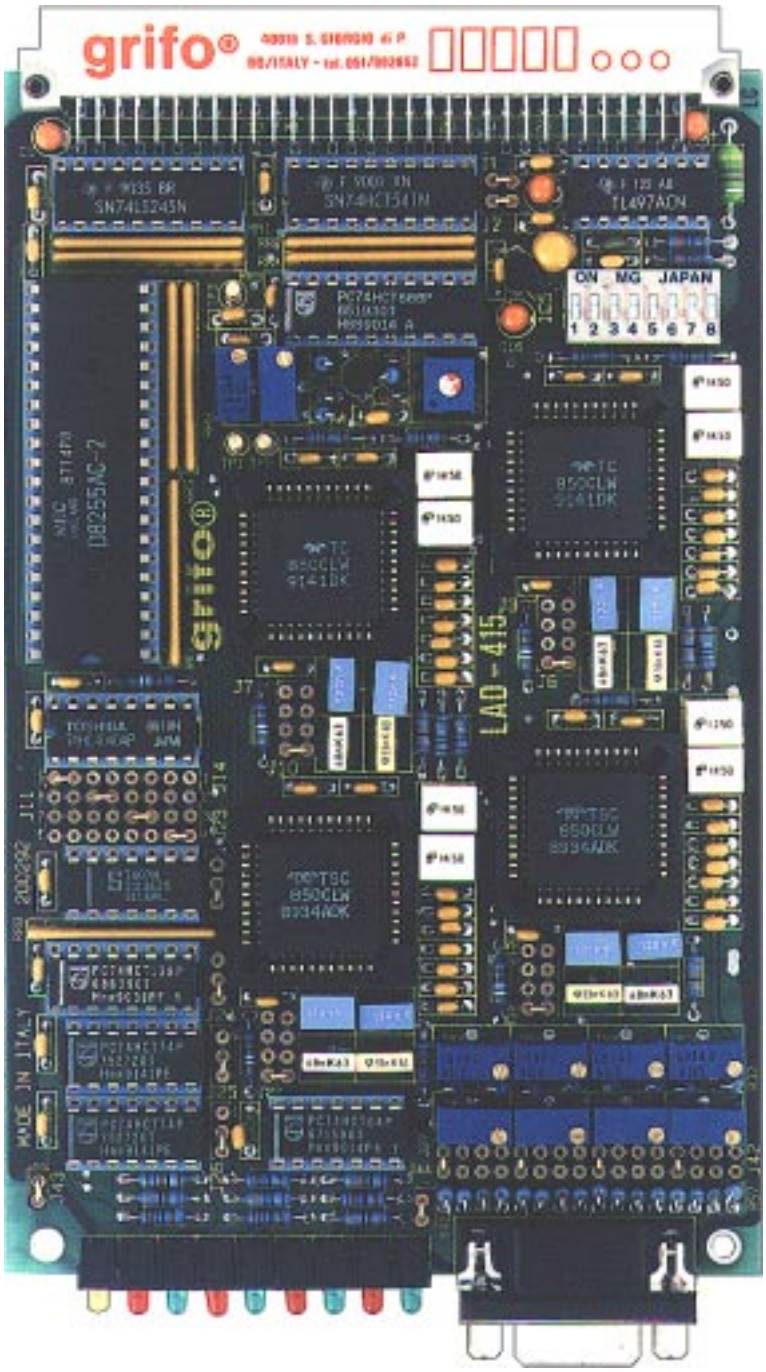

FIGURE 3: CARD PHOTO

INSTALLATION

In this chapter there are the information for a right installation and correct use of **LAD 415** card. The user can find the location and functions of each connectors, LEDs, trimmer and some explanatory diagrams.

CONNECTIONS

The board has two connectors that can be linkeded to other devices or directly to the field, according to system requirements. In this paragraph there are connectors pin outs, a short signals description (including the signals direction) and connectors location, plus some figures that describe how the interface signals are connected on the card. To easily locate the connectors please refer to figure 5.

CN1 - ANALOG INPUTS CONNECTOR

The connector for the analog input of the four TSC 850, called CN1, is a D type, 9 pins, 90 degreeses. The lines available on CN1 feature signal fitting for the ranges ±3.2768 Vdc, ±5 Vdc, ±10 Vdc or 0÷20 mA or 4÷20 mA. Signals placement on the connector has been designed to reduce problems of noise and interference and to warrant a good transmission quality.

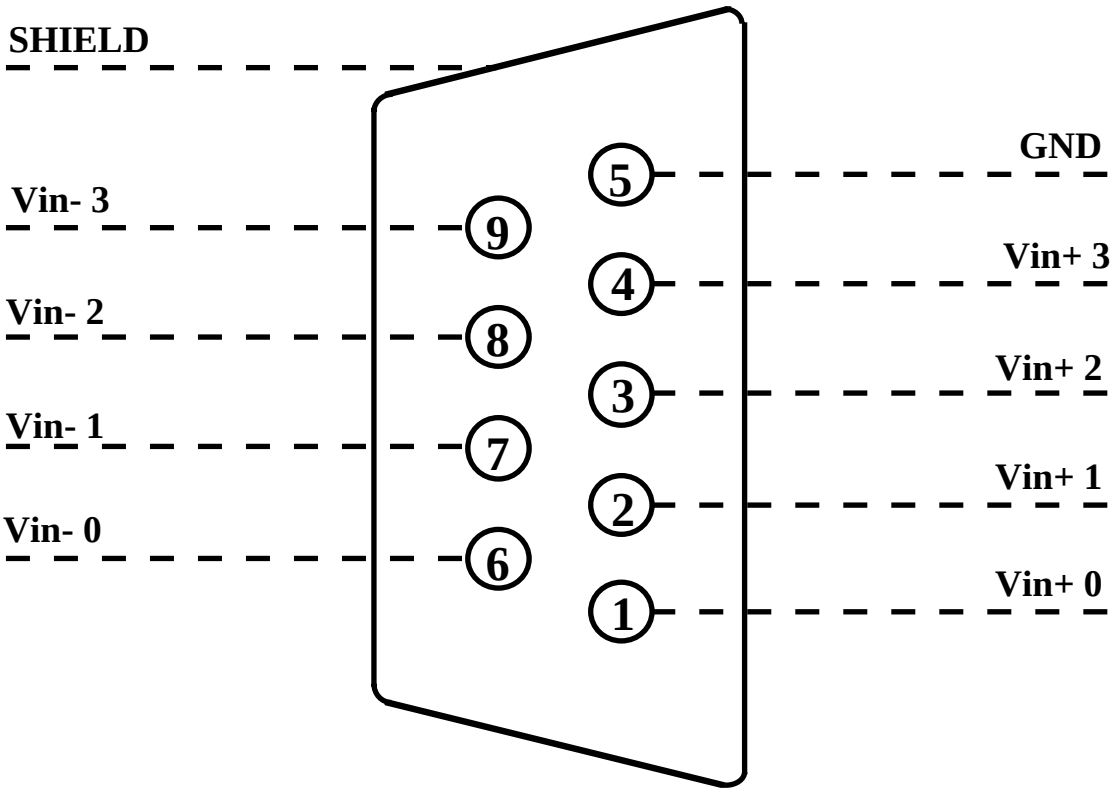

FIGURE 4: CN1 - ANALOG INPUTS CONNECTOR

Signals description:

Vin+ n	=	I	- A/D channel n-th positive differential input
Vin- n	=	I	- A/D channel n-th negative differential input
GND	=		- Ground
SHIELD	=		- Connector shield connectable to GND

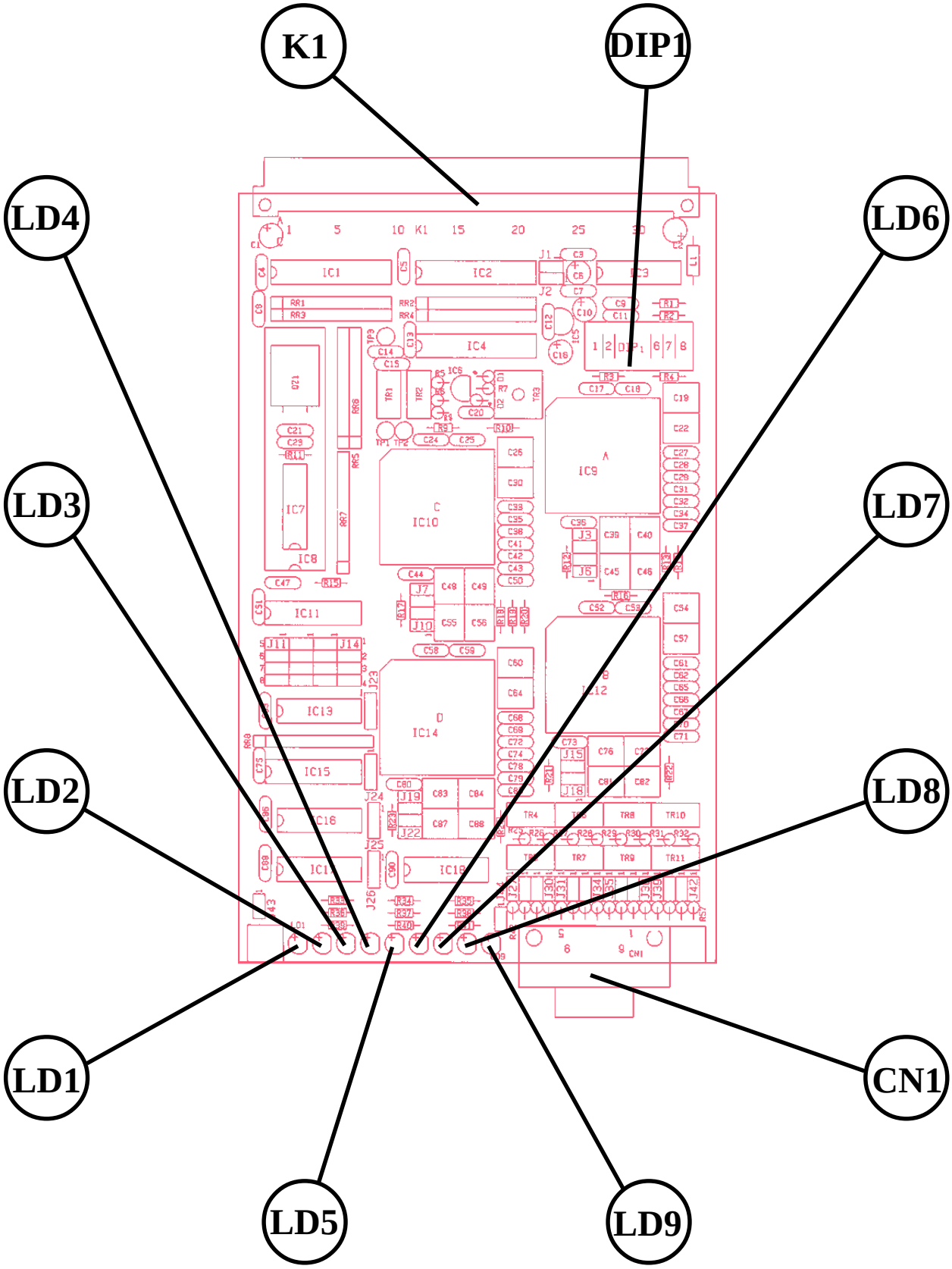

FIGURE 5: CONNECTORS, DIP SWITCH, LEDS LOCATION

K1 - CONNECTOR FOR ABACO® BUS

The connector for **ABACO® industrial BUS**, called K1 on the board,is a DIN 41612, male, a 90 °, type C, A+C.
Here follows the pin-out of the connector installed on **LAD 415**, in addition there is the standard 8 bits and 16 bits**ABACO®** BUS pin-out.
Please remark that all the signals here described are TTL, except for the power supplies.

A 16 bit BUS	A 8 bit BUS	A LAD 415	PIN	C LAD 415	C 8 bit BUS	C 16 bit BUS
GND	GND	GND	1	GND	GND	GND
+5 Vdc	+5 Vdc	+5 Vdc	2	+5 Vdc	+5 Vdc	+5 Vdc
D0	D0	D0	3	N. C.		D8
D1	D1	D1	4	N. C.		D9
D2	D2	D2	5	N. C.		D10
D3	D3	D3	6	/INT	/INT	/INT
D4	D4	D4	7	N. C.	/NMI	/NMI
D5	D5	D5	8	N. C.	/HALT	D11
D6	D6	D6	9	N. C.	/MREQ	/MREQ
D7	D7	D7	10	/IORQ	/IORQ	/IORQ
A0	A0	A0	11	/RD	/RD	/RDLDS
A1	A1	A1	12	/WR	/WR	/WRLDS
A2	A2	A2	13	N. C.	/BUSAK	D12
A3	A3	A3	14	N. C.	/WAIT	/WAIT
A4	A4	A4	15	N. C.	/BUSRQ	D13
A5	A5	A5	16	/RESET	/RESET	/RESET
A6	A6	A6	17	/M1	/M1	/IACK
A7	A7	A7	18	N. C.	/RFSH	D14
A8	A8	A8	19	N. C.	/MEMDIS	/MEMDIS
A9	A9	N. C.	20	N. C.	VDUSEL	A22
A10	A10	N. C.	21	N. C.	/IEI	D15
A11	A11	N. C.	22	N. C.		
A12	A12	N. C.	23	N. C.	CLK	CLK
A13	A13	N. C.	24	N. C.		/RDUDS
A14	A14	N. C.	25	N. C.		/WRUDS
A15	A15	N. C.	26	N. C.		A21
A16		N. C.	27	N. C.		A20
A17		N. C.	28	N. C.		A19
A18		N. C.	29	N. C.	/R.T.	/R.T.
+12 Vdc	+12 Vdc	N. C.	30	N. C.	-12 Vdc	-12 Vdc
+5 Vdc	+5 Vdc	+5 Vdc	31	+5 Vdc	+5 Vdc	+5 Vdc
+5 Vdc	+5 Vdc	GND	32	GND	GND	GND

FIGURE 6: K1 - CONNECTOR FOR ABACO® BUS

Signals description:

8 bits CPU

A0-A15	=	O	- Address BUS
D0-D7	=	I/O	- Data BUS
/INT	=	I	- Interrupt request
/NMI	=	I	- Non Maskable Interrupt
/HALT	=	O	- Halt state
/MREQ	=	O	- Memory Request
/IORQ	=	O	- Input Output Request
/RD	=	O	- Read cycle status
/WR	=	O	- Write cycle status
/BUSAK	=	O	- BUS Acknowledge
/WAIT	=	I	- Wait
/BUSRQ	=	I	- BUS Request
/RESET	=	O	- Reset
/M1	=	O	- Machine cycle one
/RFSH	=	O	- Refresh for dynamic RAM
/MEMDIS	=	I	- Memory Display
VDUSEL	=	O	- VDU Selection
/IEI	=	I	- Interrupt Enable Input
CLK	=	O	- System clock
R.B.	=	I	- Reset button
+5 Vdc	=	I	- Power supply at +5 Vdc
+12 Vdc	=	I	- Power supply at +12 Vdc
-12 Vdc	=	I	- Power supply at -12 Vdc
GND	=		- Ground signal

16 bits CPU

A16-A22	=	O	- Address BUS
D8-D15	=	I/O	- Data BUS
/RD UDS	=	O	- Read Upper Data Strobe
/WR UDS	=	O	- Write Upper Data Strobe
/IACK	=	O	- Interrupt Acknowledge
/RD LDS	=	O	- Read Lower Data Strobe
/WR LDS	=	O	- Write Lower Data Strobe

NOTE
Directionality indications as above stated are referred to a master (**GPC®**) board and have been kept untouched to avoid ambiguity in case of multi-boards systems.

VISUAL SIGNALATIONS

LAD 415 card is provided with nine signalation LEDs to show several status informations, as described in the following table:

LEDS	COLOUR	PURPOSE
LD1	Yellow	Software managed activity LED.
LD2	Red	It lights when an access to A/D channel 0 has occoured.
LD3	Green	It lights when A/D conversion end on channel 0 occours.
LD4	Red	It lights when an access to A/D channel 1 has occoured.
LD5	Green	It lights when A/D conversion end on channel 1 occours.
LD6	Red	It lights when an access to A/D channel 2 has occoured.
LD7	Green	It lights when A/D conversion end on channel 2 occours.
LD8	Red	It lights when an access to A/D channel 3 has occoured.
LD9	Green	It lights when A/D conversion end on channel 3 occours.

FIGURE 7: VISUAL SIGNALATIONS TABLE

The main purpose of LEDs is to show a visual indication about the card's status, making so easier debug and verify operations. All the LEDs are in the front of the board, near connector CN1. To easily locate these visual signalations please refer to the figure 5.

POWER SUPPLY

LAD 415 is provided with an efficent circuitery that solves in a comfortable and simple way the problem of the board's supply, under any condition of use.
Here follow the voltages nedded:

+5 Vdc: Supplies the on board logic; must be in the range +5 Vdc ± 5% and must be provided through the specific pins of connector K1 (**ABACO®** BUS).

To warrant great immunity to external noise and so a correct working of the board, it is essential that **+5 Vdc** tension is galvanically isolated.

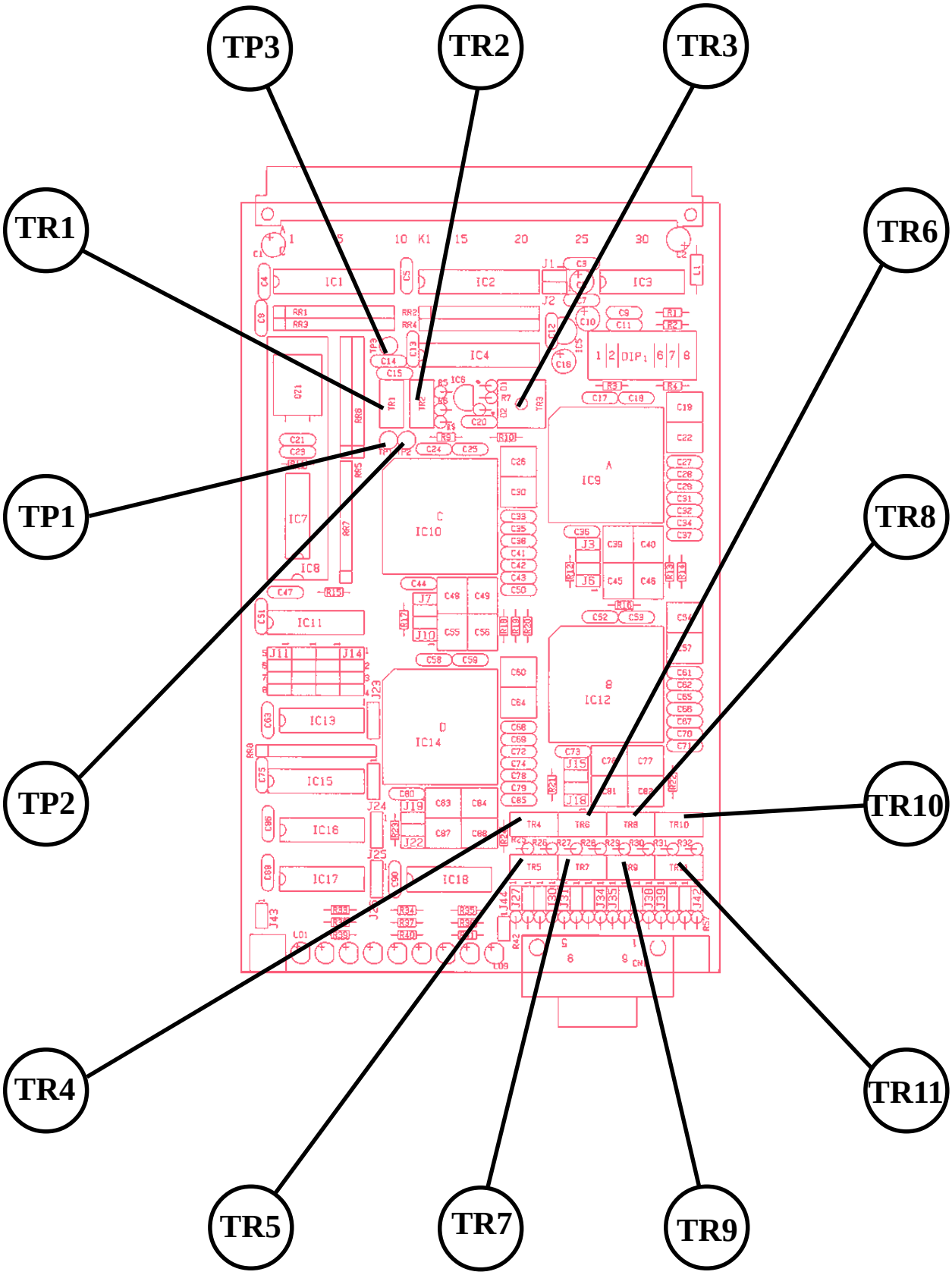

FIGURE 8: TRIMMERS AND TEST POINTS LOCATION

DIP SWITCH

LAD 415 is provided with an on board 8 pins dip switch (DIP1). Its purpose is to set the mapping address for control and data registers of the on board devices, with jumper J1. To set the connection modalities for signal /M1 jumper J2 is used, for /INT signal jumpers J23÷26 are used.
More information about card mapping and signals management can be found in chapter "PERIPHERAL DEVICES SOFTWARE DESCRIPTION" and in paragraph "JUMPERS", while to easily locate them on the board please refer to figures 8, 12 and 14.

BOARD CONNNECTIONS

To prevent possible connecting problems between **LAD 415** board and the external systems, the user has to read carefully the information of the previous paragraphs and he must follow these instructions:

- The TTL signals can be connected directly only to a device featuring the same type of interface. About the correspondance between logic signals and TTL output status, remember that a logic **0** generates a TTL 0 Vdc, while a logic **1** generates a TTL +5 Vdc.

- The analog inputs (A/D section) must be connected to signals in the following ranges: ±3.2768 Vdc, ±5 Vdc, ±10 Vdc or 0÷20 mA according to the board configuration. Please remember that the four analog inputs available on CN1 feature analog signal fitting through voltage dividers and drop resistors, to meet the requirements of TSC 850 input section, that converts the voltage range and the current signals in the voltage range accepted by A/D converter. For further information please refer to the paragraph "TYPE OF ANALOG INPUT SELECTION".

TEST POINT

The board is provided with three test points called TP1÷3, that allow to read, through a galvanically isolated multimeter, the reference voltages calibrated in laboratory and whose values are Vref1=1.6384 Vdc and Vref2=25.60 mVdc, used by the A/D converter sections:

TP1 -> Reference voltage 1 (Vref1) 1.6384 V
TP2 -> Reference voltage 2 (Vref2) 25.60 mV
TP3 -> Ground (GND)

Vref's are perfectly stabilized and completely indipendent from power supply voltage.
To easily locate the test point contacts please refer to figure 8, while for further information about Vref signals please refer to the paragraph "TRIMMER AND CALIBRATION".

INTERRUPT

LAD 415 is provided with a comfortable and efficent interrupt generation circuitery, that, if enabled, can generate an interrupt to the **GPC**® intelligent control card when one of the four analog to digital converter sections reach the end of a conversion. Such circuitery allows to optimize the time needed to manage the board, in fact the intelligent control card is not obliged to poll **LAD 415** registers, but can simply wait for an interrupt and read the conversion results.
ABACO® BUS interrupt signal, once it has been activated, remains in such status until the control card performs the read operation from **LAD 415** A/D converter data registers. This ensures a correct management also in case of contemporary interrupts, in fact the signal deactivates only after the proper software operations, which are time-indipendent. This means that if the interrupt routine reads the end of conversion bit then the data obtained by the correspondant conversion it is sure that the board interrupt are managed correctly. **LAD 415** interrupt generation circuitery can be connected or not connected to **ABACO**® BUS through jumpers J23, J24, J25 and J26.
For further information please refer to chapter "PERIPHERAL DEVICES SOFTWARE DESCRIPTION" and paragraph "JUMPERS". To locate jumpers please refer to figures 12 and 14.

TRIMMERS AND CALIBRATION

On **LAD 415** board there are eleven trimmers, called **TR1÷11**, that calibrate the reference voltages and perform input signals fitting from selected signal range to the input range of TSC 850:

TRIMMER	PURPOSE
TR1	Allows fine setting for reference voltage 1 (Vref1).
TR2	Allows fine setting for reference voltage 2 (Vref2).
TR3	Allows coarse setting for reference voltages 1 and 2 (Vref1 and Vref2).
TR4	Allows fine setting of the drop resistance value for current to voltage conversion on channel 3.
TR5	Allows fine setting of the resistance value of voltage divider for input in the ranges ±5 Vdc and ±10 Vdc on channel 3.
TR6	Allows fine setting of the drop resistance value for current to voltage conversion on channel 2.
TR7	Allows fine setting of the resistance value of voltage divider for input in the ranges ±5 Vdc and ±10 Vdc on channel 2.
TR8	Allows fine setting of the drop resistance value for current to voltage conversion on channel 1.
TR9	Allows fine setting of the resistance value of voltage divider for input in the ranges ±5 Vdc and ±10 Vdc on channel 1.
TR10	Allows fine setting of the drop resistance value for current to voltage conversion on channel 0.
TR11	Allows fine setting of the resistance value of voltage divider for input in the ranges ±5 Vdc and ±10 Vdc on channel 0.

FIGURE 9: TRIMMERS TABLE

The **LAD 415** is subjected to a careful test that verifies and calibrates all the card sections.
The calibration is executed in laboratory, with a conntrolled +20° C room temperature, following these steps:

-Reference voltages calibration: first the coarse calibration is performed through trimmer TR3, then the fine calibration of Vref1 (1.6384 Vdc) and Vref2 (25.60 mVdc) is performed respectively through trimmers TR1 and TR2. The A/D reference voltages are calibrated using a 5 digits precision multimeter connected opportunely to the test points.

-Voltage inputs fitting calibration: a reference signal in the range ±5 Vdc is provided and the value read by the A/D converter section is checked. If such value is not the one expected then the value of resistance in the input voltage divider is set using trimmers TR5, TR7, TR9, TR11. The same procedure is repeated for each of the four sections.

- Current inputs fitting calibration: a reference signal in the range 0÷20 mA is provided and the value read by the A/D converter section is checked. If such value is not the one expected then the value of drop resistance for the current input is set using trimmers TR4, TR6, TR8, TR10. The same procedure is repeated for each of the four sections.

- Trimmers are blocked with paint.

The analog interfaces use high precision components that are selected during mounting phase to avoid complicate and long calibration procedures. After the calibration, the on board trimmers are blocked with paint to mantain calibration also in presence of mechanic stresses (vibrations, movings, delivery, etc.).
The user most not intervernt on the trimmer settings, however if this should be necessary (example: for time derives) then he/she must follow the above mentioned procedure.
To easily locate the above mentioned components please refer to figure 8; for further information about test points please refer to the previous paragraph; for further information about how to read the A/D converters input voltages please refer to chapter “PERIPHERAL DEVICES SOFTWARE DESCRIPTION”.

RESET

After a reset or a power on the PPI 8255 or PPI 71055 used to drive the A/D converters TSC 850 set all its ports as inputs, while the correct use requires some of the ports to be set as outputs.
Please refer to paragraph “PERIPHERAL DEVICES SOFTWARE DESCRIPTION” for futher information.

TYPE OF ANALOG INPUT SELECTION

LAD 415 board can accept analog voltage and/or current inputs, as described in the previous paragraphs and chapters. The input type selection can be made through a set of comfortable jumpers located near connector CN1. In detail:

A/D channel	Input configuration	Jumpers			
0	as current	J39 C	J40 NC	J41 NC	J42 NC
	as voltage ±10 Vdc	J39 NC	J40 C	J41 NC	J42 NC
	as voltage ±5 Vdc	J39 NC	J40 NC	J41 C	J42 NC
	as voltage ±3.2768 Vdc	J39 NC	J40 NC	J41 NC	J42 C
1	as current	J35 C	J36 NC	J37 NC	J38 NC
	as voltage ±10 Vdc	J35 NC	J36 C	J37 NC	J38 NC
	as voltage ±5 Vdc	J35 NC	J36 NC	J37 C	J38 NC
	as voltage ±3.2768 Vdc	J35 NC	J36 NC	J37 NC	J38 C
2	as current	J31 C	J32 NC	J33 NC	J34 NC
	as voltage ±10 Vdc	J31 NC	J32 C	J33 NC	J34 NC
	as voltage ±5 Vdc	J31 NC	J32 NC	J33 C	J34 NC
	as voltage ±3.2768 Vdc	J31 NC	J32 NC	J33 NC	J34 C
3	as current	J27 C	J28 NC	J29 NC	J30 NC
	as voltage ±10 Vdc	J27 NC	J28 C	J29 NC	J30 NC
	as voltage ±5 Vdc	J27 NC	J28 NC	J29 C	J30 NC
	as voltage ±3.2768 Vdc	J27 NC	J28 NC	J29 NC	J30 C

NOTE
C means **C**onnected; **NC** means **N**ot **C**onnected

The current-to-voltage drop resistors in series totalize a precision value of **139.00 Ω**, this means that the board can accept as input ranges 4÷20 mA or 0÷20 mA corresponding to the positive first 32768 of the A/D converter resoulution.
Any eventual configuration out of this standard should be asked directly to **grifo®**.
For further information please refer to paragraph “TRIMMERS AND CALIBRATION”.

CONVERSION SPEED SELECTION

Conversion speed of **LAD 415** can be set indipendently for each of the four A/D converter sections. The speed can be selected amongst the four choices shown below
The possibility to select indipendently the conversion speeds allows to optimize the board resources utilization, according to the needs of the user application, to fulfil any of the board usage requirements.

Possible conversion speeds are:

200 ms which means 5 conversions per second
100 ms which means 10 conversions per second
50 ms which means 20 conversions per second
25 ms which means 40 conversions per second

Speed selection is performed through hardware by setting correctly the specific jumpers, as described here below:

A/D channel	Speed	Jumpers				
0	200 ms	J3 C	J4 NC	J5 NC	J6 NC	J11 in position 1-5
	100 ms	J3 NC	J4 C	J5 NC	J6 NC	J11 in position 2-6
	50 ms	J3 NC	J4 NC	J5 C	J6 NC	J11 in position 3-7
	25 ms	J3 NC	J4 NC	J5 NC	J6 C	J11 in position 4-8
1	200 ms	J15 C	J16 NC	J17 NC	J18 NC	J12 in position 1-5
	100 ms	J15 NC	J16 C	J17 NC	J18 NC	J12 in position 2-6
	50 ms	J15 NC	J16 NC	J17 C	J18 NC	J12 in position 3-7
	25 ms	J15 NC	J16 NC	J17 NC	J18 C	J12 in position 4-8
2	200 ms	J7 C	J8 NC	J9 NC	J10 NC	J13 in position 1-5
	100 ms	J7 NC	J8 C	J9 NC	J10 NC	J13 in position 2-6
	50 ms	J7 NC	J8 NC	J9 C	J10 NC	J13 in position 3-7
	25 ms	J7 NC	J8 NC	J9 NC	J10 C	J13 in position 4-8
3	200 ms	J19 C	J20 NC	J21 NC	J22 NC	J14 in position 1-5
	100 ms	J19 NC	J20 C	J21 NC	J22 NC	J14 in position 2-6
	50 ms	J19 NC	J20 NC	J21 C	J22 NC	J14 in position 3-7
	25 ms	J19 NC	J20 NC	J21 NC	J22 C	J14 in position 4-8

NOTE
C means **C**onnected; **NC** means **N**ot **C**onnected

JUMPERS

On **LAD 415** board there are 44 jumpers for card configuration. The unusually high number of jumpers is due to the possiblility to configure both conversion speed and anlog input range inidpendently for each of the four A/D converter sections. It is easy for the user to configure the board because most jumpers can be gathered in four groups featuring the same functionalities for each of the four A/D converter sections. Below there is the jumpers list, location and function.

JUMPERS	N. PINS	PURPOSE
J1	2	Select addressing mode 256 or 512 byte
J2	2	Connects signal /M1 to interfacement and addressing section
J3	2	Selects integration capacitor for channel 0 suitable for 5 conversions per second
J4	2	Selects integration capacitor for channel 0 suitable for 10 conversions per second
J5	2	Selects integration capacitor for channel 0 suitable for 20 conversions per second
J6	2	Selects integration capacitor for channel 0 suitable for 40 conversions per second
J7	2	Selects integration capacitor for channel 2 suitable for 5 conversions per second
J8	2	Selects integration capacitor for channel 2 suitable for 10 conversions per second
J9	2	Selects integration capacitor for channel 2 suitable for 20 conversions per second
J10	2	Selects integration capacitor for channel 2 suitable for 40 conversions per second
J11	8	Selects conversion speed for channel 0
J12	8	Selects conversion speed for channel 1
J13	8	Selects conversion speed for channel 2
J14	8	Selects conversion speed for channel 3

FIGURE 10: JUMPERS SUMMARIZING TABLE (PART 1)

JUMPERS	N. PINS	PURPOSE
J15	2	Selects integration capacitor for channel 1 suitable for 5 conversions per second
J16	2	Selects integration capacitor for channel 1 suitable for 10 conversions per second
J17	2	Selects integration capacitor for channel 1 suitable for 20 conversions per second
J18	2	Selects integration capacitor for channel 1 suitable for 40 conversions per second
J19	2	Selects integration capacitor for channel 3 suitable for 5 conversions per second
J20	2	Selects integration capacitor for channel 3 suitable for 10 conversions per second
J21	2	Selects integration capacitor for channel 3 suitable for 20 conversions per second
J22	3	Selects integration capacitor for channel 3 suitable for 40 conversions per second
J23	3	Connects to interfacement and addressing section the interrupt request coming from channel 0
J24	3	Connects to interfacement and addressing section the interrupt request coming from channel 1
J25	3	Connects to interfacement and addressing section the interrupt request coming from channel 2
J26	2	Connects to interfacement and addressing section the interrupt request coming from channel 3
J27	2	Selects current input for channel 3
J28	2	Selects voltage input for channel 3 in the range ±10 Vdc
J29	2	Selects voltage input for channel 3 in the range ±5 Vdc
J30	2	Selects voltage input for channel 3 in the range ±3.2768 Vdc
J31	2	Selects current input for channel 2
J32	2	Selects voltage input for channel 2 in the range ±10 Vdc
J33	2	Selects voltage input for channel 2 in the range ±5 Vdc
J34	2	Selects voltage input for channel 2 in the range ±3.2768 Vdc

FIGURE 11: JUMPERS SUMMARIZING TABLE (PART 2)

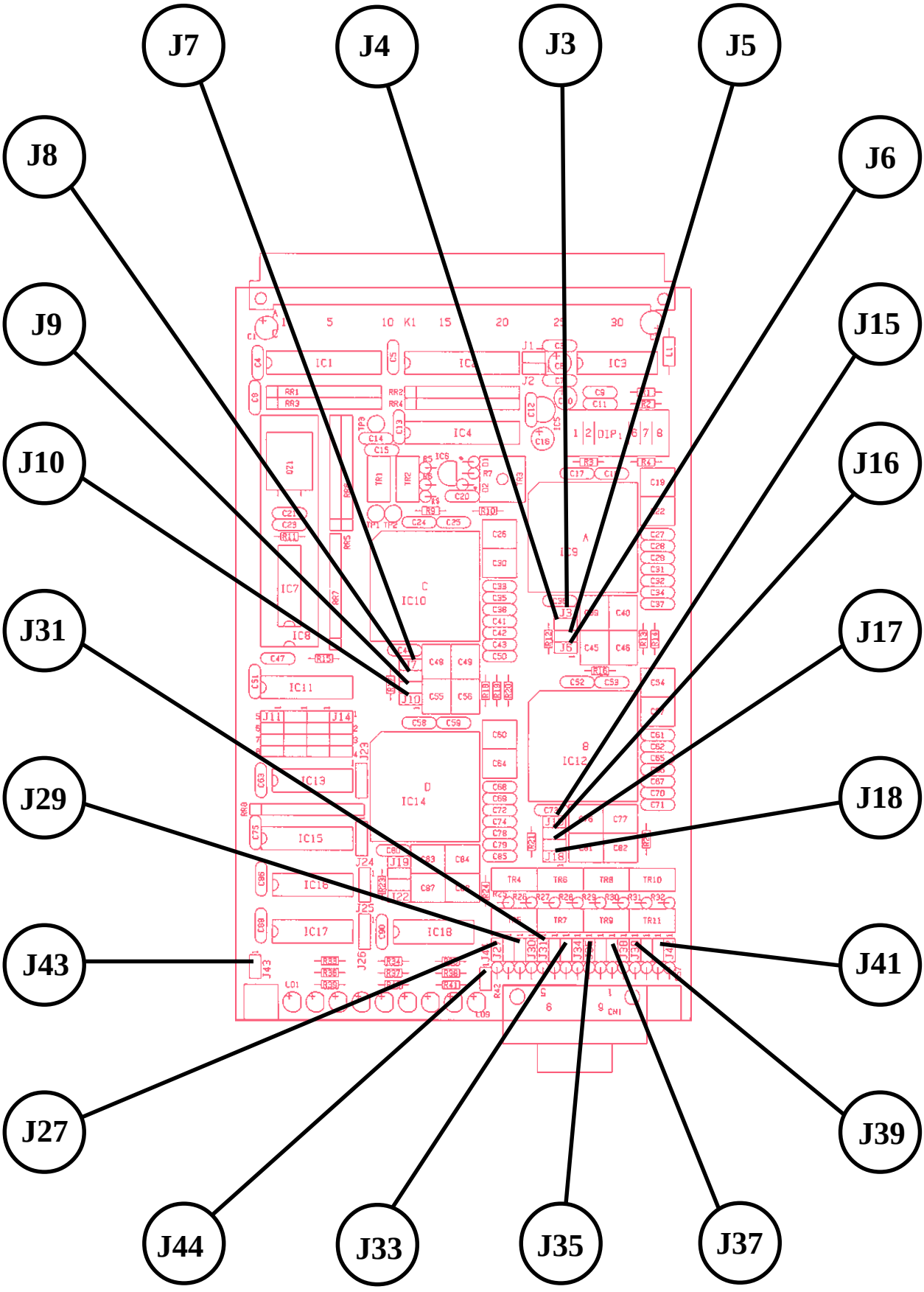

FIGURE 12: JUMPERS LOCATION (PART 1)

JUMPERS	N. PINS	PURPOSE
J35	2	Selects current input for channel 1
J36	2	Selects voltage input for channel 1 in the range range ±10 Vdc
J37	2	Selects voltage input for channel 1 in the range range ±5 Vdc
J38	2	Selects voltage input for channel 1 in the range range ±3.2768 Vdc
J39	2	Selects current input for channel 0
J40	2	Selects voltage input for channel 0 in the range range ±10 Vdc
J41	2	Selects voltage input for channel 0 in the range range ±5 Vdc
J42	2	Selects voltage input for channel 0 in the range range ±3.2768 Vdc
J43	2	Connects metallic shield to supply GND
J44	2	Connects CN1 pin 5 di CN1 to supply GND

FIGURE 13: JUMPERS SUMMARIZING TABLE (PART 3)

The following tables describe all the right connections of **LDA 415** jumpers with their relative functions. To recognize these valid connections, please refer to the board printed diagram (serigraph) or to figure 2 of this manual, where the pins numeration is listed; for recognizing jumpers location, please refer to figures 12 and 14.
The "*" used in the following tables, denotes the default connection, or on the other hand the connection set up at the end of testing phase, that is the configuration the User receives.

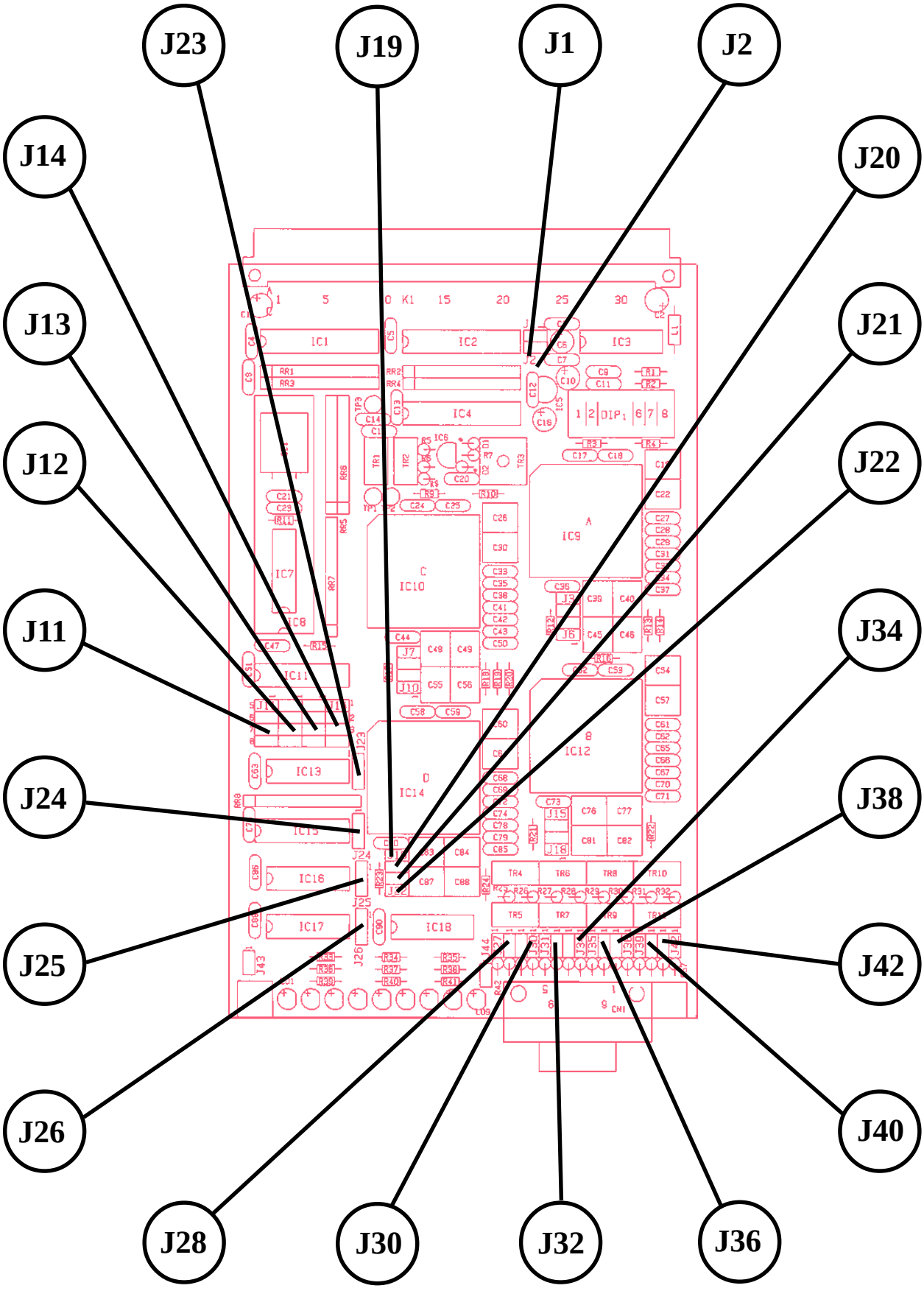

FIGURE 14: JUMPERS LOCATION (PART 2)

2 PINS JUMPERS

JUMPERS	CONNECTION	PURPOSE	DEF.
J1	not connected	Selects 256 byte of addressing space.	*
	connected	Selects 512 byte of addressing space.	
J2	not connected	Interfacing and addressing section does not manage signal /M1 from **ABACO®** BUS.	*
	connected	Interfacing and addressing section manages signal /M1 from **ABACO®** BUS.	
J3	not connected	Does not select the integration capacitor suitable for 5 conversions/second on channel 0.	*
	connected	Selects the integration capacitor suitable for 5 conversions/second on channel 0.	
J4	not connected	Does not select the integration capacitor suitable for 10 conversions/second on channel 0.	
	connected	Selects the integration capacitor suitable for 10 conversions/second on channel 0.	*
J5	not connected	Does not select the integration capacitor suitable for 20 conversions/second on channel 0.	*
	connected	Selects the integration capacitor suitable for 20 conversions/second on channel 0.	
J6	not connected	Does not select the integration capacitor suitable for 40 conversions/second on channel 0.	*
	connected	Selects the integration capacitor suitable for 40 conversions/second on channel 0.	
J7	not connected	Does not select the integration capacitor suitable for 5 conversions/second on channel 2.	*
	connected	Selects the integration capacitor suitable for 5 conversions/second on channel 2.	
J8	not connected	Does not select the integration capacitor suitable for 10 conversions/second on channel 2.	
	connected	Selects the integration capacitor suitable for 10 conversions/second on channel 2.	*

FIGURE 15: 2 PINS JUMPERS TABLE (PART 1)

JUMPERS	CONNECTION	PURPOSE	DEF.
J9	not connected	Does not select the integration capacitor suitable for 20 conversions/second on channel 2.	*
	connected	Selects the integration capacitor suitable for 20 conversions/second on channel 2.	
J10	not connected	Does not select the integration capacitor suitable for 40 conversions/second on channel 2.	*
	connected	Selects the integration capacitor suitable for 40 conversions/second on channel 2.	
J15	not connected	Does not select the integration capacitor suitable for 5 conversions/second on channel 1.	*
	connected	Selects the integration capacitor suitable for 5 conversions/second on channel 1.	
J16	not connected	Does not select the integration capacitor suitable for 10 conversions/second on channel 1.	
	connected	Selects the integration capacitor suitable for 10 conversions/second on channel 1.	*
J17	not connected	Does not select the integration capacitor suitable for 20 conversions/second on channel 1.	*
	connected	Selects the integration capacitor suitable for 20 conversions/second on channel 1.	
J18	not connected	Does not select the integration capacitor suitable for 40 conversions/second on channel 1.	*
	connected	Selects the integration capacitor suitable for 40 conversions/second on channel 1.	
J19	not connected	Does not select the integration capacitor suitable for 5 conversions/second on channel 3.	*
	connected	Selects the integration capacitor suitable for 5 conversions/second on channel 3.	
J20	not connected	Does not select the integration capacitor suitable for 10 conversions/second on channel 3.	
	connected	Selects the integration capacitor suitable for 10 conversions/second on channel 3.	*

FIGURE 16: 2 PINS JUMPERS TABLE (PART 2)

JUMPERS	CONNECTION	PURPOSE	DEF.
J21	not connected	Does not select the integration capacitor suitable for 20 conversions/second on channel 3.	*
	connected	Selects the integration capacitor suitable for 20 conversions/second on channel 3.	
J22	not connected	Does not select the integration capacitor suitable for 40 conversions/second on channel 3.	*
	connected	Selects the integration capacitor suitable for 40 conversions/second on channel 3.	
J27	not connected	Does not select input as current input for channel 3.	*
	connected	Selects input as current input for channel 3.	
J28	not connected	Does not select voltage input for channel 3 in the range ±10 Vdc.	*
	connected	Selects voltage input for channel 3 in the range ±10 Vdc.	
J29	not connected	Does not select voltage input for channel 3 in the range ±5 Vdc.	
	connected	Selects voltage input for channel 3 in the range ±5 Vdc.	*
J30	not connected	Does not select voltage input for channel 3 in the range ±3.2768 Vdc.	*
	connected	Selects voltage input for channel 3 in the range ±3.2768 Vdc.	
J31	not connected	Does not select input as current input for channel 2.	*
	connected	Selects input as current input for channel 2.	
J32	not connected	Does not select voltage input for channel 2 in the range ±10 Vdc.	*
	connected	Selects voltage input for channel 2 in the range ±10 Vdc.	
J33	not connected	Does not select voltage input for channel 2 in the range ±5 Vdc.	
	connected	Selects voltage input for channel 2 in the range ±5 Vdc.	*

FIGURE 17: 2 PINS JUMPERS TABLE (PART 3)

JUMPERS	CONNECTION	PURPOSE	DEF.
J34	not connected	Does not select voltage input for channel 2 in the range ±3.2768 Vdc.	*
	connected	Selects voltage input for channel 2 in the range ±3.2768 Vdc.	
J35	not connected	Does not select input as current input for channel 1.	*
	connected	Selects input as current input for channel 1.	
J36	not connected	Does not select voltage input for channel 1 in the range ±10 Vdc.	*
	connected	Selects voltage input for channel 1 in the range ±10 Vdc.	
J37	not connected	Does not select voltage input for channel 1 in the range ±5 Vdc.	
	connected	Selects voltage input for channel 1 in the range ±5 Vdc.	*
J38	not connected	Does not select voltage input for channel 1 in the range ±3.2768 Vdc.	*
	connected	Selects voltage input for channel 1 in the range ±3.2768 Vdc.	
J39	not connected	Does not select input as current input for channel 0.	*
	connected	Selects input as current input for channel 0.	
J40	not connected	Does not select voltage input for channel 0 in the range ±10 Vdc.	*
	connected	Selects voltage input for channel 0 in the range ±10 Vdc.	
J41	not connected	Does not select voltage input for channel 0 in the range ±5 Vdc.	
	connected	Selects voltage input for channel 0 in the range ±5 Vdc.	*
J42	not connected	Does not select voltage input for channel 0 in the range ±3.2768 Vdc.	*
	connected	Selects voltage input for channel 0 in the range ±3.2768 Vdc.	

FIGURE 18: 2 PINS JUMPERS TABLE (PART 4)

JUMPERS	CONNECTION	PURPOSE	DEF.
J43	not connected	Does not connect the board supply ground GND to the external shield.	*
	connected	Connects the board supply ground GND to the external shield.	
J44	not connected	Does not connect the board supply ground GND to pin 5 of CN1	*
	connected	Connects the board supply ground GND to tpin 5 of CN1.	

FIGURE 19: 2 PINS JUMPERS TABLE (PART 5)

3 PINS JUMPERS

JUMPERS	CONNECTION	PURPOSE	DEF.
J23	position 1-2	Connects channel 0 end conversion interrupt generation circuitery to interfacing and addressing section.	
	position 2-3	Does not connect channel 0 end conversion interrupt generation circuitery to interfacing and addressing section.	*
J24	position 1-2	Connects channel 1 end conversion interrupt generation circuitery to interfacing and addressing section.	
	position 2-3	Does not connect channel 1 end conversion interrupt generation circuitery to interfacing and addressing section.	*
J25	position 1-2	Connects channel 2 end conversion interrupt generation circuitery to interfacing and addressing section.	
	position 2-3	Does not connect channel 2 end conversion interrupt generation circuitery to interfacing and addressing section.	*
J26	position 1-2	Connects channel 3 end conversion interrupt generation circuitery to interfacing and addressing section.	
	position 2-3	Does not connect channel 3 end conversion interrupt generation circuitery to interfacing and addressing section.	*

FIGURE 20: 3 PINS JUMPERS TABLE

8 PINS JUMPERS

JUMPERS	CONNECTION	PURPOSE	DEF.
J11	position 1-5	Selects a conversion speed of 5 conversions per second for channel 0.	
	position 2-6	Selects a conversion speed of 10 conversions per second for channel 0.	*
	position 3-7	Selects a conversion speed of 20 conversions per second for channel 0.	
	position 4-8	Selects a conversion speed of 40 conversions per second for channel 0.	
J12	position 1-5	Selects a conversion speed of 5 conversions per second for channel 1.	
	position 2-6	Selects a conversion speed of 10 conversions per second for channel 1.	*
	position 3-7	Selects a conversion speed of 20 conversions per second for channel 1.	
	position 4-8	Selects a conversion speed of 40 conversions per second for channel 1.	
J13	position 1-5	Selects a conversion speed of 5 conversions per second for channel 2.	
	position 2-6	Selects a conversion speed of 10 conversions per second for channel 2.	*
	position 3-7	Selects a conversion speed of 20 conversions per second for channel 2.	
	position 4-8	Selects a conversion speed of 40 conversions per second for channel 2.	
J14	position 1-5	Selects a conversion speed of 5 conversions per second for channel 3.	
	position 2-6	Selects a conversion speed of 10 conversions per second for channel 3.	*
	position 3-7	Selects a conversion speed of 20 conversions per second for channel 3.	
	position 4-8	Selects a conversion speed of 40 conversions per second for channel 3.	

FIGURE 21: 8 PINS JUMPERS TABLE

The "*" used in the following tables, denotes the default connection, or on the other hand the connection set up at the end of testing phase, that is the configuration the User receives.

HARDWARE DESCRIPTION

This chapter provides all the hardware informations needed to use **LAD 415** board. Here the user will find information about I/O card mapping and on board peripheral devices addressing.

BOARD MAPPING

LAD 415 board is mapped into a **4** bytes I/O addressing space, that can be mapped starting from different base addresses according to how the board is configured. This feature allows to use several **LAD 415** cards on the same **ABACO®** BUS, or to install them on a BUS where other peripheral modules are installed obtaining a structure that can be expanded without any difficulty or modifications to the application software.
The base address can be defined through the specific BUS interface circuitry on the board itself; this circuitry uses the eight pins dip switch called **DIP1**, from which it reads the address set by the user. Here follows the corrispondance between dips configuration and address signals.

DIP1.1	->	Address A8
DIP1.2	->	*Not Used*
DIP1.3	->	Address A2
DIP1.4	->	Address A3
DIP1.5	->	Address A4
DIP1.6	->	Address A5
DIP1.7	->	Address A6
DIP1.8	->	Address A7

These dips are driven in complemented logic, this means that if a switch is **ON** generates a **logic zero**, viceversa if a switch is **OFF** generates a **logic one**.

Jumper J1, as previously described, selects the addressing range for card mapping. If the 256 bytes addressing range is selected (addresses from 00H to FFH) then DIP1.1 must be OFF to address the board corrrectly, while if the 512 bytes addressing range is selected (addresses from 00H to 1FFH) then DIP1.1 is used to compose the board address.
Also jumper J2 affects the addressing logic, as described before, and must be set according to the type of **GPC®** control card used. In detail, if the control card is provided with /M1 signal on the **ABACO®** BUS then jumper J2 must be connected, and viceversa.

NOTE
When allocating the mapping address of the boards, plase be careful not to allocate more than one device in the same addressing space (count also the number of bytes occupied by the card). If this condtion will not be respected, a BUS conflict will happen; such conflict will compromise the correct working of the whole system.

As an example, some possible mappings are reported here.

1) Address used to map **LAD 415**: 040H
Control board used: /M1 signal connected

Jumper J1	->	Not Connected
Jumper J2	->	Connected
DIP1.1	->	OFF
DIP1.2	->	*Don't care*
DIP1.3	->	ON
DIP1.4	->	ON
DIP1.5	->	ON
DIP1.6	->	ON
DIP1.7	->	OFF
DIP1.8	->	ON

2) Address used to map **LAD 415**: 184H
Control board used: /M1 signal not connected

Jumper J1	->	Connected
Jumper J2	->	Not Connected
DIP1.1	->	OFF
DIP1.2	->	*Don't care*
DIP1.3	->	OFF
DIP1.4	->	ON
DIP1.5	->	ON
DIP1.6	->	ON
DIP1.7	->	ON
DIP1.8	->	OFF

To easily locate jumpers and dip switches please refer to figures 5, 12 and 14.

INTERNAL REGISTERS ADDRESSING

Indicating the board base address with <**baseaddr**>, that is the address set using dip switch DIP1, as indicated in the previous paragraph **LAD 415** internal registers are addressable as explained in the following table.

REGISTER	ADDRESS	R/W	PURPOSE
PA	<baseaddr>+00	R	PPI 8255 port A data register
PB	<baseaddr>+01	W	PPI 8255 port B data register
PC	<baseaddr>+02	R/W	PPI 8255 port C data register
ST	<baseaddr>+03	W	PPI 8255 control register

FIGURE 22: INTERNAL REGISTERS ADDRESSING TABLE

NOTE
When allocating the mapping address of the boards, plase be careful not to allocate more than one device in the same addressing space (count also the number of bytes occupied by the card). If this condtion will not be respected, a BUS conflict will happen; such conflict will compromise the correct working of the whole system.

PERIPHERAL DEVICES SOFTWARE DESCRIPTION

In the previous paragraph allocation addresses of all the peripherals have been reported, here follows a detailed description of function and meaning of internal registers (please always refer to the peripheral mapping tables to understand completely the following informations). Should the present documentaion be inadequate please refer to the component's manufacturer documentation.
In the following paragraphs the indications **D0÷D7** or **D0÷D15** are used to refer the bits of the byte or word involved in the I/O operations.

PPI 82C55/71055

PPI 82C55 or PPI 71055 is used to manage the control logic of the four A/D converter sections.
Here follows a description of PPI82C55 or PPI 71055 registers (please see "INTERNAL REGISTERS ADDRESSING" for registers addresses) and how they can be programmed.
This external peripheral device is managed through 4 registers: one status register (ST) and three data registers (PA, PB, PC). The data registers are available both for input operation (to obtain signal status) and for output operation (to set signal status). PPI 82C55/71055 can work in three modes:

MODE 0 = it provides two 8 bits bidirectional ports (A,B) and two 4 bits bidirectional ports (C LOW, C HIGH); output signals are latched and input signals are not latched; no handshake signals are provided.

MODE 1 = it provides two 12 bits ports (A+C LOW and B+C HIGH) where ports A and B are used as 8 I/O lines and port C are used as 4 handshake lines. Both inputs and outputs are latched.

MODE 2 = it provides a 13 bits port (A+C3÷7) where port A is used as 8 I/O lines and the 5 bits of port C are used as handshake, and a 11 bits port (B+C0÷2) where port B is used as 8 I/O lines and the 3 bits of port C are used as handshakes. Both inputs and outputs are latched.

The device is programmed writing an 8 bits word in the status register CNT, with the following bits meaning:

CNT = SF M1 M2 A CH M3 B CL
where:

SF		= mode Set Flag: if actived (1) the device is enabled for standard I/O operation
M1	M2	= mode selection:
0	0	= mode 0
0	1	= mode 1
1	X	= mode 2
A		= port A direction: 1=input; 0=output
CH		= port C HIGH direction: 1=input; 0=output
M3		= mode selection: 1=mode 1; 0=mode 0
B		= port B direction: 1=input; 0=output
CL		= port C LOW direction: 1=input; 0=output

After Reset o r power on PPI 82C55/71055 is programmed in mode 0 with all three ports in input; in this way any connection of PPI 82C55/71055 signals can be used without conflict problems.

CONVERSION MANAGEMENT

The whole board software management is performed through a circuitery that allows, easily and efficently, to manage the four A/D converter sections. Such circuitery, called control logic, is based on one PPI 82C55/71055, device that features 24 digital I/O lines and allows to control comfortably each one of the four A/D converter sections separately, minimizing the number of bytes occupied in the addresing space. For a detailed description of such component please refer to paragraph “PPI 82C55/71055” and to manufacturer documentation, while to know the allocation of its registers please refer to paragraph “INTERNAL REGISTERS ADDRESSING”. In simple words, PPI 82C55/71055is a parallel port device featuring 24 TTL I/O signals divided in three ports (Port A, Port B, Port C). Directionality is byte level settable by software. Here follows the correspondace between port signal and their connections to board devices:

PA.0 -> DB0
PA.1 -> DB1
PA.2 -> DB2
PA.3 -> DB3
PA.4 -> DB4
PA.5 -> DB5
PA.6 -> DB6
PA.7 -> DB7

PB.0 -> CONT /DEM CH0
PB.1 -> CONT /DEM CH1
PB.2 -> CONT /DEM CH2
PB.3 -> CONT /DEM CH3
PB.4 -> L /H
PB.5 -> OVR /POL
PB.6 -> /RD
PB.7 -> /WR

PC.0 -> BUSY CH0
PC.1 -> BUSY CH1
PC.2 -> BUSY CH2
PC.3 -> BUSY CH3
PC.4 -> CE0
PC.5 -> CE1
PC.6 -> CE2
PC.7 -> LD1

where:

DB0-DB7= I - Data BUSof the 4 A/D sections

CONT /DEM CHn= O - Selects the conversion modality for n-th A/D converter section:
CONT /DEM=0 -> conversion on request
CONT /DEM=1 -> conversion continuously

L /H=	O	- Selects which conversion byte to put to the data BUS: L /H=0 -> high byte (most significant byte or MSB) L /H=1 -> low byte (least significant byte or LSB)
OVR /POL=	O	- Selects the function of bit DB7 during high byte reading. OVR /POL=0 -> DB7 is the sign of conversion value DB7=0 -> negative tension DB7=1 -> positive tension OVR /POL=1 -> DB7 indicates whether the tension if out of range DB7=0 -> tension in range DB7=1 -> tension out of range
/RD=	O	- Sets the request for a read operation from selected A/D converter.
/WR=	O	- Sets the request for a conversion from selected A/D converter.
BUSY CH n=	I	- The n-th A/D converter section inidcates the conversion end to control and interrput generation logic. BUSY=0 -> conversion finished BUSY=1 -> conversion in progress
CE2 CE1 CE0=	O	- Select which A/D converter section to enable: 0 0 1 -> select section 0 di A/D, activating its /CE 0 1 0 -> select section 1 di A/D, activating its /CE 0 1 1 -> select section 2 di A/D, activating its /CE 1 0 0 -> select section 3 di A/D, activating its /CE
LD1=	O	- Manages the activity LED LD1: LD1=0 -> Turns LED ON LD1=1 -> Turns LED OFF

NOTE

The direction of the above described signals should be considered as output (O) from the control logic so input for the A/D converter sections and, vicecersa, input (I) for the control logic so output from the A/D converter sections.

A conversion operation is made with three phases: conversion start, wait for conversion end, reading of conversion result. The management is performed completely by software setting and reading the A/D converter signals through PPI 82C55/71055ports.

Here follows a detailed description of the several conversion phases, including clear indications of what the control logic must do in each phase.

For greater evidence conversion on request and conversion continuously are described separately, in fact the two conversion modes require different actions.

CONVERSION ON REQUEST

In this modality the conversion starts when the control software performs a conversion start procedure. When the conversion ends the board is ready to let the control card read the conversion value and keeps this status until another conversion is started. The phases of this conversion are:

1R) Initialization of control logic PPI 82C55/71055 in mode 0 with port A as input, port B as output, port C LOW as input and port C HIGH as output;

2R) Setting port B to select as conversion mode on the selected channel the "Conversion on request":

CONT /DEM CH0	= PB.0	= logic 0 if channel 0 in "on request" mode and viceversa
CONT /DEM CH1	= PB.1	= logic 0 if channel 1 in "on request" mode and viceversa
CONT /DEM CH2	= PB.2	= logic 0 if channel 2 in "on request" mode and viceversa
CONT /DEM CH3	= PB.3	= logic 0 if channel 3 in "on request" mode and viceversa
L /H	= PB.4	= Indifferent
OVR /POL	= PB.5	= Indifferent
/RD	= PB.6	= logic 1
/WR	= PB.7	= logic 1

3R) Wait for BUSY signal to disengage, which indicates that it is possible to start the conversion:

Wait for:		
BUSY CH0	= PC.0	= 0 if channel 0 selected, viceversa indifferent
BUSY CH1	= PC.1	= 0 if channel 1 selected, viceversa indifferent
BUSY CH2	= PC.2	= 0 if channel 2 selected, viceversa indifferent
BUSY CH3	= PC.3	= 0 if channel 3 selected, viceversa indifferent
CE2	= PC.4	= Indifferent
CE1	= PC.5	= Indifferent
CE0	= PC.6	= Indifferent
LD1	= PC.7	= Indifferent

4R) Abilitation of A/D converter section where to perform the conversion:

BUSY CH0	= PC.0	= Indifferent
BUSY CH1	= PC.1	= Indifferent
BUSY CH2	= PC.2	= Indifferent
BUSY CH3	= PC.3	= Indifferent

CE2 PC.6	CE1 PC.5	CE0 PC.4	
0	0	1	= Abilitation and conversion for channel 0
0	1	0	= Abilitation and conversion for channel 1
0	1	1	= Abilitation and conversion for channel 2
1	0	0	= Abilitation and conversion for channel 3

LD1	= PC.7	= Indifferent

5R) Conversion starts if /WR if kept to logic level 0 for at least 2 µs:

CONT /DEM CH0	= PB.0	= logic 0 if channel 0 in “on request” mode and viceversa
CONT /DEM CH1	= PB.1	= logic 0 if channel 1 in “on request” mode and viceversa
CONT /DEM CH2	= PB.2	= logic 0 if channel 2 in “on request” mode and viceversa
CONT /DEM CH3	= PB.3	= logic 0 if channel 3 in “on request” mode and viceversa
L /H	= PB.4	= Indifferent
OVR /POL	= PB.5	= Indifferent
/RD	= PB.6	= logic 1
/WR	= PB.7	= logic 0 for at least 2 µs then logic 1

6R) Delay to wait for conversion to start. This phase has a variable duration according to the conversion speed selected, it terminates when signal BUSY becomes a logic 1. No operation must be performed to **LAD 415** in this phase.

Wait for:

BUSY CH0	= PC.0	= logic 1 if channel 0 selected, viceversa indifferent
BUSY CH1	= PC.1	= logic 1 if channel 1 selected, viceversa indifferent
BUSY CH2	= PC.2	= logic 1 if channel 2 selected, viceversa indifferent
BUSY CH3	= PC.3	= logic 1 if channel 3 selected, viceversa indifferent
CE2	= PC.4	= Indifferent
CE1	= PC.5	= Indifferent
CE0	= PC.6	= Indifferent
LD1	= PC.7	= Indifferent

7R) Wait for conversion end for selected channel through polling on signal BUSY or interrupt. In any case it is essential to exit from this phase, and continue with other phases, only when signal BUSY is disengaged.

Wait for:

BUSY CH0	= PC.0	= logic 0 if channel 0 selected, viceversa indifferent
BUSY CH1	= PC.1	= logic 0 if channel 1 selected, viceversa indifferent
BUSY CH2	= PC.2	= logic 0 if channel 2 selected, viceversa indifferent
BUSY CH3	= PC.3	= logic 0 if channel 3 selected, viceversa indifferent
CE2	= PC.4	= Indifferent
CE1	= PC.5	= Indifferent
CE0	= PC.6	= Indifferent
LD1	= PC.7	= Indifferent

8R) Disabling the section that completed the conversion:

BUSY CH0	= PC.0	= Indifferent
BUSY CH1	= PC.1	= Indifferent
BUSY CH2	= PC.2	= Indifferent
BUSY CH3	= PC.3	= Indifferent

CE2	CE1	CE0		
PC.6	PC.5	PC.4		
0	0	0		= No section enabled
LD1			= PC.7	= Indifferent

9R) Re-enabling the A/D converter section that completed the conversion:

BUSY CH0		= PC.0	= Indifferent
BUSY CH1		= PC.1	= Indifferent
BUSY CH2		= PC.2	= Indifferent
BUSY CH3		= PC.3	= Indifferent

CE2	CE1	CE0	
PC.6	PC.5	PC.4	
0	0	1	= Abilitation and conversion on channel 0
0	1	0	= Abilitation and conversion on channel 1
0	1	1	= Abilitation and conversion on channel 2
1	0	0	= Abilitation and conversion on channel 3

LD1	= PC.7	= Indifferent

10R) Setting port B control signals to perform the reading of overrange bit and of the conversion most significant byte:

CONT /DEM CH0	= PB.0	= logic 0 if channel 0 in “on request” mode and viceversa
CONT /DEM CH1	= PB.1	= logic 0 if channel 1 in “on request” mode and viceversa
CONT /DEM CH2	= PB.2	= logic 0 if channel 2 in “on request” mode and viceversa
CONT /DEM CH3	= PB.3	= logic 0 if channel 3 in “on request” mode and viceversa
L /H	= PB.4	= logic 0
OVR /POL	= PB.5	= logic 1
/RD	= PB.6	= logic 0
/WR	= PB.7	= logic 1

11R) Overrange bit reading and high byte (MSB) reading:

DB0	= PA.0	=Bit D8 of conversion value
DB1	= PA.1	=Bit D9 of conversion value
DB2	= PA.2	=Bit D10 of conversion value
DB3	= PA.3	=Bit D11 of conversion value
DB4	= PA.4	=Bit D12 of conversion value
DB5	= PA.5	=Bit D13 of conversion value
DB6	= PA.6	=Bit D14 of conversion value
DB7	= PA.7	=Overrange bit (1 = overrange and viceversa)

12R) Setting the control signals of port B to read polarity bit and conversion most significant byte (MSB):

CONT /DEM CH0	= PB.0	= logic 0 if channel 0 in “on request” mode and viceversa
CONT /DEM CH1	= PB.1	= logic 0 if channel 1 in “on request” mode and viceversa
CONT /DEM CH2	= PB.2	= logic 0 if channel 2 in “on request” mode and viceversa
CONT /DEM CH3	= PB.3	= logic 0 if channel 3 in “on request” mode and viceversa
L /H	= PB.4	= logic 0
OVR /POL	= PB.5	= logic 0
/RD	= PB.6	= logic 0
/WR	= PB.7	= logic 1

13R) Reading polarity bit and high byte (MSB) of conversion value:

DB0	= PA.0	=Bit D8 of conversion value
DB1	= PA.1	=Bit D9 of conversion value
DB2	= PA.2	=Bit D10 of conversion value
DB3	= PA.3	=Bit D11 of conversion value
DB4	= PA.4	=Bit D12 of conversion value
DB5	= PA.5	=Bit D13 of conversion value
DB6	= PA.6	=Bit D14 of conversion value
DB7	= PA.7	=Polarity bit (1 = positive and viceversa)

14R) Setting the control signals of port B to read the conversion least significant byte (LSB):

CONT /DEM CH0	= PB.0	= logic 0 if channel 0 in “on request” mode and viceversa
CONT /DEM CH1	= PB.1	= logic 0 if channel 1 in “on request” mode and viceversa
CONT /DEM CH2	= PB.2	= logic 0 if channel 2 in “on request” mode and viceversa
CONT /DEM CH3	= PB.3	= logic 0 if channel 3 in “on request” mode and viceversa
L /H	= PB.4	= 1 logico
OVR /POL	= PB.5	= 0 logico
/RD	= PB.6	= 0 logico
/WR	= PB.7	= 1 logico

15R) Reading the low byte (LSB):

DB0	= PA.0	=Bit D0 of conversion value
DB1	= PA.1	=Bit D1 of conversion value
DB2	= PA.2	=Bit D2 of conversion value
DB3	= PA.3	=Bit D3 of conversion value
DB4	= PA.4	=Bit D4 of conversion value
DB5	= PA.5	=Bit D5 of conversion value
DB6	= PA.6	=Bit D6 of conversion value
DB7	= PA.7	=Bit D7 of conversion value

16R) Setting the control signals of port B to wait for the conversion start:

CONT /DEM CH0	= PB.0	= logic 0 if channel 0 in “on request” mode and viceversa
CONT /DEM CH1	= PB.1	= logic 0 if channel 1 in “on request” mode and viceversa
CONT /DEM CH2	= PB.2	= logic 0 if channel 2 in “on request” mode and viceversa
CONT /DEM CH3	= PB.3	= logic 0 if channel 3 in “on request” mode and viceversa
L /H	= PB.4	= Indifferent
OVR /POL	= PB.5	= Indifferent
/RD	= PB.6	= logic 1
/WR	= PB.7	= logic 1

17R) Disabilitation of A/D section used:

BUSY CH0	= PC.0	= Indifferent
BUSY CH1	= PC.1	= Indifferent
BUSY CH2	= PC.2	= Indifferent
BUSY CH3	= PC.3	= Indifferent

CE2	CE1	CE0	
PC.6	PC.5	PC.4	
0	0	0	= No section enabled

LD1 = PC.7 = Indifferent

18R) To repeat the conversion from the same channel, jump back to phase 4R. To perform another conversion from a different channel, jump back to phase 2R.

The description reported in the previous 18 phases is referred to one only A/D converter section. To manage more than one A/D converter the phases to perform are the same but must be executed sequentially on all the channels.
In the following pages there is a flow chart that shows in a simple and straight way the **LAD 415** utilization in modality “Conversion on request”.
The operation is referred to channel 0.

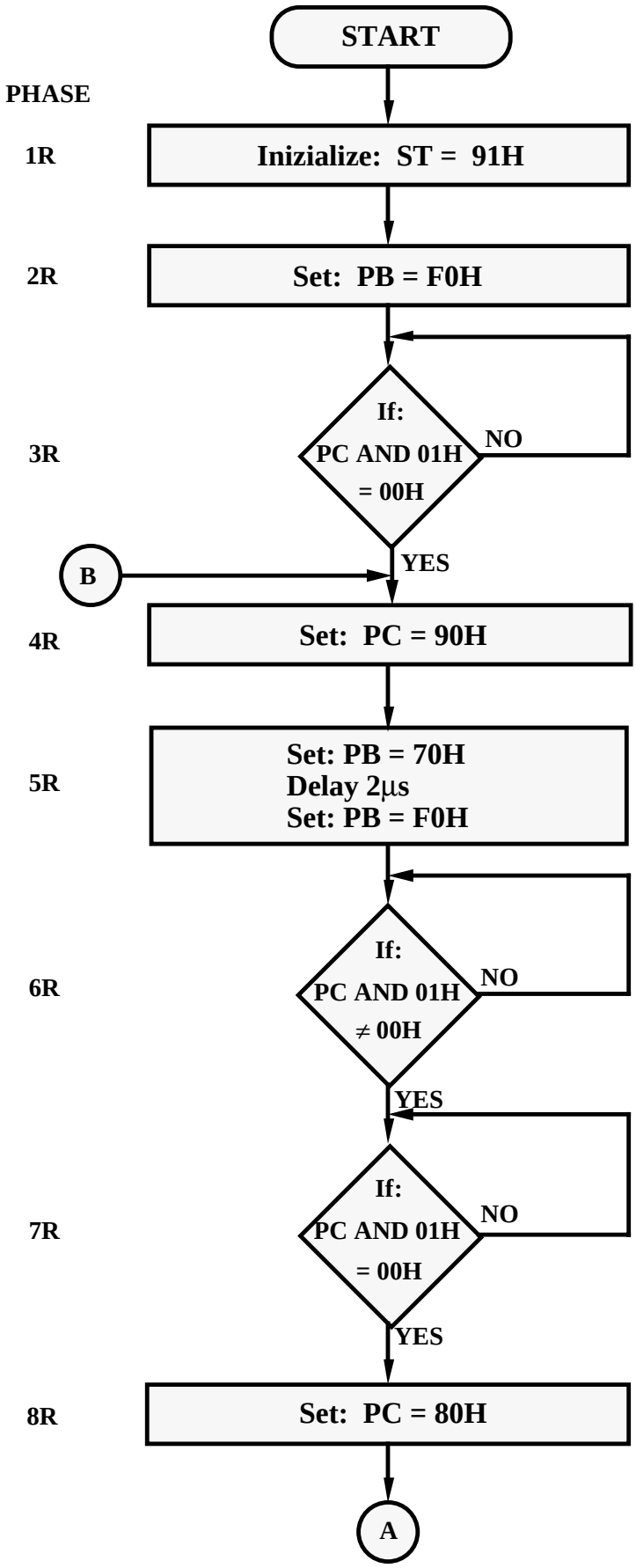

FIGURE 22: CONVERSION ON REQUEST FLOW CHART (PART 1)

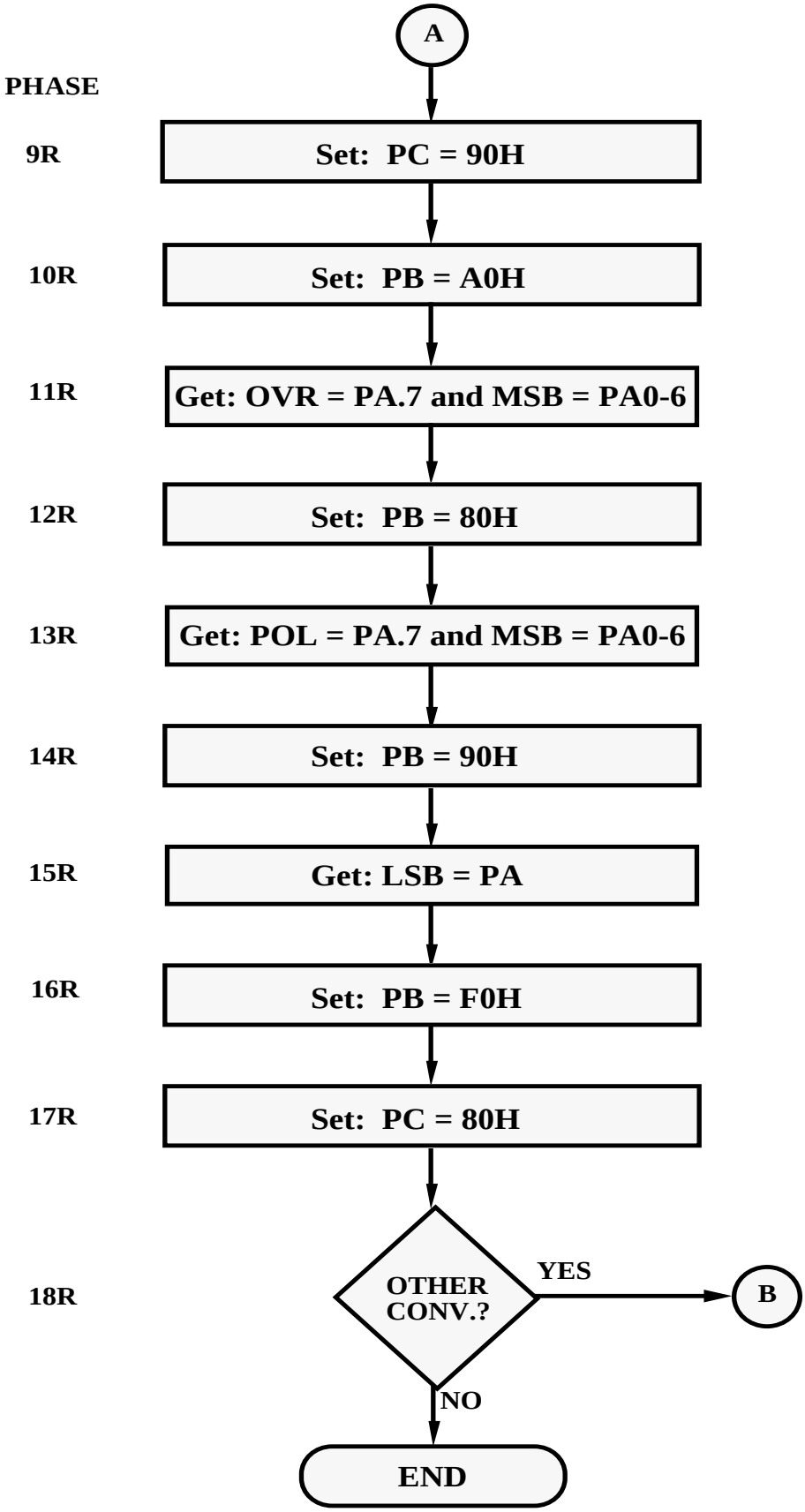

FIGURE 23: CONVERSION ON REQUEST FLOW CHART (PART 2)

CONVERSION CONTINUOUSLY

In this modality the board works continuously and in autonomy: the conversion starts when the control software gives a start command, when the conversion ends the board performs a temporized phase to let the control board read the conversion value and restarts for a new conversion without any command to be given by the control card. The phases of this conversion are:

1C) Initialization of control logic PPI 82C55/71055 in mode 0 with port A as input, port B as output, port C LOW as input and port C HIGH as output;

2C) Setting port B to select as conversion mode the "Conversion continuously":

CONT /DEM CH0	= PB.0	= logic 1 if channel 0 in "continuously" mode and viceversa
CONT /DEM CH1	= PB.1	= logic 1 if channel 1 in "continuously" mode and viceversa
CONT /DEM CH2	= PB.2	= logic 1 if channel 2 in "continuously" mode and viceversa
CONT /DEM CH3	= PB.3	= logic 1 if channel 3 in "continuously" mode and viceversa
L /H	= PB.4	= Indifferent
OVR /POL	= PB.5	= Indifferent
/RD	= PB.6	= logic 1
/WR	= PB.7	= logic 1

3C) Abilitation of A/D converter section where to perform the conversion:

BUSY CH0			= PC.0	= Indifferent
BUSY CH1			= PC.1	= Indifferent
BUSY CH2			= PC.2	= Indifferent
BUSY CH3			= PC.3	= Indifferent
CE2	CE1	CE0		
PC.6	PC.5	PC.4		
0	0	1		= Abilitation and conversion for channel 0
0	1	0		= Abilitation and conversion for channel 1
0	1	1		= Abilitation and conversion for channel 2
1	0	0		= Abilitation and conversion for channel 3
LD1			= PC.7	= Indifferent

4C) Wait for conversion end for selected channel through polling on signal BUSY or interrupt. In any case it is essential to exit from this phase, and continue with other phases, only when signal BUSY is disengaged.

Wait for:

BUSY CH0	= PC.0	= logic 0 if channel 0 selected, viceversa indifferent
BUSY CH1	= PC.1	= logic 0 if channel 1 selected, viceversa indifferent
BUSY CH2	= PC.2	= logic 0 if channel 2 selected, viceversa indifferent
BUSY CH3	= PC.3	= logic 0 if channel 3 selected, viceversa indifferent

CE2	= PC.4	= Indifferent
CE1	= PC.5	= Indifferent
CE0	= PC.6	= Indifferent
LD1	= PC.7	= Indifferent

5C) Setting port B to read the polarity bit and conversion most significant byte (MSB):

CONT /DEM CH0	= PB.0	= logic 1 if channel 0 in “continuously” mode and viceversa
CONT /DEM CH1	= PB.1	= logic 1 if channel 1 in “continuously” mode and viceversa
CONT /DEM CH2	= PB.2	= logic 1 if channel 2 in “continuously” mode and viceversa
CONT /DEM CH3	= PB.3	= logic 1 if channel 3 in “continuously” mode and viceversa
L /H	= PB.4	= Indifferent
OVR /POL	= PB.5	= Indifferent
/RD	= PB.6	= logic 0
/WR	= PB.7	= logic 1

6C) Reading polarity bit and conversion high byte (MSB) :

DB0	= PA.0	=Bit D8 of conversion value
DB1	= PA.1	=Bit D9 of conversion value
DB2	= PA.2	=Bit D10 of conversion value
DB3	= PA.3	=Bit D11 of conversion value
DB4	= PA.4	=Bit D12 of conversion value
DB5	= PA.5	=Bit D13 of conversion value
DB6	= PA.6	=Bit D14 of conversion value
DB7	= PA.7	=Polarity bit (1 = positive and viceversa)

7C) Disabling /RD signal:

CONT /DEM CH0	= PB.0	= logic 1 if channel 0 in “continuously” mode and viceversa
CONT /DEM CH1	= PB.1	= logic 1 if channel 1 in “continuously” mode and viceversa
CONT /DEM CH2	= PB.2	= logic 1 if channel 2 in “continuously” mode and viceversa
CONT /DEM CH3	= PB.3	= logic 1 if channel 3 in “continuously” mode and viceversa
L /H	= PB.4	= Indifferent
OVR /POL	= PB.5	= Indifferent
/RD	= PB.6	= logic 1
/WR	= PB.7	= logic 1

8C) Setting port B to read the conversion least significant byte (LSB):

CONT /DEM CH0	= PB.0	= logic 1 if channel 0 in “continuously” mode and viceversa
CONT /DEM CH1	= PB.1	= logic 1 if channel 1 in “continuously” mode and viceversa
CONT /DEM CH2	= PB.2	= logic 1 if channel 2 in “continuously” mode and viceversa
CONT /DEM CH3	= PB.3	= logic 1 if channel 3 in “continuously” mode and viceversa
L /H	= PB.4	= Indifferent
OVR /POL	= PB.5	= Indifferent
/RD	= PB.6	= logic 0
/WR	= PB.7	= logic 1

9C) Reading conversion low byte (LSB) :

DB0	= PA.0	=Bit D0 of conversion value
DB1	= PA.1	=Bit D1 of conversion value
DB2	= PA.2	=Bit D2 of conversion value
DB3	= PA.3	=Bit D3 of conversion value
DB4	= PA.4	=Bit D4 of conversion value
DB5	= PA.5	=Bit D5 of conversion value
DB6	= PA.6	=Bit D6 of conversion value
DB7	= PA.7	=Bit D7 of conversion value

10C) Disabling /RD signal:

CONT /DEM CH0	= PB.0	= logic 1 if channel 0 in “continuously” mode and viceversa
CONT /DEM CH1	= PB.1	= logic 1 if channel 1 in “continuously” mode and viceversa
CONT /DEM CH2	= PB.2	= logic 1 if channel 2 in “continuously” mode and viceversa
CONT /DEM CH3	= PB.3	= logic 1 if channel 3 in “continuously” mode and viceversa
L /H	= PB.4	= Indifferent
OVR /POL	= PB.5	= Indifferent
/RD	= PB.6	= logic 1
/WR	= PB.7	= logic 1

11C) Setting port B to read the overrange bit and conversion most significant byte (MSB):

CONT /DEM CH0	= PB.0	= logic 1 if channel 0 in “continuously” mode and viceversa
CONT /DEM CH1	= PB.1	= logic 1 if channel 1 in “continuously” mode and viceversa
CONT /DEM CH2	= PB.2	= logic 1 if channel 2 in “continuously” mode and viceversa
CONT /DEM CH3	= PB.3	= logic 1 if channel 3 in “continuously” mode and viceversa
L /H	= PB.4	= Indifferent
OVR /POL	= PB.5	= Indifferent
/RD	= PB.6	= logic 0
/WR	= PB.7	= logic 1

12C) Reading overrange bit and conversion high byte (MSB) :

DB0	= PA.0	=Bit D8 of conversion value
DB1	= PA.1	=Bit D9 of conversion value
DB2	= PA.2	=Bit D10 of conversion value
DB3	= PA.3	=Bit D11 of conversion value
DB4	= PA.4	=Bit D12 of conversion value
DB5	= PA.5	=Bit D13 of conversion value
DB6	= PA.6	=Bit D14 of conversion value
DB7	= PA.7	=Overrange bit (1 = overrange and viceversa)

13C) Disabling /RD signal:

CONT /DEM CH0	= PB.0	= logic 1 if channel 0 in “continuously” mode and viceversa
CONT /DEM CH1	= PB.1	= logic 1 if channel 1 in “continuously” mode and viceversa
CONT /DEM CH2	= PB.2	= logic 1 if channel 2 in “continuously” mode and viceversa
CONT /DEM CH3	= PB.3	= logic 1 if channel 3 in “continuously” mode and viceversa
L /H	= PB.4	= Indifferent
OVR /POL	= PB.5	= Indifferent
/RD	= PB.6	= logic 1
/WR	= PB.7	= logic 1

14C) To manage another conversion jump to next phase, while to quit the “conversion continuously” mode jump to phase 16C.

15C) Wait for next conversion to start for selected channel through polling on signal BUSY. Once exited from this phase, jump back to phase 4C.

Wait for:

BUSY CH0	= PC.0	= logic 1 if channel 0 selected, viceversa indifferent
BUSY CH1	= PC.1	= logic 1 if channel 1 selected, viceversa indifferent
BUSY CH2	= PC.2	= logic 1 if channel 2 selected, viceversa indifferent
BUSY CH3	= PC.3	= logic 1 if channel 3 selected, viceversa indifferent
CE2	= PC.4	= Indifferent
CE1	= PC.5	= Indifferent
CE0	= PC.6	= Indifferent
LD1	= PC.7	= Indifferent

16C) Setting the control signals of port B to disable “Conversion continuously mode”:

CONT /DEM CH0	= PB.0	= logic 0 if channel 0 in “on request” mode and viceversa
CONT /DEM CH1	= PB.1	= logic 0 if channel 1 in “on request” mode and viceversa
CONT /DEM CH2	= PB.2	= logic 0 if channel 2 in “on request” mode and viceversa
CONT /DEM CH3	= PB.3	= logic 0 if channel 3 in “on request” mode and viceversa
L /H	= PB.4	= Indifferent
OVR /POL	= PB.5	= Indifferent
/RD	= PB.6	= logic 1
/WR	= PB.7	= logic 1

17C) Disabilitation of A/D section used:

BUSY CH0	= PC.0	= Indifferent
BUSY CH1	= PC.1	= Indifferent
BUSY CH2	= PC.2	= Indifferent
BUSY CH3	= PC.3	= Indifferent

CE2	CE1	CE0	
PC.6	PC.5	PC.4	
0	0	0	= No section enabled

LD1	= PC.7	= Indifferent

The description reported in the previous 17 phases is referred to one only A/D converter section. To manage more than one A/D converter the phases to perform are the same but must be executed sequentially on all the channels.
In the following pages there is a flow chart that shows in a simple and straight way the **LAD 415** utilization in modality “Conversion continuously”.
The operation is referred to channel 2.

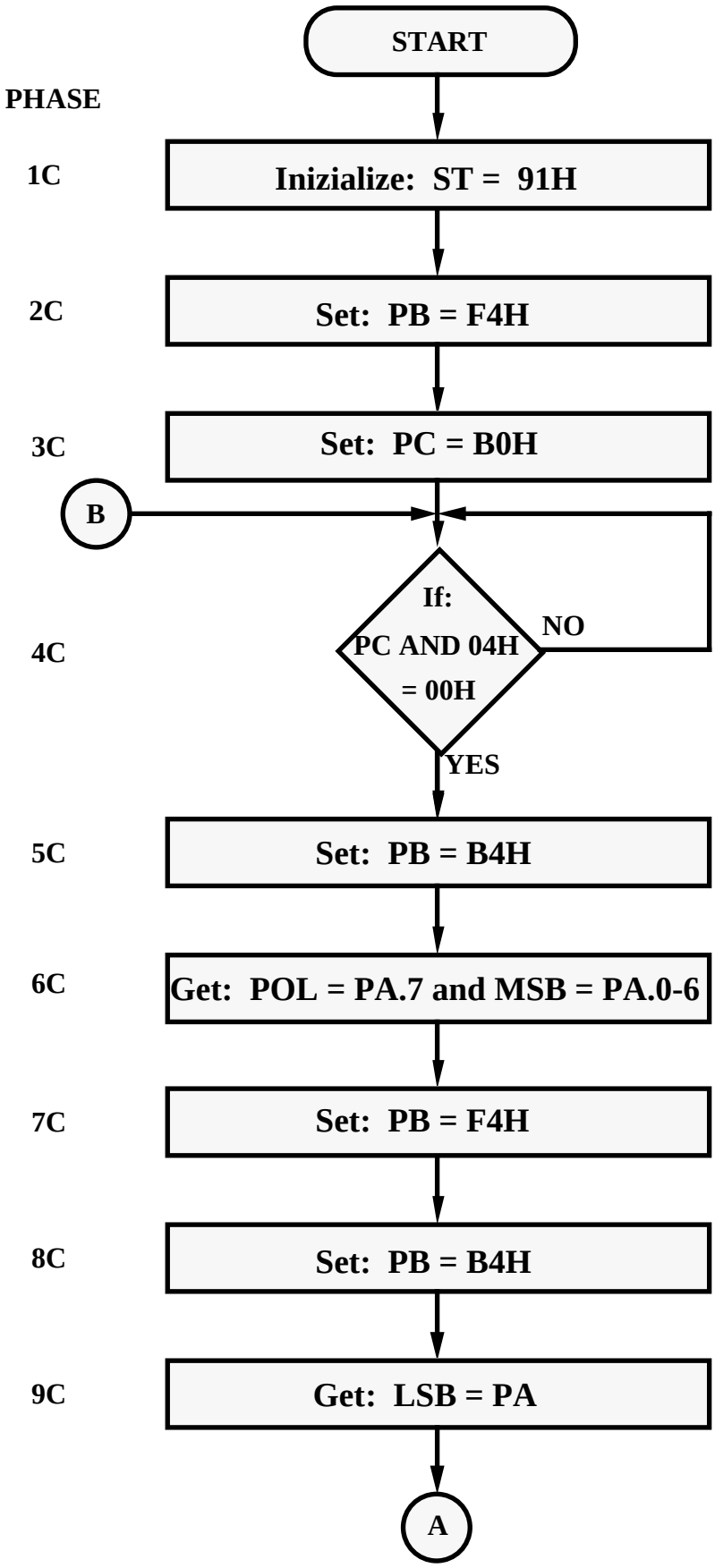

FIGURE 24: CONVERSION CONTINUOUSLY FLOW CHART (PART 1)

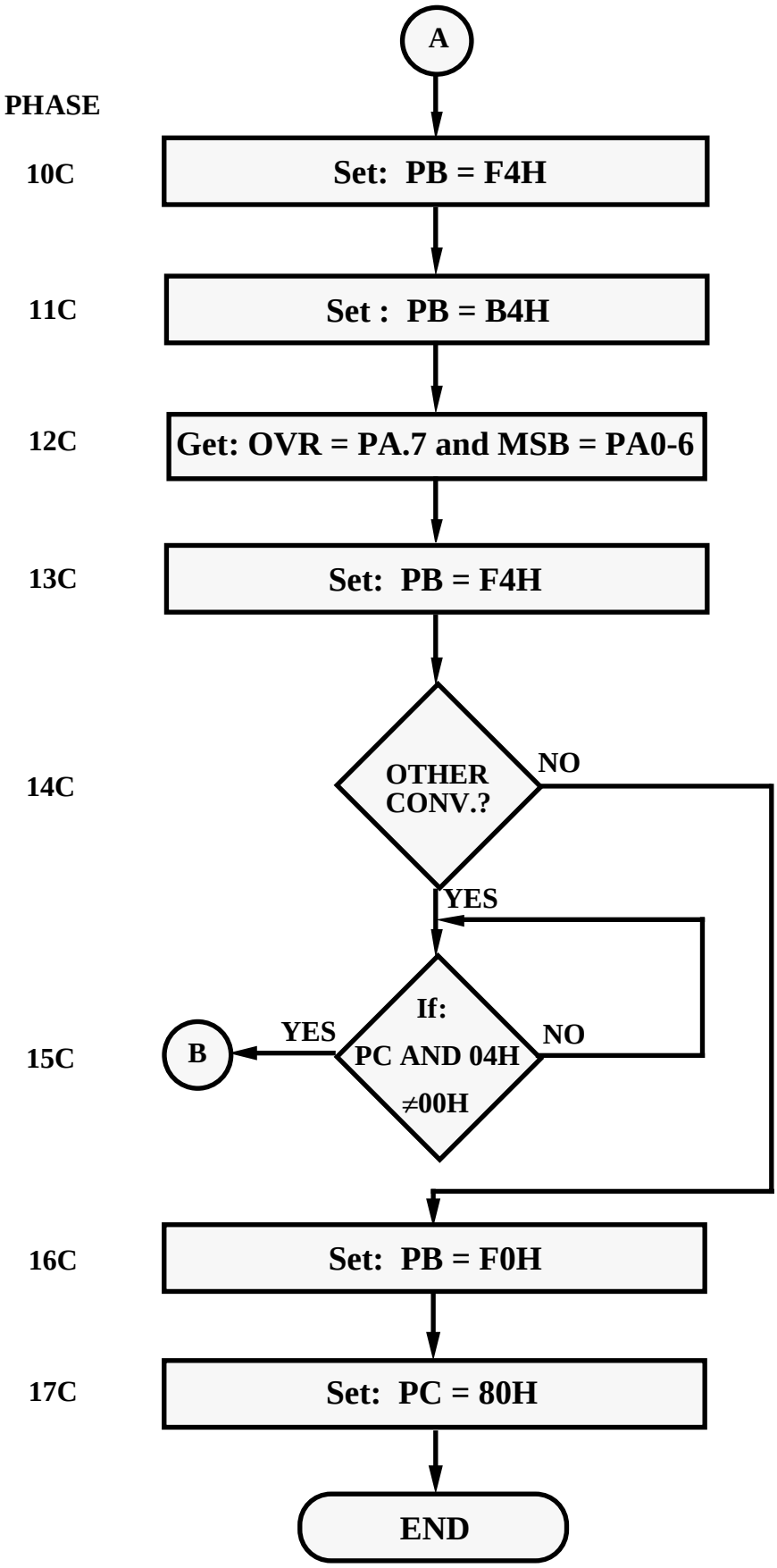

FIGURE 25: CONVERSION CONTINUOUSLY FLOW CHART (PART 2)

ACTIVITY LED

Management of the activity LED installed on **LAD 415** is performed through a write to register PC:

PC.7 -> set LD1 status

Performing a write operation the status is set as specified in the following correspondance:

Bit at logic 0 -> Activity LED ON
Bit at logic 1 -> Activity LED OFF

Register PC also sets the chip select signals for A/D converter sections 0, 1 and 2, so writing to it affects also their status. Please refer to previous paragraph for more information.

CONFIGURATION INPUTS

LAD 415 is provided with five jumpers with the specific purpose to set the connection modalities for /M1 and /INT signals as in the following correspondance:

J2 -> Connects or disconnects signal /M1
J23 -> Connects or disconnects section 0 interrupt signal
J24 -> Connects or disconnects section 1 interrupt signal
J25 -> Connects or disconnects section 2 interrupt signal
J26 -> Connects or disconnects section 3 interrupt signal

For further informations please refer to chapter “JUMPERS” and to figures 15 and 20.

EXTERNAL CARDS

LAD 415 can be connected to a wide range of block modules and operator interface system produced by **grifo®**, or to many system of other companies.The on board resources can be expanded with a simple connection to the numerous peripheral **grifo®** boards,both intelligent and not, thanks to its standard **ABACO®** BUS connector. Even cards with **ABACO®** I/O BUS can be connected, by using the proper mother boards.
Hereunder some of these cards are briefly described; ask the detailed information directly to **grifo®**, if required.

MB3 01-MB4 01-MB8 01
Mother Board 3, 4, 8 slots
Motherboard featuring 3, 4 or 8 slots of **ABACO®** industrial BUS; pitch 4 TE; standard power supply connectors; LEDs for visual feed-back of power supply; holes for rack docking.

SPB 04-SPB 08
Switch Power BUS 4-8 slots
Motherboard featuring 4-8 slots of **ABACO®** industrial BUS; pitch 4 TE; standard power supply connectors; termination resistances; connector type F for **SPC xxx** supply ; holes for rack docking.

ABB 03
ABACO® Block BUS 3 slots
3 slots **ABACO®** mother board; 4 TE pitch connectors; **ABACO®** I/O BUS connector; screw terminal for power supply; connection for DIN C type and Ω rails.

ABB 05
ABACO® Block BUS 5 slots
5 slots **ABACO®** mother board with power supply. Double power supply built in; 5Vdc 2,5A section for powering the on board logic; second section at 24Vdc 400mA galvanically coupled, for the optocoupled input lines. Auxiliary connector for **ABACO®** I/O BUS. Connection for DIN Ω rails.

SPC 03.5S
Switch Power Card +5 Vdc
Europe format switching power supply capable to provide +5 Vdc to a load of 4 A; input voltage 12÷24 Vac; power-failure; connector for back-up battery; standard connector for mother board **SPB 0x**.

SPC 512
Switch Power Card +5 Vdc +12 Vdc
Europe format switching power supply capable to provide +5 Vdc 5A and +12 Vdc 2.5 A; input voltage 12÷24 Vac; power-failure; connector for back-up battery; standard connector for mother board **SPB 0x**.

FBC 20-120
Flat Block Contact 20 vie
Interface for 2 or 1 mounting cable connectors (low profile 20 pins male) and quick release screw terminal connectors; Plastic mount for rails DIN 46277-1 and 3.

GPC® 51

General Purpose Controller fam. 51

Microprocessor family 51 INTEL including the masked BASIC chip; the board features: 16 I/O TTL lines; dip switch; 3 timer/counter; RS 232; 4 A/D converter signals resolution 11 bit; buzzer; on board EPROM programmer; RTC and 32K SRAM with Lithium battery back up; controlloer for display and keyboard.

GPC® 188F

General Purpose Controller 80C188

80C188 µP 20MHz; 1 RS 232 line; 1 RS 232, RS 422-485 or Current Loop line; 24 TTL I/O lines; 1M EPROM or 512K FLASH; 1M RAM Lithium battery backed; 8K serial EEPROM; RTC; Watch Dog; 8 Dip switch; 3 Timer Counter; 8 13 bit A/D lines; Power failure; activity LEDs; single power supply +5Vdc.

GPC® 15A

General Purpose Controller 84C15

Full CMOS card, 10÷20 MHz 84C15 CPU; 512K EPROM or FLASH; 128K RAM; 8K RAM and RTC backed; 8K serial EEPROM; 1 RS 232 line; 1 RS 232 line or RS 422-485 or Current Loop line; 32 or 40 TTL I/O lines; CTC; Watch dog; 2 Dip switches; Buzzer.

GPC® 150

General Purpose Controller 84C15

Microprocessor Z80 at 16 MHz; implementation completely CMOS; 512K EPROM or FLASH; 512K SRAM; RTC; Back-Up through external Lithium battery; 4M serail FLASH ; 1 serial line RS 232 plus 1 RS 232 or RS 422-485 or current loop; 40 I/O TTL; 2 timer/counter; 2 watch dog; dip switch; EEPROM; A/D converter with resolution 12 bit; activity LED.

GPC® 15R

General Purpose Controller 84C15

84C15 µP, 10÷16 MHz; 1 RS 232 line; 1 RS 232 or RS 422-485 or C. L. line; 16÷24 TTL I/O lines; 16 Opto-in; 8 Relays; 4 Opto Coupled Timers Counters; 512K EPROM or FLASH; 512K RAM and RTC backed; 8K serial EEPROM; 8K Backed RAM modul; Buzzer; 1 Activity LED; Watch dog; 4÷12 readable DIPs; LCD Interface.

GPC® 323

General Purpose Controller 51 family

80C32 µP, 14 MHz; Full CMOS; 1 RS 232 line (software); 1 RS 232 or RS 422-485 or Current Loop line; 24 TTL I/O lines; 11 A/D 12 bits lines; 3 Timers Counters; 64K EPROM; 64K RAM; 32K RAM and RTC backed; 32K DIL EEPROM; 8K serial EEPROM; Buzzer; 2 Activity LED; Watch dog; 5 readable DIPs; LCD Interface.

GPC® 553

General Purpose Controller 80C552

80C552 µP, 22÷33 MHz; 1 RS 232 line (software); 1 RS 232 or RS 422-485 or Current Loop line; 16 TTL I/O lines; 8 A/D 10 bits lines; 3 Timers Counters; 64K EPROM; 64K RAM; 32K RAM and RTC backed; 32K DIL EEPROM; 8K serial EEPROM; 2 PWM lines; 1 Activity LED; Watch dog; 5 readable DIPs; LCD Interface.

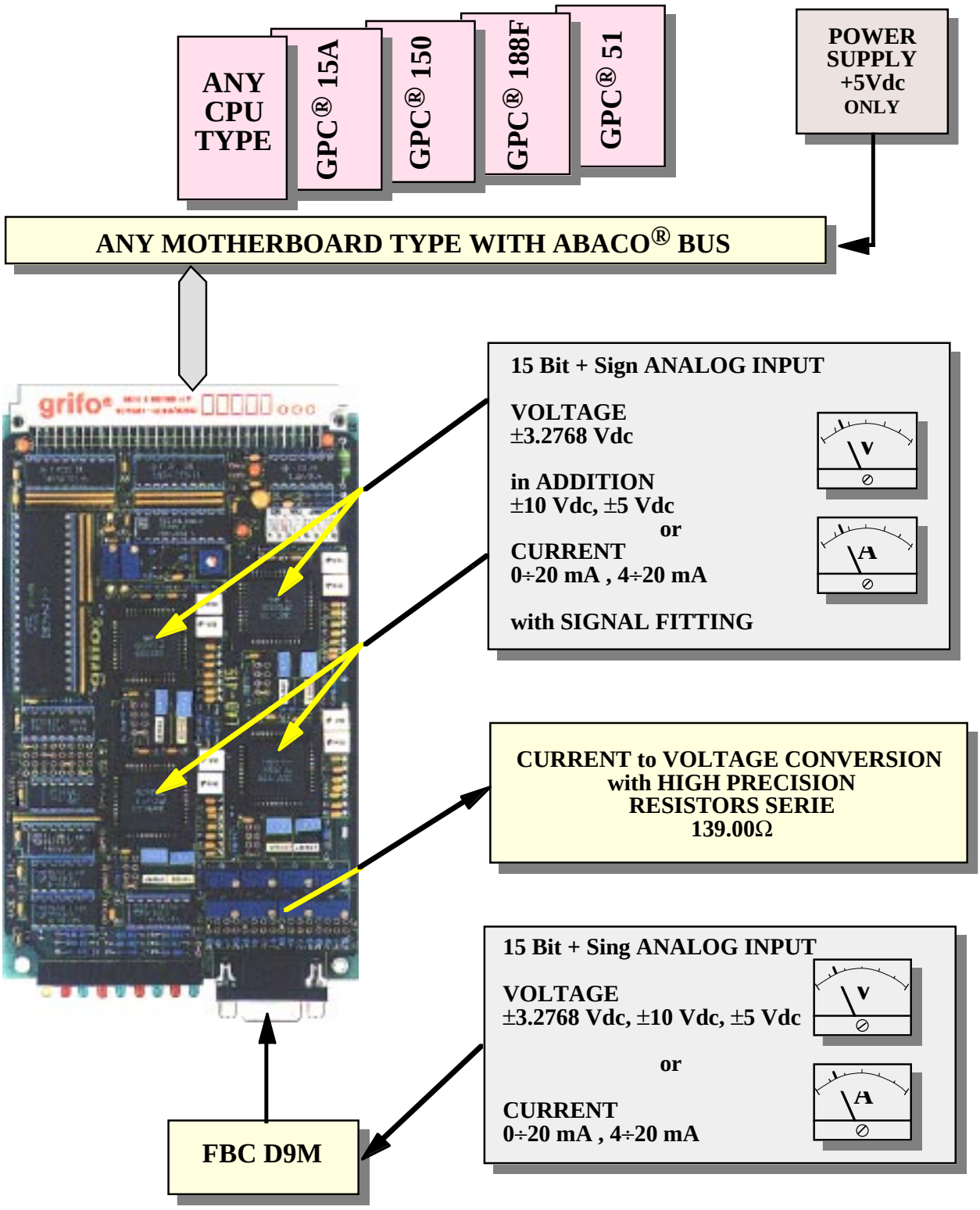

FIGURE 26: POSSIBLE CONNECTIONS DIAGRAM

GPC® 153

General Purpose Controller Z80

84C15 µP, 10÷16 MHz; Full CMOS; 1 RS 232 line; 1 RS 232 or RS 422-485 or Current Loop line; 16 TTL I/O lines; 8 A/D 12 bits lines; 2÷4 Timers Counters; 512K EPROM or FLASH; 512K RAM and RTC backed; 8K serial EEPROM; Buzzer; 1 Activity LED; Watch dog; 8 readable DIPs; LCD Interface.

GPC® 183

General Purpose Controller Z180

Z180 µP, 10÷16 MHz; Full CMOS; 1 RS 232 line; 1 RS 232 or RS 422-485 or Current Loop line; 24 TTL I/O lines; 11 A/D 12 bits lines; 2 Timers Counters; 512K EPROM or FLASH; 512K RAM and RTC backed; 8K serial EEPROM; Buzzer; 2 Activity LED; Watch dog; 4 readable DIPs; LCD Interface.

GPC® 324/D

"4" Type General Purpose Controller 80C32/320

80C32 or 80C320 µP, 14÷22 MHz; Full CMOS; 1 RS 232 line; 1 RS 232 or RS 422-485 or Current Loop line; 4÷16 TTL I/O lines; 3 Timers Counters; 64K EPROM; 64K RAM; 32K RAM backed; 32K DIL E2; 8K serial EEPROM; Watch dog; 1 readable DIP; LCD Interface; Abaco® I/O BUS; 5Vdc Power supply; Size: 100x50 mm.

GPC® 554

General Purpose Controller 80C552

Microprocessor 80C552 at 22 MHz; implementation completely CMOS; 32K EPROM; 32 K SRAM; 32 K EEPROM or SRAM; EEPROM; 2 RS 232 serial lines; 16 I/O TTL; 2 PWM lines; 16 bits Timer/Counter; Watch Dog; 6 signals A/D converter with resolution 10 bit; interface for **ABACO®** I/O BUS.

GPC® 154

"4" Type General Purpose Controller Z80

84C15 µP, 10÷16 MHz; Full CMOS; 1 RS 232 line; 1 RS 232 or RS 422-485 line; 16 TTL I/O lines; 2÷4 Timers Counters; 512K EPROM or FLASH; 512K RAM and RTC backed; 8K serial EEPROM; Watch dog; 2 readable DIPs; LCD Interface; Abaco® I/O BUS; 5Vdc Power supply; Size: 100x50 mm.

GPC® 884

General Purpose Controller Am188ES

Microprocessor AMD Am188ES up to 40 MHz16 bits; implementation completely CMOS; serie 4 format; 512K EPROM or FLASH; 512K SRAM backed with Lithium battery; RTC; 1 RS 232 serial line + 1 RS 232 or RS 422-485 or current loop; 16 I/O TTL; 3 timer/counter; watch dog; EEPROM; 11 signals A/D converter with 12 bit resolution; interface for **ABACO®** I/O BUS.

GPC® 114

General Purpose Controller 68HC11

Microprocessor 68HC11A1 at 8 MHz; implementation completely CMOS; serie 4 format; 32K EPROM; 32K SRAM backed with Lithium battery; 32K EPROM, SRAM, EEPROM; RTC; 1 serial line RS 232 or RS 422-485; 10 I/O TTL; 3 timer/counter; watch dog; 8 signals A/D converter with resolution 8 bit; 1 asunchronous serial line; extremly low power consumption; interface for **ABACO®** I/O BUS.

BIBLIOGRAPHY

Here follows a list of manuls thst can be a source of further informations about the devices installed on **LAD 415**.

Manual TEXAS INSTRUMENTS:	*The TTL Data Book - SN54/74 Families*
Manual TEXAS INSTRUMENTS:	*Linear Circuits - Volume 3*
Manual NEC:	*Microprocessors and Peripherals - Volume 3*
Data book TELCOM:	*Mixed Signal - Power Management - Smart Sensors*
Manual NATIONAL SEMICONDUCTOR:	*DataBook - Linear 2*

Please connect to the manifactures Web sites to get the latest version of all manuals and data sheets.

APPENDIX A: ALPHABETICAL INDEX

SYMBOLS

A

B

C