

LAD 13

Low cost Analog to Digital 12 bits

TECHNICAL MANUAL

Eurocard format size 100x160 mm; interface to **ABACO**[®] industrial BUS; 16 analog to digital successive approximation input lines based on DAS MAX 197 with resolution 12 bits or 11 bits+sign; conversion time 6 μ sec per channel; signal input range software selectable amongst 0÷5 Vdc, 0÷10 Vdc, \pm 5 Vdc, \pm 10 Vdc, 0÷20 mA or 4÷20 mA; 5 MHz Bandwidth Track-Hold; 100 Ksps Sampling-Rate independent for each section; Fault-Protected Input Multiplexer (\pm 16.5 V); 2 activity LEDs on the front panel; 2 LEDs to signal that /INT and conversion end occurred on the front panel; circuitry to generate interrupts on **ABACO**[®] BUS; 8 bits data BUS management; 2 low profile connectors, featuring standard 20 pins pin-out, for analog inputs; direct interfacement to **FBC** field modules; unique power supply +5Vdc

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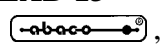
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LAD 13

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SYMBOLS DESCRIPTION

In the manual could appear the following symbols:




Attention: Generic danger



Attention: High voltage

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INTRODUCTION

The use of these devices has turned - IN EXCLUSIVE WAY - to specialized personnel.

The purpose of this handbook is to give the necessary information to the cognizant and sure use of the products. They are the result of a continual and systematic elaboration of data and technical tests saved and validated from the manufacturer, related to the inside modes of certainty and quality of the information.

The reported data are destined- IN EXCLUSIVE WAY- to specialized users, that can interact with the devices in safety conditions for the persons, for the machine and for the environment, impersonating an elementary diagnostic of breakdowns and of malfunction conditions by performing simple functional verify operations , in the height respect of the actual safety and health norms.

The informations for the installation, the assemblage, the dismantlement, the handling, the adjustment, the reparation and the contingent accessories, devices etc. installation are destined - and then executable - always and in exclusive way from specialized warned and educated personnel, or directly from the TECHNICAL AUTHORIZED ASSISTANCE, in the height respect of the manufacturer recommendations and the actual safety and health norms.

The devices can't be used outside a box. The user must always insert the cards in a container that respect the actual safety normative. The protection of this container is not threshold to the only atmospheric agents, but specially to mechanic, electric, magnetic, etc. ones.

To be on good terms with the products, is necessary guarantee legibility and conservation of the manual, also for future references. In case of deterioration or more easily for technical updates, consult the AUTHORIZED TECHNICAL ASSISTANCE directly.

To prevent problems during card utilization, it is a good practice to read carefully all the informations of this manual. After this reading, the user can use the general index and the alphabetical index, respectly at the begining and at the end of the manual, to find information in a faster and more easy way.

CARD VERSION

The present handbook is reported to the **LAD 13** card release **060296** and later. The validity of the bring informations is subordinate to the number of the card release. The user must always verify the correct correspondence among the two denotations. On the card the release number is present in more points both board printed diagram (serigraph) and printed circuit (for example near trimmer RV3 both on the component side and on the solder side).

GENERAL INFORMATION

LAD 13 (Low cost Analog to Digital 12 bits) card is a powerful Eurocard format card, provided with **ABACO**® industrial BUS interface. This card belongs to the analog peripherals units list and, in specific, its purpose is to provide sixteen Analog to Digital conversion lines.

The analog signals are connected through two 20 pins low profile standard connectors. Two independent A/D Converter circuitries, based on as many **DAS (Data Acquisition System) MultiRange MAX197**, warrant a complete separation of the signals. A/D circuitry features **12 bits** of resolution (or **11 bits+sign**), **6 µsec** conversion time.

Each analog input line is provided with an efficient protection circuitry against noise coming from external world; the signal to be acquired can be configured as voltage (**0÷5 Vdc, 0÷10 Vdc, ±5 Vdc, ±10 Vdc**) or current (**0÷20 mA or 4÷20 mA**) installing on the board an opportune module manufactured by **grifo**® (code **.8420**) for current-to-voltage conversion. To easily install such modules two sockets are present.

The 20 pins output connector is **ABACO**® standard compliant, this allows an immediate interfacing to several modules for the field, like **FBC xxx**, that untangle the signals from the flat cable to comfortable quick release screw terminal connectors. Remarkable are **FBC 20** and **FBC 120** for the specific use with this card.

LAD 13 card can be driven through any CPU board in the **ABACO**® listing and takes as low as 4 contiguous bytes in the addressing space.

A remarkable feature of **LAD 13** is the capability to be Multi-Range and to allows the acquisition of input signal with several different characteristics by a simple software setting. On the front of the board two software manageable LEDs are available, in addition there are two more LEDs that signal the end of a conversion and the generation of an **interrupt**.

LAD 13 is the ideal component for all the applications where high conversion speed, good precision, several lines and low costs are required. It is in fact more convenient to install more cards to increase the number of signals to acquire than installing multiplexing cards that degrade the conversion quality and decrease the sampling rate, vanificating the investment for an high speed card.

Overall features of **LAD 13** are as follows:

- Eurocard format size 100x160 mm; interface to **ABACO**® industrial BUS
- 16 analog to digital successive approximation input lines based on **DAS MAX 197** with resolution **12 bits** or **11 bits+sign**
- Conversion time 6 µsec per channel; signal input range software selectable amongst 0÷5 Vdc, 0÷10 Vdc, ±5 Vdc, ±10 Vdc, 0÷20 mA or 4÷20 mA
- **5 MHz Bandwidth** Track-Hold
- **100 Ksps** Sampling-Rate independent for each section
- Fault-Protected Input Multiplexer (±16.5 V)
- **2 activity LEDs** on the front panel
- 2 LEDs to signal that **/INT** and **conversion end** occurred on the front panel
- Circuitry to generate interrupts on **ABACO**® BUS
- 8 bits data BUS management
- 2 low profile connectors, featuring standard 20 pins pin-out, for analog inputs
- Direct interfacement to **FBC** field modules; unique power supply +5Vdc

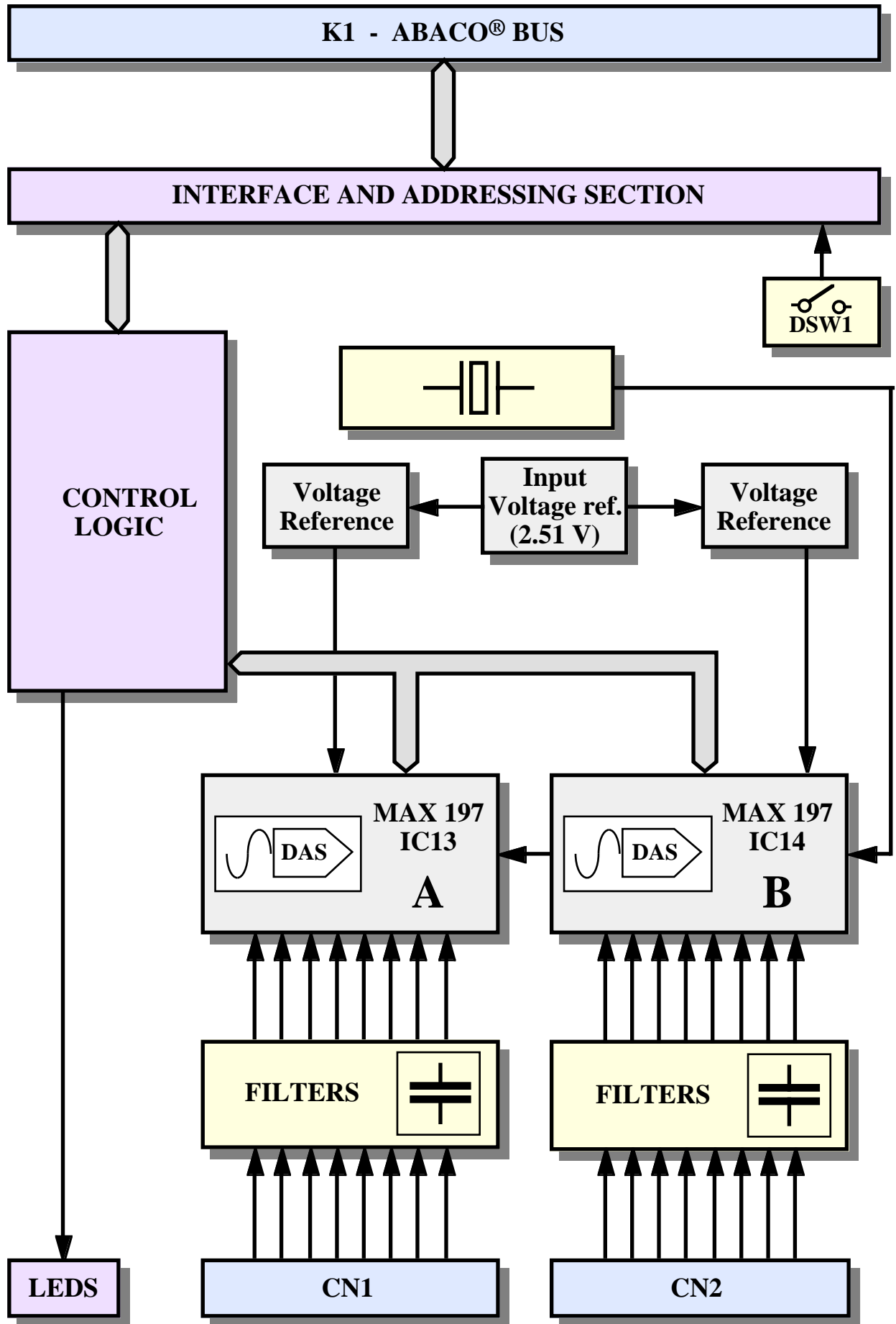


FIGURE 1: BLOCK DIAGRAM

Here follows a description of **LAD 02** board's functional blocks, with an indication of the operations performed by each one. To easily locate these blocks and verify their connections please refer to figure 1.

INTERFACING AND ADDRESSING

This section manages the data exchange between control logic and command board through **ABACO® BUS**. In particular, all written or read data transit across this section that, in addition, provides the board I/O management in a 256 bytes addressing space, by setting the dip switch **DSW1**. For further information please refer to the chapter dedicated to board's software description.

CONTROL LOGIC

This section generates all the chip select signals needed to access the several peripherals on **LAD 13** boards. Using this section the programmer can interact to the board's several sections, verifying their status, setting configuration of A/D converters, etc.

All this can be done through a simple software management based on **ABACO® BUS**, to which the control logic connects through the interfacing and addressing section. For further information please refer to the chapter dedicated to board's software description.

CLOCK

LAD 13 is provided with a circuit with an oscillator to generate the clock signal for A/D Converter. Its frequency is 2 MHz. Such frequency determines the time succession of the several A/D conversion phases process, its value has been chosen to optimize both conversion time and noise immunity.

INPUT FILTERS

Each of the 16 analog inputs is provided with a filter circuitry that protects against electric noise coming from external world. Such circuitry is based on precision components selected in laboratory, to provide the boards with the same kind of interfacement.

The filters are also ready to install an optional module for current-to-voltage conversion (option code **.8420**); such module is made with 248Ω precision resistors, opportunely selected, and allows to acquire current signals in the range 0÷20 mA or 4÷20 mA.

For further information about input circuitry please refer to figures 5 and 7.

REFERENCE VOLTAGES

A specific precision circuitry is charged to generate the two reference voltages (**Vref**) required by the A/D converters. Such voltages are perfectly stabilized and independent from the board supply and temperature variations, so to increase **LAD 13** precision and reliability.

Each A/D converter has its own independent **Vref** setting.

For further information please see paragraph "TRIMMERS AND CALIBRATION".

A/D CONVERTER

LAD 13 board features two independent A/D converter sections based on as many **DAS MAX 197**, these are precision DAS (Data Acquisition System) converters that take advantage of the SAR technique and feature an internal Track-Hold circuitry.

Overall features are:

- Resolution 12 bits or 11 bits plus sign
- 8 analog input channels with internal multiplexer
- Max linearity error ± 1 LSB
- Software configurable Multi-Range inputs: ± 5 Vdc, ± 10 Vdc, $0 \div 5$ Vdc and $0 \div 10$ Vdc
- Conversion time (per channel) 6 μ sec
- Fault-Protected Input Multiplexer (± 16.5 V).
- 5 MHz Bandwidth Track-Hold, 100 Ksps Sampling-Rate independent for each section
- Simple software management

DAS MAX 197 is the ideal component for the typical application of industrial automation, where a high conversion speed and a high grade of precision are required. For further information about this component please refer to manufacturer documentation.

TECHNICAL FEATURES

GENERAL FEATURES

On board resources:	16 analog inputs (two 8 channel A/D converters) 1 eight pins dip switch to set I/O address
BUS type:	Industrial ABACO [®]
Addressing space:	256 bytes
Bytes taken:	4
On board peripherals:	DAS MAX 197
A/D external clock frequency:	8 MHz
A/D work frequency:	2 MHz
A/D resolution:	12 bits (unipolar mode) 11 + sign (bipolar mode)
A/D conversion time:	6 µsec per channel
A/D max linearity error:	± 1 LSB (*)
A/D differential input error:	± 1 LSB (*)

PHYSICAL FEATURES

Size:	Standard EUROCARD format 100x160 mm
Weight:	140 g
Connectors:	K1: DIN 41612 64 pins M 90° A+C type C CN1: Low profile 20 pins M 90° CN2: Low profile 20 pins M 90°
Temperature range:	from 0 to 70° C
Relative humidity:	20% up to 90% (without condensing)

(*) Values referred to a working temperature of 20 °C

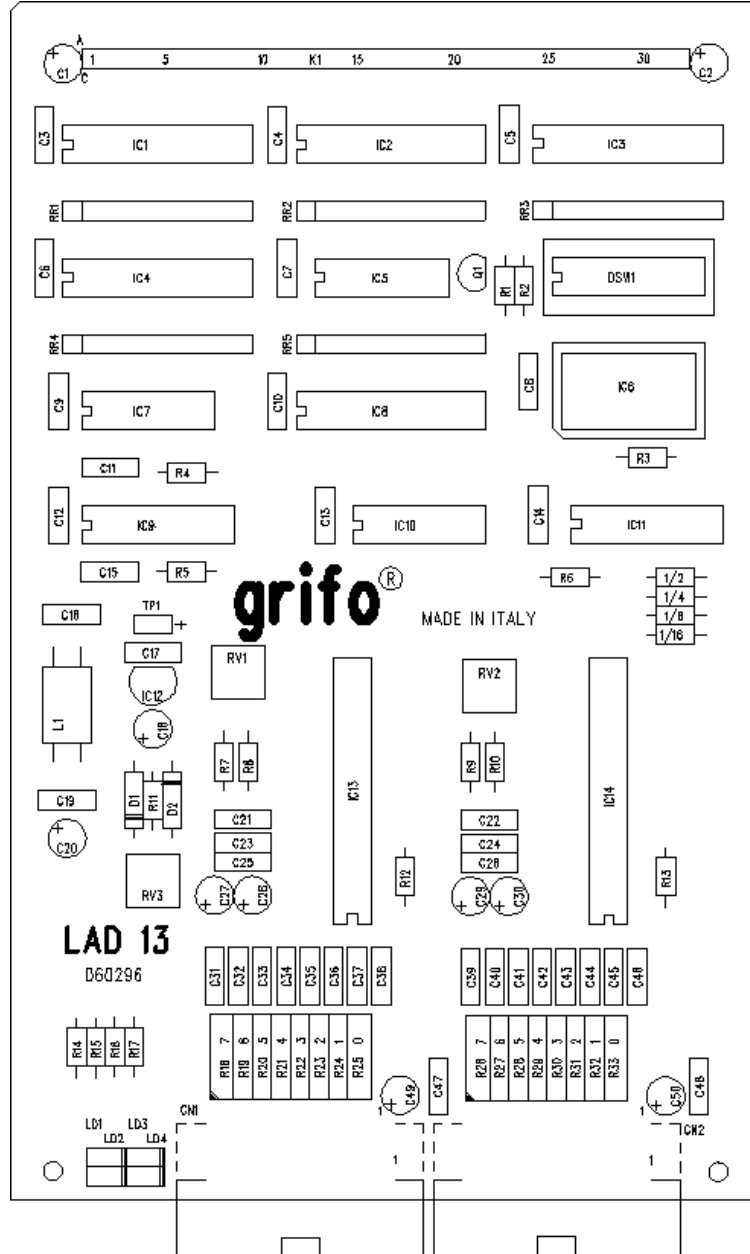


FIGURE 2: COMPONENTS MAP

ELECTRIC FEATURES

Power supply:	+5 Vdc \pm 5%
Current consumption:	170 mA
A/D input impedance:	21 K Ω (unipolar mode) 16 K Ω (bipolar mode)
Analog inputs:	0÷5 Vdc, 0÷10 Vdc, \pm 5 Vdc, \pm 10 Vdc 0÷20 mA or 4÷20 mA (using module .8420)
Curren-to-voltage conversion resistor:	248 Ω
A/D reference voltage:	2.510 Vdc generated on board
Filter on analog inputs:	capacitive filters

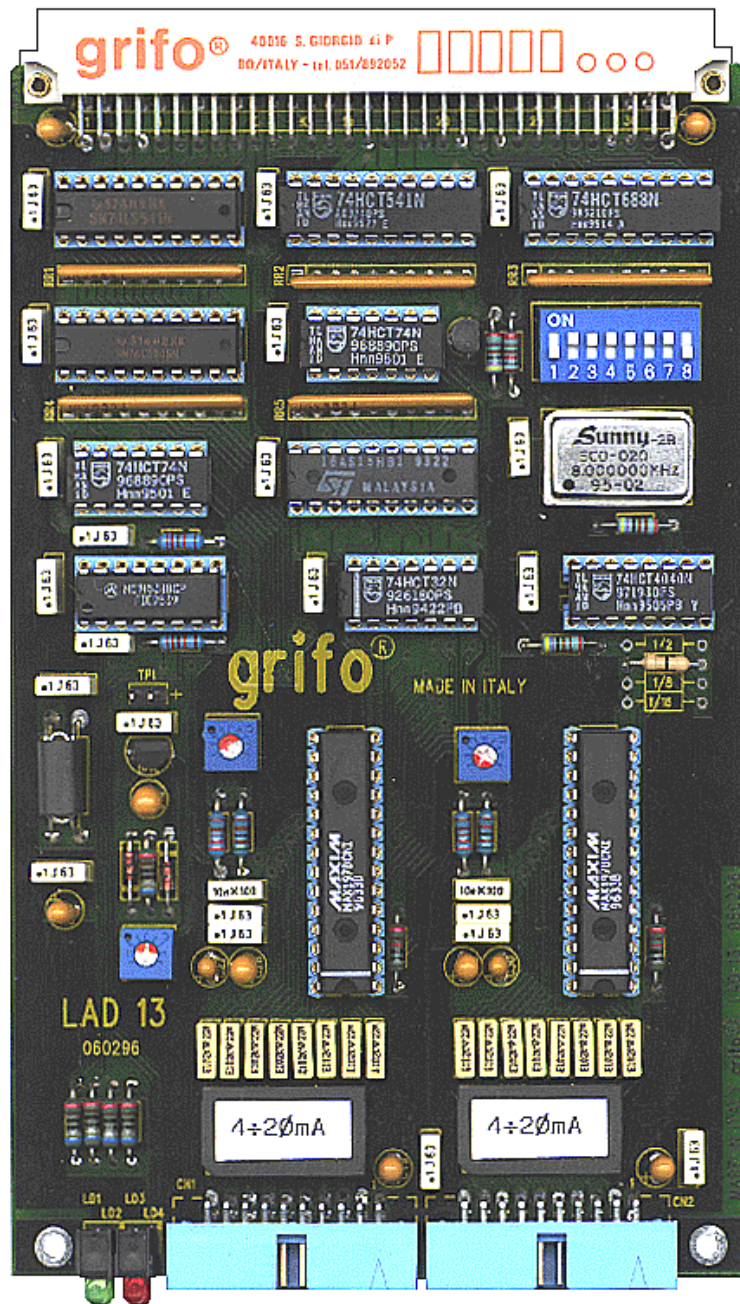


FIGURE 3: CARD PHOTO

INSTALLATION

In this chapter there are the information for a right installation and correct use of **LAD 13** card. The user can find the location and functions of each connectors, LEDs, trimmer and some explanatory diagrams.

CONNECTIONS

The board has three connectors that can be linkeded to other devices or directly to the field, according to system requirements. In this paragraph there are connectors pin outs, a short signals description (including the signals direction) and connectors location, plus some figures that describe how the interface signals are connected on the card.

To easily locate the connectors please refer to figure 7.

CN1 - ANALOG INPUTS SECTION A CONNECTOR

The connector for the 8 analog inputs of section A (DAS MAX 197 installed on IC13), called CN1, is a low profile, 20 pins, 90 degrees with 2.54 mm pitch.

The lines available on CN1 feature capacitor filters to reduce the electric noise coming from the external world. Signals that can be connected to these inputs may be in the range 0÷5 Vdc, 0÷10 Vdc, ±5 Vdc, ±10 Vdc or 0÷20 mA or 4÷20 mA, the last two are available only if converter module is installed (modul code **.8420**). Signals placement on the connector has been designed to reduce problems of noise and interference, to warrant a good transmission quality.

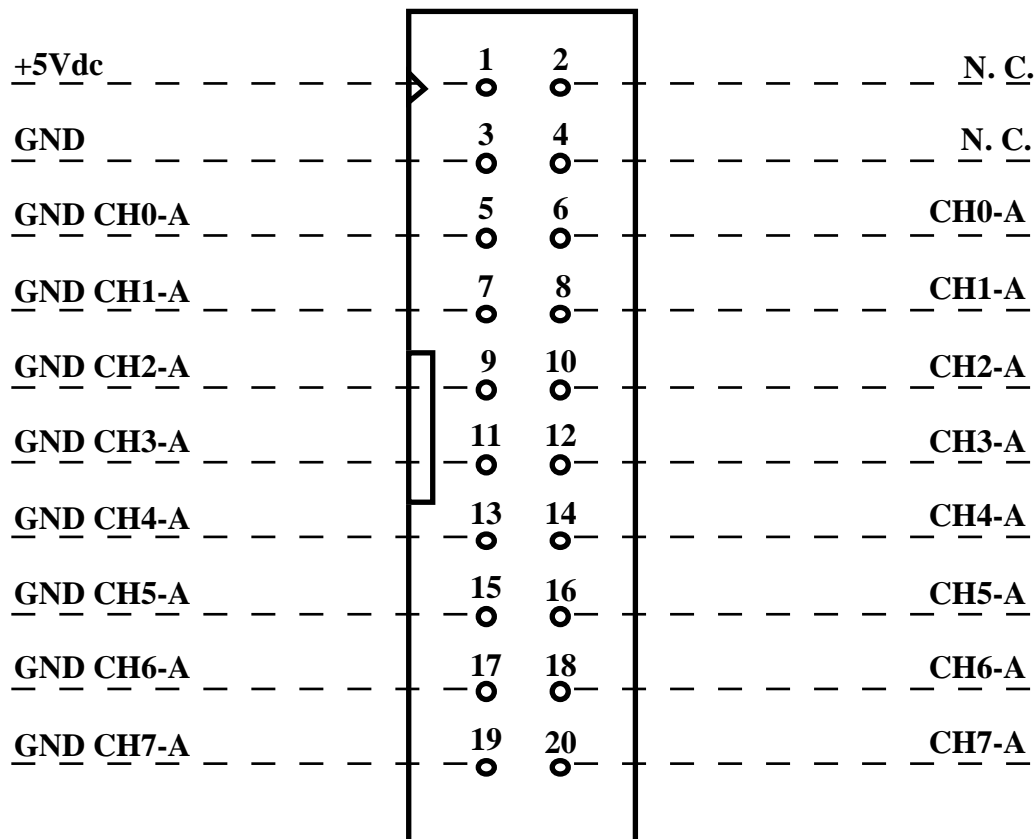


FIGURE 4: CN1 - ANALOG INPUTS SECTION A CONNECTOR

Signals description:

- CHn-A** = I - n-th A/D input channel of section A.
- GND CHn-A** = - Ground of section A A/D input channels.
- +5 Vdc** = O - Power supply +5 Vdc.
- N. C.** = - No connection.
- GND** = - Ground.

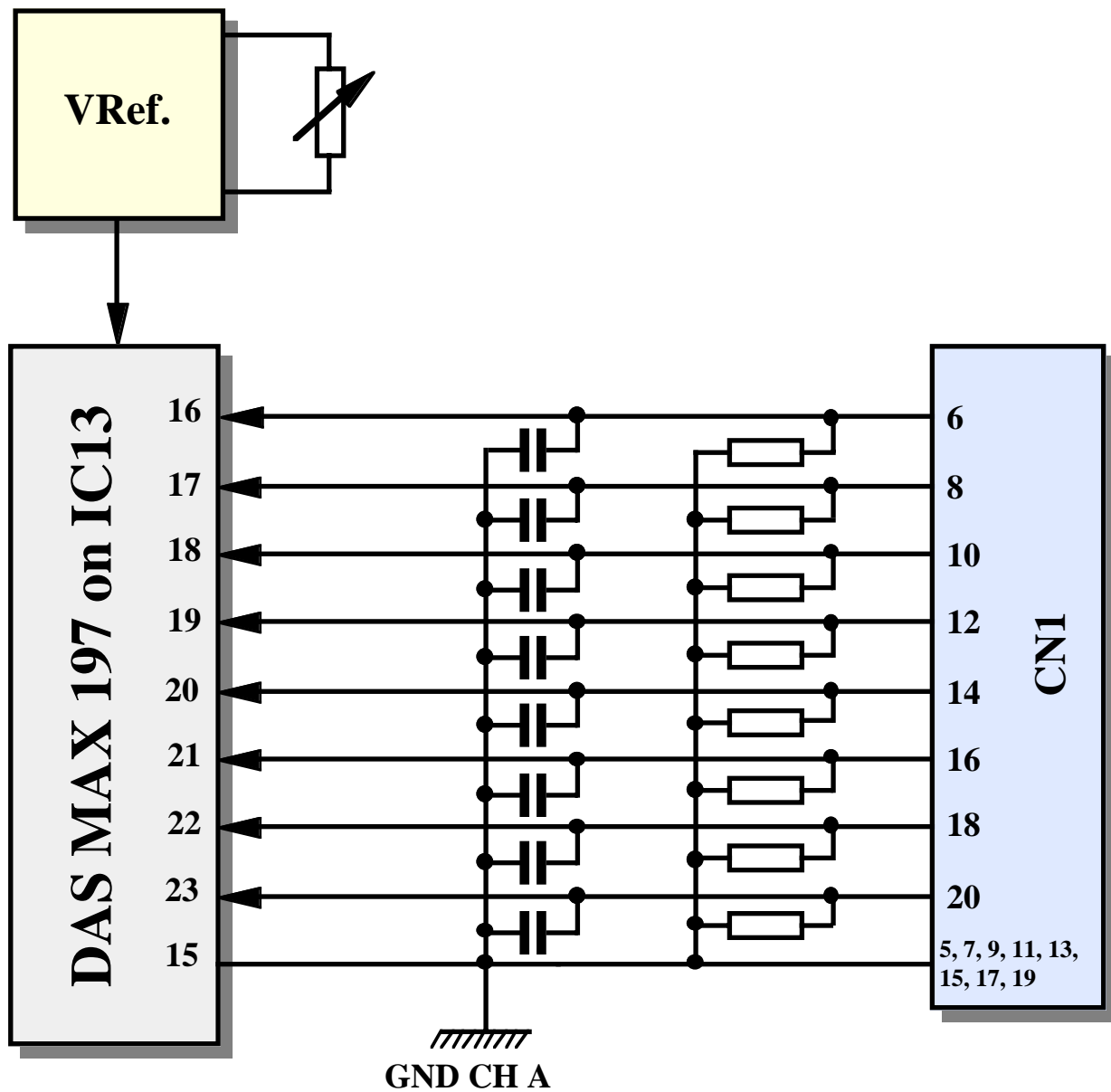


FIGURE 5: A/D CONVERTER OF SECTION A BLOCK DIAGRAM

CN2 - ANALOG INPUTS SECTION B CONNECTOR

The connector for the 8 analog inputs of section A (DAS MAX 197 installed on IC14), called CN2, is a low profile, 20 pins, 90 degrees with 2.54 mm pitch.

The lines available on CN2 feature capacitor filters to reduce the electric noise coming from the external world. The signals that can be connected to these inputs may vary in the range 0÷5 Vdc, 0÷10 Vdc, ±5 Vdc, ±10 Vdc or 0÷20 mA or 4÷20 mA, the last two are available only if converter module is installed (modul code **.8420**). Signals placement on the connector has been designed to reduce problems of noise and interference, to warrant a good transmission quality.

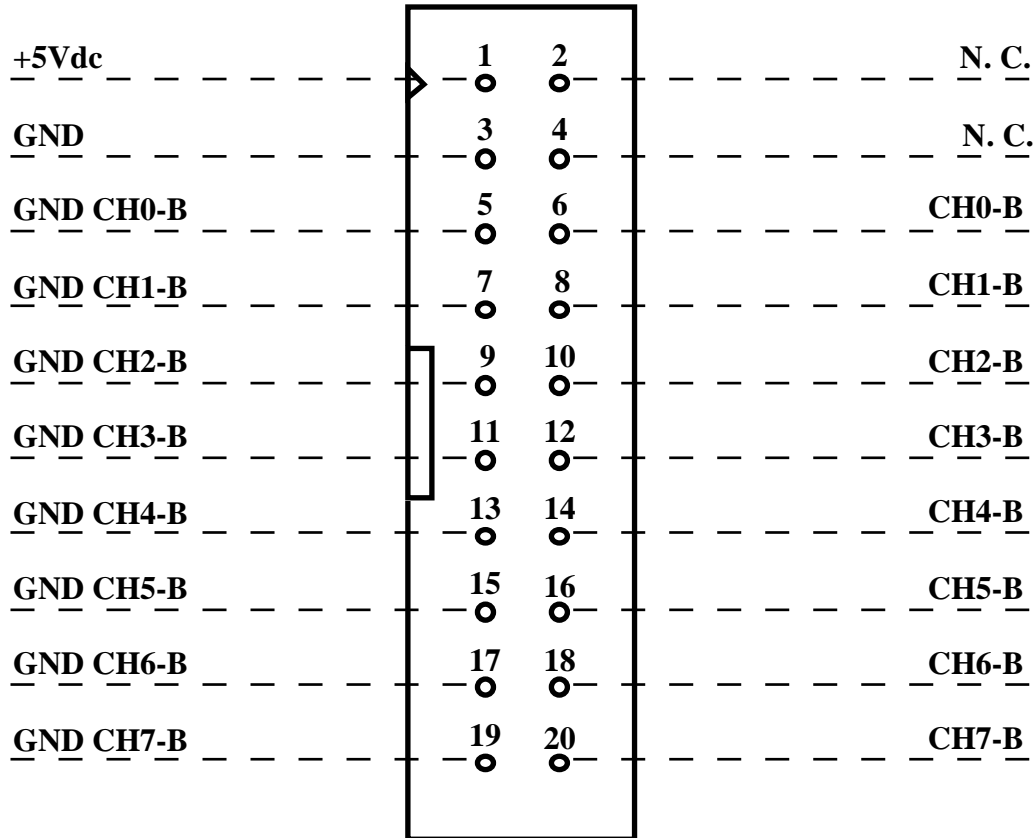


FIGURE 6: CN1 - ANALOG INPUTS SECTION B CONNECTOR

Signals description:

- CHn-B** = I - n-th A/D input channel of section B.
- GND CHn-B** = - Ground of section B A/D input channels.
- +5 Vdc** = O - Power supply +5 Vdc.
- N. C.** = - No connection.
- GND** = - Ground.

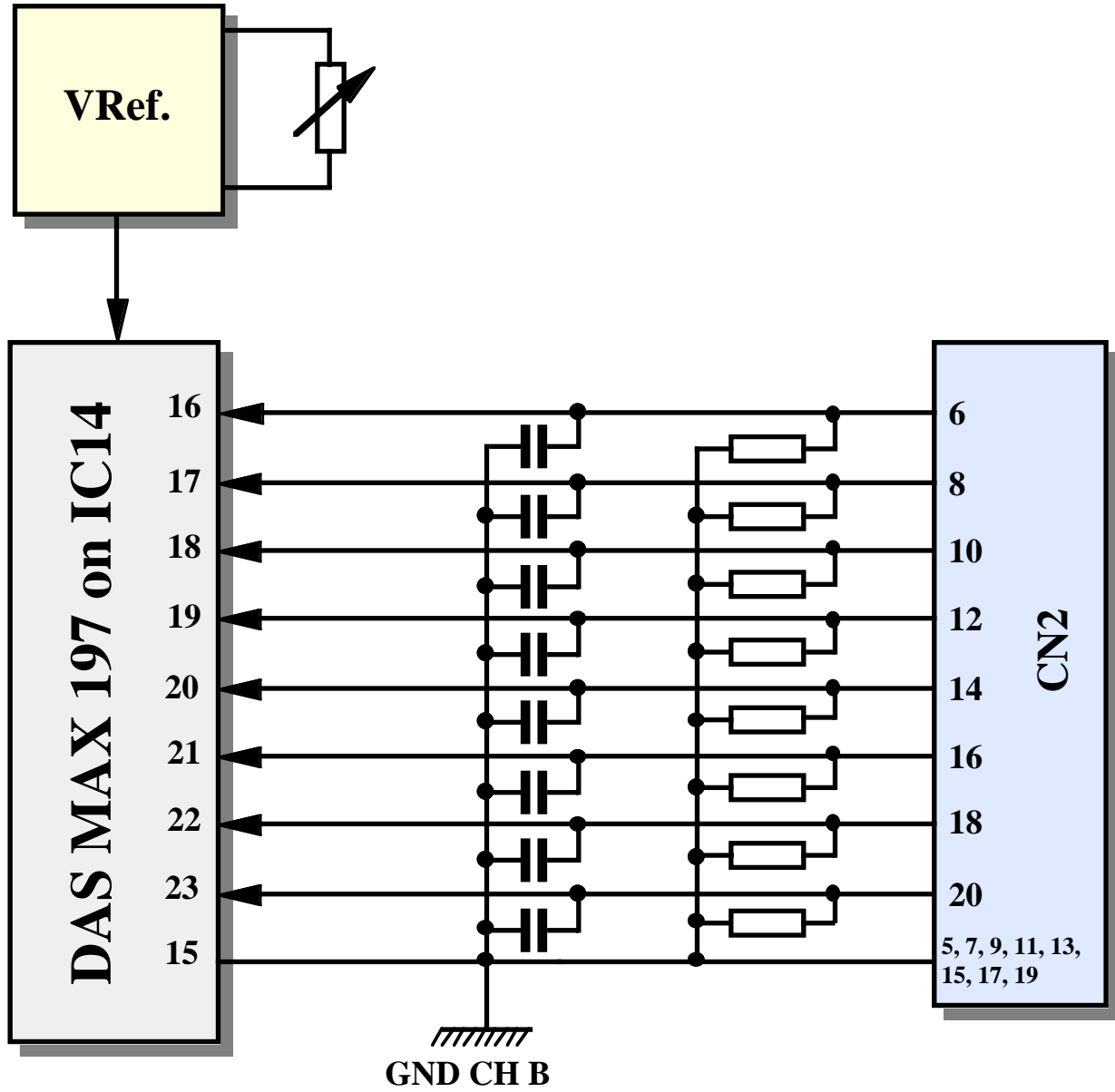


FIGURE 7: A/D CONVERTER OF SECTION B BLOCK DIAGRAM

K1 - CONNECTOR FOR ABACO® BUS

The connector for **ABACO® industrial BUS**, called K1 on the board, is a DIN 41612, male, a 90 °, type C, A+C.

Here follows the pin-out of the connector installed on **LAD 13**, in addition there is the standard 8 bits and 16 bits **ABACO® BUS** pin-out.

Please remark that all the signals here described are TTL, except for the power supplies.

A 16 bit BUS	A 8 bit BUS	A LAD 13	PIN	C LAD 13	C 8 bit BUS	C 16 bit BUS
GND	GND	GND	1	GND	GND	GND
+5 Vdc	+5 Vdc	+5 Vdc	2	+5 Vdc	+5 Vdc	+5 Vdc
D0	D0	D0	3	N. C.		D8
D1	D1	D1	4	N. C.		D9
D2	D2	D2	5	N. C.		D10
D3	D3	D3	6	/INT	/INT	/INT
D4	D4	D4	7	N. C.	/NMI	/NMI
D5	D5	D5	8	N. C.	/HALT	D11
D6	D6	D6	9	N. C.	/MREQ	/MREQ
D7	D7	D7	10	/IORQ	/IORQ	/IORQ
A0	A0	A0	11	/RD	/RD	/RD LDS
A1	A1	A1	12	/WR	/WR	/WR LDS
A2	A2	A2	13	N. C.	/BUSAK	D12
A3	A3	A3	14	N. C.	/WAIT	/WAIT
A4	A4	A4	15	N. C.	/BUSRQ	D13
A5	A5	A5	16	/RESET	/RESET	/RESET
A6	A6	A6	17	/M1	/M1	/IACK
A7	A7	A7	18	N. C.	/RFSH	D14
A8	A8	N. C.	19	N. C.	/MEMDIS	/MEMDIS
A9	A9	N. C.	20	N. C.	VDUSEL	A22
A10	A10	N. C.	21	N. C.	/IEI	D15
A11	A11	N. C.	22	N. C.		
A12	A12	N. C.	23	N. C.	CLK	CLK
A13	A13	N. C.	24	N. C.		/RD UDS
A14	A14	N. C.	25	N. C.		/WR UDS
A15	A15	N. C.	26	N. C.		A21
A16		N. C.	27	N. C.		A20
A17		N. C.	28	N. C.		A19
A18		N. C.	29	N. C.	/R.T.	/R.T.
+12 Vdc	+12 Vdc	N. C.	30	N. C.	-12 Vdc	-12 Vdc
+5 Vdc	+5 Vdc	+5 Vdc	31	+5 Vdc	+5 Vdc	+5 Vdc
+5 Vdc	+5 Vdc	GND	32	GND	GND	GND

FIGURE 8: K1 - CONNECTOR FOR ABACO® BUS

Signals description:

8 bits CPU

A0-A15	=	O	- Address BUS
D0-D7	=	I/O	- Data BUS
/INT	=	I	- Interrupt request
/NMI	=	I	- Non Maskable Interrupt
/HALT	=	O	- Halt state
/MREQ	=	O	- Memory Request
/IORQ	=	O	- Input Output Request
/RD	=	O	- Read cycle status
/WR	=	O	- Write cycle status
/BUSAK	=	O	- BUS Acknowledge
/WAIT	=	I	- Wait
/BUSRQ	=	I	- BUS Request
/RESET	=	O	- Reset
/M1	=	O	- Machine cycle one
/RFSH	=	O	- Refresh for dynamic RAM
/MEMDIS	=	I	- Memory Display
VDUSEL	=	O	- VDU Selection
/IEI	=	I	- Interrupt Enable Input
CLK	=	O	- System clock
R.B.	=	I	- Reset button
+5 Vdc	=	I	- Power supply at +5 Vdc
+12 Vdc	=	I	- Power supply at +12 Vdc
-12 Vdc	=	I	- Power supply at -12 Vdc
GND	=		- Ground signal

16 bits CPU

A16-A22	=	O	- Address BUS
D8-D15	=	I/O	- Data BUS
/RD UDS	=	O	- Read Upper Data Strobe
/WR UDS	=	O	- Write Upper Data Strobe
/IACK	=	O	- Interrupt Acknowledge
/RD LDS	=	O	- Read Lower Data Strobe
/WR LDS	=	O	- Write Lower Data Strobe

NOTE

Directionality indications as above stated are referred to a master (GPC®) board and have been kept untouched to avoid ambiguity in case of multi-boards systems.

VISUAL SIGNALATIONS

LAD 13 card is provided with signalation LEDs to show several status informations, as described in the following table:

LEDS	COLOUR	PURPOSE
LD1	Green	Software managed activity LED.
LD1	Green	Software managed activity LED.
LD3	Red	It lights when a conversion end occurs and the corresponding interrupt signal is generated by DAS MAX 197 installed on IC13.
LD4	Red	It lights when a conversion end occurs and the corresponding interrupt signal is generated by DAS MAX 197 installed on IC14.

FIGURE 9: VISUAL SIGNALATIONS TABLE

The main purpose of LEDs is to show a visual indication about the card's status, making so easier debug and verify operations. To easily locate these visual signalations please refer to the figure 10.

POWER SUPPLY

LAD 13 is provided with an efficient circuitry that solves in a comfortable and simple way the problem of the board's supply, under any condition of use.

Here follow the voltages needed:

- +5 Vdc:** Supplies the on board logic; must be in the range $+5 \text{ Vdc} \pm 5\%$ and must be provided through the specific pins of connector K1 (**ABACO**[®] BUS).
Please note that this voltage is available on connectors CN1 and CN2 to supply eventual external circuits.

To warrant great immunity to external noise and so a correct working of the board, it is essential that **+5 Vdc** tension is galvanically isolated.

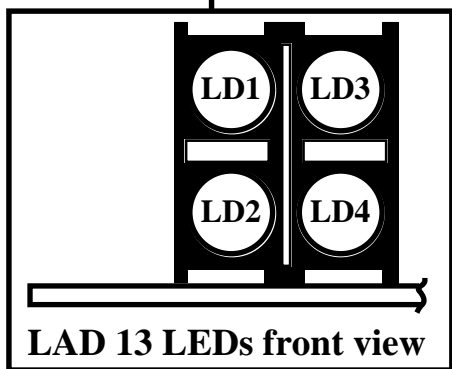
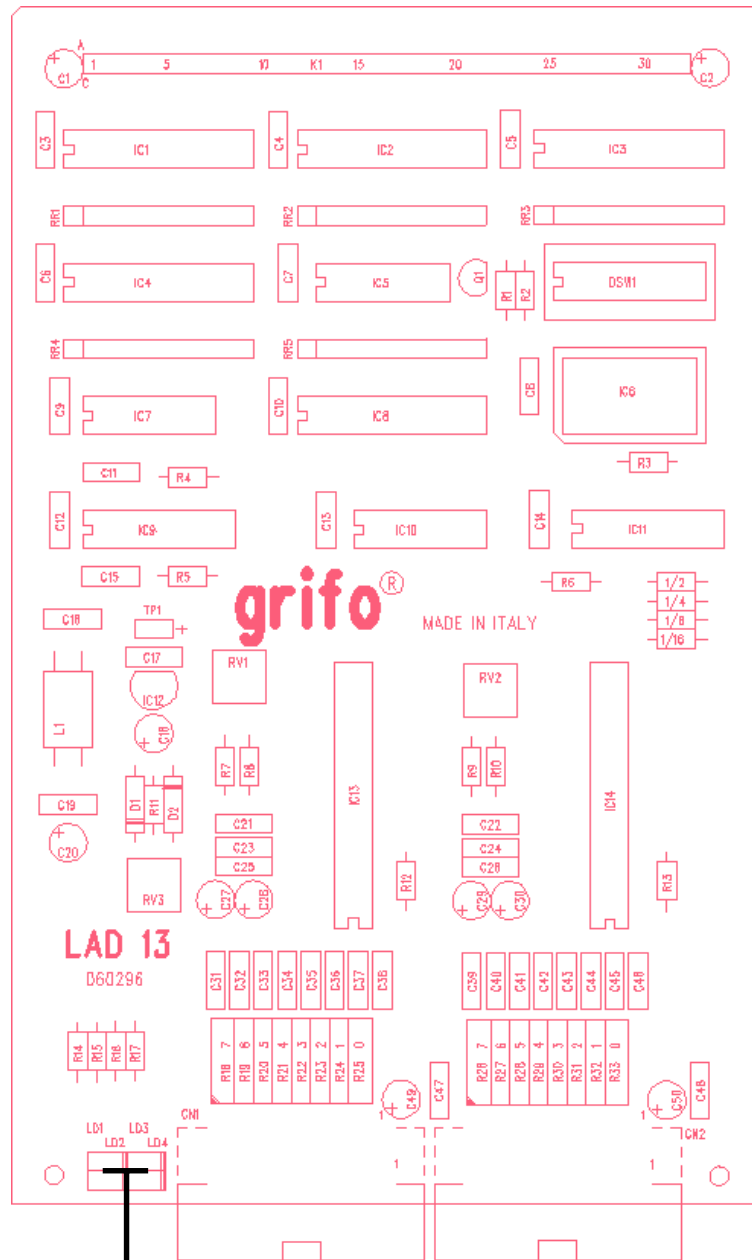


FIGURE 10: LEDs LOCATION

DIP SWITCH

LAD 13 is provided with an on board 8 pins dip switch (DSW1). Their purpose is to set the mapping address for control and data registers of the on board devices and to set the connection modalities for /M1 and /INT signals.

More information about card mapping and signals management can be found in the chapter "PERIPHERAL DEVICES SOFTWARE DESCRIPTION", while to easily locate them on the board please refer to figure 12.

BOARD CONNECTIONS

To prevent possible connecting problems between **LAD 13** board and the external systems, the user has to read carefully the information of the previous paragraphs and he must follow these instructions:

- The TTL signals can be connected directly only to a device featuring the same type of interface. About the correspondance between logic signals and TTL output status, remember that a logic **0** generates a TTL 0 Vdc, while a logic **1** generates a TTL +5 Vdc.
- The analog inputs (A/D section) must be connected to signals in the following ranges: 0÷5 Vdc, 0÷10 Vdc, ±5 Vdc, ±10 Vdc or 0÷20 mA according to the board configuration. Please remember that the sixteen analog inputs available on CN1 and CN2 are provided with capacitor filters protections that ensure an higher stability of the acquired signals, but reduce at the same time the bandwidth frequency. For further information please refer to the paragraph "TYPE OF ANALOG INPUT SELECTION".

INTERRUPT

LAD 13 is provided with a comfortable and efficient interrupt generation circuitry, that, if enabled, can generate an interrupt to the **GPC**® intelligent control card when one of the two analog to digital converter section reach the end of a conversion. Such circuitry allows to optimize the time needed to manage the board, in fact the intelligent control card is not obliged to poll **LAD 13** registers, but can simply wait for an interrupt and read the conversion results.

ABACO® BUS interrupt signal, once it has been activated, remains in such status until the control card performs the read operation from **LAD 13** A/D converter data registers. This ensures a correct management also in case of contemporary interrupts, in fact the signal deactivates only after the proper software operations, which are time-independent.

LAD 13 interrupt generation circuitry can be connected or not connected to **ABACO**® BUS through switch DSW1.2 as shown in the chapter "PERIPHERAL DEVICES SOFTWARE DESCRIPTION".

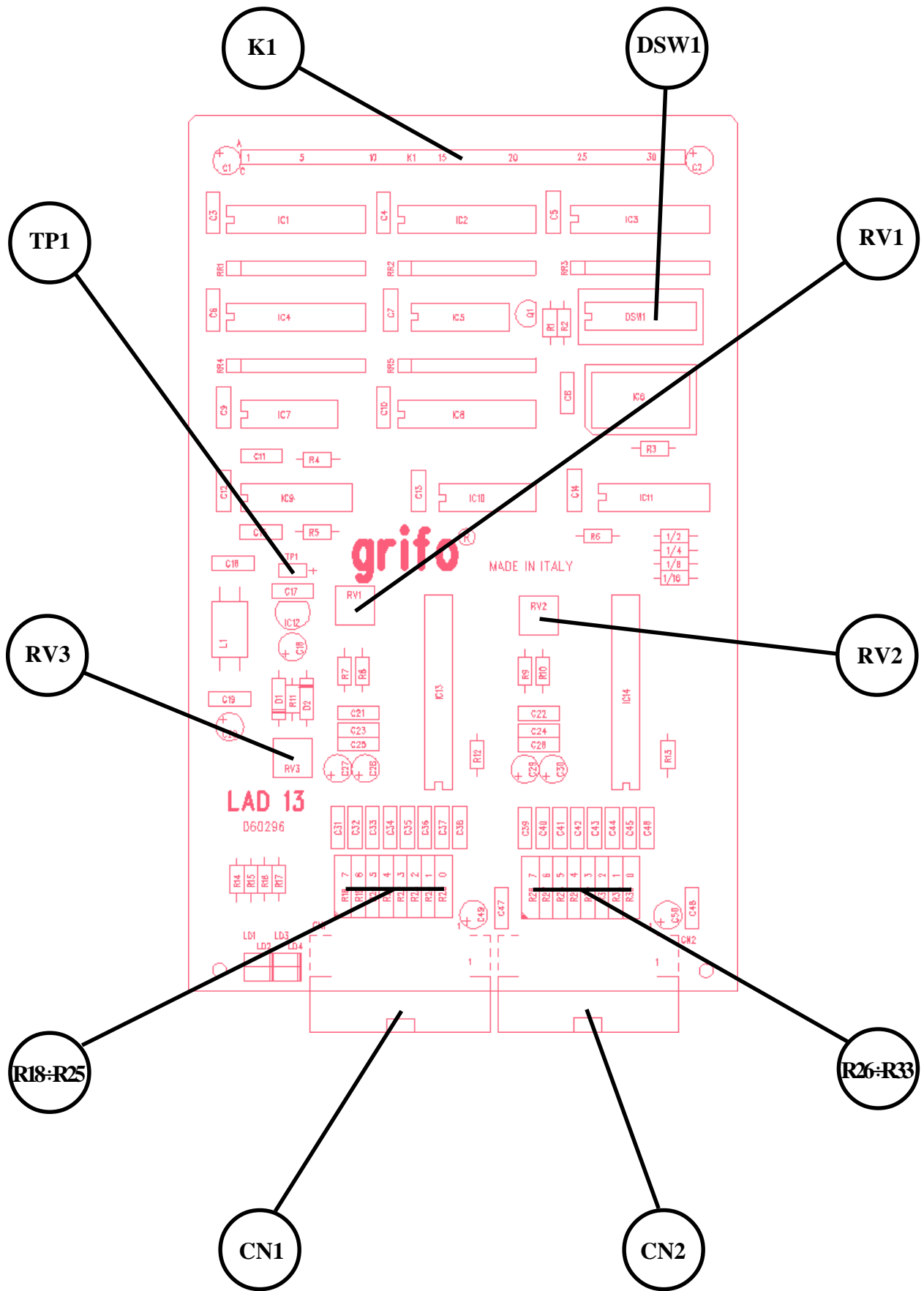


FIGURE 11: CONNECTORS, TEST POINT, DIP SWITCH, CURRENT-TO-VOLTAGE MODULES LOCATION

TEST POINT

The board is provided with a test point called TP1, that allows to read, through a galvanically isolated multimeter, the reference voltage calibrated in laboratory and whose value is $V_{ref}=2.510$ Vdc, used by the A/D converter sections. TP1 is made of two contacts:

pin +	->	V_{ref}
pin -	->	GND

V_{ref} is perfectly stabilized and completely independent from power supply voltage.

To easily locate the test point contacts please refer to figure 12, while for further information about V_{ref} signal please refer to the paragraph "TRIMMER AND CALIBRATION".

TYPE OF ANALOG INPUT SELECTION

LAD 13 board can accept analog voltage and/or current inputs, as described in the previous paragraphs and chapters. The input type selection must be made during the order phase and is performed mounting a specific current-to-voltage conversion modul (option code **.8420**) made by precision resistors. In detail:

R25	->	channel 0, section A
R24	->	channel 1, section A
R23	->	channel 2, section A
R22	->	channel 3, section A
R21	->	channel 4, section A
R20	->	channel 5, section A
R19	->	channel 6, section A
R18	->	channel 7, section A
R33	->	channel 0, section B
R32	->	channel 1, section B
R31	->	channel 2, section B
R30	->	channel 3, section B
R29	->	channel 4, section B
R28	->	channel 5, section B
R27	->	channel 6, section B
R26	->	channel 7, section B

Should the current-to-voltage conversion module not to be mounted (default case) the corresponding channel accepts a voltage input signal in the ranges $0\div 5$ Vdc, $0\div 10$ Vdc, ± 5 Vdc, ± 10 Vdc; otherwise a current input signal is accepted; in this case the channel must be configured for $0\div 5$ Vdc.

The value of the above mentioned resistors is obtained by the following spread:

$$R = 5 \text{ V} / I_{max}$$

Usually the current-to-voltage conversion modules are made using **248 Ω** precision resistors, corresponding to input ranges $4\div 20$ mA or $0\div 20$ mA. Any eventual configuration out of this standard should be asked directly to **grifo**[®]. To easily locate the conversion module please refer to figure 12.

TRIMMERS AND CALIBRATION

On **LAD 13** board there are three trimmers, called **RV1÷3**, that calibrate the output voltages of the A/D converter sections; in detail it allows to set reference voltage for both sections:

- RV1 -> Allows the fine regulation of reference voltage for section A A/D converter (DAS MAX 197 installed on IC13).
- RV2 -> Allows the fine regulation of reference voltage for section B A/D converter (DAS MAX 197 installed on IC14).
- RV3 -> Allows the regulation of reference voltage 2.510 Vdc.

The **LAD 13** is subjected to a careful test that verifies and calibrates all the card sections. The calibration is executed in laboratory, with a controlled +20° C room temperature, following these steps:

- The A/D reference voltage (Vref) is calibrated through RV3 trimmer, by using a 5 digits precision multimeter, to the value of **+2.5100 Vdc** on test point TP1.
- Fine regulation of Vref is made through trimmers RV1 and RV2.
Trimmers are regulated so that the correspondance between the analog input signal and the combination read from A/D is verified. This check is repeated with a reference signal for each A/D input and it is tested that A/D combination and theoric combination differ at maximum of the A/D section errors sum.
- Trimmers are blocked with paint.

The analog interfaces use high precision components that are selected during mounting phase to avoid complicate and long calibration procedures. After the calibration, the on board trimmers are blocked with paint to mantain calibration also in presence of mechanic stresses (vibrations, movings, delivery, etc.).

The user must not intervernt on the circuit that generates the reference voltage, however if this should be necessary (exampe: for time derives) then he/she must follow the above mentioned procedure. To easily locate the above mentioned components please refer to figure 12; for further information about test points please refer to the previous paragraph; for further information about how to set the A/D converters output voltages please refer to chapter “SOFTWARE DESCRIPTION”.

RESET

After a reset or a power on bits EOC1, EOC2 and interrupt signal are at logic level 0. This condition is ambiguous because it corresponds to an “end of conversion occoured” that did not occur. Please refer to paragraph “PERIPHERAL DEVICES SOFTWARE DESCRIPTION” for futher information.

HARDWARE DESCRIPTION

This chapter provides all the hardware informations needed to use **LAD 13** board. Here the user will find information about I/O card mapping and on board peripheral devices addressing.

BOARD MAPPING

LAD 13 board is mapped into a **4** bytes I/O addressing space, that can be mapped starting from different base addresses according to how the board is configured. This feature allows to use several **LAD 13** cards on the same **ABACO® BUS**, or to install them on a **BUS** where other peripheral modules are installed obtaining a structure that can be expanded without any difficulty or modifications to the application software.

The base address can be defined through the specific **BUS** interface circuitry on the board itself; this circuitry uses the eight pins dip switch called **DSW1**, from which it reads the address set by the user. Here follows the corrispondance between dips configuration and address signals.

DSW1.1	->	<i>Please see paragraph "CONFIGURATION INPUTS"</i>
DSW1.2	->	<i>Please see paragraph "CONFIGURATION INPUTS"</i>
DSW1.3	->	Address A2
DSW1.4	->	Address A3
DSW1.5	->	Address A4
DSW1.6	->	Address A5
DSW1.7	->	Address A6
DSW1.8	->	Address A7

These dips are driven in complemented logic, this means that if a switch is **ON** generates a **logic zero**, viceversa if a switch is **OFF** generates a **logic one**.

Also switch **DSW1.2** affects the addressing logic, as described before, and must be set according to the type of **GPC®** control card used. In detail, if the control card is provided with /M1 signal on the **ABACO® BUS** connector **DSW1.2** must be **ON**, and viceversa.

NOTE

When allocating the mapping address of the boards, please be careful not to allocate more than one device in the same addressing space (count also the number of bytes occupied by the card). If this condition will not be respected, a **BUS** conflict will happen; such conflict will compromise the correct working of the whole system.

As an example, some possible mappings are reported here.

- 1) Address used to map **LAD 13**: 048H
Control board used: /M1 signal connected
interrupt not connected

DSW1.1	->	OFF
DSW1.2	->	ON
DSW1.3	->	ON
DSW1.4	->	OFF
DSW1.5	->	ON
DSW1.6	->	ON
DSW1.7	->	OFF
DSW1.8	->	ON

- 2) Address used to map **LAD 13**: A4H
Control board used: /M1 signal not connected
interrupt connected

DSW1.1	->	ON
DSW1.2	->	OFF
DSW1.3	->	OFF
DSW1.4	->	ON
DSW1.5	->	ON
DSW1.6	->	OFF
DSW1.7	->	ON
DSW1.8	->	OFF

To easily locate jumpers and dip switches please refer to figure 12.

INTERNAL REGISTERS ADDRESSING

Indicating the board base address with **<baseaddr>**, that is the address set using dip switch DSW1, as indicated in the previous paragraph **LAD 13** internal registers are addressable as explained in the following table.

DEVICE	REGISTER	ADDRESS	R/W	PURPOSE
DAS MAX197 installed on IC13	DAS1CTRL	<baseaddr>+00	W	Control register of DAS MAX 197 installed on IC13.
	DAS1L	<baseaddr>+00	R	Data register (bit 0÷7) of DAS MAX 197 installed on IC13.
	DAS1H	<baseaddr>+01	R	Data register (bit 8÷11) and status register of DAS MAX 197 installed on IC13.
DAS MAX197 installed on IC14	DAS2CTRL	<baseaddr>+02	W	Control register of DAS MAX 197 installed on IC14.
	DAS2L	<baseaddr>+02	R	Data register (bit 0÷7) of DAS MAX 197 installed on IC14.
	DAS2H	<baseaddr>+03	R	Data register (bit 8÷11) and status register of DAS MAX 197 installed on IC14.
Activity LEDS	LED	<baseaddr>+03	W	Activity LEDs LD1 and LD2 management registers.

FIGURE 12: INTERNAL REGISTERS ADDRESSING TABLE

NOTE

When allocating the mapping address of the boards, please be careful not to allocate more than one device in the same addressing space (count also the number of bytes occupied by the card). If this condition will not be respected, a BUS conflict will happen; such conflict will compromise the correct working of the whole system.

PERIPHERAL DEVICES SOFTWARE DESCRIPTION

In the previous paragraph allocation addresses of all the peripherals have been reported, here follows a detailed description of function and meaning of internal registers (please always refer to the peripheral mapping tables to understand completely the following informations). Should the present documentaion be inadequate please refer to the component's manufacturer documentation.

In the following paragraphs the indications **D0÷D7** or **D0÷D15** are used to refer the bits of the byte or word involved in the I/O operations.

A/D CONVERTER DAS MAX 197

Management of 12 bits A/D converter DAS MAX 197 is performed through I/O operations to its specific control registers described in figure 13; in detail registers DAS1CTRL, DAS1L and DAS1H allow to manage the A/D converter of section A, while registers DAS2CTRL, DAS2L and DAS2H allow to manage the A/D converter of section B.

Here follows the meaning of the bits in the registers.

Register DASnCTRL:

This register allows to the management of DAS MAX 197; a write operation to this register will begin the conversion for the specified section (n=1 means section A, n=2 means section B).

The meaning of its bits is:

DASnCTRL.7	->	PD1
DASnCTRL.6	->	PD0
DASnCTRL.5	->	ACQMOD
DASnCTRL.4	->	RNG
DASnCTRL.3	->	BIP
DASnCTRL.2	->	A2
DASnCTRL.1	->	A1
DASnCTRL.0	->	A0

Bits called A0, A1 and A2 allow to select the DAS MAX 197 channel where the Track-Hold operatron and the conversion will be performed:

A2	A1	A0	
0	0	0	-> Channel 0
0	0	1	-> Channel 1
0	1	0	-> Channel 2
0	1	1	-> Channel 3
1	0	0	-> Channel 4
1	0	1	-> Channel 5
1	1	0	-> Channel 6
1	1	1	-> Channel 7

Bits called RNG and BIP allow to set the conversion voltage range for the channel selected with bits A0÷A2, such selection affects only the next conversion for the selected channel, so it will change for different channels and for successive conversions.

RNG	BIP		
0	0	->	Range 0÷5 V
1	0	->	Range 0÷10 V
0	1	->	Range ±5 V
1	1	->	Range ±10 V

The bit called ACQMOD allows the manual control of MAX 197 internal Track-Hold or it automatic management by the A/D converter itself, in detail:

ACQMOD = 0 -> The Track-Hold for the channel specified through bits A0÷A2 remains actived for 3 µsec the the conversion phase for the analog signal held begins.

ACQMOD = 1 -> The Track-Hold for the channel specified through bits A0÷A2 activates and stays active until the next write operation to the control register, the data written will have to be equal to the previous one but with ACQMOD=0. Using this feature the user can capture a signal for the duration he/she wants.

The bits called PD0 and PD1 allow to set the working mode of DAS MAX 197 amongst the following choices:

PD1	PD0		
0	0	->	Normal work with external clock
0	1	->	Normal work with internal clock (<u>DO NOT USE</u>)
1	0	->	Standby Power-Down mode
1	1	->	Full Power-Down mode

NOTE

Normal work with internal clock mode **must never be used**, because **LAD 13** is provided with a specific circuitry to generate the clock frequency so to optimize both conversion time and electric noise immunity.

EXAMPLE

Writing 0BH to the register DAS2CTRL will cause a conversion on channel 3 of section B DAS MAX 197 with range ±5 Vdc and automatic Track-Hold management.

Register DASnL:

This register allows to read the low byte of the converted value on DAS MAX 197; a read operation from this register will return bits 0÷7 of the last conversion value (n=1 means section A, n=2 means section B).

The meaning of its bits is:

DASnL.7	->	Bit 7 of the conversion value
DASnL.6	->	Bit 6 of the conversion value
DASnL.5	->	Bit 5 of the conversion value
DASnL.4	->	Bit 4 of the conversion value
DASnL.3	->	Bit 3 of the conversion value
DASnL.2	->	Bit 2 of the conversion value
DASnL.1	->	Bit 1 of the conversion value
DASnL.0	->	Bit 0 of the conversion value

Please remark that this register contains valid data only when DAS MAX 197 is not busy in an analog to digital conversion.

Register DASnH:

This register allows to read the high nibble of the converted value on DAS MAX 197; a read operation from this register will return bits 8÷11 of the last conversion value and the End Of Conversion flags for both the sections (n=1 means section A, n=2 means section B).

The meaning of its bits is:

DASnH.7	->	EOC2 - End Of Conversion for section B
DASnH.6	->	EOC1 - End Of Conversion for section A
DASnH.5	->	Not used
DASnH.4	->	Not used
DASnH.3	->	Bit 11 of the conversion value (unipolar mode) Sign of the conversion value (bipolar mode)
DASnH.2	->	Bit 10 of the conversion value
DASnH.1	->	Bit 9 of the conversion value
DASnH.0	->	Bit 8 of the conversion value

Bit DASnH.3 will contain the twelfth bit of the conversion value or the sign of the conversion (**0**=positive, **1**=negative) according to the range set: twelve bits in unipolar mode (0÷5 Vdc or 0÷10 Vdc) or eleven bits plus sign bit in bipolar mode (± 5 Vdc or ± 10 Vdc).

Bits DASnH.7 and DASnH.6 contain the End Of Conversion flags for the two DAS MAX 197 (EOC1 and EOC2), with the following meanings:

EOCn=0 -> DAS MAX 197 of n-th section has terminated the conversion operation and its value is ready to be read.

EOCn=1 -> DAS MAX 197 of n-th section is still executing a conversion or the conversion has already been completed and its value has already been read at least once.

In fact the signal matched to a specific section is set to logic level 1 when a write or read operation is performed to registers DASnCTRL or DASnL.

INITIALIZATION SEQUENCE

After a reset or a power on bits EOC1, EOC2 and interrupt signal are at logic level 0. This condition is ambiguous because it corresponds to an “end of conversion occurred” that did not occur.

For this reason the first operations that the control card must execute to **LAD 13** are:

- Read from address of *DAS1L* register
- Read from address of *DAS2L* register

These operation return meaningless data but allow to set the **LAD 13** signals to their normal working mode.

CONVERSION IN POLLING

Here follows the sequence of operations to perform to execute a conversion on a channel of **LAD 13**. The end of conversion signal is checked continuously (Polling) to test when the conversion value is ready to be read.

- Write to register *DASnCTRL* the data that specifies how to configure the conversion (channel, range, etc.)
- Waiting for *EOCn* to be 0 (Polling)
- Read bits 8÷11 of the converted value from bits *DASnH.0÷2*
- Read bits 0÷7 of the converted value from *DASnL* register
- Elaboration of the value obtained

CONVERSION IN INTERRUPT

Here follows the sequence of operations to perform to execute a conversion on a channel of **LAD 13**. The end of conversion signal will generate an interrupt on **ABACO® BUS** that will indicate availability of the conversion value.

NOTE: interrupt signal will be received by **LAD 13** only if the corresponding signal is connected, see paragraph “CONFIGURATION INPUTS” for more information.

Main program must perform these operations:

- Write to register *DASnCTRL* the data that specifies how to configure the conversion (channel, range, etc.)
- Elaboration of the value obtained from interrupt routine

Interrupt routine must perform these operations:

- Checks *EOCn* bits to determine which *DAS MAX 197* has completed the conversion
- Read bits 8÷11 of the converted value from bits *DASnH.0÷2*
- Read bits 0÷7 of the converted value from *DASnL* register

ACTIVITY LEDS

Management of the two activity LEDs installed on **LAD 13** is performed through a write register called LED. Its bits have the following meaning:

LED.7	->	Not used
LED.6	->	Not used
LED.5	->	Not used
LED.4	->	Not used
LED.3	->	Not used
LED.2	->	Not used
LED.1	->	set LD2 status
LED.0	->	set LD1 status

Performing a write operation to the allocation address of LED register their status is set as specified in the following correspondance:

Bit at logic 0	->	Activity LED OFF
Bit at logic 1	->	Activity LED ON

Value of bits marked as “Not used” is indifferent.

CONFIGURATION INPUTS

LAD 13 is provided with an on board 8 pins dip switch (DSW1). Their purpose is to set the mapping address for control and data registers of the on board devices and to set the connection modalities for /M1 and /INT signals as in the following table:

SWITCH	CONNECTION	PURPOSE	DEF.
DSW1.1	OFF	Interfacement and addressing section does not manage signal /M1 coming from the BUS.	*
	ON	Interfacement and addressing section manages signal /M1 coming from the BUS.	
DSW1.2	OFF	Does not connect LAD 13 interrupt signal to the oportune signal of ABACO ® BUS.	*
	ON	Connects LAD 13 interrupt signal to the oportune signal of ABACO ® BUS.	

FIGURE 13: CONFIGURATION INPUTS TABLE

EXTERNAL CARDS

LAD 13 can be connected to a wide range of block modules and operator interface system produced by **grifo**[®], or to many system of other companies. The on board resources can be expanded with a simple connection to the numerous peripheral **grifo**[®] boards, both intelligent and not, thanks to its standard **ABACO**[®] BUS connector. Even cards with **ABACO**[®] I/O BUS can be connected, by using the proper mother boards.

Hereunder some of these cards are briefly described; ask the detailed information directly to **grifo**[®], if required.

MB3 01-MB4 01-MB8 01

Mother Board 3, 4, 8 slots

Motherboard featuring 3, 4 or 8 slots of **ABACO**[®] industrial BUS; pitch 4 TE; standard power supply connectors; LEDs for visual feed-back of power supply; holes for rack docking.

SPB 04-SPB 08

Switch Power BUS 4-8 slots

Motherboard featuring 4-8 slots of **ABACO**[®] industrial BUS; pitch 4 TE; standard power supply connectors; termination resistances; connector type F for **SPC xxx** supply ; holes for rack docking.

ABB 03

ABACO[®] Block BUS 3 slots

3 slots **ABACO**[®] mother board; 4 TE pitch connectors; **ABACO**[®] I/O BUS connector; screw terminal for power supply; connection for DIN C type and Ω rails.

ABB 05

ABACO[®] Block BUS 5 slots

5 slots **ABACO**[®] mother board with power supply. Double power supply built in; 5Vdc 2,5A section for powering the on board logic; second section at 24Vdc 400mA galvanically coupled, for the optocoupled input lines. Auxiliary connector for **ABACO**[®] I/O BUS. Connection for DIN Ω rails.

SPC 03.5S

Switch Power Card +5 Vdc

Europe format switching power supply capable to provide +5 Vdc to a load of 4 A; input voltage 12÷24 Vac; power-failure; connector for back-up battery; standard connector for mother board **SPB 0x**.

SPC 512

Switch Power Card +5 Vdc +12 Vdc

Europe format switching power supply capable to provide +5 Vdc 5A and +12 Vdc 2.5 A; input voltage 12÷24 Vac; power-failure; connector for back-up battery; standard connector for mother board **SPB 0x**.

FBC 20-120

Flat Block Contact 20 vie

Interface for 2 or 1 mounting cable connectors (low profile 20 pins male) and quick release screw terminal connectors; Plastic mount for rails DIN 46277-1 and 3.

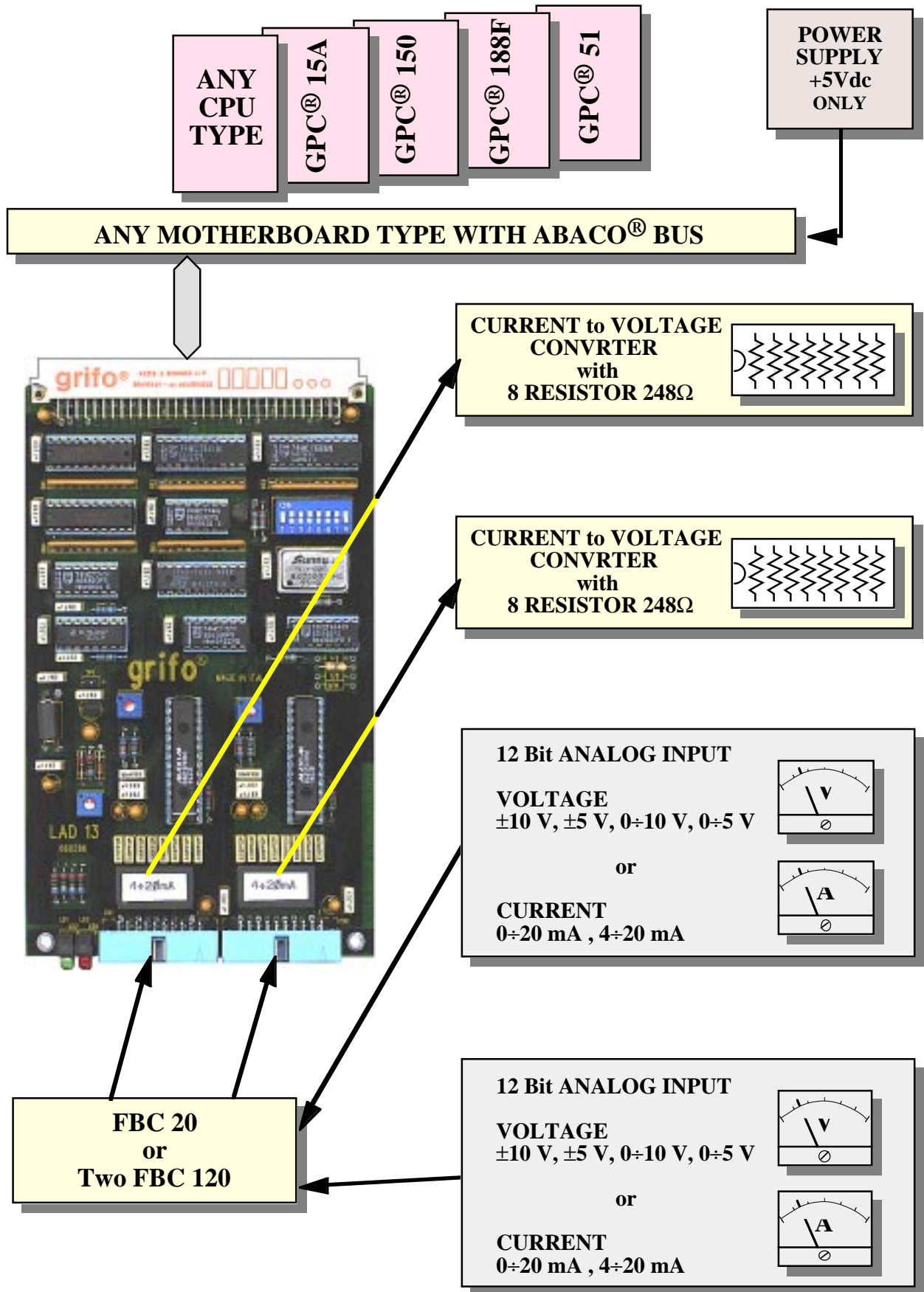


FIGURE 14: POSSIBLE CONNECTIONS DIAGRAM

GPC® 51

General Purpose Controller fam. 51

Microprocessor family 51 INTEL including the masked BASIC chip; the board features: 16 I/O TTL lines; dip switch; 3 timer/counter; RS 232; 4 A/D converter signals resolution 11 bit; buzzer; on board EPROM programmer; RTC and 32K SRAM with Lithium battery back up; controller for display and keyboard.

GPC® 188F

General Purpose Controller 80C188

80C188 μ P 20MHz; 1 RS 232 line; 1 RS 232, RS 422-485 or Current Loop line; 24 TTL I/O lines; 1M EPROM or 512K FLASH; 1M RAM Lithium battery backed; 8K serial EEPROM; RTC; Watch Dog; 8 Dip switch; 3 Timer Counter; 8 13 bit A/D lines; Power failure; activity LEDs; single power supply +5Vdc.

GPC® 15A

General Purpose Controller 84C15

Full CMOS card, 10÷20 MHz 84C15 CPU; 512K EPROM or FLASH; 128K RAM; 8K RAM and RTC backed; 8K serial EEPROM; 1 RS 232 line; 1 RS 232 line or RS 422-485 or Current Loop line; 32 or 40 TTL I/O lines; CTC; Watch dog; 2 Dip switches; Buzzer.

GPC® 150

General Purpose Controller 84C15

Microprocessor Z80 at 16 MHz; implementation completely CMOS; 512K EPROM or FLASH; 512K SRAM; RTC; Back-Up through external Lithium battery; 4M serial FLASH; 1 serial line RS 232 plus 1 RS 232 or RS 422-485 or current loop; 40 I/O TTL; 2 timer/counter; 2 watch dog; dip switch; EEPROM; A/D converter with resolution 12 bit; activity LED.

GPC® 15R

General Purpose Controller 84C15

84C15 μ P, 10÷16 MHz; 1 RS 232 line; 1 RS 232 or RS 422-485 or C. L. line; 16÷24 TTL I/O lines; 16 Opto-in; 8 Relays; 4 Opto Coupled Timers Counters; 512K EPROM or FLASH; 512K RAM and RTC backed; 8K serial EEPROM; 8K Backed RAM modul; Buzzer; 1 Activity LED; Watch dog; 4÷12 readable DIPs; LCD Interface.

GPC® 323

General Purpose Controller 51 family

80C32 μ P, 14 MHz; Full CMOS; 1 RS 232 line (software); 1 RS 232 or RS 422-485 or Current Loop line; 24 TTL I/O lines; 11 A/D 12 bits lines; 3 Timers Counters; 64K EPROM; 64K RAM; 32K RAM and RTC backed; 32K DIL EEPROM; 8K serial EEPROM; Buzzer; 2 Activity LED; Watch dog; 5 readable DIPs; LCD Interface.

GPC® 553

General Purpose Controller 80C552

80C552 μ P, 22÷33 MHz; 1 RS 232 line (software); 1 RS 232 or RS 422-485 or Current Loop line; 16 TTL I/O lines; 8 A/D 10 bits lines; 3 Timers Counters; 64K EPROM; 64K RAM; 32K RAM and RTC backed; 32K DIL EEPROM; 8K serial EEPROM; 2 PWM lines; 1 Activity LED; Watch dog; 5 readable DIPs; LCD Interface.

GPC® 153

General Purpose Controller Z80

84C15 μ P, 10÷16 MHz; Full CMOS; 1 RS 232 line; 1 RS 232 or RS 422-485 or Current Loop line; 16 TTL I/O lines; 8 A/D 12 bits lines; 2÷4 Timers Counters; 512K EPROM or FLASH; 512K RAM and RTC backed; 8K serial EEPROM; Buzzer; 1 Activity LED; Watch dog; 8 readable DIPs; LCD Interface.

GPC® 183

General Purpose Controller Z180

Z180 μ P, 10÷16 MHz; Full CMOS; 1 RS 232 line; 1 RS 232 or RS 422-485 or Current Loop line; 24 TTL I/O lines; 11 A/D 12 bits lines; 2 Timers Counters; 512K EPROM or FLASH; 512K RAM and RTC backed; 8K serial EEPROM; Buzzer; 2 Activity LED; Watch dog; 4 readable DIPs; LCD Interface.

GPC® 324/D

“4” Type General Purpose Controller 80C32/320

80C32 or 80C320 μ P, 14÷22 MHz; Full CMOS; 1 RS 232 line; 1 RS 232 or RS 422-485 or Current Loop line; 4÷16 TTL I/O lines; 3 Timers Counters; 64K EPROM; 64K RAM; 32K RAM backed; 32K DIL E2; 8K serial EEPROM; Watch dog; 1 readable DIP; LCD Interface; Abaco® I/O BUS; 5Vdc Power supply; Size: 100x50 mm.

GPC® 554

General Purpose Controller 80C552

Microprocessor 80C552 at 22 MHz; implementation completely CMOS; 32K EPROM; 32 K SRAM; 32 K EEPROM or SRAM; EEPROM; 2 RS 232 serial lines; 16 I/O TTL; 2 PWM lines; 16 bits Timer/Counter; Watch Dog; 6 signals A/D converter with resolution 10 bit; interface for **ABACO®** I/O BUS.

GPC® 154

“4” Type General Purpose Controller Z80

84C15 μ P, 10÷16 MHz; Full CMOS; 1 RS 232 line; 1 RS 232 or RS 422-485 line; 16 TTL I/O lines; 2÷4 Timers Counters; 512K EPROM or FLASH; 512K RAM and RTC backed; 8K serial EEPROM; Watch dog; 2 readable DIPs; LCD Interface; Abaco® I/O BUS; 5Vdc Power supply; Size: 100x50 mm.

GPC® 884

General Purpose Controller Am188ES

Microprocessor AMD Am188ES up to 40 MHz 16 bits; implementation completely CMOS; serie 4 format; 512K EPROM or FLASH; 512K SRAM backed with Lithium battery; RTC; 1 RS 232 serial line + 1 RS 232 or RS 422-485 or current loop; 16 I/O TTL; 3 timer/counter; watch dog; EEPROM; 11 signals A/D converter with 12 bit resolution; interface for **ABACO®** I/O BUS.

GPC® 114

General Purpose Controller 68HC11

Microprocessor 68HC11A1 at 8 MHz; implementation completely CMOS; serie 4 format; 32K EPROM; 32K SRAM backed with Lithium battery; 32K EPROM, SRAM, EEPROM; RTC; 1 serial line RS 232 or RS 422-485; 10 I/O TTL; 3 timer/counter; watch dog; 8 signals A/D converter with resolution 8 bit; 1 asynchronous serial line; extremely low power consumption; interface for **ABACO®** I/O BUS.

BIBLIOGRAPHY

Here follows a list of manuals that can be a source of further information about the devices installed on **LAD 13**.

Manual TEXAS INSTRUMENTS:	<i>The TTL Data Book - SN54/74 Families</i>
Manual SGS-THOMSON:	<i>Programmable logic manual - GAL products</i>
Manual MAXIM:	<i>New Releases Data Book 1996 - Volume V</i>
Manual NATIONAL SEMICONDUCTOR:	<i>DataBook - Linear 2</i>

Please connect to the manufacturer's Web sites to get the latest version of all manuals and data sheets.

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