LAD 12

Low cost Analog to Digital 12 bits

TECHNICAL MANUAL

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ITALIAN TECHNOLOGY

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LAD 12 Edition 5.10 *Rel. 28 March 2001*

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Eurocard format size 100x160 mm; interface to **ABACO**® industrial BUS; 16 analog to digital conversion lines with resolution 12 bits plus sign; conversion speed 130 msec and full range ±2.048 Vdc; 2 inipendent A/D converter sections based on as many TSC 7109A double slope precision converters; voltage full range ±2.048 Vdc or, optionally, current input ranges 0÷20 mA or 4÷20 mA using current-to-voltage converter module (code **.8420**); noise reduction low-pass filter on each analog input; DC/DC converter on board to generate all the voltages needed by A/D sections; circuitry to generate interrupts on **ABACO**® BUS provided with two visualization LEDs; 2 software readable TTL inputs; 2 software manageable activity LEDs; I/O mapping through on board dip switch; only as low as **4 bytes** taken; 2 standard 20 pins low profile connectors for analog signals input ; direct interfacement to **FBC** field modules; unique power supply **+5Vdc**

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For specific informations on the components mounted on the card, please refer to the Data Book of the builder or second sources.

SYMBOLS DESCRIPTION

In the manual could appear the following symbols:

Attention: Generic danger

Attention: High voltage

Trade Marks

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GENERAL INDEX

FIGURES INDEX

INTRODUCTION

The use of these devices has turned - IN EXCLUSIVE WAY - to specialized personnel.

The purpose of this handbook is to give the necessary information to the cognizant and sure use of the products. They are the result of a continual and systematic elaboration of data and technical tests saved and validated from the manufacturer, related to the inside modes of certainty and quality of the information.

The reported data are destined- IN EXCLUSIVE WAY- to specialized users, that can interact with the devices in safety conditions for the persons, for the machine and for the enviroment, impersonating an elementary diagnostic of breakdowns and of malfunction conditions by performing simple functional verify operations , in the height respect of the actual safety and health norms.

The informations for the installation, the assemblage, the dismantlement, the handling, the adjustment, the reparation and the contingent accessories, devices etc. installation are destined - and then executable - always and in exclusive way from specialized warned and educated personnel, or directly from the TECHNICAL AUTHORIZED ASSISTANCE, in the height respect of the manufacturer recommendations and the actual safety and health norms.

The devices can't be used outside a box. The user must always insert the cards in a container that rispect the actual safety normative. The protection of this container is not threshold to the only atmospheric agents, but specially to mechanic, electric, magnetic, etc. ones.

To be on good terms with the products, is necessary guarantee legibility and conservation of the manual, also for future references. In case of deterioration or more easily for technical updates, consult the AUTHORIZED TECHNICAL ASSISTANCE directly.

To prevent problems during card utilization, it is a good practice to read carefully all the informations of this manual. After this reading, the user can use the general index and the alphabetical index, respectly at the begining and at the end of the manual, to find information in a faster and more easy way.

CARD VERSION

The present handbook is reported to the **LAD 12** card release **050595** and later. The validity of the bring informations is subordinate to the number of the card release. The user must always verify the correct correspondence among the two denotations. On the card the release number is present in more points both board printed diagram (serigraph) and printed circuit (for example between trimmer RV2 and the four LEDs both on the component side and on the solder side).

GENERAL INFORMATION

LAD 12 (**L**ow cost **A**nalog to **D**igital converter 12 bits) is a powerful Eurocard format card, provided with **ABACO®** industrial BUS interface. This card belongs to the analog peripherals units list and, in specific, its purpose is to provide sixteen high precision Analog to Digital conversion lines.
Two indipendent A/D Converter circuitries, based on as many **TSC 7109A**, warrant a complete separation of the signals. A/D circuitry features **12 bits** of resolution plus sign, conversion time **130 msec** and full range **2.048 Vdc**. The analog signals are connected through two standard 20 pins low profile connector, 8 analog lines per connector.
Each line is provided with a low-pass fileter to enhance noise immunity; the signal to be acquired can be configured as voltage (**±2.048 Vdc**) or current (**0÷20 mA** or **4÷20 mA**) indipenndently for each section simply by installing an optional current-to-voltage conversion module (option code**.8420**).
A DC/DC converter is charged to generate all the voltages essential for the correct working from the unique power supply of +5 Vdc.
LAD 12 board features also two TTL signals that allow to improve the board potentialities; for example it is possible to perform conversions triggered by specific signals coming from external devices.
The two 20 pins output connectors allows an immediate interfacing to modules for the field, like BLOCK type **FBC**, that untangle the signals from the flat cable to comfortable quick release screw terminal connectors.
Two frontal LEDs, one each A/D section, inidicate the end of a conversion and the generation of an **interrupt** to the CPU control card; two more LEDs, put in the same location, are completely software manageable so the user can employ them as activity LEDs.
LAD 12 card can be driven through any CPU board in the **ABACO®** listing and takes as low as 4 contiguous bytes in the addressing space.
LAD 12 is the ideal component for all the applications where highconversion speed, high precision, several lines and low costs are required.
Amongst its various applications we would want to remark: interfacement to transductors, like pressure, temperature, humidity, optical sensors, etc.
Overall features of **LAD 12** are as follows:

- Eurocard format size 100x160 mm
- Interface to **ABACO®** industrial BUS
- **16** analog to digital conversion lines with resolution **12 bits plus sign** ,conversion speed **130 msec** and full range **±2.048 Vdc**
- **2** inipendent A/D converter sections based on as many **TSC 7109A double slope precision converters**
- Voltage full range ±2.048 Vdc or, optionally, current input ranges 0÷20 mA or 4÷20 mA using current-to-voltage converter module (code **.8420**)
- Noise reduction low-pass filter on each analog input
- DC/DC converter on board to generate all the voltages needed by A/D sections
- Circuitry to generate **interrupts** on **ABACO®** BUS provided with two visualization **LEDs**
- 2 software readable **TTL inputs**
- 2 software manageable activity **LEDs**
- I/O mapping through on board **dip switch**
- Only as low as **4 bytes** taken
- **2** standard **20 pins** low profile connectors for analog signals input
- Direct interfacement to **FBC** field modules
- Unique power supply **+5Vdc**

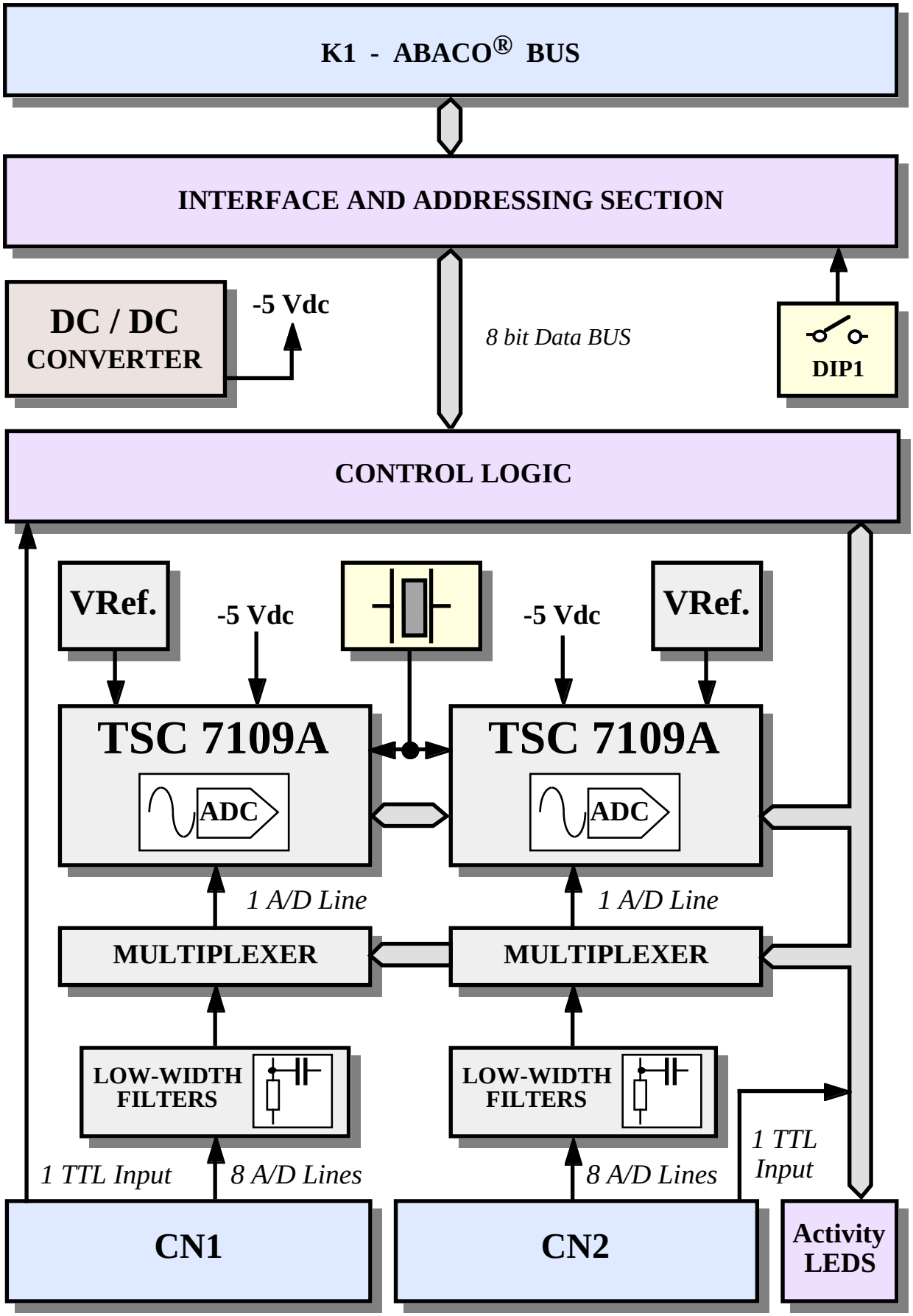

FIGURE 1: BLOCK DIAGRAM

Here follows a description of **LAD 12** board's functional blocks, with an indication of the operations performed by each one. To easily locate these blocks and verify their connections pleare refer to figure 1.

INTERFACING AND ADDRESSING

This section manages the data exchange between contol logic and command board through **ABACO®** BUS. In particular, all written or read data transit across this section that, in addition, provides the board I/O management in a 256 or 512 bytes addressing space, by setting the dip switch **DIP1**.
For further information please refer to the chapter dedicated to board's software description.

CONTROL LOGIC

This section generates all the chip select signals needed to acces the several peripherals on **LAD 12** boards. Using this section the programmer can interact to the board's several sections, verifing their status, setting configuration of A/D converters, etc.
All this can be done through a simple software management based on **ABACO®** BUS, to which the contol logic connects through the interfacing and addressing section. For further information please refer to chapter “PERIPHERAL DEVICES SOFTWARE DESCRIPTION”.

DC/DC CONVERTER

A positive booster installed on **LAD 12** board is charged to provide the voltages needed by the digital to analog conversion section. Such DC/DC converter generates the -5 Vdc voltage starting from the unique +5 Vdc power supply and needs no software management.

CLOCK

LAD 12 is provided with an oscillator circuit to generate the clock signals indipendently needed by the two A/D converter sections. Required frequences are generated from a 3.6864 MHz quartz. Such frequence determines the time succession of the several A/D conversion phases process, its value has been chosen to optimize both conversion time and noise immunity.

REFERENCE VOLTAGES

A specific precision circuitery is charged to generate the reference voltage (**Vref**) required by the A/D converters. Such voltage is perfectly stabilized and indipendent from the board supply and temperature variations, so to increase **LAD 12** precision and reliability.
Each A/D converter has its own indipendent **Vref** setting.
For further information please see paragraph “TRIMMERS AND CALIBRATION”.

A/D CONVERTER

LAD 12 board features two indipendent A/D converter sections based on as many **TSC 7109A**, these are precision A/D converters that take advantage of the double slope technique. This allows to feature the same precision of standard double slope converters and, in addition, allows to reduce the effects due to input anlog signal multiplexing and so to obtain a greater number of conversions per second. Overall features are:

- Resolution 12 bits plus sign
- high noise immunity
- Max linearity error ±1 LSB
- Max roll-over error ±1 LSB
- Max conversion time per channel is 130 msec
- High input impedance
- Analog internal circuitery requires no calibrations (self zero)
- Quick calibration after an input runs out of range

TSC 7109A is the ideal component for the typical application of industrial automation, where a high conversion speed and a high grade of precision are required.
For further information about this component please refer to manufacturer documentation.

The signal to acquire can be configured as voltage (**±2.048 Vdc**) or current (**0÷20 mA** or **4÷20 mA**) indipendently for each section simply by installing an optional current-to-voltage conversion module (option code**.8420**).
Each line is provided with a low-pass fileter to enhance noise immunity.

MULTIPLEXER

The sixteen analog input signals are divided in two groups of 8 lines, such groups are multiplexed to the A/D converters sections inputs. The multiplexing sections of **LAD 12** are based on two solid state multiplexers that are directly software managed through the on board control logic.
For further information please see the chapter “PERIPHERAL DEVICES SOFTWARE DESCRIPTION”.

TTL INPUT SIGNALS AND ACTIVITY LEDS

LAD 12 board features also two TTL signals that allow to improve the board potentialities; for example it is possible to perform conversions triggered by specific signals coming from external devices.
In addition two completely software manageable LEDs can bu used as activity LEDs.
For further information please see the chapter “PERIPHERAL DEVICES SOFTWARE DESCRIPTION”.

TECHNICAL FEATURES

GENERAL FEATURES

On board resources:	16 analog inputs (two 8 channels A/D converters) 2 TTL digital inputs 2 software manageable activity LEDs 1 eight pins dip switch to set I/O address
BUS type:	Industrial **ABACO®** 8 bits data BUS
Addressing space:	256 or 512 bytes
Bytes taken:	4
On board peripherals:	TSC 7109A 74 HCT 4051
A/D external clock frequence:	3.6864 MHz
A/D max conversion time:	130 msec per channel
A/D resolution:	12 bits + sign
A/D max linearity:	±1 LSB (*)
A/D max roll-over error:	±1 LSB (*)

PHYSICAL FEATURES

Size:	Standard EUROCARD format 100x160 mm
Weight:	148 g
Connectors:	K1: DIN 41612 64 pins M 90° A+C type C CN1: 20 pins low profile M 90° CN2: 20 pins low profile M 90°
Temperature range:	from 0 to 70° C
Relative humidity:	20% up to 90% (without condensing)

(*) Values referred to a working temperature of 25 °C

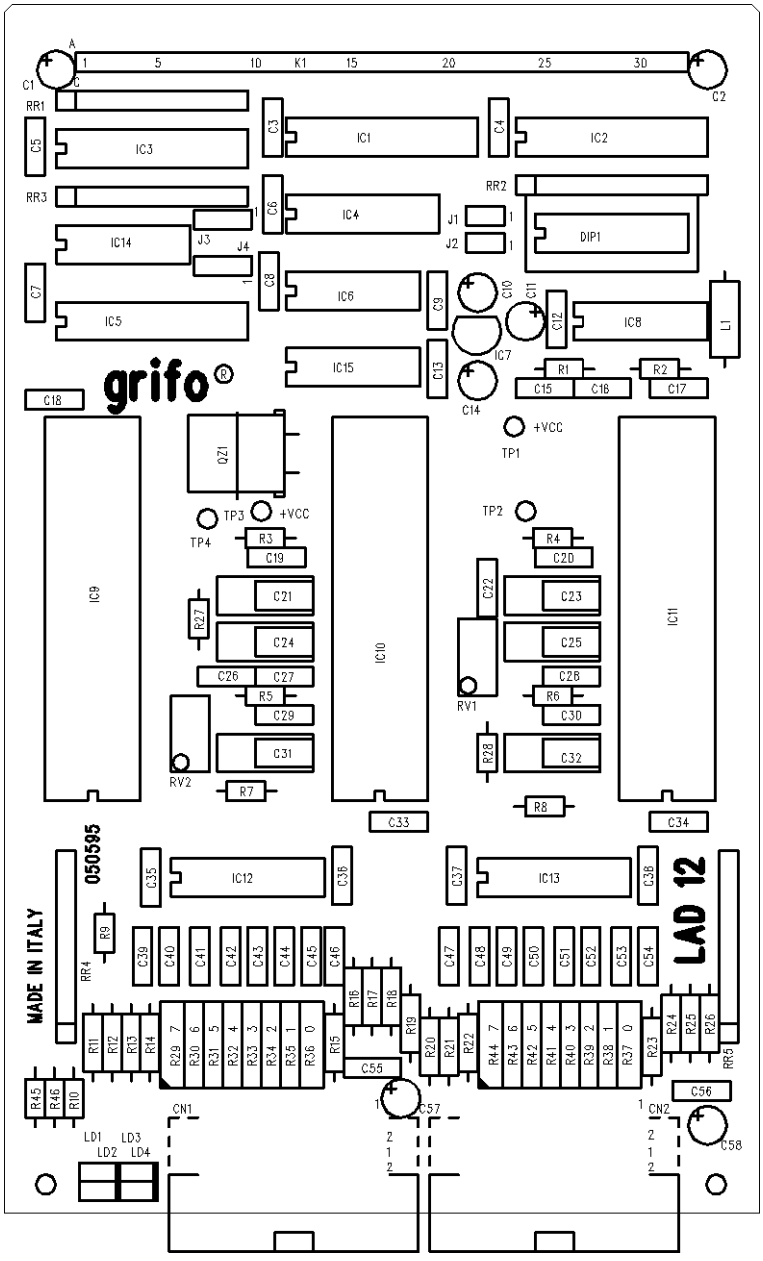

FIGURE 2: COMPONENTS MAP

ELECTRIC FEATURES

Power supply:	+5 Vdc ± 5%
Current consumption:	120 mA
A/D input impedance:	very high, not declared by manufacturer
Analog inputs:	±2.048 Vdc 0÷20 mA or 4÷20 mA
Current-to-voltage conversion resistors:	100 Ω
A/D reference voltages:	Generated on board
Noise reduction filters:	Low-pass filters
TTL voltage levels:	0 Vdc (low level); +5 Vdc (high level)

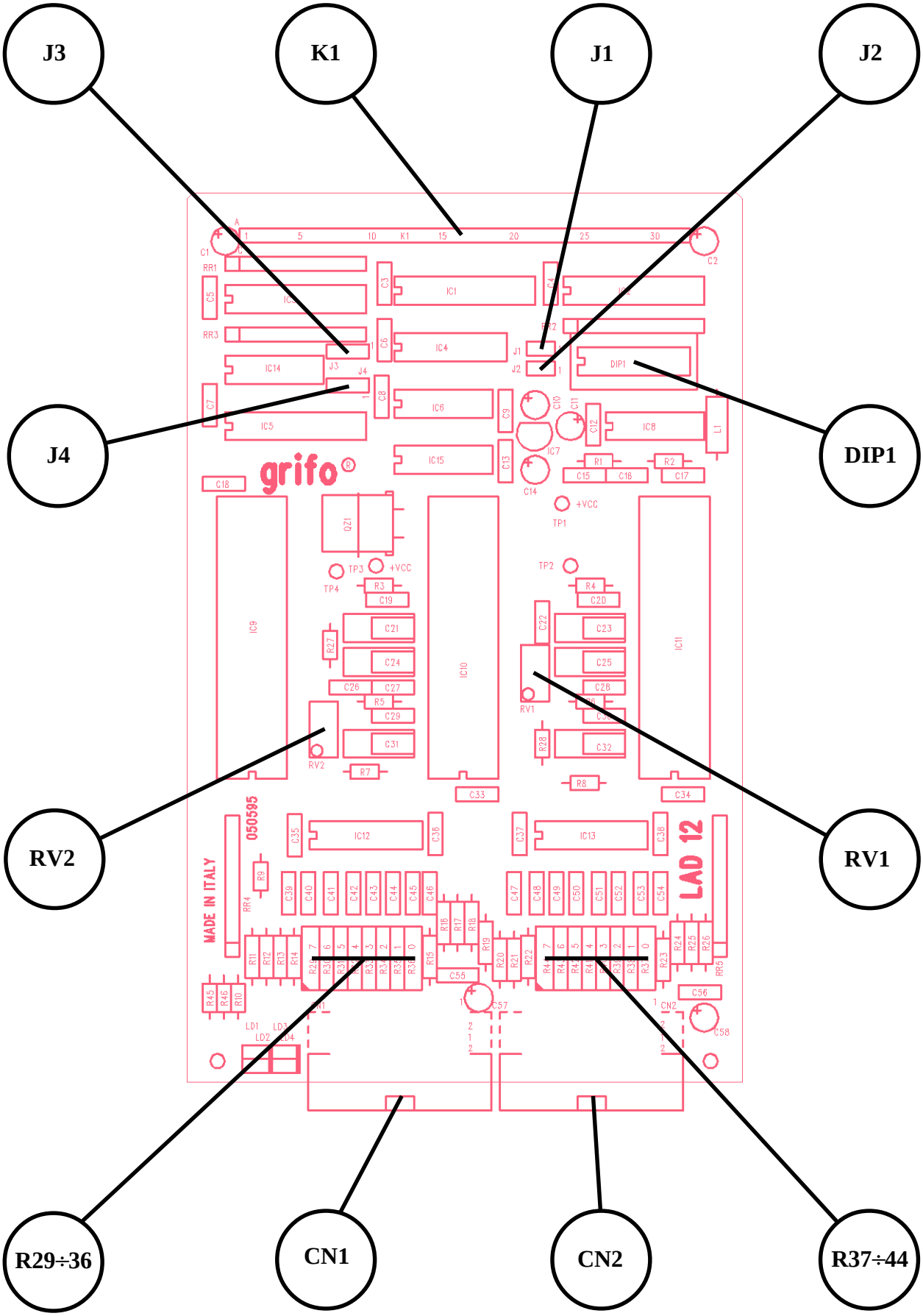

FIGURE 3: CONNECTORS, DIP-SWITCH, JUMPERS, TRIMMES, ETC. LOCATION

INSTALLATION

In this chapter there are the information for a right installation and correct use of **LAD 12** card. The user can find the location and functions of each connectors, LEDs, trimmer and some explanatory diagrams.

CONNECTIONS

The board has three connectors that can be linkeded to other devices or directly to the field, according to system requirements. In this paragraph there are connectors pin outs, a short signals description (including the signals direction) and connectors location, plus some figures that describe how the interface signals are connected on the card. To easily locate the connectors please refer to figure 3.

CN1 - ANALOG INPUTS SECTION A CONNECTOR

The connector for the eight analog inputs and the TTL digital input section A, called CN1, is a 20 pins low profile male 90 degreeses connector with 2.54 mm pitch.
The lines available on CN1 feature high input impedance and a low-pass filter to reduce the electric noise coming from the external world. The signals on these lines may vary in the range ±2.048 Vdc or 0÷20 mA or 4÷20 mA if the board is provided with the current-to-voltage conversion module code **.8420**. Signals placement on the connector has been designed to reduce problems of noise and interference and to warrant a good transmission quality.

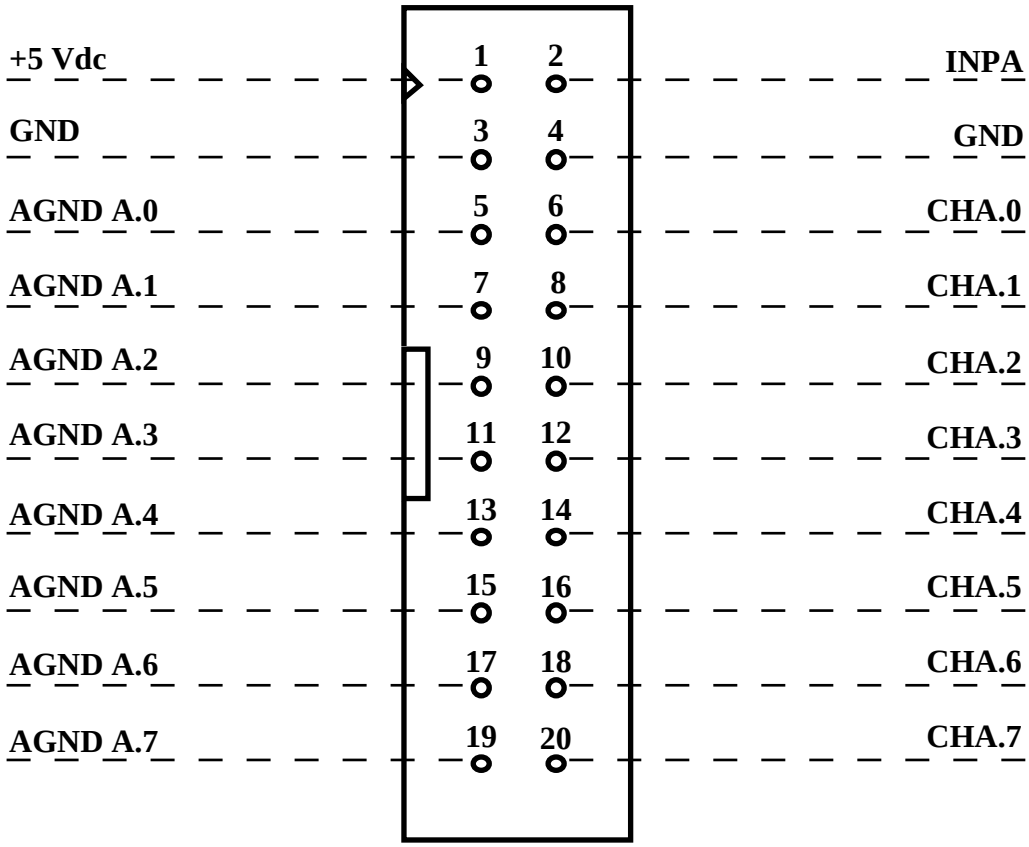

FIGURE 4: CN1 - ANALOG INPUTS CONNECTOR SECTION A

Signals description:

CHA.n = I - A/D channel n-th section A input
AGNDA.n = I - A/D channel n-th section A input analog ground and shielding line
INPA = I - Digital TTL input A
+5 Vdc = O - +5 Vdc power supply
GND = - Ground

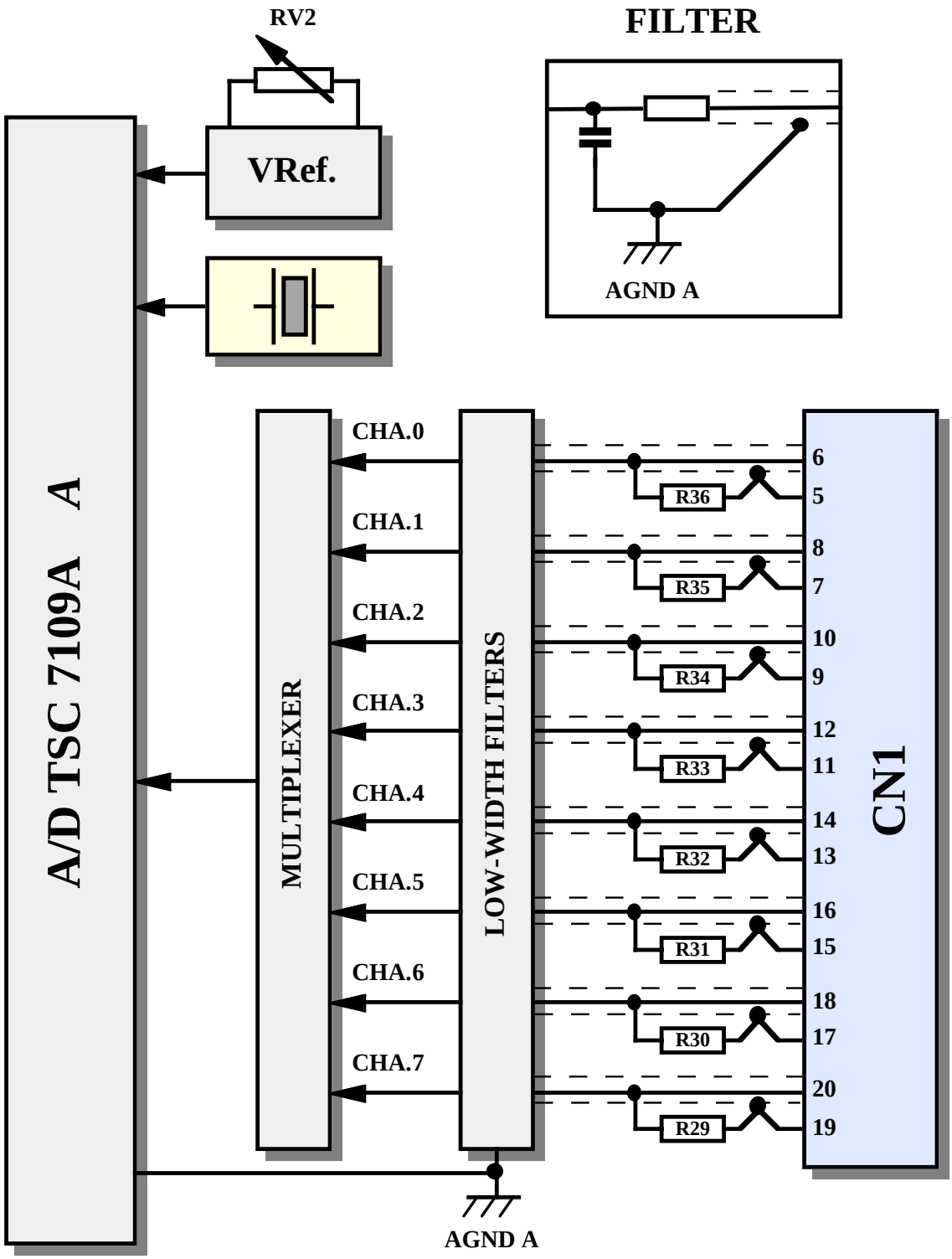

FIGURE 5: SECTION A A/D CONVERTER BLOCK DIAGRAM

CN2 - ANALOG INPUTS SECTION B CONNECTOR

The connector for the eight analog inputs and the TTL digital input section B, called CN2, is a 20 pins low profile male 90 degreeses connector with 2.54 mm pitch.
The lines available on CN2 feature high input impedance and a low-pass filter to reduce the electric noise coming from the external world. The signals on these lines may vart in the range ±2.048 Vdc or 0÷20 mA or 4÷20 mA if the board is provided with the current-to-voltage conversion module code **.8420**. Signals placement on the connector has been designed to reduce problems of noise and interference and to warrant a good transmission quality.

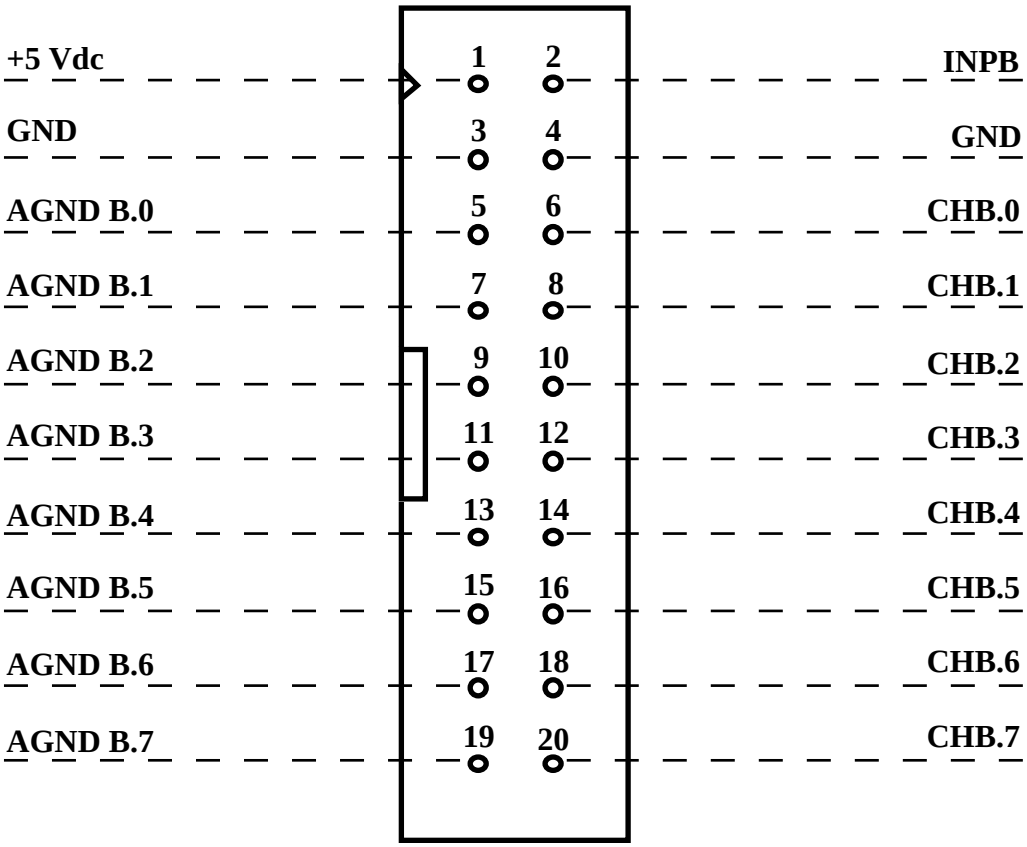

FIGURE 6: CN2 - ANALOG INPUTS CONNECTOR SECTION B

Signals description:

CHB.n	=	I	- A/D channel n-th section B input
AGNDB.n	=	I	- A/D channel n-th section B input analog ground and shielding line
INPB	=	I	- Digital TTL input B
+5 Vdc	=	O	- +5 Vdc power supply
GND	=		- Ground

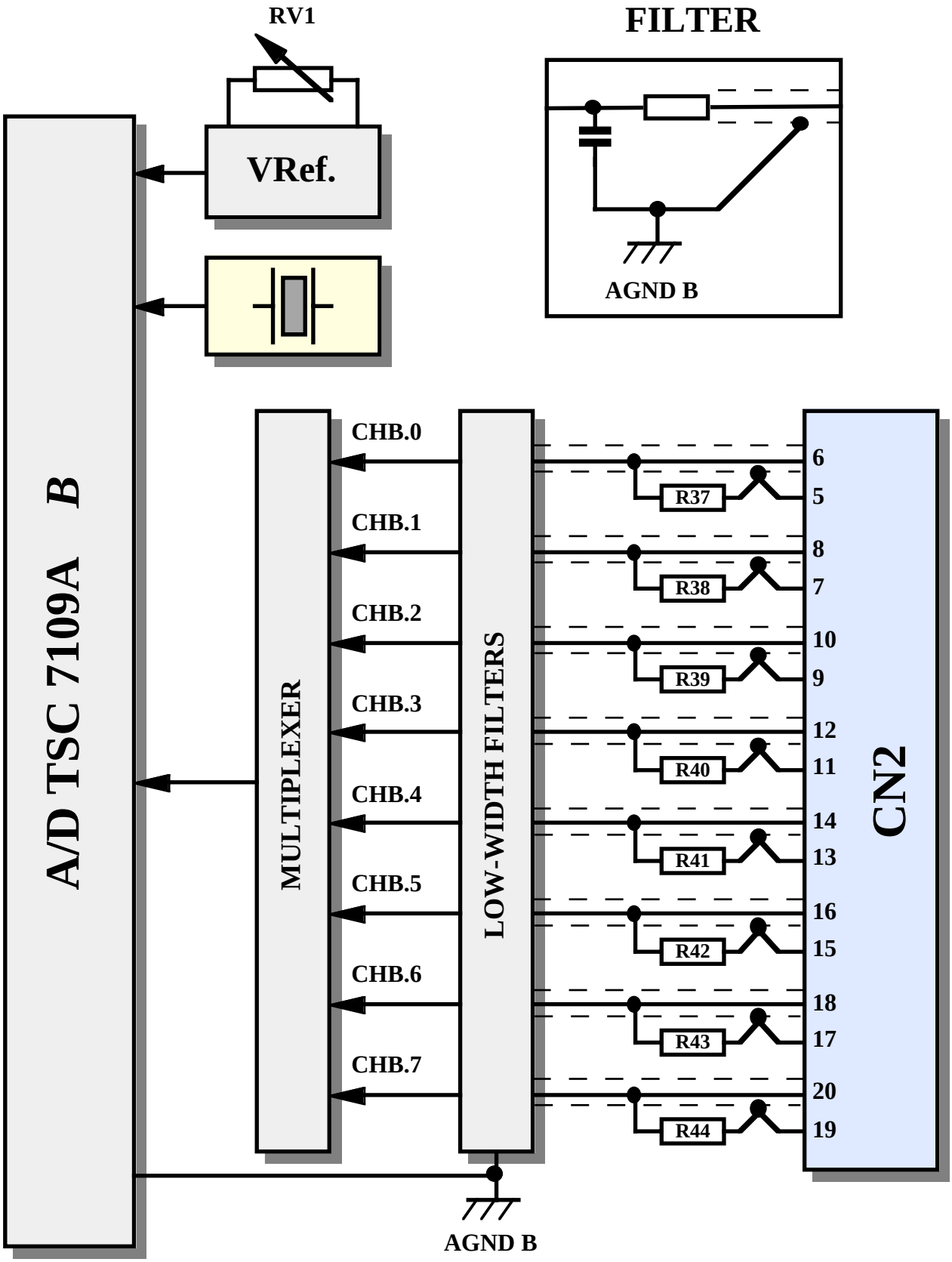

FIGURE 7: SECTION B A/D CONVERTER BLOCK DIAGRAM

K1 - CONNECTOR FOR ABACO® BUS

The connector for **ABACO® industrial BUS**, called K1 on the board,is a DIN 41612, male, a 90 °, type C, A+C.
Here follows the pin-out of the connector installed on **LAD 12**, in addition there is the standard 8 bits and 16 bits**ABACO®** BUS pin-out.
Please remark that all the signals here described are TTL, except for the power supplies.

A 16 bit BUS	A 8 bit BUS	A LAD 12	PIN	C LAD 12	C 8 bit BUS	C 16 bit BUS
GND	GND	GND	1	GND	GND	GND
+5 Vdc	+5 Vdc	+5 Vdc	2	+5 Vdc	+5 Vdc	+5 Vdc
D0	D0	D0	3	N.C.		D8
D1	D1	D1	4	N.C.		D9
D2	D2	D2	5	N.C.		D10
D3	D3	D3	6	/INT	/INT	/INT
D4	D4	D4	7	N.C.	/NMI	/NMI
D5	D5	D5	8	N.C.	/HALT	D11
D6	D6	D6	9	N.C.	/MREQ	/MREQ
D7	D7	D7	10	/IORQ	/IORQ	/IORQ
A0	A0	A0	11	/RD	/RD	/RDLDS
A1	A1	A1	12	/WR	/WR	/WRLDS
A2	A2	A2	13	N.C.	/BUSAK	D12
A3	A3	A3	14	N.C.	/WAIT	/WAIT
A4	A4	A4	15	N.C.	/BUSRQ	D13
A5	A5	A5	16	/RESET	/RESET	/RESET
A6	A6	A6	17	/M1	/M1	/IACK
A7	A7	A7	18	N.C.	/RFSH	D14
A8	A8	A8	19	N.C.	/MEMDIS	/MEMDIS
A9	A9	N.C.	20	N.C.	VDUSEL	A22
A10	A10	N.C.	21	N.C.	/IEI	D15
A11	A11	N.C.	22	N.C.		
A12	A12	N.C.	23	N.C.	CLK	CLK
A13	A13	N.C.	24	N.C.		/RDUDS
A14	A14	N.C.	25	N.C.		/WRUDS
A15	A15	N.C.	26	N.C.		A21
A16		N.C.	27	N.C.		A20
A17		N.C.	28	N.C.		A19
A18		N.C.	29	N.C.	/R.T.	/R.T.
+12 Vdc	+12 Vdc	N.C.	30	N.C.	-12 Vdc	-12 Vdc
+5 Vdc	+5 Vdc	+5 Vdc	31	+5 Vdc	+5 Vdc	+5 Vdc
GND	GND	GND	32	GND	GND	GND

FIGURE 8: K1 - CONNECTOR FOR ABACO® BUS

Signals description:

8 bits CPU

A0-A15	=	O	- Address BUS
D0-D7	=	I/O	- Data BUS
/INT	=	I	- Interrupt request
/NMI	=	I	- Non Maskable Interrupt
/HALT	=	O	- Halt state
/MREQ	=	O	- Memory Request
/IORQ	=	O	- Input Output Request
/RD	=	O	- Read cycle status
/WR	=	O	- Write cycle status
/BUSAK	=	O	- BUS Acknowledge
/WAIT	=	I	- Wait
/BUSRQ	=	I	- BUS Request
/RESET	=	O	- Reset
/M1	=	O	- Machine cycle one
/RFSH	=	O	- Refresh for dynamic RAM
/MEMDIS	=	I	- Memory Display
VDUSEL	=	O	- VDU Selection
/IEI	=	I	- Interrupt Enable Input
CLK	=	O	- System clock
R.B.	=	I	- Reset button
+5 Vdc	=	I	- Power supply at +5 Vdc
+12 Vdc	=	I	- Power supply at +12 Vdc
-12 Vdc	=	I	- Power supply at -12 Vdc
GND	=		- Ground signal

16 bits CPU

A16-A22	=	O	- Address BUS
D8-D15	=	I/O	- Data BUS
/RD UDS	=	O	- Read Upper Data Strobe
/WR UDS	=	O	- Write Upper Data Strobe
/IACK	=	O	- Interrupt Acknowledge
/RD LDS	=	O	- Read Lower Data Strobe
/WR LDS	=	O	- Write Lower Data Strobe

NOTE
Directionality indications as above stated are referred to a master (**GPC®**) board and have been kept untouched to avoid ambiguity in case of multi-boards systems.

VISUAL SIGNALATIONS

LAD 12 card is provided with four signalation LEDs to show several status informations, as described in the following table:

LED	COLOUR	PURPOSE
LD1	Green	Software managed activity LED.
LD2	Green	Software managed activity LED.
LD3	Red	It turns ON at the end of the conversion, when the A/D converter of section A generates an interrupt.
LD4	Red	It turns ON at the end of the conversion, when the A/D converter of section B generates an interrupt.

FIGURE 9: VISUAL SIGNALATIONS TABLE

The main purpose of LEDs is to show a visual indication about the card's status, making so easier debug and verify operations. All the LEDs are in the front of the board, near connector CN1. To easily locate these visual signalations please refer to figure 10.

POWER SUPPLY

LAD 12 is provided with an efficent circuitery that solves in a comfortable and simple way the problem of the board's supply, under any condition of use.
Here follow the voltages nedded:

+5 Vdc: Supplies the on board logic; must be in the range +5 Vdc ± 5% and must be provided through the specific pins of connector K1 (**ABACO®** BUS).

A positive booster installed on **LAD 12** board is charged to provide the voltages needed by the digital to analog conversion section. Such DC/DC converter generates the voltages needed starting from the unique +5 Vdc power supply and needs no software management.

To warrant great immunity to external noise and so a correct working of the board, it is essential that **+5 Vdc** tension is galvanically isolated.

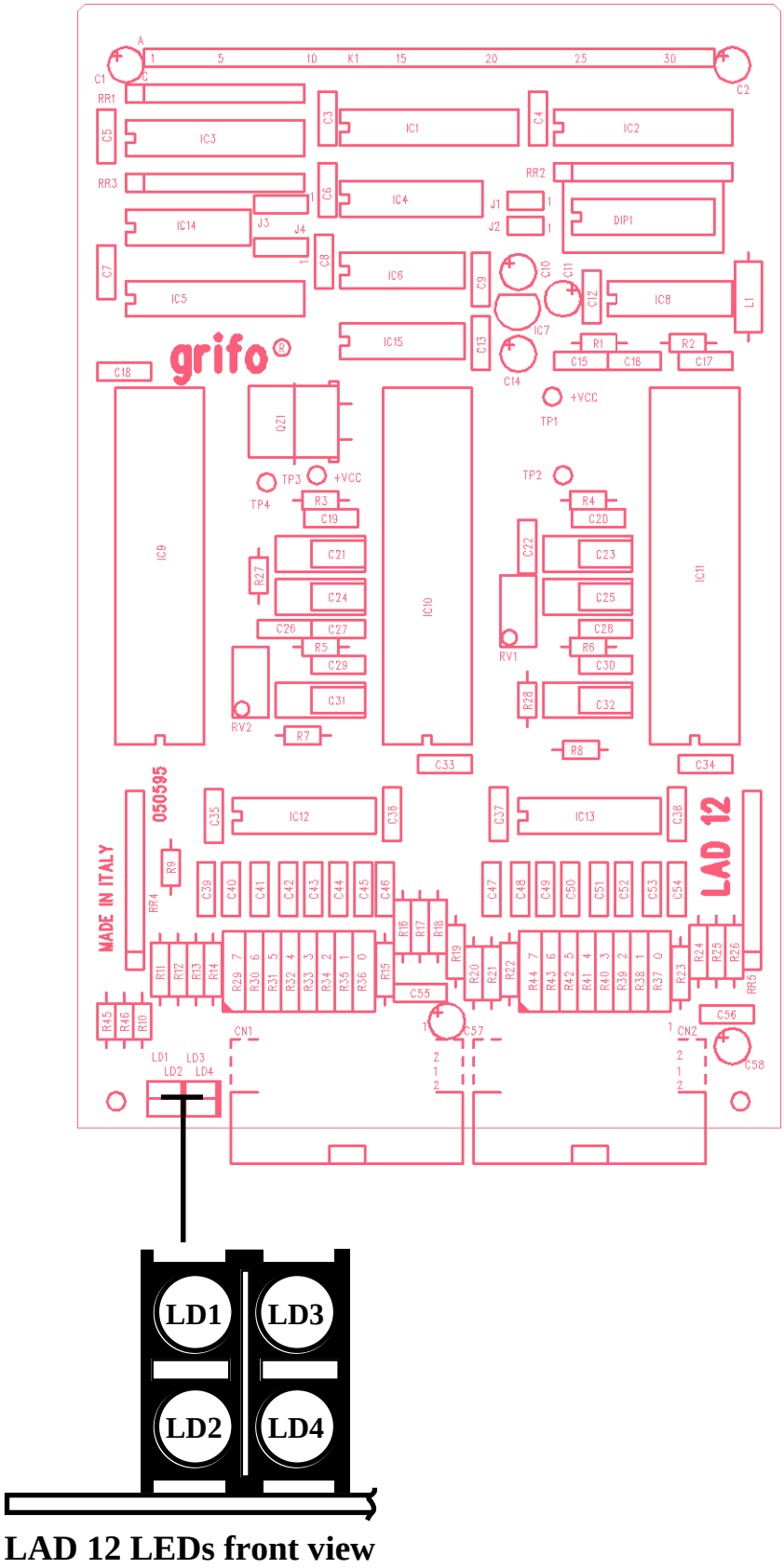

FIGURE 10: LEDS LOCATION

JUMPERS

On **LAD 12** board there are 4 jumpers for card configuration. Below there is the jumpers list, location and function.

JUMPERS	N. PINS	PURPOSE
J1	2	It selects the addressing range for the board between 256 bytes or 512 bytes.
J2	2	It selects the connection modality for signal /M1 coming from **ABACO®** BUS on the board.
J3	3	It selects the connection modality of A/D converter on section A interrupt signal to the /INT signal of **ABACO®** BUS.
J4	3	It selects the connection modality of A/D converter on section B interrupt signal to the /INT signal of **ABACO®** BUS.

FIGURE 11: JUMPERS SUMMARIZING TABLE

The following tables describe all the right connections of **LDA 12** jumpers with their relative functions. To recognize these valid connections, please refer to the board printed diagram (serigraph) or to figure 2 of this manual, where the pins numeration is listed; for recognizing jumpers location, please refer to figure 3.
The "*" used in the following tables, denotes the default connection, or on the other hand the connection set up at the end of testing phase, that is the configuration the User receives.

2 PINS JUMPERS

JUMPER	CONNECTION	PURPOSE	DEF.
J1	not connected	Selects the 256 bytes addressing range.	*
	connected	Selects the 512 bytes addressing range, connecting also address line A8 to interfacing and addressing circuitery.	
J2	not connected	Addressing and interfacing circuitery does not manage /M1 signal coming from **ABACO®** BUS.	
	connected	Addressing and interfacing circuitery manages /M1 signal coming from **ABACO®** BUS.	*

FIGURE 12: 2 PINS JUMPERS TABLE

3 PINS JUMPERS

JUMPER	CONNECTION	PURPOSE	DEF.
J3	position 1-2	Connects the interrupt signal generated by A/D converter of section A to singal /INT on **ABACO®** BUS.	
	position 2-3	Does not connect the interrupt signal generated by A/D converter of section A to singal /INT on **ABACO®** BUS.	*
J4	position 1-2	Connects the interrupt signal generated by A/D converter of section B to singal /INT on **ABACO®** BUS.	
	position 2-3	Does not connect the interrupt signal generated by A/D converter of section B to singal /INT on **ABACO®** BUS.	*

FIGURE 13: 3 PINS JUMPERS TABLE

TYPE OF ANALOG INPUT SELECTION

LAD 12 board can accept analog voltage and/or current inputs, as described in the previous paragraphs and chapters. The input type selection must be made during the order phase and is performed mounting a specific current-to-voltage conversion module (option code **.8420**) made by precision resistors. In detail:

R36	->	channel CHA.0
R35	->	channel CHA.1
R34	->	channel CHA.2
R33	->	channel CHA.3
R32	->	channel CHA.4
R31	->	channel CHA.5
R30	->	channel CHA.6
R29	->	channel CHA.7
R37	->	channel CHB.0
R38	->	channel CHB.1
R39	->	channel CHB.2
R40	->	channel CHB.3
R41	->	channel CHB.4
R42	->	channel CHB.5
R43	->	channel CHB.6
R44	->	channel CHB.7

Should the current-to-voltage conversion module not to be mounted (default case) the corresponding channel accepts a voltage input signal in the range ± 2.048 Vdc; otherwise a current input signal is accepted in the range 0÷20 mA.

The value of the above mentioned resistors is obtained by the following spread;

R = 2.048 V / Imax

Usually the current-to-voltage conversion modules are made using **100 Ω** precision resistors, corresponding to input ranges 4÷20 mA or 0÷20 mA.
Any eventual configuration out of this standard shold be asked directly to **grifo®**.
To easily locate the current-to-voltage conversion module please refer to figure 3.

TRIMMERS AND CALIBRATION

On **LAD 12** board there are two trimmers, called **RV1** and **RV2**, that calibrate the output voltages of the A/D converter sections; in detail it allows to set reference voltage for both sections.
The **LAD 12** is subjected to a careful test that verifies and calibrates all the card sections.
The calibration is executed in laboratory, with a conntrolled +20° C room temperature, following these steps:

- Trimmer **RV2** is used to calibrate the reference voltage of A/D converter on section **A**. In detail, the full range voltage is provided to each input of the section through a calibrator, then the trimmer value is changed until the correspondance between the analog input signal and the combination read from A/D is verified. This check is performed with a reference signal connected to A/D inputs and testing that the A/D combination and the theoric combination differ at maximum of the A/D section errors sum.

- Trimmer **RV1** is used to calibrate the reference voltage of A/D converter on section **B**. In detail, the full range voltage is provided to each input of the section through a calibrator, then the trimmer value is changed until the correspondance between the analog input signal and the combination read from A/D is verified. This check is performed with a reference signal connected to A/D inputs and testing that the A/D combination and the theoric combination differ at maximum of the A/D section errors sum.

- The trimmers are blocked with paint.

The analog interfaces use high precision components that are selected during mounting phase to avoid complicate and long calibration procedures. After the calibration, the on board trimmers are blocked with paint to mantain calibration also in presence of mechanic stresses (vibrations, movings, delivery, etc.).
The user most not intervent on the circuit that generates the reference voltage, however if this should be necessary (example: for time derives) then he/she must follow the above mentioned procedure.
To easily locate the above mentioned components please refer to figure 3; for further information about test points please refer to the previous paragraph; for further information about how to set the A/D converters output voltages please refer to chapter “PERIPHERAL DEVICES SOFTWARE DESCRIPTION”.

FIGURE 14: CARD PHOTO

INTERRUPT

LAD 12 is provided with a comfortable and efficent interrupt generation circuitery, that, if enabled, can generate an interrupt to the **ABACO®** BUS when one of the two analog to digital converter sections reach the end of a conversion. Such circuitery allows to optimize the time needed to manage the board, in fact the **GPC®** intelligent control card is not obliged to poll **LAD 12** registers, but can simply wait for an interrupt and read the conversion results.
Here follows a short description of the devices that can generate an interrupt; for more information about interrupts management please refer to the technical manual of the **GPC®** card being used.

- TSC 7109A, section A -> If jumper J3 is in position 1-2, it generates an /INT on **ABACO®** BUS when the end of a conversion occours; this interrupt event is automatically reset, when the value measured by A/D converter on section A is read.
  The status of this interrupt is visualized by LED LD3.

- TSC 7109A, section B -> If jumper J4 is in position 1-2, it generates an /INT on **ABACO®** BUS when the end of a conversion occours; this interrupt event is automatically reset, when the value measured by A/D converter on section B is read.
  The status of this interrupt is visualized by LED LD4.

For further information about jumpers J3 and J4 please refer to paragraph “3 PINS JUMPERS” .
Please remark that **LAD 12** is designed to allow more than one card at the same time with interrupt request activated, however it is not possible to use a vectored interrupt.

NOTE
After a power on or a reset occoured both the interrupt signal are **actived**, so before starting to use the A/D converters it is essential to disengage them, by acquiring two combinations (whose value is meaningless) from the A/D converters.

RESET CIRCUITERY

LAD 12 performs an efficent circuitery that, after a power on occoured or a /RESET signal from **ABACO®** BUS actived, sets the on board resources in the following status:

A/D converter sections A and B:	Not initialized
Multiplexer sections A and B:	Channel 0 selected
Activity LEDs LD1, LD2:	OFF
Interrupt signals:	Activated

The purpose of this circuitery is to avoid random setting and/or unwanted changes and to warrant a known status during this critical phase.

BOARD CONNNECTIONS

To prevent possible connecting problems between **LAD 12** board and the external systems, the user has to read carefully the information of the previous paragraphs and he must follow these instructions:

- The TTL signals can be connected directly only to a device featuring the same type of interface. About the correspondance between logic signals and TTL output status, remember that a logic **0** generates a TTL 0 Vdc, while a logic **1** generates a TTL +5 Vdc.

- The analog inputs (A/D section) must be connected to signals in the following ranges: ±2.048 Vdc or 0÷20 mA according to the board configuration. Please remember that the analog inputs available on CN1 and CN2 feature a low-pass filter to reduce noise from external world, that warrants greater safety and stability for the signal. For further information please refer to the paragraph “TYPE OF ANALOG INPUT SELECTION”.

HARDWARE DESCRIPTION

This chapter provides all the hardware informations needed to use **LAD 12** board. Here the user will find information about I/O card mapping and on board peripheral devices addressing.

BOARD MAPPING

LAD 12 board is mapped into a **4** bytes I/O addressing space, that can be mapped starting from different base addresses according to how the board is configured. This feature allows to use several **LAD 12** cards on the same **ABACO®** BUS, or to install them on a BUS where other peripheral modules are installed obtaining a structure that can be expanded without any difficulty or modifications to the application software.
The base address can be defined through the specific BUS interface circuitry on the board itself; this circuitry uses the eight pins dip switch called **DIP1**, from which it reads the address set by the user. Here follows the corrispondance between dips configuration and address signals.

DIP1.1	->	**OFF**	*256 bytes addressing space*	*(**J1** not connected)*
		Address A8	*512 bytes addressing space*	*(**J1** connected)*
DIP1.2	->	*Not Used*		
DIP1.3	->	Address A2		
DIP1.4	->	Address A3		
DIP1.5	->	Address A4		
DIP1.6	->	Address A5		
DIP1.7	->	Address A6		
DIP1.8	->	Address A7		

These dips are driven in complemented logic, this means that if a switch is **ON** generates a **logic zero**, viceversa if a switch is **OFF** generates a **logic one**.

Jumper J1, as previously described, selects the addressing range for card mapping. If the 256 bytes addressing range is selected (addresses from 00H to FFH) then DIP1.1 must be OFF to address the board corrrectly, while if the 512 bytes addressing range is selected (addresses from 00H to 1FFH) then DIP1.1 is used to compose the board address.

Also jumper J2 affects the addressing logic, as described before, and must be set according to the type of **GPC®** control card used. In detail, if the control card is provided with /M1 signal on the **ABACO®** BUS then jumper J2 must be connected, and viceversa.

NOTE
When allocating the mapping address of the boards, plase be careful not to allocate more than one device in the same addressing space (count also the number of bytes occupied by the card). If this condtion will not be respected, a BUS conflict will happen; such conflict will compromise the correct working of the whole system.

As an example, some possible mappings are reported here.

1) Address used to map **LAD 12**: 040H with 256 bytes addressing space
Control board used: /M1 signal connected

Jumper J1 -> Not Connected
Jumper J2 -> Connected

DIP1.1 -> OFF
DIP1.2 -> *Don't care*
DIP1.3 -> OFF
DIP1.4 -> OFF
DIP1.5 -> ON
DIP1.6 -> ON
DIP1.7 -> OFF
DIP1.8 -> ON

2) Address used to map **LAD 12**: 0A4H with 512 bytes addressing space
Control board used: /M1 signal not connected

Jumper J1 -> Connected
Jumper J2 -> Not Connected

DIP1.1 -> ON
DIP1.2 -> *Don't care*
DIP1.3 -> OFF
DIP1.4 -> ON
DIP1.5 -> ON
DIP1.6 -> OFF
DIP1.7 -> ON
DIP1.8 -> OFF

To easily locate jumpers and dip switches please refer to figures 2 and 3.

INTERNAL REGISTERS ADDRESSING

Indicating the board base address with <**baseaddr**>, that is the address set using dip switch DIP1, as indicated in the previous paragraph **LAD 12** internal registers are addressable as explained in the following table.

DEVICE	REG.	ADDRESS	R/W	MEANING
Multiplexer	MUX	<baseaddr>+00H	W	Multiplexer management register of sections A and B.
LD1,2	LED	<baseaddr>+00H	W	Activity LEDs management register.
TSC 7109A A and B	ADL	<baseaddr>+00H	R	Low byte (bit D0÷D7) of A/D TSC 7109A data register, sections A and B.
	ADH	<baseaddr>+01H	R	High byte (bit D8÷D11) of A/D TSC 7109A data register, sections A and B.
	CTRL	<baseaddr>+02H	R/W	Status and control register of A/D TSC 7109A, sections A and B.
	INIT	<baseaddr>+03H	W	Initialization register of A/D TSC 7109A, sections A and B.
INPUT	INP	<baseaddr>+02H	R	Digital TTL inputs acquisition register, sections A and B.

FIGURE 15: INTERNAL REGISTERS ADDRESSING TABLE

NOTE

When allocating the mapping address of the boards, plase be careful not to allocate more than one device in the same addressing space (count also the number of bytes occupied by the card). If this condtion will not be respected, a BUS conflict will happen; such conflict will compromise the correct working of the whole system.

PERIPHERAL DEVICES SOFTWARE DESCRIPTION

In the previous paragraph allocation addresses of all the peripherals have been reported, here follows a detailed description of function and meaning of internal registers (please always refer to the peripheral mapping tables to understand completely the following informations). Should the present documentaion be inadequate please refer to the component's manufacturer documentation.
In the following paragraphs the indications **D0÷D7** or **D0÷D15** are used to refer the bits of the byte or word involved in the I/O operations.

MULTIPLEXER

This write register allows to program the multiplexer of sections A and B, so to select the channels on which the conversions must be performed.
The meaning of their bits is:

MUX.D6	->	CH2B
MUX.D5	->	CH1B
MUX.D4	->	CH0B
MUX.D2	->	CH2A
MUX.D1	->	CH1A
MUX.D0	->	CH0A

where: CH2x	CH1x	CH0x	= Selects the input channel of A/D section x:
0	0	0	-> Channel 0
0	0	1	-> Channel 1
0	1	0	-> Channel 2
0	1	1	-> Channel 3
1	0	0	-> Channel 4
1	0	1	-> Channel 5
1	1	0	-> Channel 6
1	1	1	-> Channel 7

NOTE
Please remark that register MUX is allocated at the same I/O address of register LED, so every write operation to the remaining bits, not described above, affects the activity LEDs status, as described in the following paragraph; so every operation on such registers must consider also the influence on the devices the user is not intentioned to program.

Register MUX is reset (all bits set to 0) when a power on or a reset occour; so after one of these events the multiplexer will select channel 0.

ACTIVITY LEDS

Management of the activity LEDs installed on **LAD 12** is performed through a write register called LED:

LED.D7	->	LD2
LED.D3	->	LD1

Performing a write operation the status is set as specified in the following correspondance:
The correspondance between bit value and LED status is:

Bit at logic 0	->	Activity LED OFF
Bit at logic 1	->	Activity LED ON

NOTE
Please remark that register LED is allocated at the same I/O address of register MUX, so every write operation to the remaining bits, not described above, affects the multiplexer status, as described in the previous paragraph; so every operation on such registers must consider also the influence on the devices the user is not intentioned to program.

Register LED is reset (all bits set to 0) when a power on or a reset occour; so after one of these events the activity LEDs are OFF.

TTL DIGITAL INPUTS

LAD 12 is provided with two TTL digital inputs that can be read by software performing a read operation form register INPUT.
The meaning of its bits is:

INPUT.D7	->	INB
INPUT.D6	->	INA

The indication INA and INB means the digital input lines, available respectively on connectors CN1 and CN2.

Performing a read operation form register INPUT the status of the digital inputs is acquired.
The correspondance between bit value and input status is:

Bit at logic 0	->	Input TTL at 0 Vdc
Bit at logic 1	->	Input TTL at +5 Vdc or not connected

A/D CONVERTER TSC 7109A

The 12 bits A/D converters TSC 7109A installed on **LAD 12** is performed through I/O operations to the registers listed in the table of figure 15.
Here follows their purpose and use.

Register INIT:
LAD 12 is provided with a control logic specific to manage the A/D converters that must be initialized.
Write register INIT can perform this initialization and must be programmed as follows:

INIT = **154 (9AH)**

NOTE
It is not possible to manage the A/D converters until the control logic on **LAD 12** board has been opportunely initialized. This operation must be always done after a reset or a power on.

Register CTRL:
This read/write register allows to manage the conversion modality on the desired section, select the A/D converter from which to read the value and acquire the end of conversion signals.
The meaning of its bits is:

CTRL.D5 -> EOC B
CTRL.D4 -> EOC A
CTRL.D3 -> RUN - /HOLD B
CTRL.D2 -> /CE B
CTRL.D1 -> RUN - /HOLD A
CTRL.D0 -> /CE A

where:
/CE x = O - Selects A/D converter of section x, to read the value of the last conversion.
/CE x = 0 -> A/D converter selected.
/CE x = 1 -> A/D converter not selected.
RUN - /HOLD x = O - Selects management modality for A/D converter of section x.
RUN - /HOLD x = 0 -> Do not perform another conversion, after the one in progress.
RUN - /HOLD x = 1 -> Conversion continuously.
EOC x = I - Indicates whether A/D converter of section x has terminated the conversion and the converted value is ready to be read.
EOF x = 0 -> Conversion ended.
EOF x = 1 -> Conversion in progress.

NOTE
The end of conversion signals can be matched to the board interrupt requests (please see the paragraph “INTERRUPTS” for further information). This way it is not essential any more to acquire the status of EOC A and/or EOC B, the **LAD 12** itself will advise the control card by activating the /INT signal on **ABACO®** BUS.

Registers ADL and ADH:
These read registers allow to acquire the conversion value obtained by the A/D converter previously selected through bit /CE x of register CTRL.
The meaning of their bits is:

ADH.D7	->	NU
ADH.D6	->	NU
ADH.D5	->	POL
ADH.D4	->	OVR
ADH.D3	->	C11
ADH.D2	->	C10
ADH.D1	->	C9
ADH.D0	->	C8
ADL.D7	->	C7
ADL.D6	->	C7
ADL.D5	->	C5
ADL.D4	->	C4
ADL.D3	->	C3
ADL.D2	->	C2
ADL.D1	->	C1
ADL.D0	->	C0

Where: NU = Not Used.
OVR = Input voltage out of range.
OVR =0 -> Input voltage in range ±2.048 Vdc.
OVR =1 -> Input voltage out of range ±2.048 Vdc.
POL = Sign of the conversion value and of the input voltage.
POL= 0 -> Negative sign.
POL= 1 -> Positive sign.
C11÷C0 = Absolute value of the 12 bit combination.

The 12 bit plus sign digital value acquired by the A/D converter is bound to the input voltage according to the following correspondace:

Tensione		*Digital Value*	*POL*
- 2.048 Vdc	->	4095 (FFF_{HEX})	0
0 V	->	0	1
+2.048 Vdc	->	4095 (FFF_{HEX})	1

NOTE
It is possible to read the digital value of the last conversion only after having opportunely selected the A/D converter of section A or B by programming register CTRL as previously described.

A conversion operation is made with three phases: conversion start, wait for conversion end, reading of conversion result.
Here follows a detailed description of the several conversion phases, including clear indications of what the control logic must do in each phase.
For greater evidence conversion on request and conversion continuously are described separately, in fact the two conversion modes require different actions.

CONVERSION ON REQUEST

In this modality the conversion starts when the control software performs a conversion start procedure. When the conversion ends the board is ready to let the control card read the conversion value and keeps this status until another conversion is started.
The description reported in the following 13 phases is referred to one only A/D converter section. Please remark that, in this modality, it is possible to perform the contemporary conversion on both sections A and B. This allows to reduce the total acquisition time for more analog channels of the board. The phases of the conversion on request may also be optimized according to how the board must be used.
In the following pages (figure 16) there is a flow chart that shows in a simple and straight way the **LAD 12** utilization in modality "Conversion on request".
The following description is refered to a generic A/D converter section indicated with **x**; please refer to bits of register CTRL to activate the desired section.
The operation is referred to channel 0.

1R) Initialization of control logic that manages A/D converters sections:
INIT=9AH

2R) Setting register CTRL to start condition, that is no one of the two A/D converters are selected and eventual conversions in progress are stopped:

CTRL =	NU	NU	NU	NU	RUN - /HOLD B	/CEB	RUN - /HOLD A	/CE A
	0	0	0	0	0	1	0	1

3R) Acquisition cycle on register CTRL, waiting for the end of the eventual conversion in progress on A/D converter of section x:
WAIT FOR: EOF x=0

4R) Programming of register MUX to select the channel of section x where the conversion must be performed:
MUX -> CH2x, CH1x, CH0x = Channel

NOTE
This operation may be performed only once if the conversion on section x involves always the same channel; this way the selected analog input remains selected.

5R) Programming of register CTRL to start the conversion on the A/D converter of the selected section:
CTRL -> RUN - /HOLD x = 1

6R) Acquisition cycle of register CTRL; watiting for the conversion process on A/D converter of section x begins:
WAIT FOR: EOF x = 1

7R) Programming of register CTRL to stop the A/D converter of section x when the conversion in progress is finished:
CTRL -> RUN - /HOLD x = 0

8R) Acquisition cycle of register CTRL; watiting for the conversion process on A/D converter of section x ends:
WAIT FOR: EOF x = 0

9R) Programming of register CTRL to select the A/D converter of section x for reading the digital value of the last conversion:
CTRL -> /CE x = 0

10R) Reading the low bite of the digital value (bits C7÷C0) from register ADL:

ADL <-	D7	D6	D5	D4	D3	D2	D1	D0
	C7	C6	C5	C4	C3	C2	C1	C0

11R) Reading the high nibble of the digital value (bits C11÷C8), the overrange flas (OVR) and the polarity flag (POL) from ADH:

ADH <-	D7	D6	D5	D4	D3	D2	D1	D0
	NU	NU	POL	OVR	C11	C10	C9	C8

12R) Programming of register CTRL to select the A/D converter of section x for reading the digital value of the last conversion:
CTRL -> /CE x = 1

13R) To repeat the conversion jump back to point **4R**, viceversa the board can be left in this status.

NOTE
The above description is referred to a management of **LAD 12** that does not involve the interrupt, generated by the card whenever an end of conversion occours.
To take advantage of this feature the phase **8R** must be eliminated, because the end of a conversion is signaled by the activation of **ABACO®** BUS /INT signal; in addition phases **9R÷12R** make the body of the interrupt response procedure.

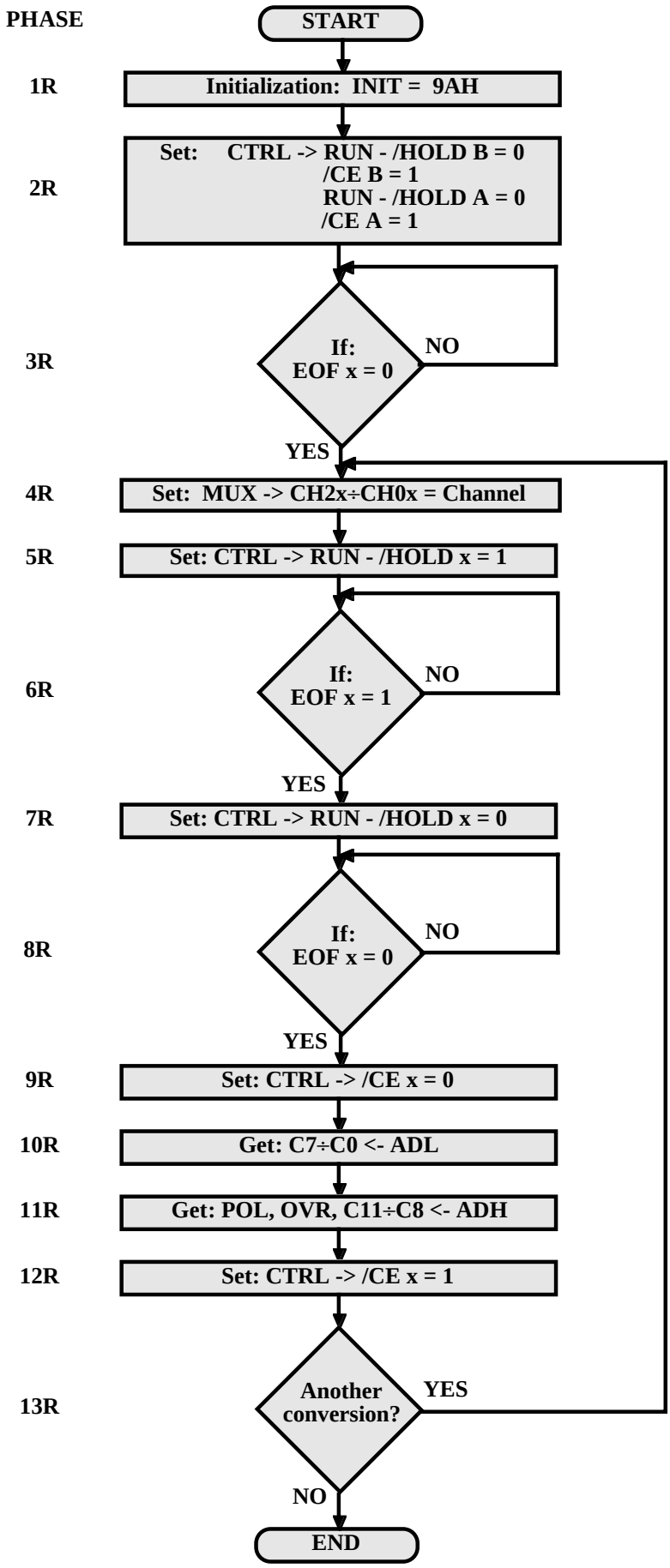

FIGURE 16: CONVERSION ON REQUEST FLOW CHART

CONVERSION CONTINUOUSLY

IIn this modality the conversions occour continuously and in automatically: once the conversion process has been started by the control process, the conversions continue without having to start them individually; the control card has just to fetch the digital value of the conversion as soon as available and before the next conversion starts.
The description reported in the following 12 phases is referred to one only A/D converter section. Please remark that, in this modality, it is not possible to perform the contemporary conversion on both sections A and B, unless a proper software management considers the asynchronicity of the two sections. Also in this modality, the phases can be otpimized according to the board configuration. In the following pages (figure 17) there is a flow chart that shows in a simple and straight way the **LAD 12** utilization in modality "Conversion continuously".
The following description is refered to a generic A/D converter section indicated with **x**; please refer to bits of register CTRL to activate the desired section.

1C) Initialization of control logic that manages A/D converters sections:
INIT=9AH

2C) Setting register CTRL to start condition, that is no one of the two A/D converters are selected and eventual conversions in progress are stopped:

CTRL =	NU	NU	NU	NU	RUN - /HOLD B	/CEB	RUN - /HOLD A	/CE A
	0	0	0	0	0	1	0	1

3C) Programming of register CTRL to start the conversion on the A/D converter of the wanted section:
CTRL -> RUN - /HOLD x = 1

4C) Acquisition cycle on register CTRL, waiting for the end of the eventual conversion in progress on A/D converter of section x:
WAIT FOR: EOF x=0

5C) Programming of register MUX to select the channel of section x where the conversion must be performed:
MUX -> CH2x, CH1x, CH0x = Channel

NOTE
This operation may be performed only once if the conversion on section x involves always the same channel; this way the selected analog input remains selected.

6C) Acquisition cycle of register CTRL; watiting for the conversion process on A/D converter of section x begins:
WAIT FOR: EOF x = 1

7C) Acquisition cycle on register CTRL, waiting for the end of the eventual conversion in progress on A/D converter of section x:
WAIT FOR: EOF x=0

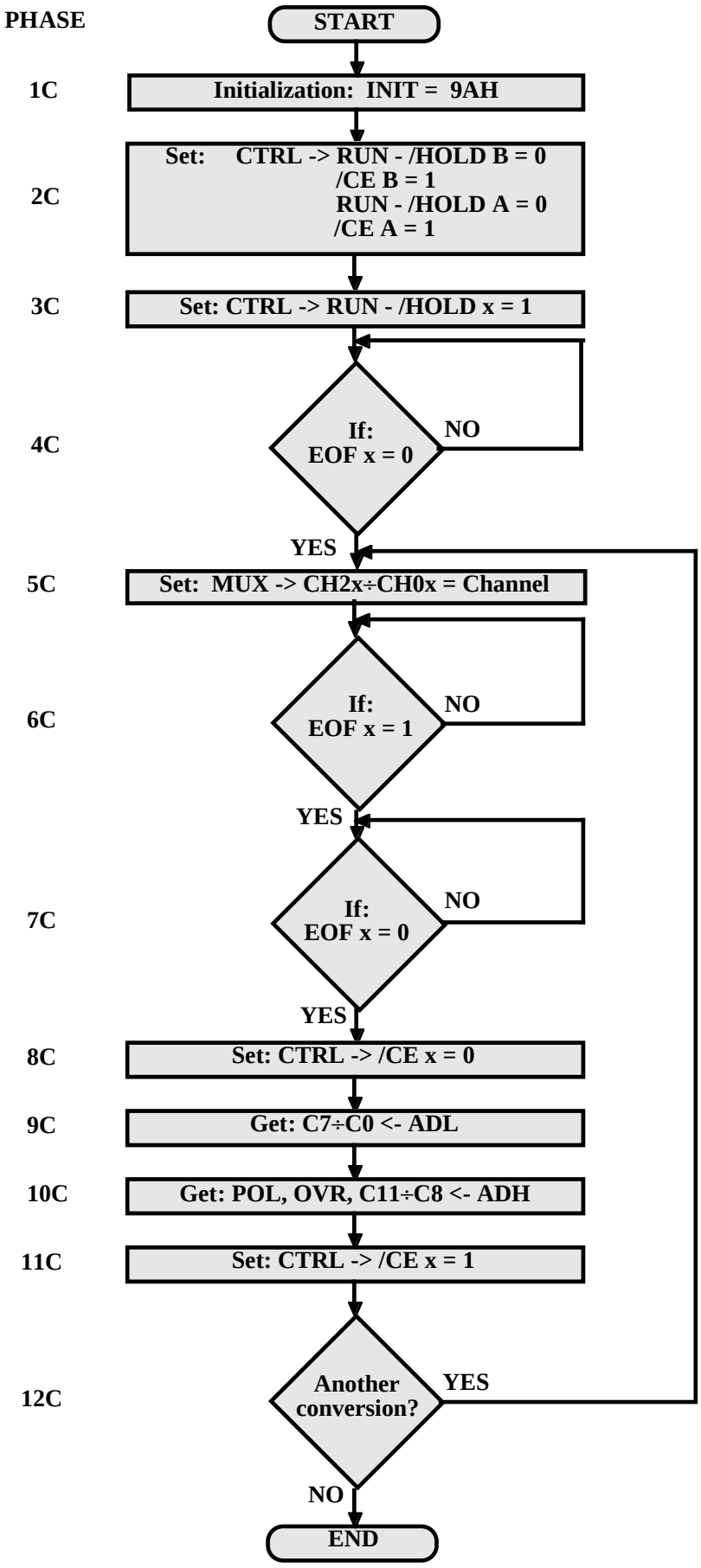

FIGURE 17: CONVERSION CONTINUOUSLY FLOW CHART

8C) Programming of register CTRL to select the A/D converter of section x for reading the digital value of the last conversion:

CTRL -> /CE x = 0

9C) Reading the low bite of the digital value (bits C7÷C0) from register ADL:

ADL <-	D7	D6	D5	D4	D3	D2	D1	D0
	C7	C6	C5	C4	C3	C2	C1	C0

10C) Reading the high nibble of the digital value (bits C11÷C8), the overrange flas (OVR) and the polarity flag (POL) from ADH:

ADH <-	D7	D6	D5	D4	D3	D2	D1	D0
	NU	NU	POL	OVR	C11	C10	C9	C8

11C) Programming of register CTRL to disable A/D converter of section x:

CTRL -> /CE x = 1

12C) To repeat the conversion jump back to point **5C**, viceversa the board can be left in this status or, eventually, the conversion process can be stopped on A/D converter of section x:
CTRL -> RUN - /HOLD x = 0.

NOTE

The above description is referred to a management of **LAD 12** that does not involve the interrupt, generated by the card whenever an end of conversion occours.
To take advantage of this feature the phases **6C** and **7C** must be eliminated, because the end of a conversion is signaled by the activation of **ABACO®** BUS /INT signal; in addition phases **8C÷11C** make the body of the interrupt response procedure.

EXTERNAL CARDS

LAD 12 can be connected to a wide range of block modules and operator interface system produced by **grifo®**, or to many system of other companies.The on board resources can be expanded with a simple connection to the numerous peripheral **grifo®** boards,both intelligent and not, thanks to its standard **ABACO®** BUS connector. Even cards with **ABACO®** I/O BUS can be connected, by using the proper mother boards.
Hereunder some of these cards are briefly described; ask the detailed information directly to **grifo®**, if required.

MB3 01-MB4 01-MB8 01
Mother Board 3, 4, 8 slots
Motherboard featuring 3, 4 or 8 slots of **ABACO®** industrial BUS; pitch 4 TE; standard power supply connectors; LEDs for visual feed-back of power supply; holes for rack docking.

SPB 04-SPB 08
Switch Power BUS 4-8 slots
Motherboard featuring 4-8 slots of **ABACO®** industrial BUS; pitch 4 TE; standard power supply connectors; termination resistances; connector type F for **SPC xxx** supply ; holes for rack docking.

ABB 03
ABACO® Block BUS 3 slots
3 slots **ABACO®** mother board; 4 TE pitch connectors; **ABACO®** I/O BUS connector; screw terminal for power supply; connection for DIN C type and Ω rails.

ABB 05
ABACO® Block BUS 5 slots
5 slots **ABACO®** mother board with power supply. Double power supply built in; 5Vdc 2,5A section for powering the on board logic; second section at 24Vdc 400mA galvanically coupled, for the optocoupled input lines. Auxiliary connector for **ABACO®** I/O BUS. Connection for DIN Ω rails.

SPC 03.5S
Switch Power Card +5 Vdc
Europe format switching power supply capable to provide +5 Vdc to a load of 4 A; input voltage 12÷24 Vac; power-failure; connector for back-up battery; standard connector for mother board **SPB 0x**.

SPC 512
Switch Power Card +5 Vdc +12 Vdc
Europe format switching power supply capable to provide +5 Vdc 5A and +12 Vdc 2.5 A; input voltage 12÷24 Vac; power-failure; connector for back-up battery; standard connector for mother board **SPB 0x**.

FBC 20-120
Flat Block Contact 20 vie
Interface for 2 or 1 mounting cable connectors (low profile 20 pins male) and quick release screw terminal connectors; Plastic mount for rails DIN 46277-1 and 3.

GPC® 51

General Purpose Controller fam. 51

Microprocessor family 51 INTEL including the masked BASIC chip; the board features: 16 I/O TTL lines; dip switch; 3 timer/counter; RS 232; 4 A/D converter signals resolution 11 bit; buzzer; on board EPROM programmer; RTC and 32K SRAM with Lithium battery back up; controlloer for display and keyboard.

GPC® 188F

General Purpose Controller 80C188

80C188 µP 20MHz; 1 RS 232 line; 1 RS 232, RS 422-485 or Current Loop line; 24 TTL I/O lines; 1M EPROM or 512K FLASH; 1M RAM Lithium battery backed; 8K serial EEPROM; RTC; Watch Dog; 8 Dip switch; 3 Timer Counter; 8 13 bit A/D lines; Power failure; activity LEDs; single power supply +5Vdc.

GPC® 15A

General Purpose Controller 84C15

Full CMOS card, 10÷20 MHz 84C15 CPU; 512K EPROM or FLASH; 128K RAM; 8K RAM and RTC backed; 8K serial EEPROM; 1 RS 232 line; 1 RS 232 line or RS 422-485 or Current Loop line; 32 or 40 TTL I/O lines; CTC; Watch dog; 2 Dip switches; Buzzer.

GPC® 150

General Purpose Controller 84C15

Microprocessor Z80 at 16 MHz; implementation completely CMOS; 512K EPROM or FLASH; 512K SRAM; RTC; Back-Up through external Lithium battery; 4M serail FLASH ; 1 serial line RS 232 plus 1 RS 232 or RS 422-485 or current loop; 40 I/O TTL; 2 timer/counter; 2 watch dog; dip switch; EEPROM; A/D converter with resolution 12 bit; activity LED.

GPC® 15R

General Purpose Controller 84C15

84C15 µP, 10÷16 MHz; 1 RS 232 line; 1 RS 232 or RS 422-485 or C. L. line; 16÷24 TTL I/O lines; 16 Opto-in; 8 Relays; 4 Opto Coupled Timers Counters; 512K EPROM or FLASH; 512K RAM and RTC backed; 8K serial EEPROM; 8K Backed RAM modul; Buzzer; 1 Activity LED; Watch dog; 4÷12 readable DIPs; LCD Interface.

GPC® 323

General Purpose Controller 51 family

80C32 µP, 14 MHz; Full CMOS; 1 RS 232 line (software); 1 RS 232 or RS 422-485 or Current Loop line; 24 TTL I/O lines; 11 A/D 12 bits lines; 3 Timers Counters; 64K EPROM; 64K RAM; 32K RAM and RTC backed; 32K DIL EEPROM; 8K serial EEPROM; Buzzer; 2 Activity LED; Watch dog; 5 readable DIPs; LCD Interface.

GPC® 553

General Purpose Controller 80C552

80C552 µP, 22÷33 MHz; 1 RS 232 line (software); 1 RS 232 or RS 422-485 or Current Loop line; 16 TTL I/O lines; 8 A/D 10 bits lines; 3 Timers Counters; 64K EPROM; 64K RAM; 32K RAM and RTC backed; 32K DIL EEPROM; 8K serial EEPROM; 2 PWM lines; 1 Activity LED; Watch dog; 5 readable DIPs; LCD Interface.

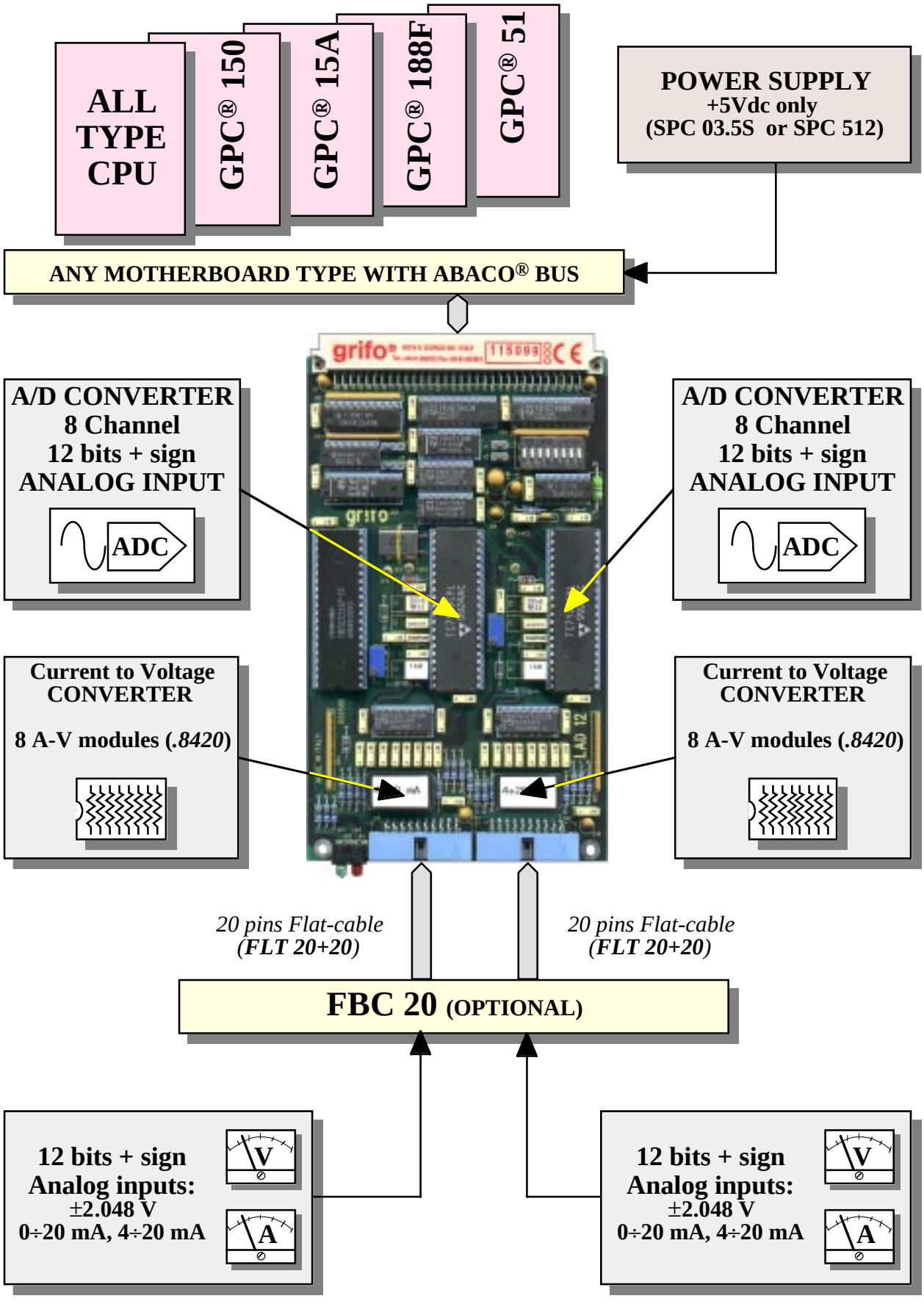

FIGURE 18: POSSIBLE CONNECTIONS DIAGRAM

GPC® 153

General Purpose Controller Z80

84C15 µP, 10÷16 MHz; Full CMOS; 1 RS 232 line; 1 RS 232 or RS 422-485 or Current Loop line; 16 TTL I/O lines; 8 A/D 12 bits lines; 2÷4 Timers Counters; 512K EPROM or FLASH; 512K RAM and RTC backed; 8K serial EEPROM; Buzzer; 1 Activity LED; Watch dog; 8 readable DIPs; LCD Interface.

GPC® 183

General Purpose Controller Z180

Z180 µP, 10÷16 MHz; Full CMOS; 1 RS 232 line; 1 RS 232 or RS 422-485 or Current Loop line; 24 TTL I/O lines; 11 A/D 12 bits lines; 2 Timers Counters; 512K EPROM or FLASH; 512K RAM and RTC backed; 8K serial EEPROM; Buzzer; 2 Activity LED; Watch dog; 4 readable DIPs; LCD Interface.

GPC® 324/D

"4" Type General Purpose Controller 80C32/320

80C32 or 80C320 µP, 14÷22 MHz; Full CMOS; 1 RS 232 line; 1 RS 232 or RS 422-485 or Current Loop line; 4÷16 TTL I/O lines; 3 Timers Counters; 64K EPROM; 64K RAM; 32K RAM backed; 32K DIL E2; 8K serial EEPROM; Watch dog; 1 readable DIP; LCD Interface; Abaco® I/O BUS; 5Vdc Power supply; Size: 100x50 mm.

GPC® 554

General Purpose Controller 80C552

Microprocessor 80C552 at 22 MHz; implementation completely CMOS; 32K EPROM; 32 K SRAM; 32 K EEPROM or SRAM; EEPROM; 2 RS 232 serial lines; 16 I/O TTL; 2 PWM lines; 16 bits Timer/Counter; Watch Dog; 6 signals A/D converter with resolution 10 bit; interface for **ABACO®** I/O BUS.

GPC® 154

"4" Type General Purpose Controller Z80

84C15 µP, 10÷16 MHz; Full CMOS; 1 RS 232 line; 1 RS 232 or RS 422-485 line; 16 TTL I/O lines; 2÷4 Timers Counters; 512K EPROM or FLASH; 512K RAM and RTC backed; 8K serial EEPROM; Watch dog; 2 readable DIPs; LCD Interface; Abaco® I/O BUS; 5Vdc Power supply; Size: 100x50 mm.

GPC® 884

General Purpose Controller Am188ES

Microprocessor AMD Am188ES up to 40 MHz16 bits; implementation completely CMOS; serie 4 format; 512K EPROM or FLASH; 512K SRAM backed with Lithium battery; RTC; 1 RS 232 serial line + 1 RS 232 or RS 422-485 or current loop; 16 I/O TTL; 3 timer/counter; watch dog; EEPROM; 11 signals A/D converter with 12 bit resolution; interface for **ABACO®** I/O BUS.

GPC® 114

General Purpose Controller 68HC11

Microprocessor 68HC11A1 at 8 MHz; implementation completely CMOS; serie 4 format; 32K EPROM; 32K SRAM backed with Lithium battery; 32K EPROM, SRAM, EEPROM; RTC; 1 serial line RS 232 or RS 422-485; 10 I/O TTL; 3 timer/counter; watch dog; 8 signals A/D converter with resolution 8 bit; 1 asunchronous serial line; extremly low power consumption; interface for **ABACO®** I/O BUS.

GPC® 184

General Purpose Controller Z80195

Microprocessor Z80195 at 22 MHz; implementation completely CMOS; 512K EPROM or FLASH; 512K RAM; Back-Up with Lithium battery internal or external; 1 serial line RS 232 + 1 RS 232 or RS 422-485 or current loop + 1 TTL; 18 I/O TTL; 4 timer/counter 8 bits; 2 timer 16 bits; Watch Dog; Real Time Clock; activity LED; EEPROM; interface for **ABACO®** I/O BUS.

GPC® AM4

General Purpose Controller ATmega103

Microprocessor ATmega103 at 5.5 MHz; implementation completely CMOS; 128K internal FLASH; 32K SRAM; Back-Up with Lithium battery internal or external; 1 serial line RS 232 or RS 422-485 or current loop; 16 I/O TTL; 8 linee A/D resolution 10 bits; 2 timer/counter; Watch Dog; Real Time Clock; 4K internal EEPROM; interface for ISP programming; interface forr **ABACO®** I/O BUS.

BIBLIOGRAPHY

Here follows a list of manuls thst can be a source of further informations about the devices installed on **LAD 12**.

Manual TEXAS INSTRUMENTS: *The TTL data Book - SN54/74 Families*
Manual TEXAS INSTRUMENTS: *Linear Circuits - Volume 3*

Manual NEC: *Microprocessor and Peripheral - Data Book Volume I*

Manual TELCOM: *Mixed signal, Power management, Smart sensors - Data Book*

Please connect to the manifactures Web sites to get the latest version of all manuals and data sheets.

APPENDIX A: ALPHABETICAL INDEX