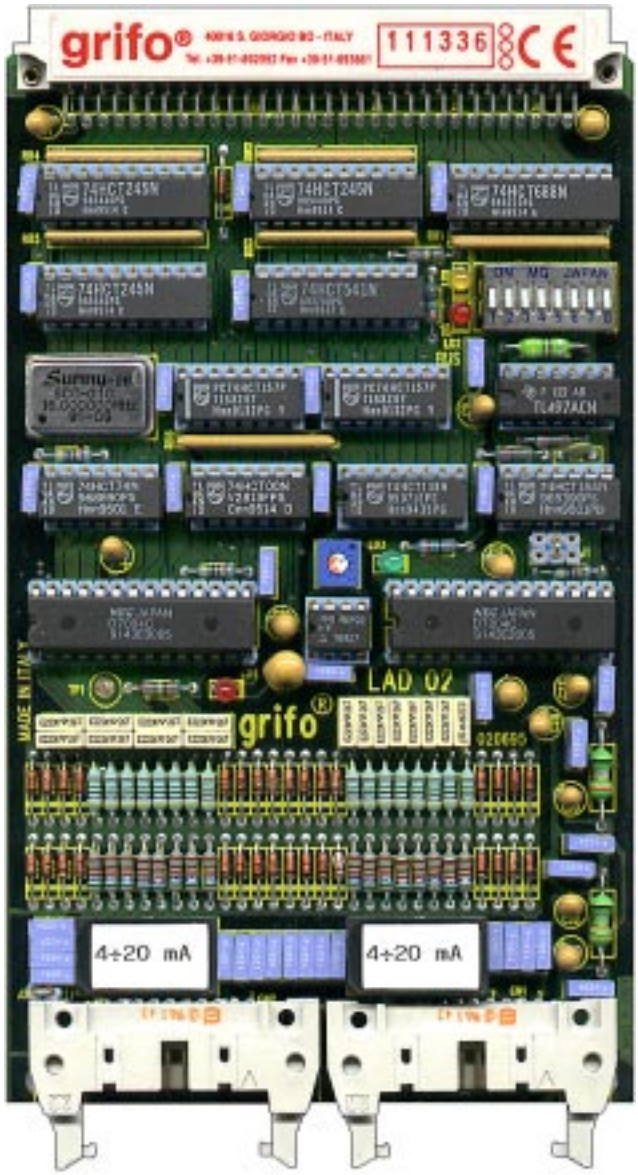
LAD 02

Low cost Analog to Digital converter

TECHNICAL MANUAL



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LAD 02 Edition 5.00 *Rel. 06 March 2001*

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Eurocard format size 100x160 mm; interface to **ABACO**® industrial BUS; 16 analog to digital input lines with resolution 10 bits, conversion time 100 µsec and full range voltage 5.120 V**;** 2 indipendent A/D conversion sections featuring each 8 signals, based on as many µPD 7004; signals acquisition in voltage (0÷5.120 V) or current (0÷20 or 4÷20 mA), through a specific current-to-voltage conversion module; **π-filter** based protection circuitery on each analog input; DC/DC converter to generate all the voltages needed to the analog section; on board generated A/D converter reference voltage; wait generate for inserting 4, 6, 8 wait states in the I/O operations execution; I/O address mapping selection through on board dip switch; only as low as 4 contiguous bytes occupied in the addresses space; data BUS management 8 or 16 Bits, selectable through dip switch; 2 LEDs to visualize the BUS interface configuration; 2 low profile connectors, featuring standard 20 pins pin-out, for analog inputs; direct interfacement to **FBC** field modules; unique power supply +5Vdc

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For specific informations on the components mounted on the card, please refer to the Data Book of the builder or second sources.

SYMBOLS DESCRIPTION

In the manual could appear the following symbols:

Attention: Generic danger

Attention: High voltage

Trade Marks

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Other Product and Company names listed, are trade marks of their respective companies.

GENERAL INDEX

FIGURES INDEX

INTRODUCTION

The use of these devices has turned - IN EXCLUSIVE WAY - to specialized personnel.

The purpose of this handbook is to give the necessary information to the cognizant and sure use of the products. They are the result of a continual and systematic elaboration of data and technical tests saved and validated from the manufacturer, related to the inside modes of certainty and quality of the information.

The reported data are destined- IN EXCLUSIVE WAY- to specialized users, that can interact with the devices in safety conditions for the persons, for the machine and for the enviroment, impersonating an elementary diagnostic of breakdowns and of malfunction conditions by performing simple functional verify operations , in the height respect of the actual safety and health norms.

The informations for the installation, the assemblage, the dismantlement, the handling, the adjustment, the reparation and the contingent accessories, devices etc. installation are destined - and then executable - always and in exclusive way from specialized warned and educated personnel, or directly from the TECHNICAL AUTHORIZED ASSISTANCE, in the height respect of the manufacturer recommendations and the actual safety and health norms.

The devices can't be used outside a box. The user must always insert the cards in a container that rispect the actual safety normative. The protection of this container is not threshold to the only atmospheric agents, but specially to mechanic, electric, magnetic, etc. ones.

To be on good terms with the products, is necessary guarantee legibility and conservation of the manual, also for future references. In case of deterioration or more easily for technical updates, consult the AUTHORIZED TECHNICAL ASSISTANCE directly.

To prevent problems during card utilization, it is a good practice to read carefully all the informations of this manual. After this reading, the user can use the general index and the alphabetical index, respectly at the begining and at the end of the manual, to find information in a faster and more easy way.

CARD VERSION

The present handbook is reported to the **LAD 02** card release **020695** and later. The validity of the bring informations is subordinate to the number of the card release. The user must always verify the correct correspondence among the two denotations. On the card the release number is present in more points both board printed diagram (serigraph) and printed circuit (for example near A/D converter intalled on IC14 both on the component side and on the solder side).

GENERAL INFORMATION

LAD 02 (**L**ow cost **A**nalog to **D**igital converter) card is a powerful Eurocard format card, provided with **ABACO®** industrial BUS interface. This card belongs to the analog peripherals units list and, in specific, its purpose is to provide sixteen Analog to Digital conversion lines.
The analog signals are connected through two 20 pins low profile standard connectors. Two indipendent A/D Converter circuitries, based on as many **µPD 7004**, warrant a complete separation of the signals. A/D circuitry is features **10 bits** of resolution, **100 µsec** conversion time and **5.120 V** full range.
Each analog input line is provided with an efficent protection circuitery against overvoltages and a **π-filter** to reduce the noise coming from external world; the signal to acquire can be configured as tension (**0÷5.120 V**) or current (**0÷20 mA or 4÷20 mA**) installing on the board an opportune module for current-voltage conversion.
A DC/DC converter is charged to generate all the voltages essential for the correct working from the unique power supply of +5 Vdc.
The 20 pins output connector is **ABACO®** standard compliant, this allows an immediate interfacing to several modules for the field, like FBC xxx, that untangle the signals from the flat cable to comfortable quick release screw terminal connectors.
LAD 02 card can be driven through any CPU board in the **ABACO®** listing and takes as low as 4 contiguous bytes in the addressing space.
A remarkable feature of **LAD 02** is the capability to use 8 or 16 bits wide bus data path . Comfortable dip switches allow to select between Byte or Word modality and the addressing range, these information are visualized through specific LEDs.
LAD 02 is the ideal component for all the applications where high conversion speed, failrly good precision, several lines and low costs are required.
Amongst its various applications we would want to remark: interfacement to transductors, like pressure, temperature, humidity, optical sensors, etc.
Overall features of **LAD 02** are as follows:

- Eurocard format size 100x160 mm; interface to **ABACO®** industrial BUS
- 16 A/D input lines, resolution **10 bits**, conversion time **100 µsec**, full range **5.120 V**
- 2 indipendent A/D conversion sections featuring each 8 signals, based on as many **µPD 7004**
- Signals acquisition in tension (**0÷5.120 V**) or current (**0÷20 or 4÷20 mA**), through a specific current-to-voltage conversion module
- **π-filter** based protection circuitery on each analog input
- **DC/DC converter** to generate all the voltages needed to the analog section
- On board generated A/D converter reference voltage
- Wait generate for inserting 4, 6, 8 wait states in the I/O operations execution
- I/O address mapping selection through on board dip switch
- Only as low as 4 contiguous bytes occupied in the addresses space
- Data BUS management 8 or 16 Bits, selectable through dip switch
- 2 LEDs to visualize the BUS interface configuration
- 2 low profile connectors, featuring standard 20 pins pin-out, for analog inputs
- Direct interfacement to **FBC** field modules; unique power supply +5Vdc

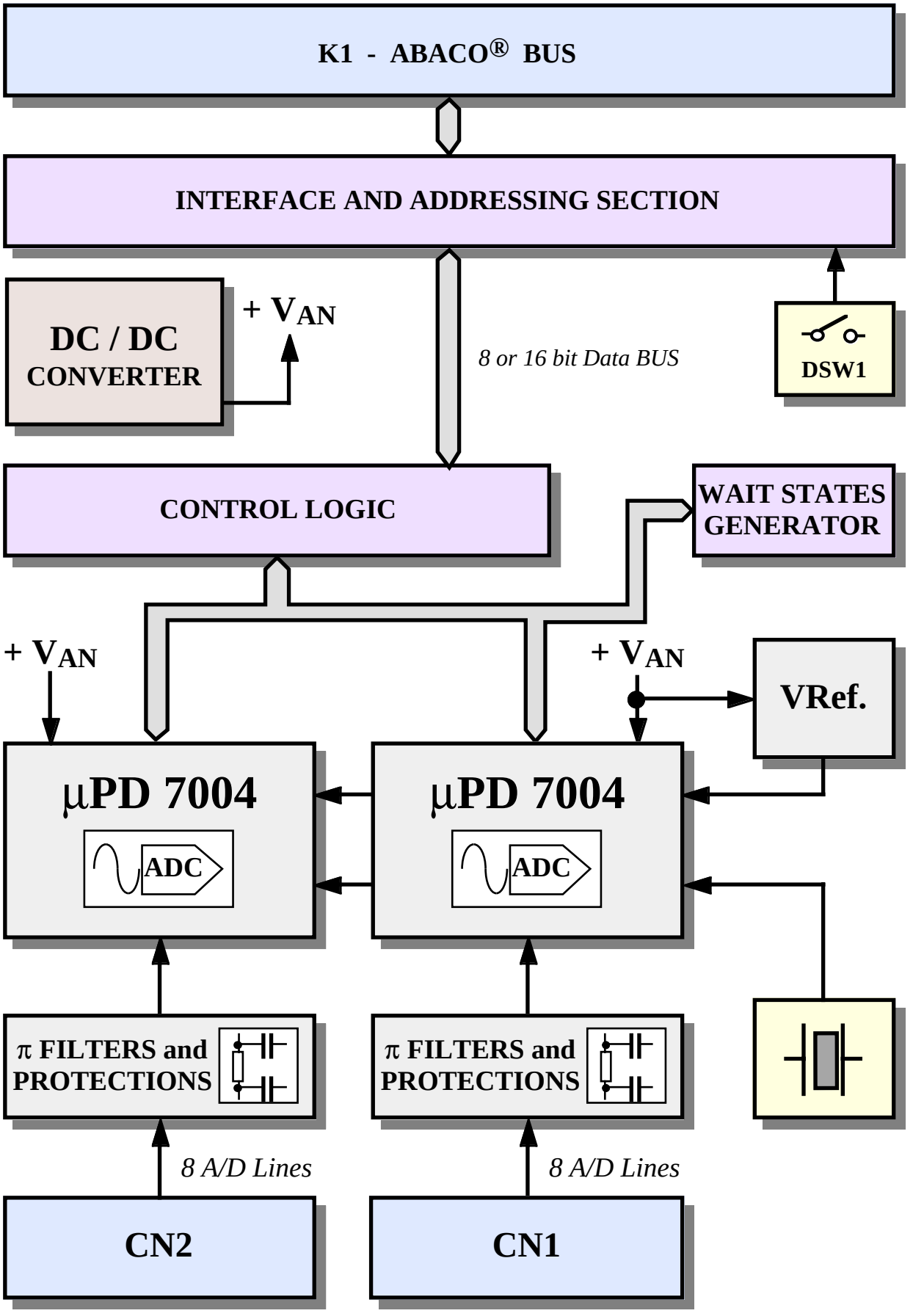

FIGURE 1: BLOCK DIAGRAM

Here follows a description of **LAD 02** board's functional blocks, with an indication of the operations performed by each one. To easily locate these blocks and verify their connections pleare refer to figure 1.

INTERFACING AND ADDRESSING SECTION

This section manages the data exchange between contol logic and command board through **ABACO®** BUS. In particular, all written or read data transit across this section that, in addition, provides the board I/O management, by setting the dip switch **DIP1**.
ABACO® industrial BUS supports both 8 bits and 16 bits addressing mode.
For further informations please refer to the chapter dedicated to board's software description.

CONTROL LOGIC

This section generates all the chip select signals needed to acces the several peripherals on **LAD 02** boards. Using this section the programmer can interact to the board's several sections, verifing their status, setting configuration of A/D converters, etc.
All this can be done through a simple software management based on **ABACO®** BUS, to which the contol logic connects through the interfacing and addressing section. For further informations please refer to the chapter dedicated to board's software description.

WAIT STATE GENERATOR

The sophisticated wait state generator installed on **LDA 02** intervents directly to **ABACO®** BUS and allows to insert a programmable number of wait states whenever **LDA 02** performs an I/O operation. A set of comfortable jumpers allow to decide the configuration of this circuitery (number of wait states can be 4, 6 or 8).
The main purpose of this section is to allow to use **LDA 02** also matched with very fast CPU boards, and so to increase its versatility.

DC/DC CONVERTER

A positive booster installed on **LAD 02** board is charged to provide the voltages needed by the digital to analog conversion section. Such DC/DC converter generates the +9 Vdc voltagesstarting from the unique +5 Vdc power supply and needs no software management.

CLOCK

LAD 02 is provided with a circuit with an oscillator to generate the clock signal for A/D Converter. Its frequence is 8 MHz. Such frequence determines the time succession of the several A/D conversion phases process, its value has been chosen to optimize both conversion time and noise immunity.

REFERENCE VOLTAGE

A specific precision circuitery is charged to generate the 5.120 Vdc reference voltage (**Vref**) required by the A/D converters. Such voltage is perfectly stabilized and indipendent from the board supply and temperature variations, so to increase **LAD 0**2 precision and reliability.
For further information please see paragraph “TRIMMER AND CALIBRATION”.

A/D CONVERTER

LAD 02 board features two indipendent A/D converter sections based on as many **µPD 7004**, these are precision converters that take advantage of the SAR technique.
Its overall features are:

- Resolution 10 bits.
- 8 analog input channels with internal multiplexer.
- Max linearity error ±1 LSB.
- Max offset error ±0.5 LSB.
- Conversion time (per channel) 100 µsec.
- High input impedance.
- Simple software management.

µPD 7004 is the ideal component for the typical application of industrial automation, where a high conversion speed and a failrly good precision is required. For further information about this component please refer to manufacturer documentation.

The 16 inputs are acquirable as tensions, in the range 0÷5.120 V, or as current in the range 0÷20 mA or 4÷20 mA, installing the specific current-to-voltage module.
Such module is optional and must be specified in the order with the code **.8420**.
Each analog input line is provided with an efficent protection circuitery against overvoltages and a **π-filter** to reduce the noise coming from external world.

TECHNICAL FEATURES

GENERAL FEATURES

On board resources:	16 analog inputs (two 8 channel A/D converters) 1 Wait state generator 1 eight pins dip switch to set I/O address
BUS type:	Industrial **ABACO®** Manageable 8 or 16 bits.
Addressing space:	256 bytes
Number of wait states:	Selectable amongst 4, 6 or 8
Byte / word taken:	4 / 2
On board peripherals:	µPD 7004
A/D external clock frequence:	8 MHz
A/D work frequence:	1 MHz
A/D resolution:	10 bits
A/D conversion time:	100 µsec per channel
A/D max linearity error:	± 1 LSB (*)
A/D max offset error:	± 0.5 LSB (*)

PHYSICAL FEATURES

Size:	Standard EUROCARD format 100x160 mm
Weight:	146 g
Connectors:	K1: DIN 41612 64 pins M 90° A+C type C CN1: Low profile 20 pins M 90° strain clamp relief CN2: Low profile 20 pins M 90° strain clamp relief
Temperature range:	from 0 to 70° C
Relative humidity:	20% up to 90% (without condensing)

(*) Values referred to a working temperature of 20 °C

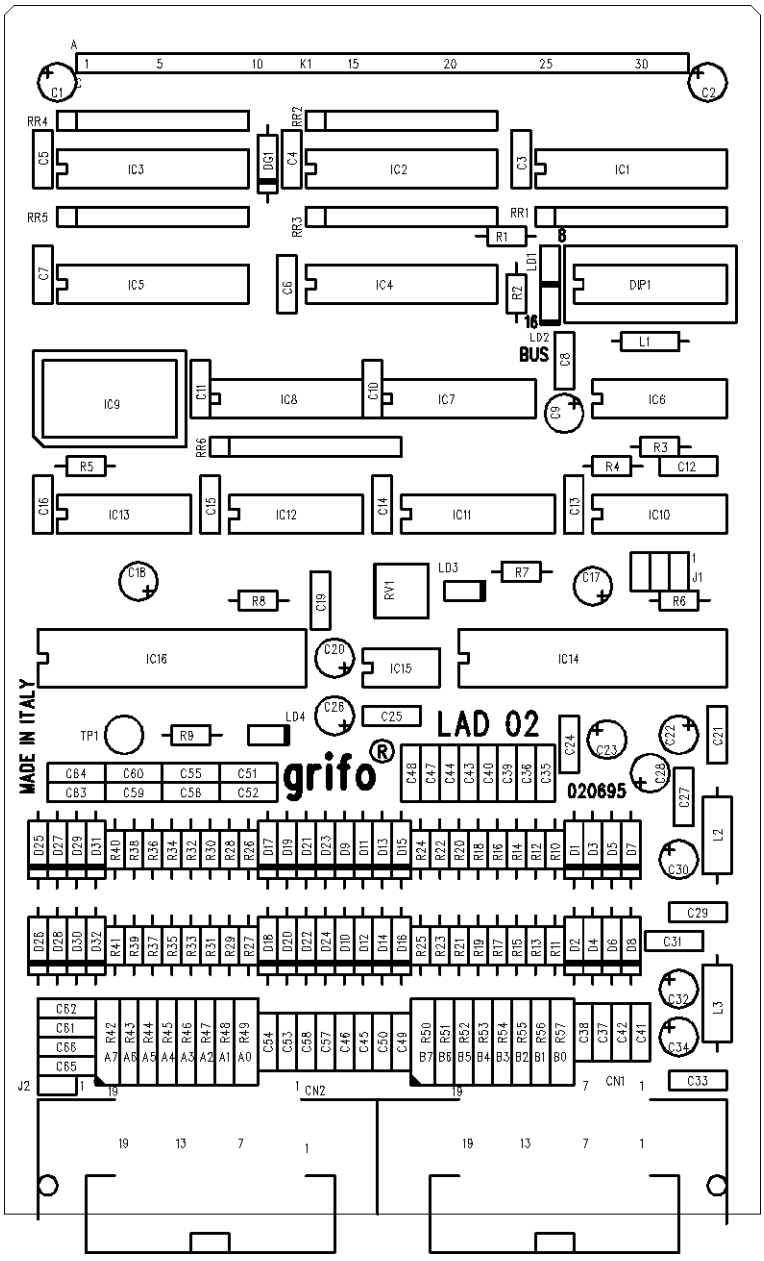

FIGURE 2: COMPONENTS MAP

ELECTRIC FEATURES

Power supply:	+5 Vdc ± 5% +12 Vdc (**)
Current consumption:	205 mA
Max current from CN1 and CN2:	600 mA (from +5 Vdc) 500 mA (from +12 Vdc)
A/D input impedance:	1000 MΩ
Analog inputs:	0÷5.120 V 0÷20 mA or 4÷20 mA (using modul **.8420**)
Curren-to-voltage conversion resistor:	249Ω
A/D reference voltage:	5.120 Vdc generated on board
Filter on analog inputs:	π-filter

(**) The +12 Vdc voltage, coming from **ABACO®** BUS, is not used by the board but is available on CN1 and CN2 to supply eventual external circuits.

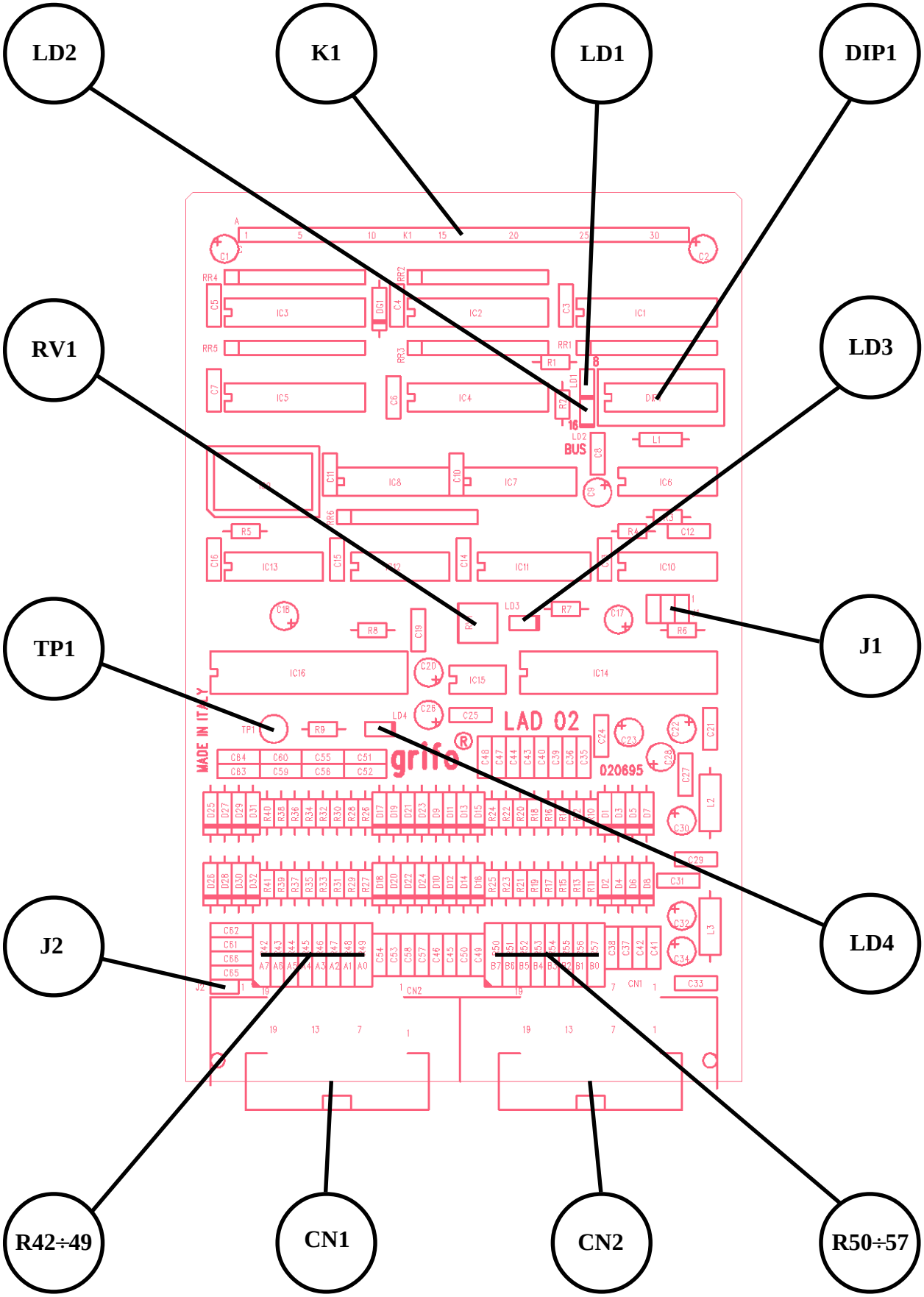

FIGURE 3: CONNECTORS, DIP SWITCH, LEDS, JUMPERS, ETC. LOCATION

INSTALLATION

In this chapter there are the information for a right installation and correct use of **LAD 02** card. The user can find the location and functions of each connectors, jumpers, LEDs, trimmer and some explanatory diagrams.

CONNECTIONS

The board has seven connectors that can be linkeded to other devices or directly to the field, according to system requirements. In this paragraph there are connectors pin outs, a short signals description (including the signals direction) and connectors location, plus some figures that describe how the interface signals are connected on the card.
To easily locate the connectors please refer to figure 3.

CN1 - ANALOG INPUTS SECTION B CONNECTOR

The connector for the 8 analog inputs of section B, called CN1, is a low profile, 20 pins, 90 degreeses with 2.54 mm pitch and strain relief clamp.
The lines available on CN1 feature high impedance and are provided with protection circuit against overvoltages and π-filter to reduce the electric noise coming from the external world. The signals that can be connected to these inputs may vary in the range 0÷5.120 V or 0÷20 mA or 4÷20 mA, the last two are available only if converter module is installed (modul code **.8420**).
Signals placement on the connector has been designed to reduce problems of noise and interference, to warrant a good transmission quality.

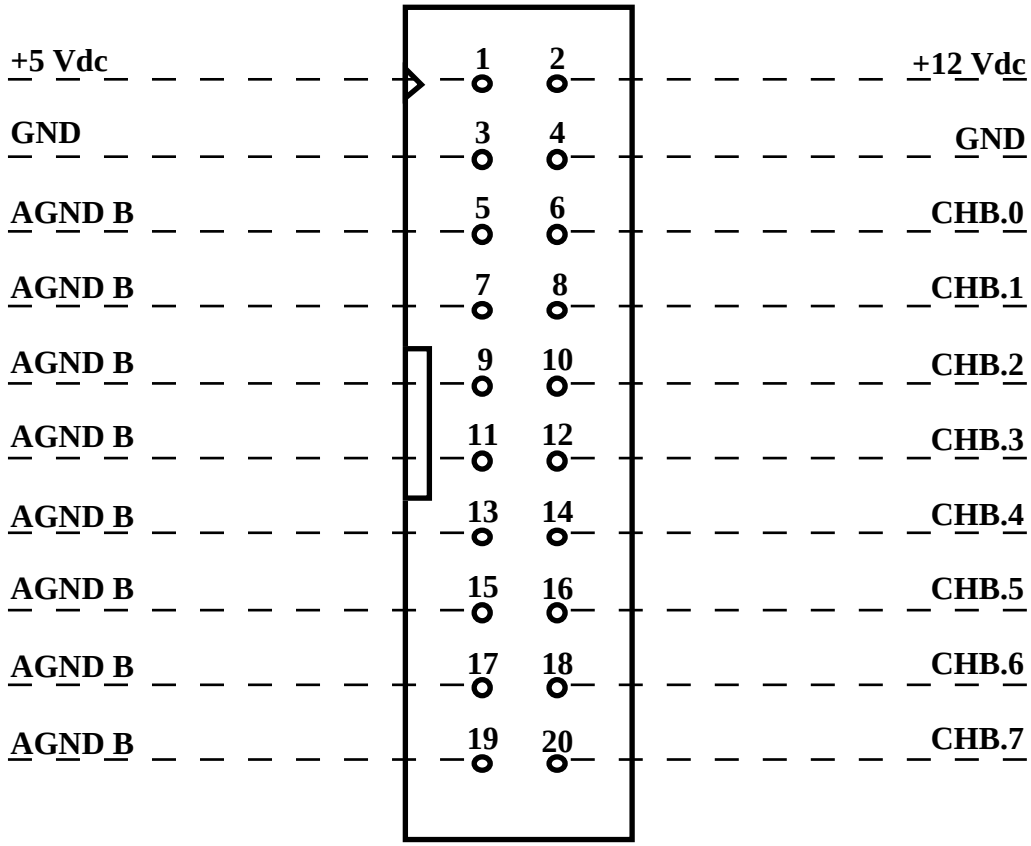

FIGURE 4: CN1 - ANALOG INPUTS SECTION B CONNECTOR

Signals description:

CHB.n	=	I	- n-th A/D input channel of section B.
AGND B	=		- Ground of section B A/D input channels.
+5 Vdc	=	O	- Power supply +5 Vdc.
+12 Vdc	=	O	- Power supply +12 Vdc, coming from **ABACO®** BUS.
GND	=		- Ground.

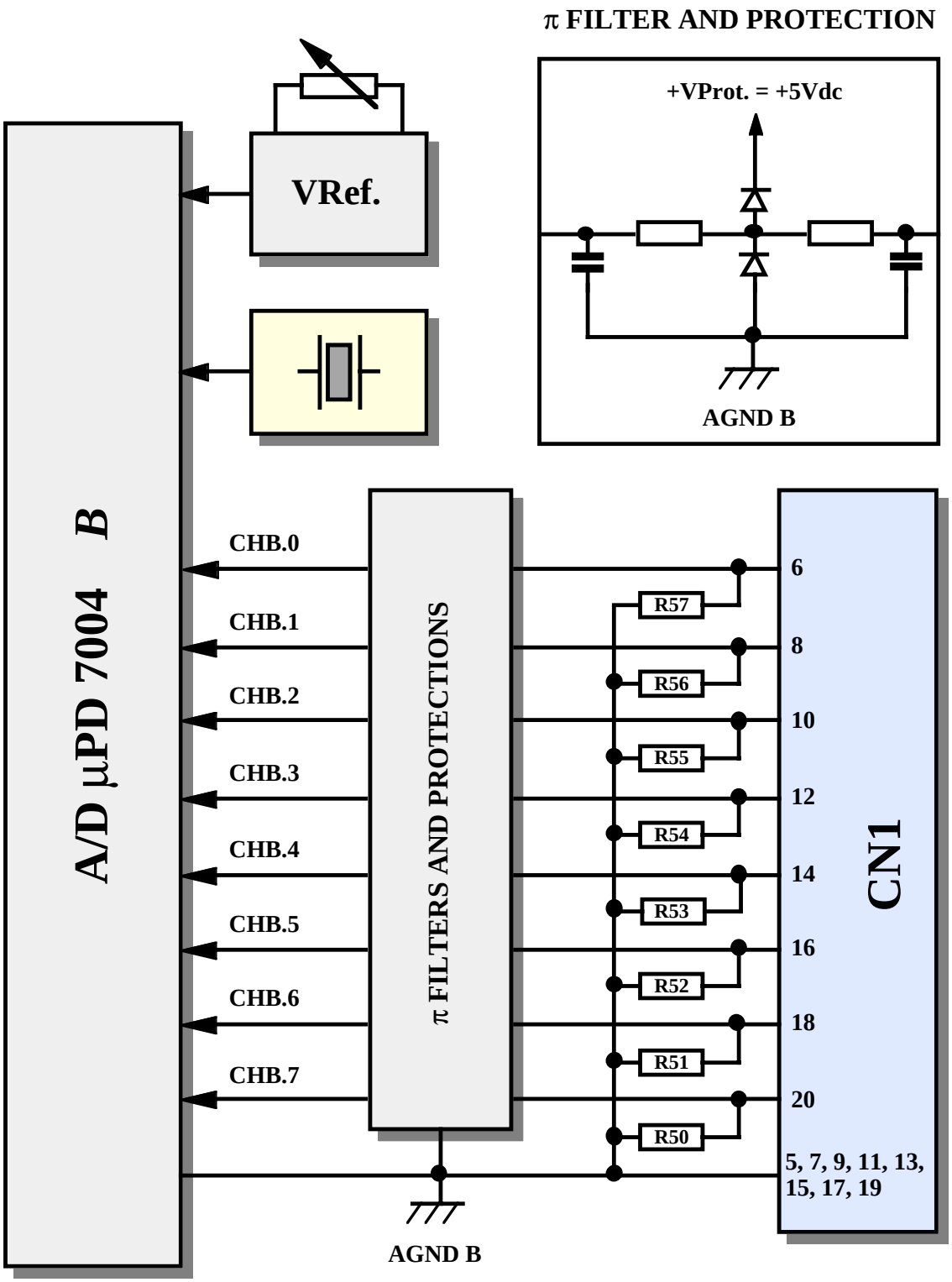

FIGURE 5: A/D CONVERTER OF SECTION B BLOCK DIAGRAM

CN2 - ANALOG INPUTS SECTION A CONNECTOR

The connector for the 8 analog inputs of section A, called CN2, is a low profile, 20 pins, 90 degreeses with 2.54 mm pitch and strain relief clamp.
The lines available on CN2 feature high impedance and are provided with protection circuit against overvoltages and π-filter to reduce the electric noise coming from the external world. The signals that can be connected to these inputs may vary in the range 0÷5.120 V or 0÷20 mA or 4÷20 mA, the last two are available only if converter module is installed (modul code **.8420**).
Signals placement on the connector has been designed to reduce problems of noise and interference, to warrant a good transmission quality.

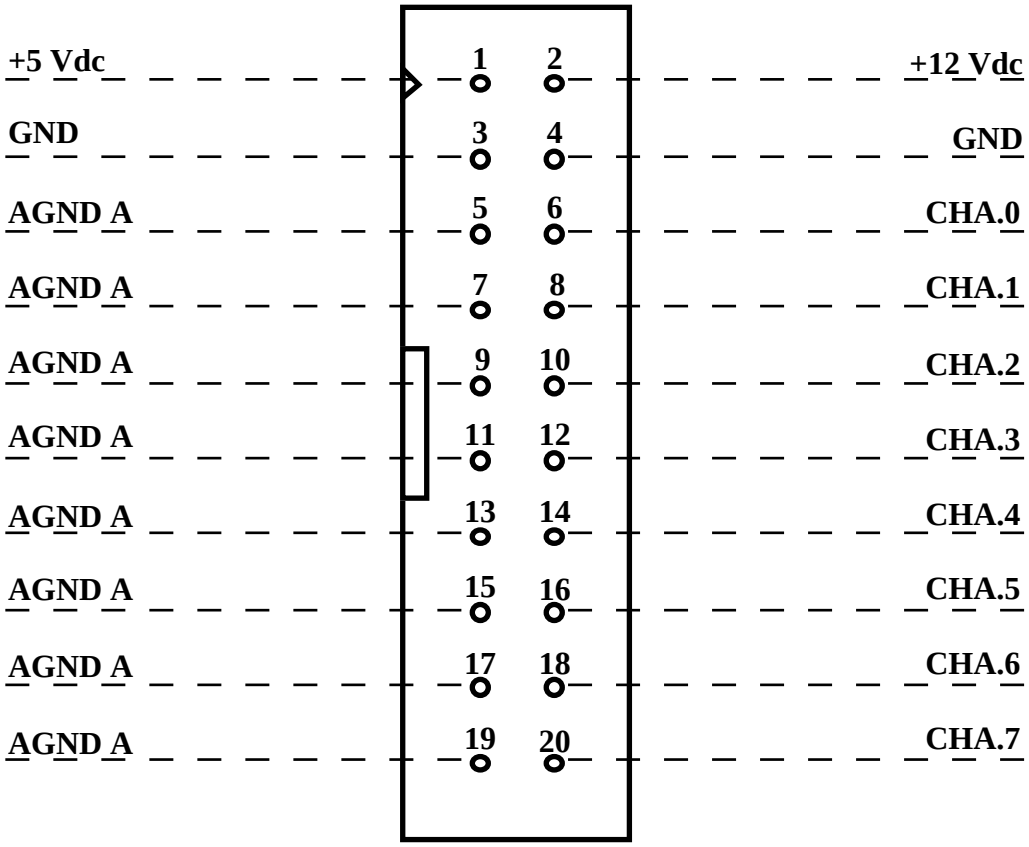

FIGURE 6: CN2 - ANALOG INPUTS SECTION A CONNECTOR

Signals description:

CHA.n	=	I	- n-th A/D input channel of section A.
AGND A	=		- Ground of section A A/D input channels.
+5 Vdc	=	O	- Power supply +5 Vdc.
+12 Vdc	=	O	- Power supply +12 Vdc, coming from **ABACO®** BUS.
GND	=		- Ground.

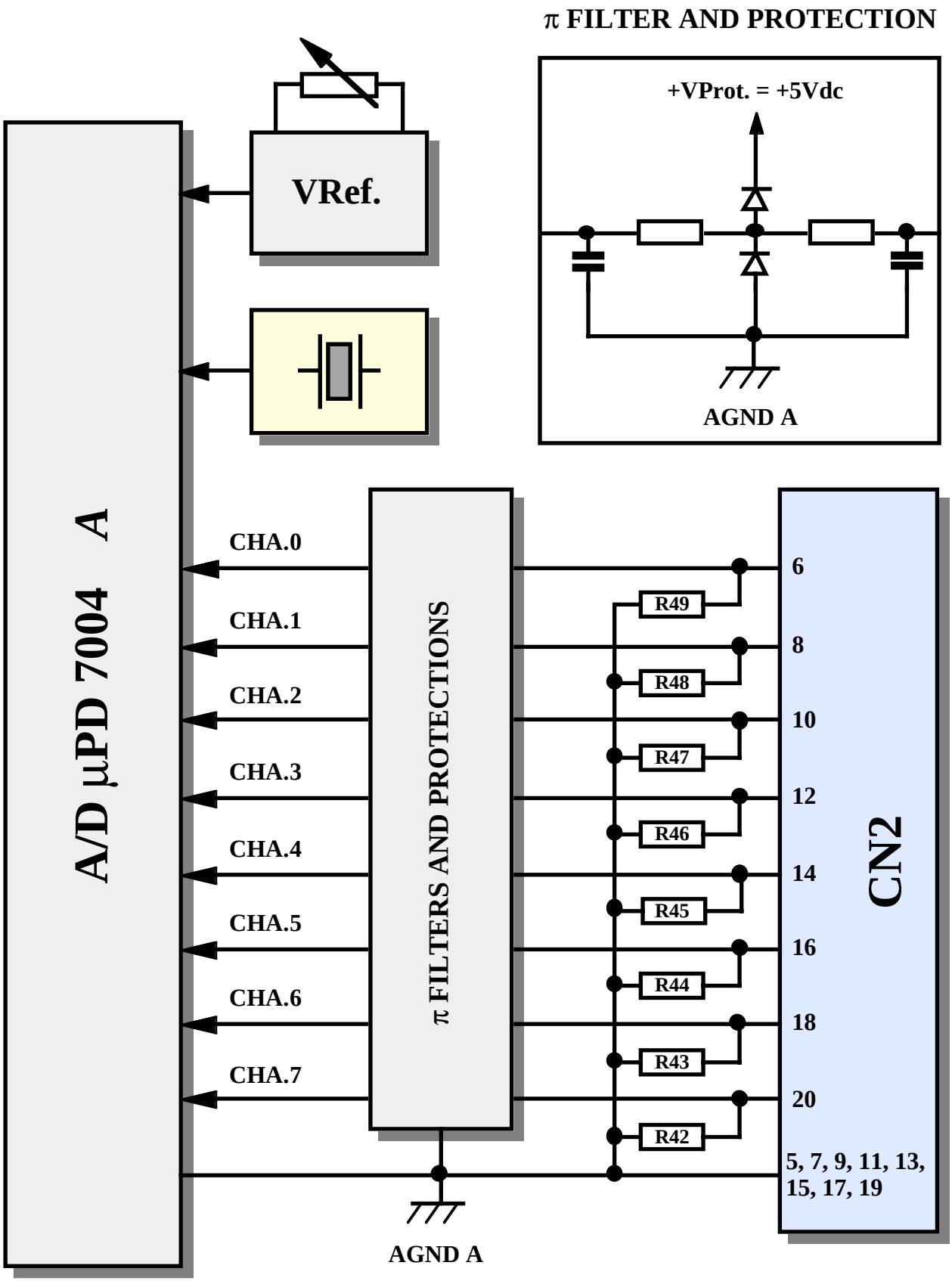

FIGURE 7: A/D CONVERTER OF SECTION A BLOCK DIAGRAM

K1 - CONNECTOR FOR ABACO® BUS

The connector for **ABACO® industrial BUS**, called K1 on the board,is a DIN 41612, male, a 90 °, type C, A+C.
Here follows the pin-out of the connector installed on **LAD 02**, in addition there is the standard 8 bits and 16 bits**ABACO®** BUS pin-out.
Please remark that all the signals here described are TTL, except for the power supplies.

A 16 bit BUS	A 8 bit BUS	A LAD 02	PIN	C LAD 02	C 8 bit BUS	C 16 bit BUS
GND	GND	GND	1	GND	GND	GND
+5 Vdc	+5 Vdc	+5 Vdc	2	+5 Vdc	+5 Vdc	+5 Vdc
D0	D0	D0	3	D8		D8
D1	D1	D1	4	D9		D9
D2	D2	D2	5	D10		D10
D3	D3	D3	6	N.C.	/INT	/INT
D4	D4	D4	7	N.C.	/NMI	/NMI
D5	D5	D5	8	D11	/HALT	D11
D6	D6	D6	9	N.C.	/MREQ	/MREQ
D7	D7	D7	10	/IORQ	/IORQ	/IORQ
A0	A0	A0	11	/RD	/RD	/RDLDS
A1	A1	A1	12	/WR	/WR	/WRLDS
A2	A2	A2	13	D12	/BUSAK	D12
A3	A3	A3	14	/WAIT	/WAIT	/WAIT
A4	A4	A4	15	D13	/BUSRQ	D13
A5	A5	A5	16	N.C.	/RESET	/RESET
A6	A6	A6	17	/M1	/M1	/IACK
A7	A7	A7	18	D14	/RFSH	D14
A8	A8	N.C.	19	N.C.	/MEMDIS	/MEMDIS
A9	A9	N.C.	20	N.C.	VDUSEL	A22
A10	A10	N.C.	21	D15	/IEI	D15
A11	A11	N.C.	22	N.C.		
A12	A12	N.C.	23	CLK	CLK	CLK
A13	A13	N.C.	24	/RDUDS		/RDUDS
A14	A14	N.C.	25	/WRUDS		/WRUDS
A15	A15	N.C.	26	N.C.		A21
A16		N.C.	27	N.C.		A20
A17		N.C.	28	N.C.		A19
A18		N.C.	29	N.C.	/R.T.	/R.T.
+12 Vdc	+12 Vdc	+12 Vdc	30	N.C.	-12 Vdc	-12 Vdc
+5 Vdc	+5 Vdc	+5 Vdc	31	+5 Vdc	+5 Vdc	+5 Vdc
GND	GND	GND	32	GND	GND	GND

FIGURE 8: K1 - CONNECTOR FOR ABACO® BUS

Signals description:

8 bits CPU

A0-A15	=	O	- Address BUS
D0-D7	=	I/O	- Data BUS
INT	=	I	- Interrupt request
NMI	=	I	- Non Maskable Interrupt
HALT	=	O	- Halt state
MREQ	=	O	- Memory Request
IORQ	=	O	- Input Output Request
RD	=	O	- Read cycle status
WR	=	O	- Write cycle status
BUSAK	=	O	- BUS Acknowledge
WAIT	=	I	- Wait
BUSRQ	=	I	- BUS Request
RESET	=	O	- Reset
M1	=	O	- Machine cycle one
RFSH	=	O	- Refresh for dynamic RAM
MEMDIS	=	I	- Memory Display
VDUSEL	=	O	- VDU Selection
IEI	=	I	- Interrupt Enable Input
CLK	=	O	- System clock
R.B.	=	I	- Reset button
+5 Vdc	=	I	- Power supply at +5 Vdc
+12 Vdc	=	I	- Power supply at +12 Vdc
-12 Vdc	=	I	- Power supply at -12 Vdc
GND	=		- Ground signal

16 bits CPU

A16-A22	=	O	- Address BUS
D8-D15	=	I/O	- Data BUS
RD UDS	=	O	- Read Upper Data Strobe
WR UDS	=	O	- Write Upper Data Strobe
IACK	=	O	- Interrupt Acknowledge
RD LDS	=	O	- Read Lower Data Strobe
WR LDS	=	O	- Write Lower Data Strobe

NOTE
Directionality indications as above stated are referred to a master (**GPC®**) board and have been kept untouched to avoid ambiguity in case of multi-boards systems.

VISUAL SIGNALATIONS

LAD 02 card is provided with signalation LEDs to show several status informations, as described in the following table:

LED	COLOUR	PURPOSE
LD1	Yellow	If ON, indicates that 8 bit data BUS has been selected.
LD2	Red	If ON, indicates that 16 bit data BUS has been selected.
LD3	Green	Indicates the presence of **+Van** supply voltage for analog section, generated by the on board DC/DC converter.
LD4	Red	Indicates the presence of 5.120 Vdc, reference voltage for A/D converters.

FIGURE 9: VISUAL SIGNALATIONS TABLE

The main purpose of LEDs is to show a visual indication about the card's status, making so easier debug and verify operations. To easily locate these visual signalations please refer to the figure 3.

POWER SUPPLY

LAD 02 is provided with an efficent circuitery that solves in a comfortable and simple way the problem of the board's supply, under any condition of use.
Here follow the voltages nedded:

+5 Vdc: Supplies the on board logic; must be in the range +5 Vdc ± 5% and must be provided through the specific pins of connector K1 (**ABACO®** BUS).
Please note that this voltage is available on connectors CN1 and CN2 to supply eventual external circuits; maximum total current is 600 mA.

+12 Vdc: Not used by the board but hawever available on connectors CN1 and CN2 to supply eventual external circuits. It must be provided through pin 30A of connector K1 (**ABACO®** BUS). It can be used to supply eventual external circuits that condition the analog signals; maximum total current is 500 mA.

A positive booster installed on **LAD 02** board is charged to provide the voltages needed by the digital to analog conversion section. Such DC/DC converter generates the voltages starting from the unique +5 Vdc power supply and needs no software management.

To warrant great immunity to external noise and so a correct working of the board, it is essential that **+5 Vdc** tension is galvanically isolated.

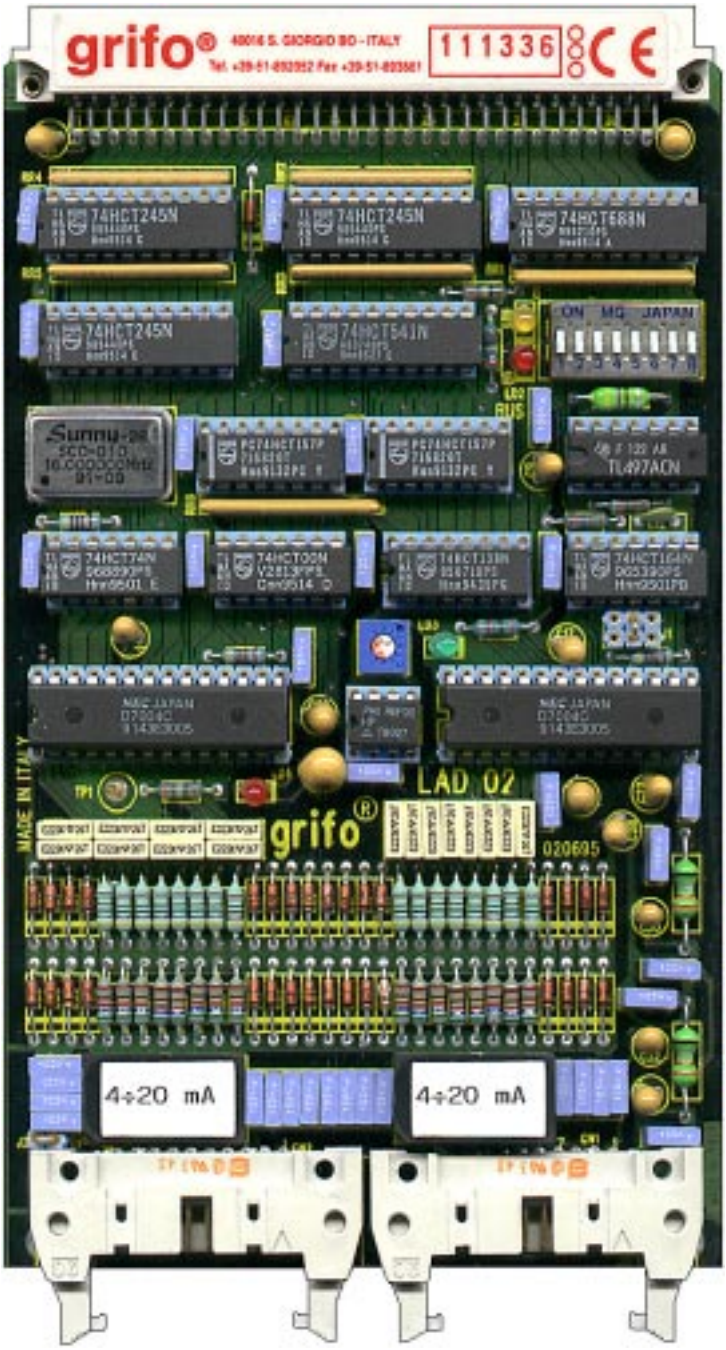

FIGURE 10: CARD PHOTO

JUMPERS

On **LAD 02** board there are 3 jumpers for card configuration. Below there is the jumpers list, location and function.

JUMPERS	N. PINS	PURPOSE
J1	6	Selects the number of wait cycles generated by the specific circuitry.
J2	2	Selects whether to connect or not the front panel mechanical mounting holes to the on board ground line.
DIP1.1	2	Selects between 8 or 16 bits data BUS.

FIGURE 11: JUMPERS SUMMARIZING TABLE

The following tables describe all the right connections of **LDA 01** jumpers with their relative functions. To recognize these valid connections, please refer to the board printed diagram (serigraph) or to figure 2 of this manual, where the pins numeration is listed; for recognizing jumpers location, please refer to figure 3.
The "*" used in the following tables, denotes the default connection, or on the other hand the connection set up at the end of testing phase, that is the configuration the User receives.

2 PINS JUMPERS

JUMPER	CONNECTION	PURPOSE	DEF.
J2	not connected	It does not connect the front panel mechanical mounting holes to the on board ground line.	*
	connected	It connects the front panel mechanical mounting holes to the on board ground line.	
DIP1.1	OFF	Configures the board to be managed through a 16 bits wide data BUS.	
	ON	Configures the board to be managed through an 8 bits wide data BUS.	*

FIGURE 12: 2 PINS JUMPERS TABLE

6 PINS JUMPERS

JUMPER	CONNECTION	PURPOSE	DEF.
J1	position 1-4	Configures the board to introduce 4 Wait cycles in the I/O operations.	*
	position 2-5	Configures the board to introduce 6 Wait cycles in the I/O operations.	
	position 3-6	Configures the board to introduce 8 Wait cycles in the I/O operations.	

FIGURE 13: 6 PINS JUMPERS TABLE

WAIT STATE GENERATOR

LAD 02 board is provided with a sophisticated Wait State generator designed to act directly to **ABACO®** BUS and, if enabled, capable to insert a configurable number of wait states in the I/O operations of **LAD 02** board.
The previously described jumper J1 is used to set the number of wait states to introduce (4, 6 or 8). In its default configuration **LAD 02** board is delivered with wait state circuitry disabled (the output is not connected to the /WAIT signal of **ABACO®** BUS). Please contact **grifo®** directly is you need to enable this functionality.
To easily locate jumper J1 please refer to figure 3.

NOTE
The correct working of on board wait state generator depends on the presence of CLK signal from **ABACO®** BUS. Please refer to the technical manual of the intelligent control card being used (**GPC®** serie) to chek its effective presence.
For further information please contact **grifo®** directly.

BOARD CONNNECTIONS

To prevent possible connecting problems between **LAD 02** board and the external systems, the user has to read carefully the information of the previous paragraphs and he must follow these instrunctions:

- The TTL signals can be connected directly only to a device featuring the same type of interface. About the correspondance between logic signals and TTL output status, remember that a logic **0** generates a TTL 0 Vdc, while a logic **1** generates a TTL +5 Vdc.

- The analog inputs (A/D section) must be connected to signals in the following ranges: 0÷5.120 V or 0÷20 mA according to the board configuration. Please remember that the sixteen analog inputs available on CN1 and CN2 are provided of π-filters and overvoltage protections that ensure an higher stability of the acquired signals, but reduce at the same time the bandwith frequency. For further informations please refer to the paragraph “TYPE OF ANALOG INPUT SELECTION”.

TEST POINT

The board is provided with one test point called **TP1**, that allow to read, through a galvanically isolated multimeter, the reference voltage (**Vref**) of the analog to digital conversion sections set in laboratory to 5.120 Vdc.
To easily locate the test points contacts please refer to figure 3, while for further information about the signal Vref please refer to the following paragraphs.

TYPE OF ANALOG INPUT SELECTION

LAD 02 board can accept analog voltage and/or current inputs, as described in the previous paragraphs and chapters. The input type selection must be made during the order phase and is performed mounting a specific current-to-voltage conversion modul (option code **.8420**) made by precision resistors. In detail:

R49	->	channel CHA.0
R48	->	channel CHA.1
R47	->	channel CHA.2
R46	->	channel CHA.3
R45	->	channel CHA.4
R44	->	channel CHA.5
R43	->	channel CHA.6
R42	->	channel CHA.7
R57	->	channel CHB.0
R56	->	channel CHB.1
R55	->	channel CHB.2
R54	->	channel CHB.3
R53	->	channel CHB.4
R52	->	channel CHB.5
R51	->	channel CHB.6
R50	->	channel CHB.7

Should the current-to-voltage conversion module not to be mounted (default case) the corresponding channel accepts a voltage input signal in the range 0÷5.120 V; otherwise a current input signal is accepted.
The value of the above mentioned resistors is obtained by the following spread;

R = 5.120 V / Imax

Usually the current-to-voltage conversion modules are made using **249 Ω** precision resistors, corresponding to input ranges 4÷20 mA or 0÷20 mA.
Any eventual configuration out of this standard shold be asked directly to **grifo®**.
To easily locate the current-to-voltage conversion module please refer to figure 3.

TRIMMERS AND CALIBRATION

On **LAD 02** board there is one trimmer, called **RV1**, that calibrate the output voltages of the A/D converter sections; in detail it allows to set reference voltage for both sections.
The **LAD 02** is subjected to a careful test that verifies and calibrates all the card sections.
The calibration is executed in laboratory, with a conntrolled +20° C room temperature, following these steps:

-The A/D reference voltage (Vref) is calibrated through RV1 trimmer, by using a 5 digits precision multimeter, to the value of +5.120 Vdc on test point TP1.

- The corrispondance between the analog input signal and the combination read from A/D is verified. This check is performed with a reference signal connected to A/D inputs and testing that the A/D combination and the theoric combination differ at maximum of the A/D section errors sum.

- The trimmer is blocked with paint.

The analog interfaces use high precision components that are selected during mounting phase to avoid complicate and long calibration procedures. After the calibration, the on board trimmers are blocked with paint to mantain calibration also in presence of mechanic stresses (vibrations, movings, delivery, etc.).
The reference voltage circuitery determines also the full range value for all the 16 analog input channels.
The user most not intervernt on the circuit that generates the reference voltage, however if this should be necessary (exampe: for time derives) then he/she must follow the above mentioned procedure.
To easily locate the above mentioned components please refer to figure 3; for further information about test points please refer to the previous paragraph; for further information about how to set the A/D converters output voltages please refer to chapter “SOFTWARE DESCRIPTION”.

HARDWARE DESCRIPTION

This chapter provides all the hardware informations needed to use **LAD 02** board. Here the user will find informations about I/O card mapping and on board peripheral devices addressing.

BOARD MAPPING

LAD 02 board is mapped into a **4** bytes I/O addressing space (or two words in 16 bits addressing mode), that can be mapped starting from different base addresses according to how the board is configured. This feature allows to use several **LAD 02** cards on the same **ABACO®** BUS, or to install them on a BUS where other peripheral modules are installed obtaining a structure that can be expanded without any difficulty or modifications to the application software.
The base address can be defined through the specific BUS interface circuitry on the board itself; this circuitry uses the eight pins dip switch called **DIP1**, from which it reads the address set by the user. Here follows the corrispondance between dips configuration and address signals.

DIP1.1	->	*Please see paragraph "2 PINS JUMPERS"*	
DIP1.2	->	*Don't care*	*8 bits BUS data path (DIP1.1 **ON**)*
		Address A1, must be always ON	*16 bits BUS data path (DIP1.1 **OFF**)*
DIP1.3	->	Address A2	
DIP1.4	->	Address A3	
DIP1.5	->	Address A4	
DIP1.6	->	Address A5	
DIP1.7	->	Address A6	
DIP1.8	->	Address A7	

These dips are driven in complemented logic, this means that if a switch is **ON** generates a **logic zero**, viceversa if a switch is **OFF** generates a **logic one**.

When the board is configured for 16 bit BUS data path, DIP1.2 must be always **ON**, so **LAD 02** will be mapped only from addresses with **A1=0**.

NOTE
When allocating the mapping address of the boards, plase be careful not to allocate more than one device in the same addressing space (count also the number of bytes occupied by the card). If this condtion will not be respected, a BUS conflict will happen; such conflict will compromise the correct working of the whole system.

As an example, some possible mappings are reported here.

1) Address used to map **LAD 02**: 048H
Control board used: featuring 8 bits BUS.

DIP1.1	->	ON
DIP1.2	->	Don't care
DIP1.3	->	ON
DIP1.4	->	OFF
DIP1.5	->	ON
DIP1.6	->	ON
DIP1.7	->	OFF
DIP1.8	->	ON

2) Address used to map **LAD 02**: A4H
Control board used: featuring 16 bits BUS.

DIP1.1	->	OFF
DIP1.2	->	ON
DIP1.3	->	OFF
DIP1.4	->	ON
DIP1.5	->	ON
DIP1.6	->	OFF
DIP1.7	->	ON
DIP1.8	->	OFF

To easily locate jumpers and dip switches please refer to figure 3.

INTERNAL REGISTERS ADDRESSING

Indicating the board base address with <**baseaddr**>, that is the address set using dip switch DIP1, as indicated in the previous paragraph **LAD 02** internal registers are addressable as explained in the following tables, respectively when addressing mode is 8 bit and 16 bit.

INTERNAL REGISTERS ADDRESSING FOR 8 BIT ADDRESSING MODE

DEVICE	REG.	ADDRESS	R/W	PURPOSE
µPD 7004 A	ADLA	<baseaddr>+00H	R	Data register Low (bit D0÷D1) of section A µPD 7004 A/D converter.
	ADHA	<baseaddr>+01H	R	Data register High (bit D2÷D9) of section A µPD 7004 A/D converter.
	MUXA	<baseaddr>+00H	W	Channel selection register of section A µPD 7004 A/D converter.
	INITA	<baseaddr>+01H	W	Initialization register of section A µPD 7004 A/D converter.
µPD 7004 B	ADLB	<baseaddr>+02H	R	Data register Low (bit D0÷D1) of section B µPD 7004 A/D converter.
	ADHB	<baseaddr>+03H	R	Data register High (bit D2÷D9) of section B µPD 7004 A/D converter.
	MUXB	<baseaddr>+02H	W	Channel selection register of section B µPD 7004 A/D converter.
	INITB	<baseaddr>+03H	W	Initialization register of section B µPD 7004 A/D converter.

FIGURE 14: INTERNAL REGISTERS ADDRESSING TABLE FOR 8 BIT ADDRESSING MODE

INTERNAL REGISTERS ADDRESSING FOR 16 BIT ADDRESSING MODE

DEVICES	REG.	INDIRIZZO	R/W	SIGNIFICATO
µPD 7004 A and B	ADL	<baseaddr>+00H	R	Data register Low (bit D0÷D1) of sections A and B µPD 7004 A/D converters.
	ADH	<baseaddr>+02H	R	Data register High (bit D2÷D9) of sections A and B µPD 7004 A/D converters.
	MUX	<baseaddr>+00H	W	Channel selection register of sections A and B µPD 7004 A/D converters.
	INIT	<baseaddr>+02H	W	Initialization register of sections A and B µPD 7004 A/D converters.

FIGURE 15: INTERNAL REGISTERS ADDRESSING TABLE FOR 16 BIT ADDRESSING MODE

PERIPHERAL DEVICES SOFTWARE DESCRIPTION

In the previous paragraph allocation addresses of all the peripherals have been reported, here follows a detailed description of function and meaning of internal registers (please always refer to the peripheral mapping tables to understand completely the following informations). Should the present documentaion be inadequate please refer to the component's manufacturer documentation.
In the following paragraphs the indications **D0÷D7** or **D0÷D15** are used to refer the bits of the byte or word involved in the I/O operations.

A/D CONVERTER µPD 7004

Management of 10 bits A/D converters µPD 7004 is performed through I/O operations to its specific control registers described in figures 14 and 15.
Here follows the meaning of the bits in the registers.

Registers MUXA, MUXB and MUX:
These write registers allow to program the A/D converter internal multiplexer to select which channel must be converted.
The meaning of their bits is:

8 bits data BUS			*16 bits data BUS*		
MUXB.D7÷D3	->	NU	**MUX.D15÷D11**	->	NU
MUXB.D2	->	CH2B	**MUX.D10**	->	CH2B
MUXB.D1	->	CH1B	**MUX.D9**	->	CH1B
MUXB.D0	->	CH0B	**MUX.D8**	->	CH0B
MUXA.D7÷D3	->	NU	**MUX.D7÷D3**	->	NU
MUXA.D2	->	CH2A	**MUX.D2**	->	CH2A
MUXA.D1	->	CH1A	**MUX.D1**	->	CH1A
MUXA.D0	->	CH0A	**MUX.D0**	->	CH0A

where:NU = Not Used

CH2x	CH1x	CH0x	= It selects input channel for A/D of section x:
0	0	0	-> channel 0
0	0	1	-> channel 1
0	1	0	-> channel 2
0	1	1	-> channel 3
1	0	0	-> channel 4
1	0	1	-> channel 5
1	1	0	-> channel 6
1	1	1	-> channel 7

NOTE
The conversion on the selected channel starts only when both write registers (MUX and INIT) are set. The sequence by which they are written to is not important (first MUX next INIT is the same as first INIT next MUX).

Registers INITA, INITB and INIT:
These write register allow to initialize A/D converters of sections A and B, selecting the format of the data returned and the division factor for the external clock.
The meaning of their bits is:

8 bits data BUS			*16 bits data BUS*		
INITB.D7÷D3	->	NU	**INIT.D15÷D11**	->	NU
INITB.D2	->	B/CB	**INIT.D10**	->	B/CB
INITB.D1	->	DV1B	**INIT.D9**	->	DV1B
INITB.D0	->	DV0B	**INIT.D8**	->	DV0B
INITA.D7÷D3	->	NU	**INIT.D7÷D3**	->	NU
INITA.D2	->	B/CA	**INIT.D2**	->	B/CA
INITA.D1	->	DV1A	**INIT.D1**	->	DV1A
INITA.D0	->	DV0A	**INIT.D0**	->	DV0A

where:NU = Not Used
B/Cx = It selects the format of data returned by A/D on section x:
0 -> Two's complement
1 -> Binary
DV1x DV0x = Programs theclock frequence divider of A/D on section x:
0 0 -> A/D work frequence = external clock divided by 1
0 1 -> A/D work frequence = external clock divided by 2
1 0 -> A/D work frequence = external clock divided by 4
1 1 -> A/D work frequence = external clock divided by 8

NOTE
1) LAD 02 is capable to generate the clock signal for the A/D converters through its 8 MHz clock source; **µPD 7004** maximum work frequence is 1 MHz, so the bits of clock divider must be always programmed to 1 (division by 8). Any other combination will cause board malfunctions.

2) The conversion on the selected channel starts only when both write registers (MUX and INIT) are set. The sequence by which they are written to is not important (first MUX next INIT is the same as first INIT next MUX).

Registers ADLA, ADHA, ADLB, ADHB, ADL and ADH:
There read registers allow to acquire the conversion value measured by A/D converters of sections A and B. Such 10 bits value is proportional to the input analog voltage according to the following correspondance:

Voltage		*Combination*
0 V	->	0
5,120 V	->	1023 ($3FF_{HEX}$)

The meaning of their bits is:

8 bits data BUS			*16 bits data BUS*		
ADHB.D7	->	C9B	**ADH.D15**	->	C9B
ADHB.D6	->	C8B	**ADH.D14**	->	C8B
ADHB.D5	->	C7B	**ADH.D13**	->	C7B
ADHB.D4	->	C6B	**ADH.D12**	->	C6B
ADHB.D3	->	C5B	**ADH.D11**	->	C5B
ADHB.D2	->	C4B	**ADH.D10**	->	C4B
ADHB.D1	->	C3B	**ADH.D9**	->	C3B
ADHB.D0	->	C2B	**ADH.D8**	->	C2B
ADHA.D7	->	C9A	**ADH.D15**	->	C9A
ADHA.D6	->	C8A	**ADH.D14**	->	C8A
ADHA.D5	->	C7A	**ADH.D13**	->	C7A
ADHA.D4	->	C6A	**ADH.D12**	->	C6A
ADHA.D3	->	C5A	**ADH.D11**	->	C5A
ADHA.D2	->	C4A	**ADH.D10**	->	C4A
ADHA.D1	->	C3A	**ADH.D9**	->	C3A
ADHA.D0	->	C2A	**ADH.D8**	->	C2A
ADLB.D7	->	C1B	**ADL.D15**	->	C1B
ADLB.D6	->	C0B	**ADL.D14**	->	C0B
ADLB.D5÷D0	->	NU	**ADL.D13÷D8**	->	NU
ADLA.D7	->	C1A	**ADL.D7**	->	C1A
ADLA.D6	->	C0A	**ADL.D6**	->	C0A
ADLA.D5÷D0	->	NU	**ADL.D5÷D0**	->	NU

where:NU = Not Used
C9x÷C0x = 10 bit combination read by A/D converter on section x

CONVERSION EXECUTION

Here follows the sequence of operations to perform for executing an A/D conversion on a channel of **LAD 02**:

1) Write to MUXx register (8 bit data BUS) or MUX register (16 bit data BUS) the data to select which channel to convert.
2) Write to INITx register (8 bit data BUS) or INIT register (16 bit data BUS) the data to select which conversion value format is needed and how to program the internal clock divider; please remark that on **LAD 02** this setting must be always 8.
This second write operation starts the conversion on the selected channel.
3) Wait for **100 µsec** to have the conversion executed.
4) Read from ADHx register (8 bit data BUS) or ADH register (16 bit data BUS) bits D9÷D2 of the conversione value.
5) Read from ADLx register (8 bit data BUS) or ADL register (16 bit data BUS) bits D1÷D0 of the conversione value.
6) Elaboration of the value obtained.

EXTERNAL CARDS

LAD 02 can be connected to a wide range of block modules and operator interface system produced by **grifo®**, or to many system of other companies.The on board resources can be expanded with a simple connection to the numerous peripheral **grifo®** boards,both intelligent and not, thanks to its standard **ABACO®** BUS connector. Even cards with **ABACO®** I/O BUS can be connected, by using the proper mother boards.
Hereunder some of these cards are briefly described; ask the detailed information directly to **grifo®**, if required.

MB3 01-MB4 01-MB8 01
Mother Board 3, 4, 8 slots
Motherboard featuring 3, 4 or 8 slots of **ABACO®** industrial BUS; pitch 4 TE; standard power supply connectors; LEDs for visual feed-back of power supply; holes for rack docking.

SPB 04-SPB 08
Switch Power BUS 4-8 slots
Motherboard featuring 4-8 slots of **ABACO®** industrial BUS; pitch 4 TE; standard power supply connectors; termination resistances; connector type F for **SPC xxx** supply ; holes for rack docking.

ABB 03
ABACO® Block BUS 3 slots
3 slots **ABACO®** mother board; 4 TE pitch connectors; **ABACO®** I/O BUS connector; screw terminal for power supply; connection for DIN C type and Ω rails.

ABB 05
ABACO® Block BUS 5 slots
5 slots **ABACO®** mother board with power supply. Double power supply built in; 5Vdc 2,5A section for powering the on board logic; second section at 24Vdc 400mA galvanically coupled, for the optocoupled input lines. Auxiliary connector for **ABACO®** I/O BUS. Connection for DIN Ω rails.

SPC 03.5S
Switch Power Card +5 Vdc
Europe format switching power supply capable to provide +5 Vdc to a load of 4 A; input voltage 12÷24 Vac; power-failure; connector for back-up battery; standard connector for mother board **SPB 0x**.

SPC 512
Switch Power Card +5 Vdc +12 Vdc
Europe format switching power supply capable to provide +5 Vdc 5A and +12 Vdc 2.5 A; input voltage 12÷24 Vac; power-failure; connector for back-up battery; standard connector for mother board **SPB 0x**.

FBC 20-120
Flat Block Contact 20 vie
Interface for 2 or 1 mounting cable connectors (low profile 20 pins male) and quick release screw terminal connectors; Plastic mount for rails DIN 46277-1 and 3.

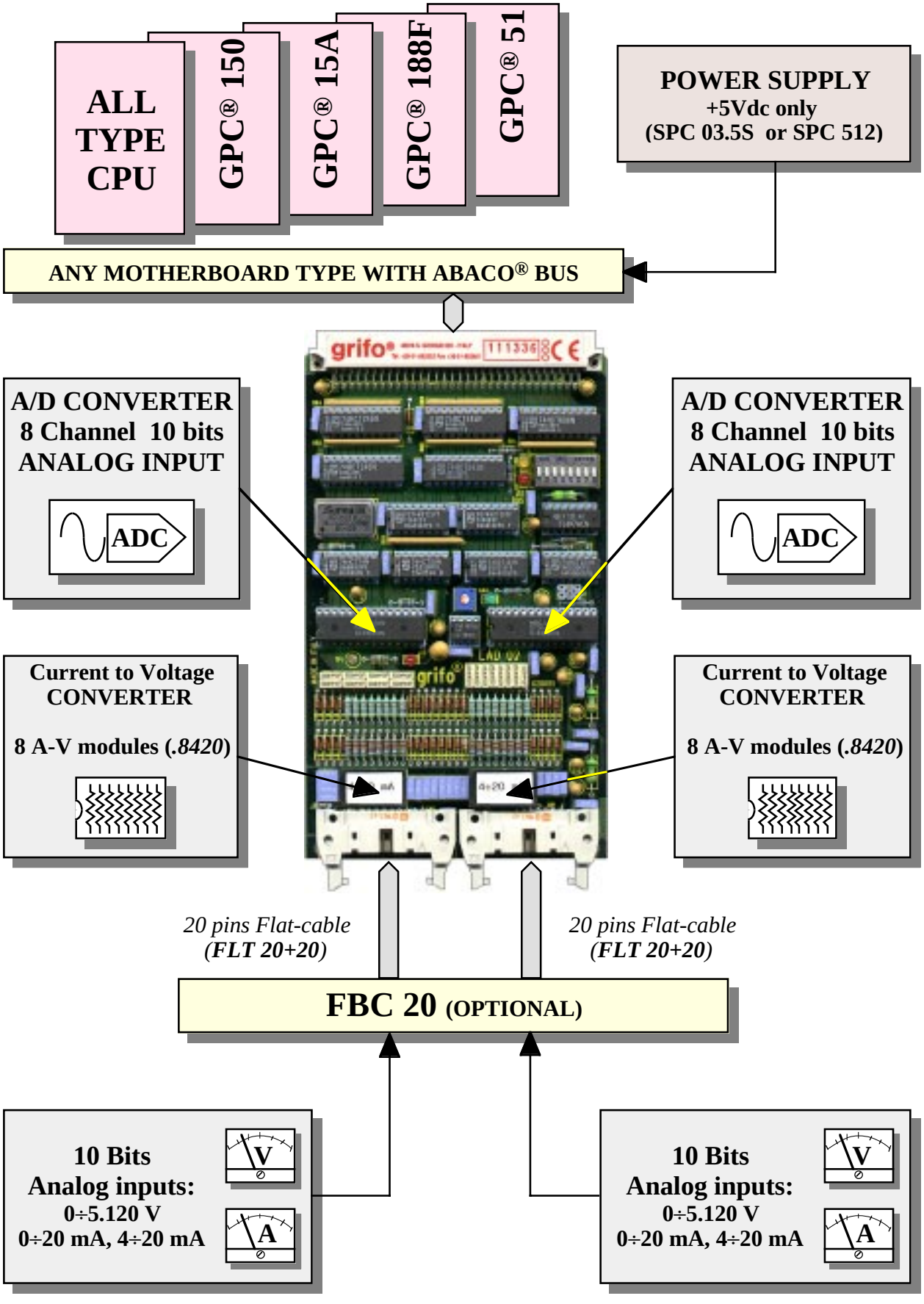

FIGURE 16: POSSIBLE CONNECTIONS DIAGRAM

GPC® 51

General Purpose Controller fam. 51

Microprocessor family 51 INTEL including the masked BASIC chip; the board features: 16 I/O TTL lines; dip switch; 3 timer/counter; RS 232; 4 A/D converter signals resolution 11 bit; buzzer; on board EPROM programmer; RTC and 32K SRAM with Lithium battery back up; controlloer for display and keyboard.

GPC® 188F

General Purpose Controller 80C188

80C188 µP 20MHz; 1 RS 232 line; 1 RS 232, RS 422-485 or Current Loop line; 24 TTL I/O lines; 1M EPROM or 512K FLASH; 1M RAM Lithium battery backed; 8K serial EEPROM; RTC; Watch Dog; 8 Dip switch; 3 Timer Counter; 8 13 bit A/D lines; Power failure; activity LEDs; single power supply +5Vdc.

GPC® 15A

General Purpose Controller 84C15

Full CMOS card, 10÷20 MHz 84C15 CPU; 512K EPROM or FLASH; 128K RAM; 8K RAM and RTC backed; 8K serial EEPROM; 1 RS 232 line; 1 RS 232 line or RS 422-485 or Current Loop line; 32 or 40 TTL I/O lines; CTC; Watch dog; 2 Dip switches; Buzzer.

GPC® 150

General Purpose Controller 84C15

Microprocessor Z80 at 16 MHz; implementation completely CMOS; 512K EPROM or FLASH; 512K SRAM; RTC; Back-Up through external Lithium battery; 4M serail FLASH ; 1 serial line RS 232 plus 1 RS 232 or RS 422-485 or current loop; 40 I/O TTL; 2 timer/counter; 2 watch dog; dip switch; EEPROM; A/D converter with resolution 12 bit; activity LED.

GPC® 15R

General Purpose Controller 84C15

84C15 µP, 10÷16 MHz; 1 RS 232 line; 1 RS 232 or RS 422-485 or C. L. line; 16÷24 TTL I/O lines; 16 Opto-in; 8 Relays; 4 Opto Coupled Timers Counters; 512K EPROM or FLASH; 512K RAM and RTC backed; 8K serial EEPROM; 8K Backed RAM modul; Buzzer; 1 Activity LED; Watch dog; 4÷12 readable DIPs; LCD Interface.

GPC® 323

General Purpose Controller 51 family

80C32 µP, 14 MHz; Full CMOS; 1 RS 232 line (software); 1 RS 232 or RS 422-485 or Current Loop line; 24 TTL I/O lines; 11 A/D 12 bits lines; 3 Timers Counters; 64K EPROM; 64K RAM; 32K RAM and RTC backed; 32K DIL EEPROM; 8K serial EEPROM; Buzzer; 2 Activity LED; Watch dog; 5 readable DIPs; LCD Interface.

GPC® 553

General Purpose Controller 80C552

80C552 µP, 22÷33 MHz; 1 RS 232 line (software); 1 RS 232 or RS 422-485 or Current Loop line; 16 TTL I/O lines; 8 A/D 10 bits lines; 3 Timers Counters; 64K EPROM; 64K RAM; 32K RAM and RTC backed; 32K DIL EEPROM; 8K serial EEPROM; 2 PWM lines; 1 Activity LED; Watch dog; 5 readable DIPs; LCD Interface.

GPC® 153

General Purpose Controller Z80

84C15 µP, 10÷16 MHz; Full CMOS; 1 RS 232 line; 1 RS 232 or RS 422-485 or Current Loop line; 16 TTL I/O lines; 8 A/D 12 bits lines; 2÷4 Timers Counters; 512K EPROM or FLASH; 512K RAM and RTC backed; 8K serial EEPROM; Buzzer; 1 Activity LED; Watch dog; 8 readable DIPs; LCD Interface.

GPC® 183

General Purpose Controller Z180

Z180 µP, 10÷16 MHz; Full CMOS; 1 RS 232 line; 1 RS 232 or RS 422-485 or Current Loop line; 24 TTL I/O lines; 11 A/D 12 bits lines; 2 Timers Counters; 512K EPROM or FLASH; 512K RAM and RTC backed; 8K serial EEPROM; Buzzer; 2 Activity LED; Watch dog; 4 readable DIPs; LCD Interface.

GPC® 324/D

"4" Type General Purpose Controller 80C32/320

80C32 or 80C320 µP, 14÷22 MHz; Full CMOS; 1 RS 232 line; 1 RS 232 or RS 422-485 or Current Loop line; 4÷16 TTL I/O lines; 3 Timers Counters; 64K EPROM; 64K RAM; 32K RAM backed; 32K DIL E2; 8K serial EEPROM; Watch dog; 1 readable DIP; LCD Interface; Abaco® I/O BUS; 5Vdc Power supply; Size: 100x50 mm.

GPC® 554

General Purpose Controller 80C552

Microprocessor 80C552 at 22 MHz; implementation completely CMOS; 32K EPROM; 32 K SRAM; 32 K EEPROM or SRAM; EEPROM; 2 RS 232 serial lines; 16 I/O TTL; 2 PWM lines; 16 bits Timer/Counter; Watch Dog; 6 signals A/D converter with resolution 10 bit; interface for **ABACO®** I/O BUS.

GPC® 154

"4" Type General Purpose Controller Z80

84C15 µP, 10÷16 MHz; Full CMOS; 1 RS 232 line; 1 RS 232 or RS 422-485 line; 16 TTL I/O lines; 2÷4 Timers Counters; 512K EPROM or FLASH; 512K RAM and RTC backed; 8K serial EEPROM; Watch dog; 2 readable DIPs; LCD Interface; Abaco® I/O BUS; 5Vdc Power supply; Size: 100x50 mm.

GPC® 884

General Purpose Controller Am188ES

Microprocessor AMD Am188ES up to 40 MHz16 bits; implementation completely CMOS; serie 4 format; 512K EPROM or FLASH; 512K SRAM backed with Lithium battery; RTC; 1 RS 232 serial line + 1 RS 232 or RS 422-485 or current loop; 16 I/O TTL; 3 timer/counter; watch dog; EEPROM; 11 signals A/D converter with 12 bit resolution; interface for **ABACO®** I/O BUS.

GPC® 114

General Purpose Controller 68HC11

Microprocessor 68HC11A1 at 8 MHz; implementation completely CMOS; serie 4 format; 32K EPROM; 32K SRAM backed with Lithium battery; 32K EPROM, SRAM, EEPROM; RTC; 1 serial line RS 232 or RS 422-485; 10 I/O TTL; 3 timer/counter; watch dog; 8 signals A/D converter with resolution 8 bit; 1 asunchronous serial line; extremly low power consumption; interface for **ABACO®** I/O BUS.

BIBLIOGRAPHY

Here follows a list of manuls thst can be a source of further informations about the devices installed on **LAD 02**.

Manual TEXAS INSTRUMENTS: *The TTL data Book - SN54/74 Families*
Manual TEXAS INSTRUMENTS: *Linear Circuits - Volume 3*

Manual NEC: *Microprocessor and Peripheral - Data Book Volume III*

Manual PMI: *Analog IC Data Book*

Please connect to the manifactures Web sites to get the latest version of all manuals and data sheets.

APPENDIX A: ALPHABETICAL INDEX

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