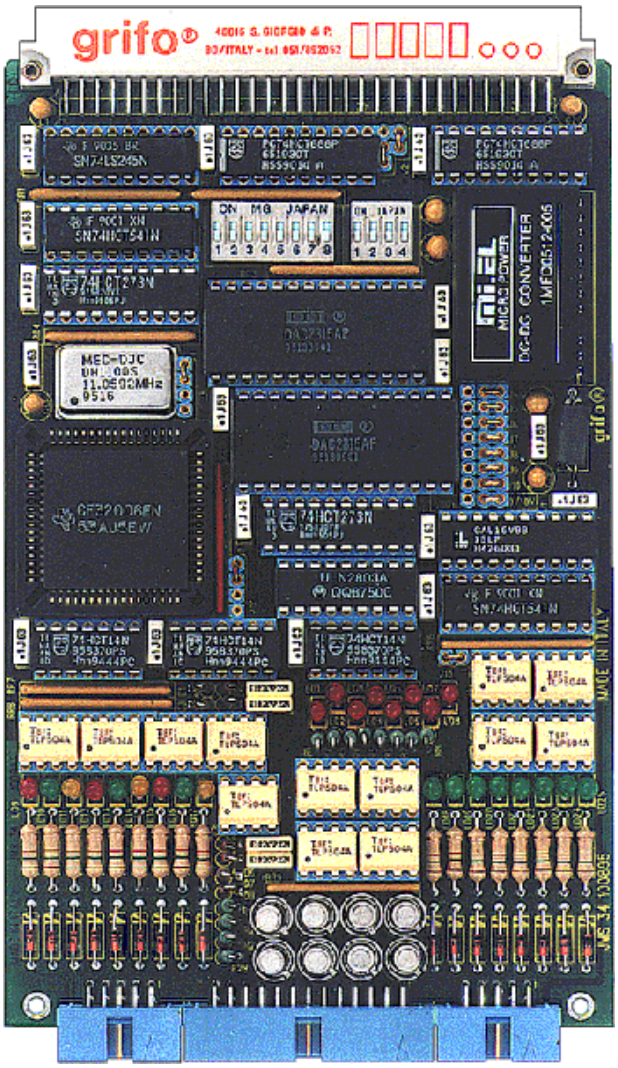
JMS 34

Jumbo Multifunction Support

TECHNICAL MANUAL



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JMS 34 Edition 5.00 *Rel. 09 January 2001*

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TECHNICAL MANUAL

JMS 34 board is a very powerful support module specifically designed to solve the problematics of axis control; in particular it can work out with encoder counting and acquisition and DC engines control management.
It works through the powerful 16 bit **ABACO®** industrial BUS and it can take advantage of the wide range of intelligent cards **ABACO®** compliant.
JMS 34 takes only 16 bytes in the bus addressing space; the base address can be allocated in the I/O addressing space through two comfortable dip switches. To improve the flexibility of the board it can be driven through 16 bit words across a 64 Kbyte addressing space.
JMS 34 can be provided with four **12 bit D/A converter** channels, or two channels only or no channel at all, and 3 **Encoders** or no encoders at all; it can be employed whenever problematics of counting, frequence or periods measurement, mixed analog and digital signals management, etc. must be solved.

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For specific informations on the components mounted on the card, please refer to the Data Book of the builder or second sources.

SYMBOLS DESCRIPTION

In the manual could appear the following symbols:

Attention: Generic danger

Attention: High voltage

Trade Marks

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Other Product and Company names listed, are trade marks of their respective companies.

GENERAL INDEX

FIGURES INDEX

INTRODUCTION

The use of these devices has turned - IN EXCLUSIVE WAY - to specialized personnel.

The purpose of this handbook is to give the necessary information to the cognizant and sure use of the products. They are the result of a continual and systematic elaboration of data and technical tests saved and validated from the manufacturer, related to the inside modes of certainty and quality of the information.

The reported data are destined- IN EXCLUSIVE WAY- to specialized users, that can interact with the devices in safety conditions for the persons, for the machine and for the enviroment, impersonating an elementary diagnostic of breakdowns and of malfunction conditions by performing simple functional verify operations , in the height respect of the actual safety and health norms.

The informations for the installation, the assemblage, the dismantlement, the handling, the adjustment, the reparation and the contingent accessories, devices etc. installation are destined - and then executable - always and in exclusive way from specialized warned and educated personnel, or directly from the TECHNICAL AUTHORIZED ASSISTANCE, in the height respect of the manufacturer recommendations and the actual safety and health norms.

The devices can't be used outside a box. The user must always insert the cards in a container that rispect the actual safety normative. The protection of this container is not threshold to the only atmospheric agents, but specially to mechanic, electric, magnetic, etc. ones.

To be on good terms with the products, is necessary guarantee legibility and conservation of the manual, also for future references. In case of deterioration or more easily for technical updates, consult the AUTHORIZED TECHNICAL ASSISTANCE directly.

To prevent problems during card utilization, it is a good practice to read carefully all the informations of this manual. After this reading, the user can use the general index and the alphabetical index, respectly at the begining and at the end of the manual, to find information in a faster and more easy way.

CARD VERSION

This handbook makes reference to boards version **100895** and following ones. The validity of the information contained in this manual is subordinated to the card version, so the user must always verify the correct correspondence beetween the notations. On the card the release number is present in more points both on printed diagram (serigraph) and printed circuit (for example in the lower right corner near DZ17 and R25).

GENERAL INFORMATIONS

JMS 34 (Jumbo Multifunction Support, 3 Encoder, 4 D/A) board is a very powerful support module specifically designed to solve the problematics of axis control; in particular it can work out with encoder counting and acquisition and DC engines control management.
It works through the powerful 16 bit **ABACO®** industrial BUS and it can take advantage of the wide range of intelligent cards **ABACO®** compliant, such as **GPC® F2**, **GPC® 51**, **GPC® 80F**, **GPC® 81F**, **GPC® 15A**, **GPC® 15R**, **GPC® 150**, **GPC® 188F**, etc..
All the components normally needed to drive **DC** or **BRUSHLESS** motors is already installed on **JMS 34** board.
JMS 34 takes only 16 bytes in the bus addressing space; the base address can be set in the I/O addressing space through two comfortable dip switches. To improve the flexibility of the board it can be driven through 16 bit words across a 64 Kbyte addressing space.
JMS 34 can be provided with four 12 bit D/A converter channels, or two channels only or no channel at all, and 3 Encoders or no encoders at all; it can be employed whenever problematics of counting, frequence or periods measurement, mixed analog and digital signals management, etc. must be solved.
To ease the connection to the external world, a set of **FBC** type **BLOCK** modules are available. These modules allow to untangle the wires of the flat cable to comfortable quick release screw terminal connectors.
The main features of **JMS 34** are:

- Eurocard format size 100x160 mm.
- Interface to **ABACO® Industrial BUS.**
- **Three Encoder** acquisition or **Counter** channels, galvanically isolated, capable to:
  Acquire three 16 bit incremental bidirectional , or one 32 bit bidirectional encoder and one 16 bit bidirectional encoder.
  Each counter can indipendently multiply the impulses in input by 1, 2 or 4.
  Galvanically isolated separate **zero pulse** input.
  Direction discriminator disconnectable.
  Inputs for +12÷24 Vdc encoder .
  Visualization through LEDs of the encoder lines status.
- Up to **four** 12 bits **D/A Converter** signals, output level selectable between ±10 Vdc or 0/10 Vdc.
- **8** NPN digital optocoupled inputs signals, visualized thtough LEDs.
  Inputs for +12÷24 Vdc.
- **8** optocoupled digital output signals, visualized through LEDs and buffered by open collector transistors. Outputs load 500 mA, 45 Vdc.
- On board DC/DC converter to generate the voltages required by the analog section.
- Unique power supply voltage +5 Vdc.

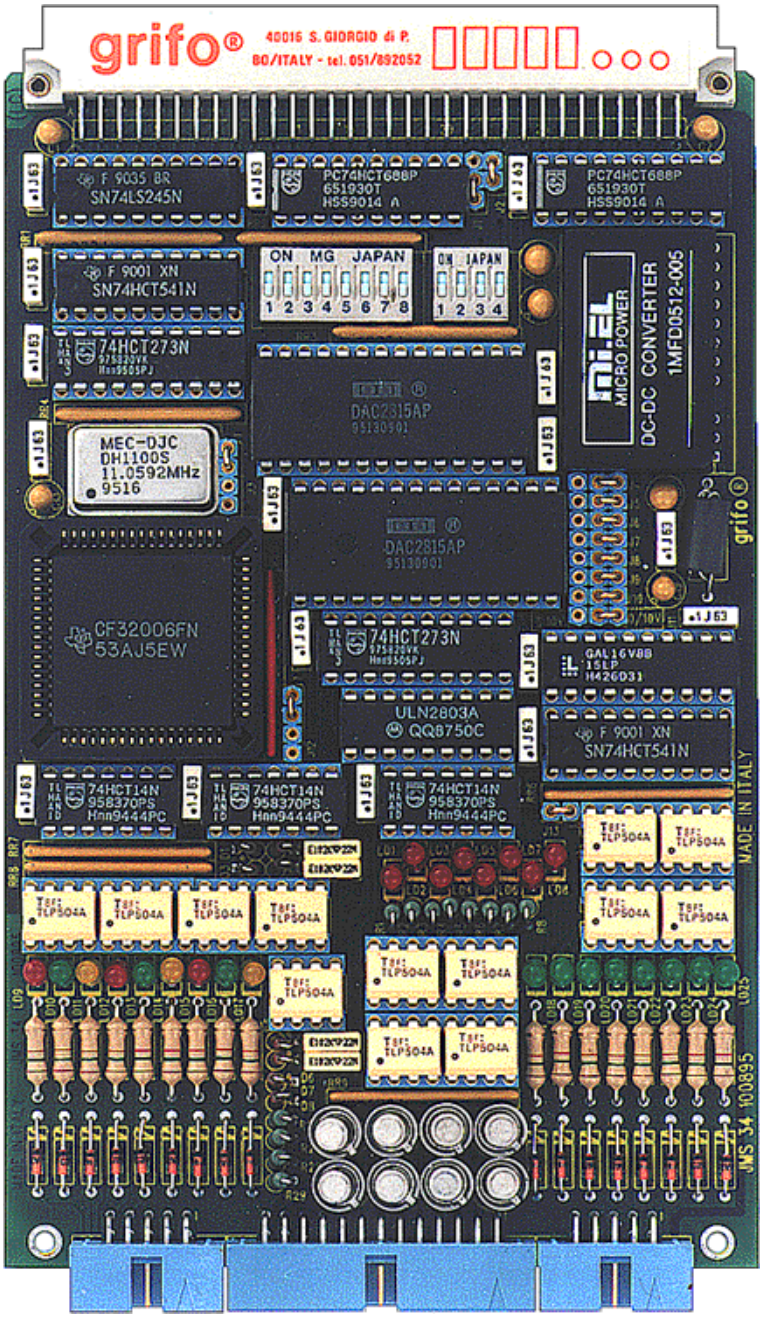


FIGURE 1: CARD PHOTO

Here follows a description of the board's functional blocks, with an indication of the operations performed by each one.
To easily locate the blocks and their interconnection please refer to figure 2.

CLOCK DEVICE

JMS 34 is provided with an on board clock circuitery section capable to generate the synchronization signal required by the peripherals. This allows to use the board matched to any CPU card regardless of its speed.

ENCODER INTERFACE SECTION

This section is based on a three channels up/down counter with separate reset input especially designed to acquire bidirectional encoders with separate zero pulse input.
Count mode can be selected by software, while by hardware it is possible to cascade two counters out of three to obtain one 32 bit counter and one 16 bit counter.
Software management of this peripheral is performed through 6 bytes (2 per counter) addressed according to the settings showed in the paragraph “BOARD MAPPING”.
All the input signals, including the zero pulses, are galvanically isolated and visualized through LEDs, optocouplers supply voltage may vary from +12 to +24 Vdc.
This section also includes an 8 bit latch, addressed according to the settings showed in the paragraph “BOARD MAPPING”, to manage by sofware the count mode of the encoder. Through this latch it is possible to set the status of 8 out of 9 counters configuration lines, the nineth line is configured moving a specific jumper.

D/A CONVERTER SECTION

This section is based on two 12 bits D/A converter each one featuring two independent conversion channels. On both devices the output voltage range can be set independently selecting between the ranges ±10 V or 0/10 V by acting on two specific groups of 3 pins jumpers.
Peripheral sofware programming is performed through 8 bytes addressed according to the settings showed in the chapter “BOARD MAPPING”.

DC/DC CONVERTER SECTION

JMS 34 features an on board positive booster whose task is to provide all the supply voltages needed by the digital-to-analog conversion section. This component generates two ±15 V voltages from the unique +5 Vdc board supply voltage and needs no software management.

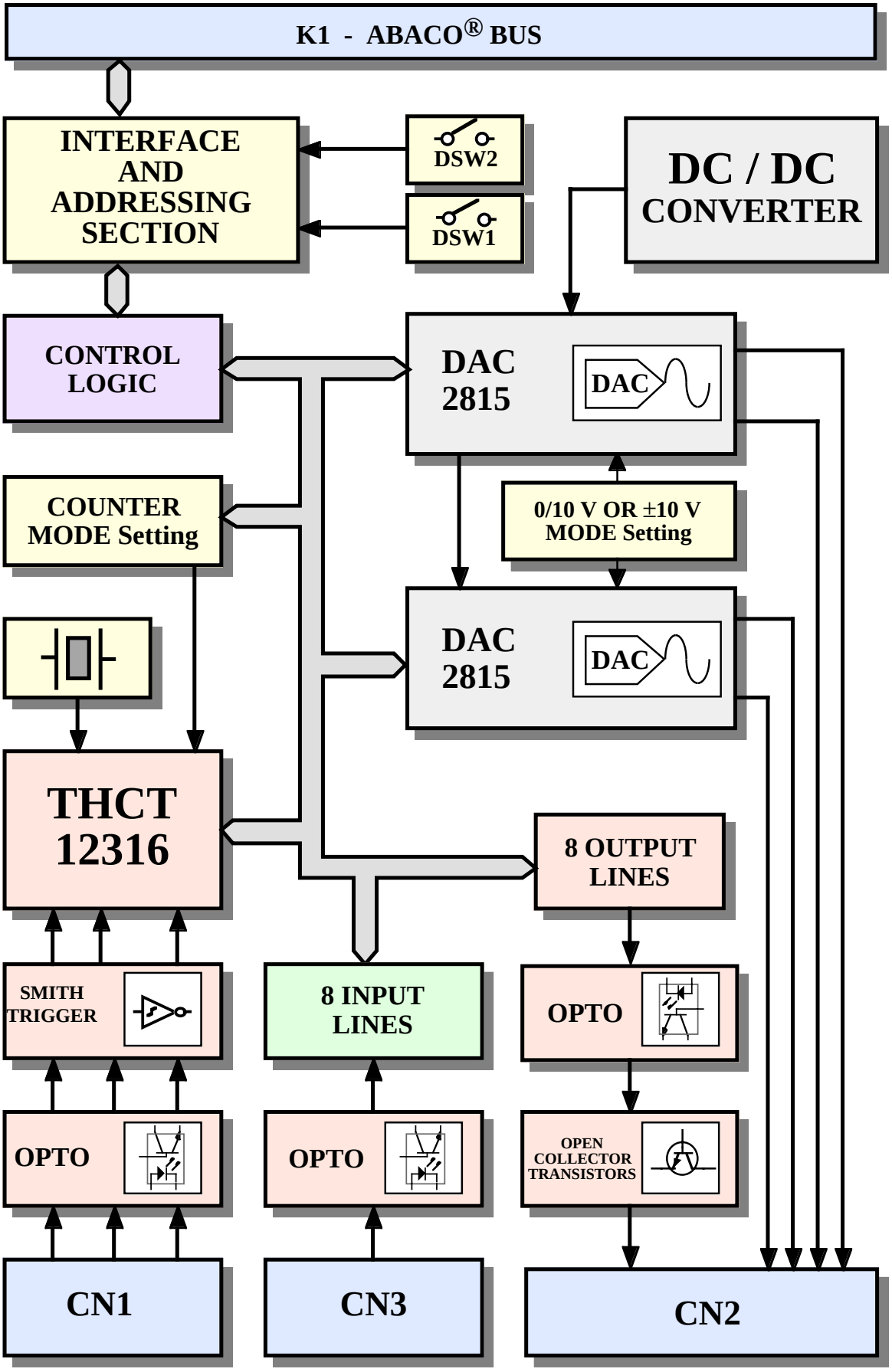


FIGURE 2: BLOCK DIAGRAM

INPUT SECTION

This section manages 8 TTL buffered input signals. Its management is performed through one register allocated in microprocessor I/O addressing space by a specific control logic, for further information please refer to paragraph “BOARD MAPPING”. Each input signal is galvanically isolated by a NPN optocoupler and its status is visualized through a green LED; optocoupler power supply may vary in the range +12÷24 Vdc.

OUTPUT SECTION

This section manages 8 TTL latched output signals. Its management is performed through one register allocated in microprocessor I/O addressing space by a specific control logic, for further information please refer to paragraph “BOARD MAPPING”. Each output signal drives an open collector transistor and its status is visualized through a red LED; maximum load for each transistor is +45 Vdc, 500 mA.

CONTROL LOGIC

This section generates all the chip select signals essential to access the **JMS 34** on board peripherals. It allows the programmer to reach the board devices and check their status, read the digital inputs and outputs, set the digital values to drive analog outputs, etc.
The control logic interfaces to **ABACO® Industrial BUS** through the addressing and interfacement section, the BUS connection allows an easy software management of al the sections.
For further information please refer to chapter “SOFTWARE DESCRIPTION”.

ADDRESSING AND INTERFACEMENT SECTION

This section manages the information interchange between control logic and external **GPC®** control cards. In detail, each byte read or written passes through this section, that also provides the I/O board mapping by one or two dip swithces.
In fact this section can be configured to address **JMS 34** in a 256 bytes or 64Kbytes I/O addressing range.
The **ABACO® Industrial BUS** interfacement has been designed anticipating an 8 bits data path.
For further information please refer to chapter “SOFTWARE DESCRIPTION”.

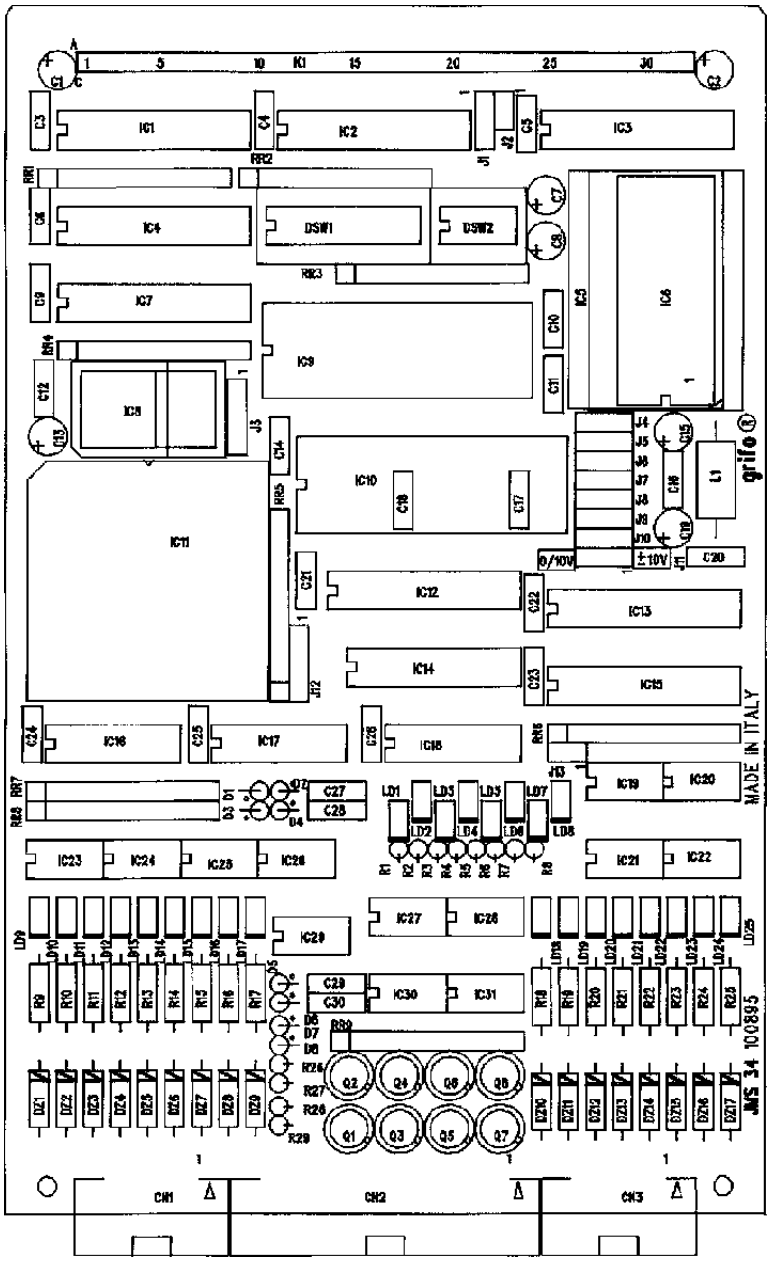


FIGURE 3: COMPONENTS MAP

TECHNICAL FEATURES

GENERAL FEATURES

On board resources:	**ABACO® Industrial BUS** 8 optocoupled digital input lines visualized through LED 8 open collector output lines visualized through LED 3 channels bidirectional encoder Up to 4 D/A converter channels
D/A converter resolution:	12 bit
D/A maximum nonlinearity:	±1/2 LSB
Encoder zero pulse input:	hardware managed
Addressing range:	selectable between 256 bytes and 64 Kbytes (65535)
Bytes taken:	16
Encoder clock:	11.0592 MHz
On board resources:	DAC2815 THCT 12316

PHYSICAL FEATURES

Size:	Standard Eurocard format 100x160 mm
Weight:	190 g
Connectors:	64 pins DIN 41612 M 90° A+C type C CN1: 10 pins low profile 90° M CN2: 26 pins low profile 90° M CN3: 10 pins low profile 90° M
Temperature range:	from 0 to 70 °C
Relative humidity:	20% up to 90% (without condense)

ELECTRIC FEATURES

Supply voltages: +5 Vdc (logic circuits)
+12÷24 Vdc (optocouplers for encoder and inputs)

Current consumption on +5Vdc: (*) - With only one DAC 2815 installed on IC10 (2 channels):
315 mA if all Input/Output are not actived and DAC has no load
480 mA if all Input/Output are actived and DAC output is set to +10V with a load of 2 KΩ
- With two DAC 2815 installed on IC9÷10 (4 channels):
400 mA if all Input/Output are not actived and DAC has no load
590 mA if all Input/Output are actived and DAC output is set to +10V with a load of 2 KΩ

Current consumption on +24 Vdc: (*) **215 mA**

Maximum voltage on transistor: (*) +30 Vdc

Maximum current on transistor: (*) 500 mA

Maximum power on transistor: (*) 500 mW

D/A converter output ranges: Selectable between ±10V or 0/10V

Maximum DAC output current: ±5 mA

DAC reference voltage: +10 Vdc generated on board

Optocouplers maximum frequence: (*)10 kHz

(*)
These values have been measured at 20 °C of environment temperature.

INSTALLATION

In this chapter there are the information for a right installation and correct use of the board. The user can find the location and functions of each connectors, trimmers, jumpers and some explanatory diagrams.

CONNECTIONS

The board has four connectors that can be linkeded to other devices or directly to the field, according to system requirements. In this paragraph there are connectors pin outs, a short signals description (including the signals direction) and connectors location, plus some figures that describe how the interface signals are connected on the card.
To easily locate the connectors please refer to figure 12.

CN3 - OPTOCOUPLED INPUTS CONNECTOR

CN3 is a 10 pins low profile 90° male 2.54 mm pitch connector.
On this connector the 8 NPN optocoupled digital inputs can be acquired; open collector transistors inputs and optocouplers supply pins ,+Vopto, are present.

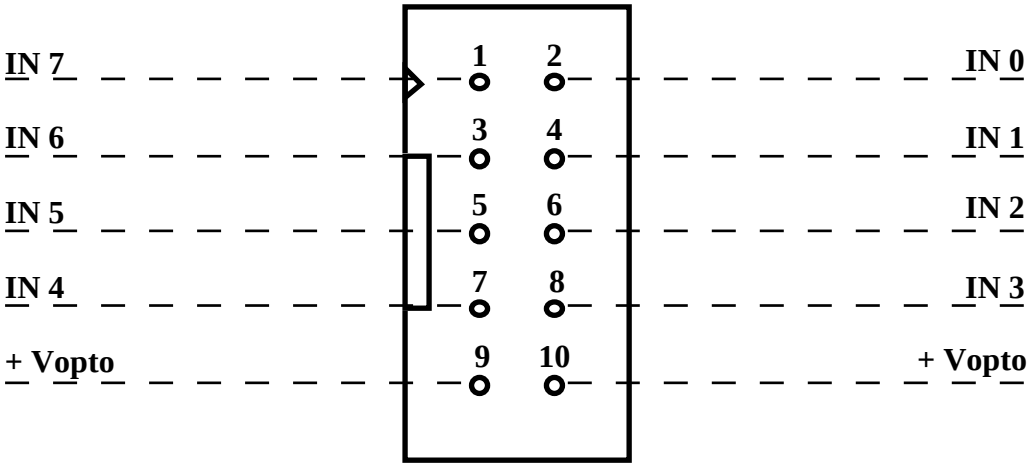


FIGURE 4: CN3 - OPTOCOUPLED INPUTS CONNECTOR

Signals description:

+Vopto = I - Positive terminal of optocouplers supply
IN n = I - n-th digital NPN optocoupled input

The 8 input signals available on **JMS 34** are Optocoupled to warrant a high degree of protecion for on board electronics against noise and disturbs from the external world.
Each signal is provided with a LED for visual feed back (the LED will light whenever the input will have the potential of GND opto signal); this means that the inputs are going to support normally open contacts. These contacts are suitable to be connected to NPN drivers. In case the User would want to connect PNP drivers then he/she will have to put a **PBI 01** BLOCK module between the drivers and the card.
The interface circuitry for this 8 inputs section is shown in the following diagram.
The Optocouplers power supply voltage may vary in the range from 12 Vdc to 24 Vdc and must be provided through the specific pins of connector CN3.

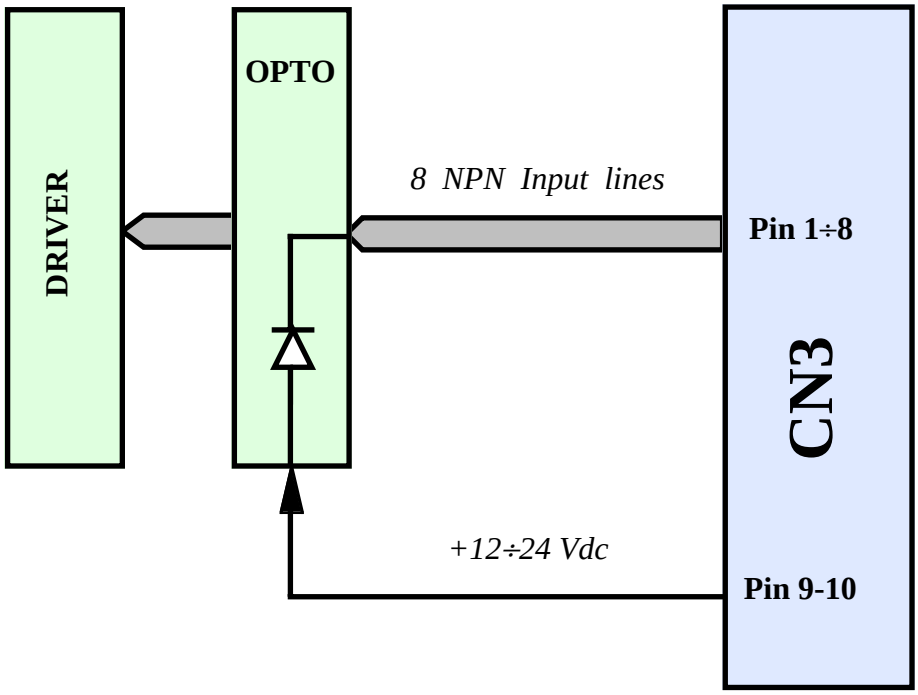


FIGURE 5: OPTOCOUPLED INPUT SECTION BLOCK DIAGRAM

CN1 - COUNTER INPUTS CONNECTOR

CN1 is a 10 pins low profile 90° male 2.54 mm pitch connector.
On this connector the NPN optocoupled digital inputs of the three counters in IC11 can be reached; optocouplers supply pin ,+Vopto, are present.

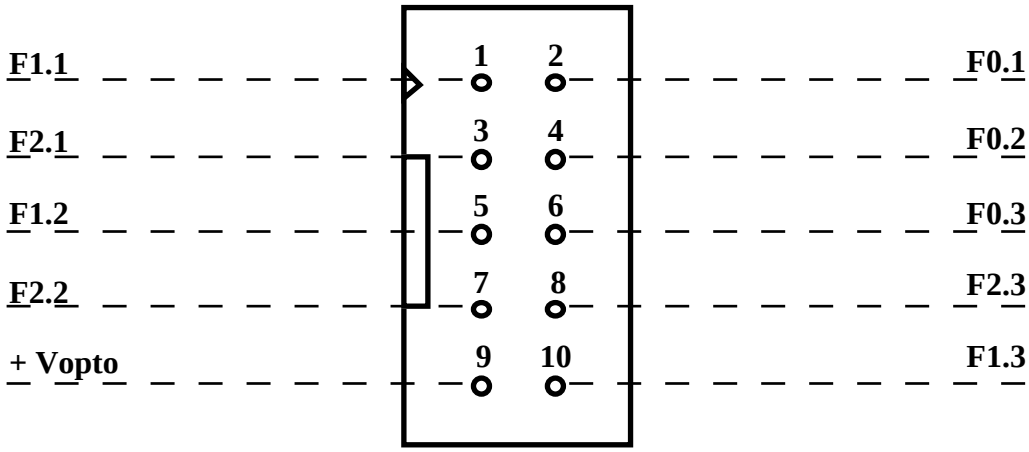


FIGURE 6: CN1 - COUNTER INPUTS CONNECTOR

Signals description:

+Vopto	=	I - Positive terminal of optocouplers supply
F1.1	=	I - Counter 1 quadrature signal 1 input
F2.1	=	I - Counter 1 quadrature signal 2 input
F0.1	=	I - Counter 1 zero pulse input
F0.2	=	I - Counter 2 zero pulse input
F1.2	=	I - Counter 2 quadrature signal 1 input
F2.2	=	I - Counter 2 quadrature signal 2 input
F0.3	=	I - Counter 3 zero pulse input
F1.3	=	I - Counter 3 quadrature signal 1 input
F2.3	=	I - Counter 3 quadrature signal 2 input

The count signals available on **JMS 34** are Optocoupled to warrant a high degree of protecion for on board electronics against noise and disturbs from the external world.
Each signal is provided with a LED for visual feed back (the LED will light whenever the input will have the potential of GND opto signal); this means that the inputs are going to support normally open contacts. These contacts are suitable to be connected to NPN drivers. In case the User would want to connect PNP drivers then he/she will have to put a **PBI 01** BLOCK module between the drivers and the card.
The interface circuitry for this 8 inputs section is shown in the following diagram.
The Optocouplers power supply voltage may vary in the range from 12 Vdc to 24 Vdc and must be provided through the specific pins of connector CN3.

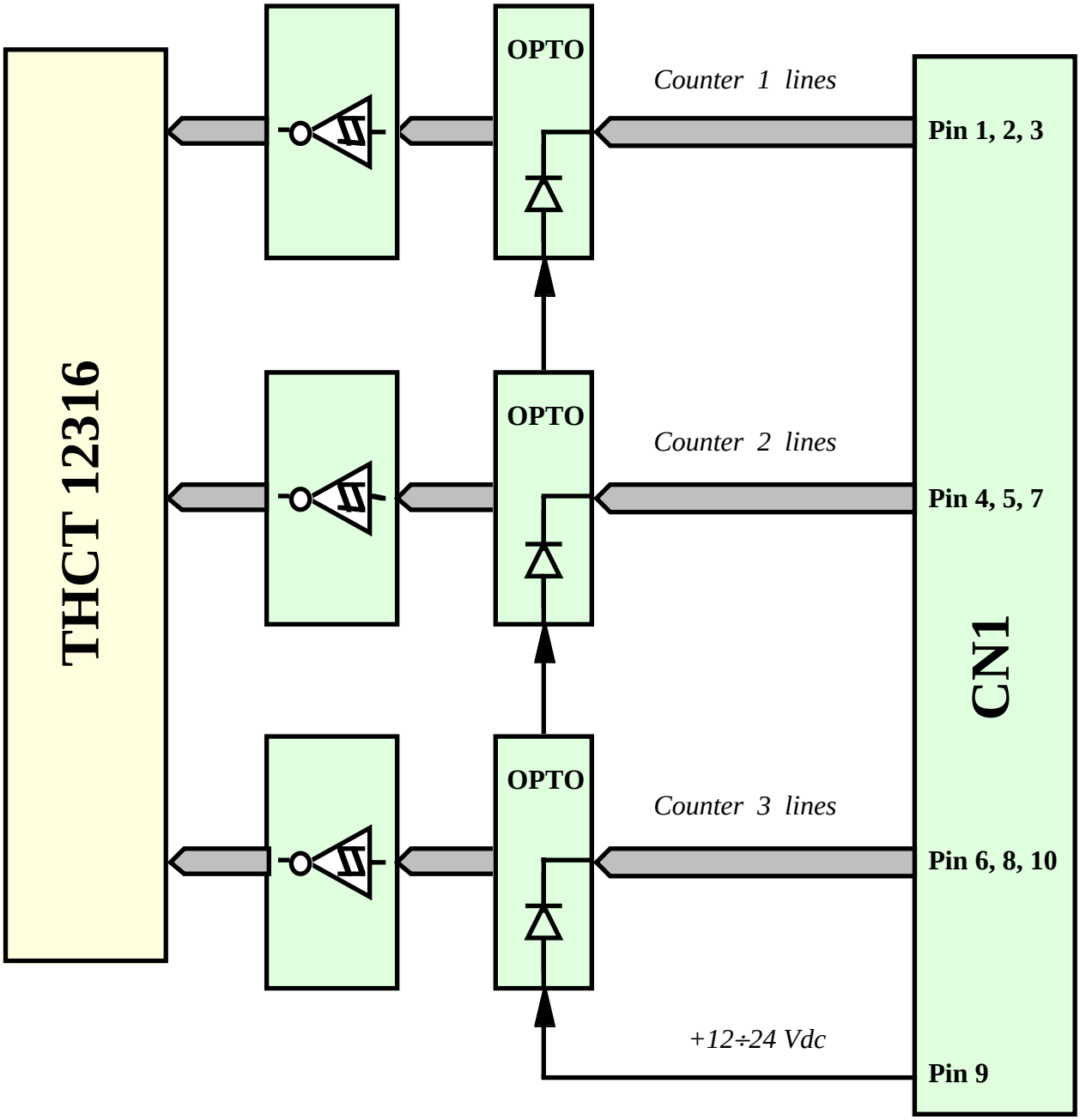


FIGURE 7: COUNTER SECTION BLOCK DIAGRAM

CN2 - OPEN COLLECTOR AND D/A CONVERTER OUTPUTS CONNECTOR

CN2 is a 26 pins low profile 90° male 2.54 mm pitch connector.
On this connector the 8 NPN open collector transistor digital outputs can be acquired and the 4 digital to analog converter outputs can be accessed.

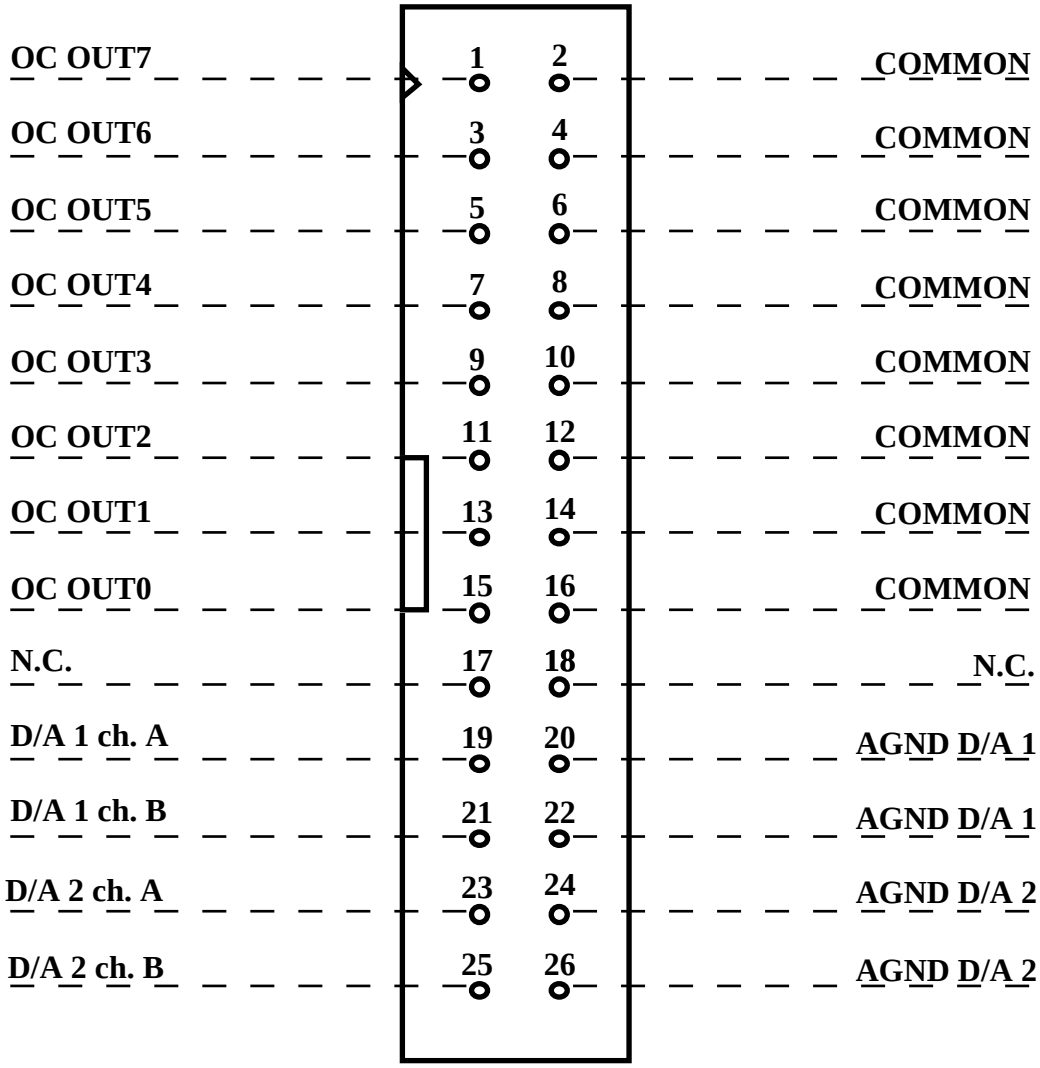


FIGURE 8: CN3 - OPTOCOUPLED OUTPUTS CONNECTOR

Signals description:

OC OUTn	=	O - n-th Open Collector NPN output
COMMON	=	- Open Collector common terminal
D/A n ch. A/B	=	O - n-th D/A converter channel A/B analog output signal
AGND D/A n	=	- n-th D/A converter analog ground signal
N.C.	=	- Not connected

The transistor output signals available are provided with a LED for visual feed back (the LED will light whenever the transistor is ON); they are optocoupled to warrant galvanical isolation between on board electronics and the external world
The final stage of these outputs is made by a **NPN** Open Collector transistor, capable to bear a maximum current of 500 mA non continuous, with a maximum tension that can be +30 Vdc.

NOTE
In the output section the board performs a logic complement on each of the 8 singals available. The complement affects only the final output stage, in fact the 8 red LEDs that provide the visual feedback reflect the bit stored in the latch. For example, if a logic 0 is written to a digital output control line, the corresponding LED will be OFF while the corresponding output on connector CN2 will assume the logic value 1 corresponding to transistor contact open.

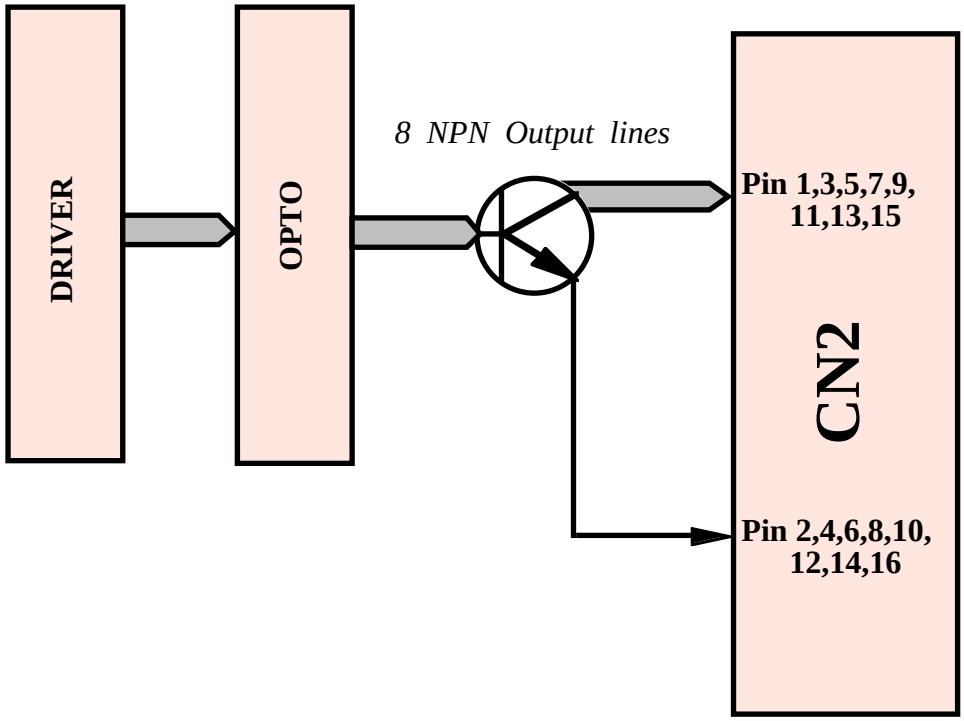


FIGURE 9: OUTPUT SECTION BLOCK DIAGRAM

K1 - CONNECTOR FOR ABACO® BUS

K1 is a 64 pins, male, 90°, DIN 41612 connector with 2.54 pitch.
On K1 are available all the industrial **ABACO®** BUS signals and it can be used for connections to many other peripheral cards. In the table below there are the standard pin outs both for 8 bits and 16 bits CPU and the signal connected on **JMS 34**. All signals follow TTL standard.

A 16 bit BUS	A 8 bit BUS	A JMS 34	PIN	C JMS 34	C 8 bit BUS	C 16 bit BUS
GND	GND	GND	1	GND	GND	GND
+5 Vdc	+5 Vdc	+5 Vdc	2	+5 Vdc	+5 Vdc	+5 Vdc
D0	D0	D0	3	N. C.		D8
D1	D1	D1	4	N. C.		D9
D2	D2	D2	5	N. C.		D10
D3	D3	D3	6	N. C.	/INT	/INT
D4	D4	D4	7	N. C.	/NMI	/NMI
D5	D5	D5	8	N. C.	/HALT	D11
D6	D6	D6	9	N. C.	/MREQ	/MREQ
D7	D7	D7	10	/IORQ	/IORQ	/IORQ
A0	A0	A0	11	/RD	/RD	/RDLDS
A1	A1	A1	12	/WR	/WR	/WRLDS
A2	A2	A2	13	N. C.	/BUSAK	D12
A3	A3	A3	14	N. C.	/WAIT	/WAIT
A4	A4	A4	15	N. C.	/BUSRQ	D13
A5	A5	A5	16	/RESET	/RESET	/RESET
A6	A6	A6	17	/M1	/M1	/IACK
A7	A7	A7	18	N. C.	/RFSH	D14
A8	A8	A8	19	N. C.	/MEMDIS	/MEMDIS
A9	A9	A9	20	N. C.	VDUSEL	A22
A10	A10	A10	21	N. C.	/IEI	D15
A11	A11	A11	22	N. C.		
A12	A12	A12	23	N. C.	CLK	CLK
A13	A13	A13	24	N. C.		/RDUDS
A14	A14	A14	25	N. C.		/WRUDS
A15	A15	A15	26	N. C.		A21
A16		N. C.	27	N. C.		A20
A17		N. C.	28	N. C.		A19
A18		N. C.	29	N. C.	/R.T.	/R.T.
+12 Vdc	+12 Vdc	N. C.	30	N. C.	-12 Vdc	-12 Vdc
+5 Vdc	+5 Vdc	+5 Vdc	31	+5 Vdc	+5 Vdc	+5 Vdc
		GND	32	GND	GND	GND

FIGURE 10: K1 - ABACO® BUS CONNECTOR

Signals description:

8 bits CPU

A0-A15	=	O	- Address BUS
D0-D7	=	I/O	- Data BUS
/INT	=	I	- Interrupt request
/NMI	=	I	- Non Maskable Interrupt
/HALT	=	O	- Halt state
/MREQ	=	O	- Memory Request
/IORQ	=	O	- Input Output Request
/RD	=	O	- Read cycle status
/WR	=	O	- Write cycle status
/BUSAK	=	O	- BUS Acknowledge
/WAIT	=	I	- Wait
/BUSRQ	=	I	- BUS Request
/RESET	=	O	- Reset
/M1	=	O	- Machine cycle one
/RFSH	=	O	- Refresh for dynamic RAM
/MEMDIS	=	I	- Memory Display
/VDUSEL	=	O	- VDU Selection
/IEI	=	I	- Interrupt Enable Input
CLK	=	O	- System clock
R.T.	=	I	- Reset button
+5 Vdc	=	I	- Power supply at +5 Vdc
+12 Vdc	=	I	- Power supply at +12 Vdc
-12 Vdc	=	I	- Power supply at -12 Vdc
GND	=		- Ground signal

16 bits CPU

A16-A22	=	O	- Address BUS
D8-D15	=	I/O	- Data BUS
/RD UDS	=	O	- Read Upper Data Strobe
/WR UDS	=	O	- Write Upper Data Strobe
/IACK	=	O	- Interrupt Acknowledge
/RD LDS	=	O	- Read Lower Data Strobe
/WR LDS	=	O	- Write Lower Data Strobe
N. C.	=		- Not Connected

NOTE
Directionality indications as above stated are referred to a master (**GPC®**) board and have been kept untouched to avoid ambiguity in case of multi-boards systems.

VISUAL FEEDBACK

JMS 34 board is provided with twenty-five LEDs to signal status conditions, as described in the following table:

LED	COLOUR	FUNCTION
LD1÷LD8	Red	Visualize the status of the eight open collector transistor outputs OC OUT0÷7. If the LED is ON then its corresponding output contact is closed to the common pin.
LD9	Red	Visualizes the status of optocoupled counter signal F1.1. When the LED is ON it means input contact closed.
LD10	Green	Visualizes the status of optocoupled counter signal F2.1. When the LED is ON it means input contact closed.
LD11	Yellow	Visualizes the status of optocoupled counter signal F0.1. When the LED is ON it means input contact closed.
LD12	Red	Visualizes the status of optocoupled counter signal F1.2. When the LED is ON it means input contact closed.
LD13	Green	Visualizes the status of optocoupled counter signal F2.2. When the LED is ON it means input contact closed.
LD14	Yellow	Visualizes the status of optocoupled counter signal F0.2. When the LED is ON it means input contact closed.
LD15	Red	Visualizes the status of optocoupled counter signal F1.3. When the LED is ON it means input contact closed.
LD16	Green	Visualizes the status of optocoupled counter signal F2.3. When the LED is ON it means input contact closed.
LD17	Yellow	Visualizes the status of optocoupled counter signal F0.3. When the LED is ON it means input contact closed.
LD18÷LD25	Green	Visualize the status of the eight optocoupled NPN inputs IN 0÷7. If the LED is ON then its corresponding input contact is closed.

FIGURE 11: VISUAL FEEDBACK TABLE

The main purpose of these LEDs is to give a visual indication of the board status, making easier the operations of system working verify. To easily locate these LEDs on the board, please refer to figure 12.

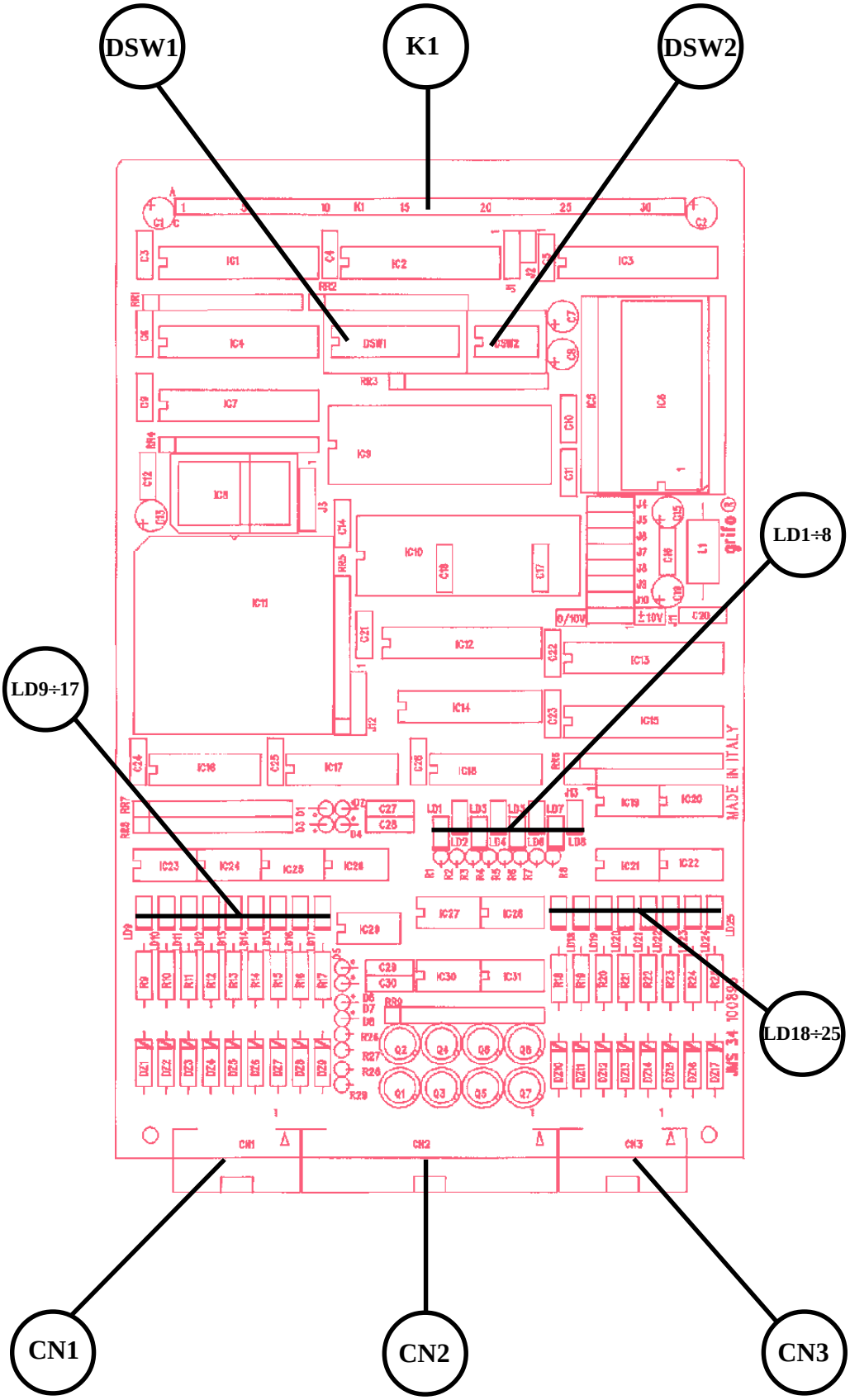


FIGURE 12: LEDS, CONNECTORS AND DIP SWITCHES LOCATION

JUMPERS

On **JMS 34** there are 13 jumpers for card configuration. Connecting these jumpers, the user can define for example the memory type and size, the peripheral devices functionality and so on. Below there is the jumpers list, location and function:

JUMPERS	N. PINS	PURPOSE
J1	3	Selects I/O addressing mode between 256 bytes or 64 Kbyte.
J2	2	Connects signal /M1 to addressing and interfacing section.
J3	4	With jumper J12, it selects the source of count signal for counter 2 of device installed on IC11.
J4	3	With jumpers J5, J6 and J7, it selects the output voltage range of D/A Converter installed on IC10 between ranges 0/10V and ±10V.
J5	3	With jumpers J4, J6 and J7, it selects the output voltage range of D/A Converter installed on IC10 between ranges 0/10V and ±10V.
J6	3	With jumpers J4, J5 and J7, it selects the output voltage range of D/A Converter installed on IC10 between ranges 0/10V and ±10V.
J7	3	With jumpers J4, J5 and J6, it selects the output voltage range of D/A Converter installed on IC10 between ranges 0/10V and ±10V.
J8	3	With jumpers J9, J10 and J11, it selects the output voltage range of D/A Converter installed on IC9 between ranges 0/10V and ±10V.
J9	3	With jumpers J8, J10 and J11, it selects the output voltage range of D/A Converter installed on IC9 between ranges 0/10V and ±10V.
J10	3	With jumpers J8, J9 and J11, it selects the output voltage range of D/A Converter installed on IC9 between ranges 0/10V and ±10V.
J11	3	With jumpers J8, J9 and J10, it selects the output voltage range of D/A Converter installed on IC9 between ranges 0/10V and ±10V.
J12	4	With jumper J3, it selects the source of count signal for counter 2 of device installed on IC11.
J13	2	It selects count mode for counter 3 of device installed on IC11.

FIGURE 13: JUMPERS SUMMARIZING TABLE

The following tables describe all the right connections of **JMS 34** jumpers with their relative functions. To recognize these valid connections, please refer to the board printed diagram (serigraph) or to figure 3 of this manual, where the pins numeration is listed; for recognizing jumpers location, please refer to figure 14.
The "*" used in the following tables, denotes the default connection, or on the other hand the connection set up at the end of testing phase, that is the configuration the User receives.

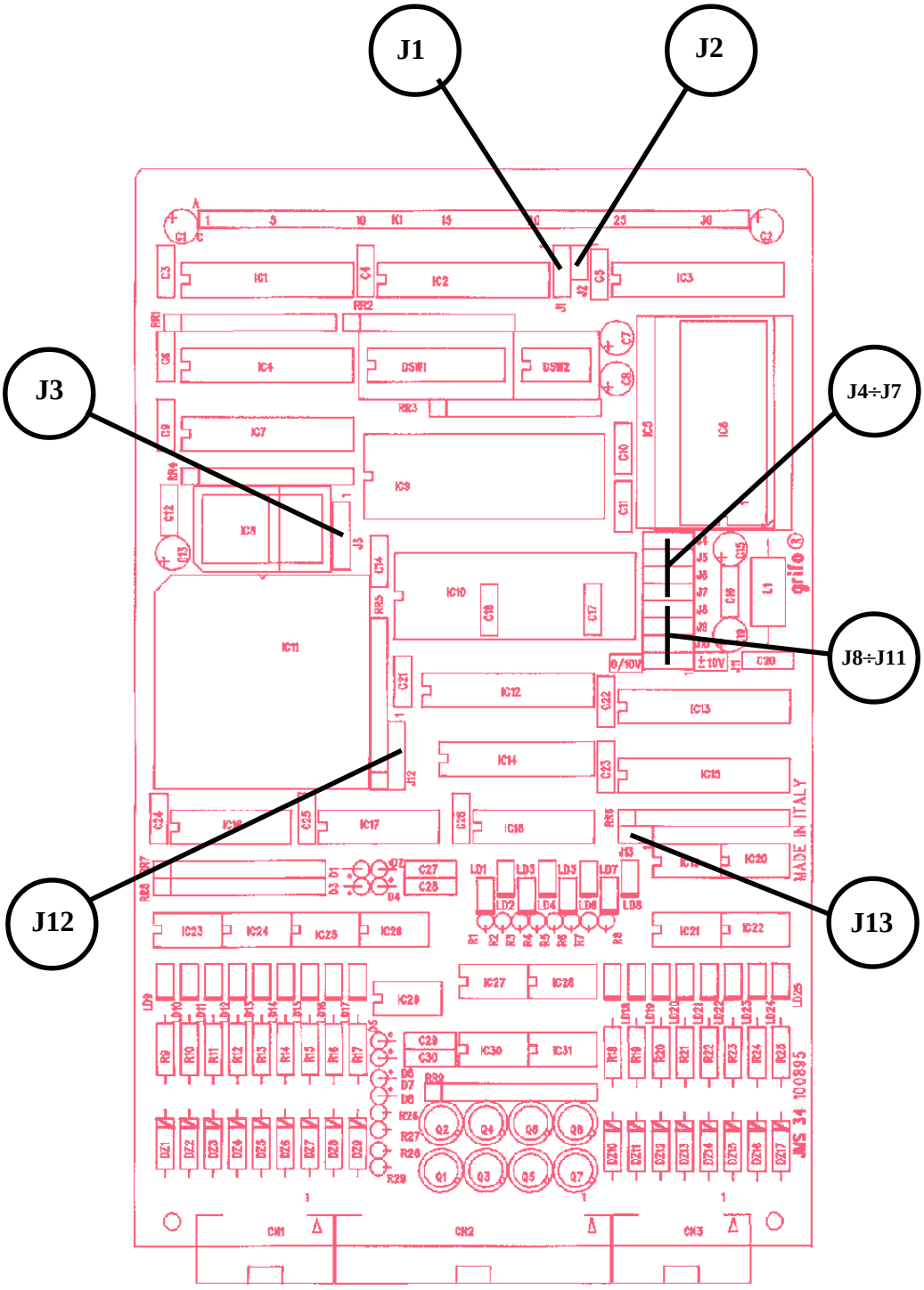


FIGURE 14: JUMPERS LOCATION

2 PINS JUMPERS

JUMPER	CONNECTION	PURPOSE	DEF.
J2	Not connected	Addressing and interfacement section does not manage BUS /M1 signal.	
	Connected	Addressing and interfacement section can manage BUS /M1 signal.	*
J13	Not connected	It connects +Vdc (logic level 1) to signal M23 of encoder installed on IC11, which selects the count mode of the third counter.	*
	Connected	It connects GND (logic level 0) to signal M23 of encoder installed on IC11, which selects the count mode of the third counter.	

FIGURE 15: 2 PINS JUMPERS TABLE

The "*" used in the following tables, denotes the default connection, or on the other hand the connection set up at the end of testing phase, that is the configuration the User receives.

4 PINS JUMPERS

JUMPER	CONNECTION	PURPOSE	DEF.
J3	position 1-2	With J12, it sets the section 2 of encoder installed on IC11 to work as counter with direction discriminator.	*
	position 2-3	With J12, it sets the section 2 of encoder installed on IC11 to work as a normal counter.	
	position 3-4	With J12, it cascades the sections 1 and 2 of encoder installed on IC11 to work as a 32 bits counter.	
J12	position 1-2	With J3, it sets the section 2 of encoder installed on IC11 to work as counter with direction discriminator.	*
	position 2-3	With J3, it sets the section 2 of encoder installed on IC11 to work as a normal counter.	
	position 3-4	With J3, it cascades the sections 1 and 2 of encoder installed on IC11 to work as a 32 bits counter.	

FIGURE 16: 4 PINS JUMPERS TABLE

The "*" used in the following tables, denotes the default connection, or on the other hand the connection set up at the end of testing phase, that is the configuration the User receives.

NOTE
For a correct working of encoder installed on IC11, jumpers J3 and J12 must always have the same connection; this means they must be all in position 1-2 or all in position 2-3 or all in position 3-4, no other combination is allowed.

3 PINS JUMPERS

JUMPER	CONNECTION	PURPOSE	DEF.
J1	position 1-2	It selects the 64 Kbyte extended addressing mode.	
	position 2-3	It selects the 256 byte normal addressing mode.	*
J4	position 1-2	With jumpers J5, J6 and J7, it sets the output voltage range of D/A Converter installed on IC10 as ±10V.	*
	position 2-3	With jumpers J5, J6 and J7, it sets the output voltage range of D/A Converter installed on IC10 as 0/10V.	
J5	position 1-2	With jumpers J4, J6 and J7, it sets the output voltage range of D/A Converter installed on IC10 as ±10V.	*
	position 2-3	With jumpers J4, J6 and J7, it sets the output voltage range of D/A Converter installed on IC10 as 0/10V.	
J6	position 1-2	With jumpers J4, J5 and J7, it sets the output voltage range of D/A Converter installed on IC10 as ±10V.	*
	position 2-3	With jumpers J4, J5 and J7, it sets the output voltage range of D/A Converter installed on IC10 as 0/10V.	
J7	position 1-2	With jumpers J4, J5 and J6, it sets the output voltage range of D/A Converter installed on IC10 as ±10V.	*
	position 2-3	With jumpers J4, J5 and J6, it sets the output voltage range of D/A Converter installed on IC10 as 0/10V.	

FIGURE 17: 3 PINS JUMPERS TABLE PART 1

The "*" used in the following tables, denotes the default connection, or on the other hand the connection set up at the end of testing phase, that is the configuration the User receives.

NOTE

For a correct working of D/A converter installed on IC10, jumper J4, J5, J6 and J7 must always have the same connection; this means that they must be all in position 1-2 or all in position 2-3, no other combination is allowed.

JUMPER	CONNECTION	PURPOSE	DEF.
J8	position 1-2	With jumpers J9, J10 and J11, it sets the output voltage range of D/A Converter installed on IC9 as ±10V.	*
	position 2-3	With jumpers J9, J10 and J11, it sets the output voltage range of D/A Converter installed on IC9 as 0/10V.	
J9	position 1-2	With jumpers J8, J10 and J11, it sets the output voltage range of D/A Converter installed on IC9 as ±10V.	*
	position 2-3	With jumpers J8, J10 and J11, it sets the output voltage range of D/A Converter installed on IC9 as 0/10V.	
J10	position 1-2	With jumpers J8, J9 and J11, it sets the output voltage range of D/A Converter installed on IC9 as ±10V.	*
	position 2-3	With jumpers J8, J9 and J11, it sets the output voltage range of D/A Converter installed on IC9 as 0/10V.	
J11	position 1-2	With jumpers J8, J9 and J10, it sets the output voltage range of D/A Converter installed on IC9 as ±10V.	*
	position 2-3	With jumpers J8, J9 and J10, it sets the output voltage range of D/A Converter installed on IC9 as 0/10V.	

FIGURE 18: 3 PINS JUMPERS TABLE PART 2

The "*" used in the following tables, denotes the default connection, or on the other hand the connection set up at the end of testing phase, that is the configuration the User receives.

NOTE
For a correct working of D/A converter installed on IC9, jumper J8, J9, J10 and J11 must always have the same connection; this means that they must be all in position 1-2 or all in position 2-3, no other combination is allowed.

INTRODUCTION

This chapter provides all the hardware informations needed to use **JMS 34** board. Here the user will find informations about I/O card mapping and on board peripheral devices addressing.

BOARD MAPPING

JMS 34 board is mapped into a **16** consecutive bytes I/O addressing space that can be based starting from different base addresses according to how the board is configured. This feature allows to use several **JMS 34** cards on the same **ABACO® BUS**, or to install them on a BUS where other peripheral modules are installed obtaining a structure that can be expanded without any difficulty or modifications to the application software.
The base address can be defined through the specific BUS interface circuitry on the board itself; this circuitry uses two dip switches, one featuring 8 pins while the other one features 4 pins, from which it reads the address set by the user. Here follows the corrispondance between dip switches configuration and address signals.

DSW1.1	->	Address BUS signal A8
DSW1.2	->	Address BUS signal A9
DSW1.3	->	Address BUS signal A10
DSW1.4	->	Address BUS signal A11
DSW1.5	->	Address BUS signal A12
DSW1.6	->	Address BUS signal A13
DSW1.7	->	Address BUS signal A14
DSW1.8	->	Address BUS signal A15
DSW2.1	->	Address BUS signal A4
DSW2.2	->	Address BUS signal A5
DSW2.3	->	Address BUS signal A6
DSW2.4	->	Address BUS signal A7

These dip switches are driven in complemented logic, this means that if a switch is **ON it** generates a **logic zero**, viceversa if a switch is **OFF** it generates a **logic one**.

Jumper J1 described in the previous chapter selects the range of addressing space where the base address of the board can be selected. If a 256 bytes addressing space is selected, then only DSW2 is used to allocate the board; otherwise if a 64Kbyte addressing space is selected (from 0H to FFFFH), then both DSW1 and DSW2 must be set correctly.
Also jumper J3 affects the addressing section and must be set according to the type of master control board (**CPU** or **GPC®**) used to drive the **JMS 34**. In detail if the master control board is provided with signal /M1 on **ABACO® BUS** connector, then jumper J3 must be connected and viceversa.

To ease the board use here follow two mapping examples.

EXAMPLE 1

If the user has to map the board in a 256 bytes addressing space, driven by a master control card provided with the signal /M1, starting from base address 040H, jumpers and dip swithces status must be as follows:

J1	->	Position 2-3
J3	->	Connected
DSW1.?	->	Indifferent
DSW2.1	->	ON
DSW2.2	->	ON
DSW2.3	->	OFF
DSW2.4	->	ON

EXAMPLE 2

If the user has to map the board in a 64K bytes addressing space, driven by a master control card not provided with the signal /M1, starting from base address 14F0H, jumpers and dip swithces status must be as follows:

J1	->	Position 1-2
J3	->	Not connected
DSW1.1	->	ON
DSW1.2	->	ON
DSW1.3	->	OFF
DSW1.4	->	ON
DSW1.5	->	OFF
DSW1.6	->	ON
DSW1.7	->	ON
DSW1.8	->	ON
DSW2.1	->	OFF
DSW2.2	->	OFF
DSW2.3	->	OFF
DSW2.4	->	OFF

To easily locate the dip swithces, please refer to figure 12, to easily locate the jumpers please refer to figure 14.

INTERNAL REGISTERS ADDRESSING

Indicating the board base address with <**baseaddr**>, that is the address set using DSW1 and DSW2, as indicated in the previous paragraph, **JMS 34** internal registers are addressable as explained in the following table.

DEVICE	REG.	ADDRESS	R/W	MEANING
OUTPUT	OUT	<baseaddr>+00H	W	Register that sets the 8 digital outputs
INPUT	INP	<baseaddr>+00H	R	Register to read the 8 digital inputs
LATCH for ENCODER	MOD	<baseaddr>+01H	W	Register to set the working mode of IC11 encoder counters (see also jumpers J3, J12, J13)
ENCODER	CT3H	<baseaddr>+02H	R/W	Read/Set High byte of IC11 encoder counter 3
	CT3L	<baseaddr>+03H	R/W	Read/Set Low byte of IC11 encoder counter 3
	CT2H	<baseaddr>+04H	R/W	Read/Set High byte of IC11 encoder counter 2
	CT2L	<baseaddr>+05H	R/W	Read/Set Low byte of IC11 encoder counter 2
	CT1H	<baseaddr>+06H	R/W	Read/Set High byte of IC11 encoder counter 1
	CT1L	<baseaddr>+07H	R/W	Read/Set Low byte of IC11 encoder counter 1

FIGURE 19: INTERNAL REGISTERS ADDRESSES TABLE PART 1

DEVICE	REG.	ADDRESS	R/W	MEANING
DAC installed on IC10	D1AL	<baseaddr>+08H	W	Set Low byte of channel A register
	D1AH	<baseaddr>+09H	W	Set High nibble of channel A register
	D1BL	<baseaddr>+0AH	W	Set Low byte of channel B register
	D1BH	<baseaddr>+0BH	W	Set High nibble of channel B register
	D1SET	<baseaddr>+08H .... <baseaddr>+0BH	R	Channels A and B simultaneously generate the output voltage set by the values written to the 4 writable registers
DAC installed on IC9	D2AL	<baseaddr>+0CH	W	Set Low byte of channel A register
	D2AH	<baseaddr>+0DH	W	Set High nibble of channel A register
	D2BL	<baseaddr>+0EH	W	Set Low byte of channel B register
	D2BH	<baseaddr>+0FH	W	Set High nibble of channel B register
	D2SET	<baseaddr>+0CH .... <baseaddr>+0FH	R	Channels A and B simultaneously generate the output voltage set by the values written to the 4 writable registers

FIGURE 20: INTERNAL REGISTERS ADDRESSES TABLE PART 2

NOTE
If using several boards on the same **ABACO® BUS**, when setting the boards mapping address the user shold be careful not to allocate more than one board in the same addressing space (consider the base address plus the bytes taken by the board addressing). If this condition is not satisfied a BUS conflict situation will occour, prejudicing the correct working of the whole system.

POWER SUPPLY

JMS 34 is provided with an efficent circuitery that solves in a comfortable and simple way the problem of the board's supply, under any condition of use.
Here follow the voltages nedded:

+V opto: Supplies the optocouplers of the input section; must be in the range +12÷24 Vdc and must be provided through pins 9 and 10 of CN3 and pin 9 of CN1.

+5 Vdc: Supplies the on board logic; must be in the range +5 Vdc ± 5% and must be provided through the specific pins of connector K1 (**ABACO**® BUS).

To warrant great immunity to external noise and so a correct working of the board, it is essential that **+V opto** tension is galvanically isolated from **+5 Vdc**.

BOARD CONNNECTIONS

To prevent possible connecting problems between **JMS 34** board and the external systems, the user has to read carefully the information of the previous paragraphs and he must follow these instrunctions:

- To connect to the optocoupled input signals, only the contacts to acquire must be connected from the external system(s). These contacts (relays, switches, etc.) must connect or not connect the input signal INx to GND of opto power supply. About the correspondance between logic signals and contact status, an open contact generates a logic **1**, a closed contact generates a logic **0**, following the NPN standard.

- The NPN open collector transistors output signals must be connected directly to the load to drive (power relays, etc.). The board provides the open collector outputs called OC OUTx, capable to bear a maximum current of **500 mA** with a tension that can be **+30 Vdc**.

- The TTL signals can be connected directly only to a device featuring the same type of interface. About the correspondance between logic signals and TTL output status, remember that a logic **0** generates a TTL 0 Vdc, while a logic **1** generates a TTL +5 Vdc.

RESET CIRCUITRY

JMS 34 features an efficent reset circuitery that, whenever a reset or a Power On occour, disables all the output transistors (contacts open), resets to zero the encoder counters and its output registers and resets to zero the DAC output voltages and the content of its write registers. Please refer to chapter “SOFTWARE DESCRIPTION” for more information about how to manage DACs after a reset or a Power On.

PERIPHERAL DEVICES SOFTWARE DESCRIPTION

In the previous paragraphs are described the external registers addresses, while in this one there is a specific description of registers meaning and function (please refer to I/O addresses table, for the registers names and addresses values). For a more detailed description of the devices, please refer to manufacturing company documentation; for more informaton about encoder THCT 12316 and compatible devices, please refer to appendix B. In the following paragraphs the **D7÷D0** and **.0÷7** indications denote the eight bits of the combination used in I/O operations.

ENCODER THCT 12316 AND COMPATIBLE

For the desctription of this triple counter please refer to the specific technical documentation in the appendix B of this manual.
The three counters of this device can be managed through read and write operations to the allocation addresses of registers CT**n**H and CT**n**L, referring respectively to High and Low bytes of the **n**-th counter, where **n** can be in the range 1÷3.

LATCH FOR ENCODER WORKING MODE

JMS 34 features a latch that allows to program by software the encoder working mode. In fact the encoder is provided with 9 signals to set the working mode of the three internal counters. These signals are called M2**n**, M1**n** and M0**n**, where **n** can be in the range 1÷3, and can be set by software through the write register called **MOD** and by hardware through jumper J13 as described in the following correspondance:

MOD.0	->	Signal M01
MOD.1	->	Signal M11
MOD.2	->	Signal M21
MOD.3	->	Signal M02
MOD.4	->	Signal M12
MOD.5	->	Signal M22
MOD.6	->	Signal M03
MOD.7	->	Signal M13
J13	->	Signal M23

Performing a write operation to the allocation address of register MOD and setting opportunely the connection of jumper J13 it is possible to select one of the eight working mode for each of the three counters. Here follows the correspondance between bit logic status and logic status of the corresponding encoder signal:

Bit at logic 0	->	Signal Mx**n** at logic 0
Bit at logic 1	->	Signal Mx**n** at logic 1

For further information about the counters working modes and the signals status to set them, please refer to documentation in appendix B.

TRANSISTOR OUTPUTS

Output registers OUT is used to perform the management of the 8 open collector transistor output signals on **JMS 34** board. The 8 bits of these registers have the following meaning:

D7	->	OC OUT7
D6	->	OC OUT6
D5	->	OC OUT5
D4	->	OC OUT4
D3	->	OC OUT3
D2	->	OC OUT2
D1	->	OC OUT1
D0	->	OC OUT0

Performing an output operation at the address of OUT the corresponding eight outputs are set by the output data .The correspondance between status of an output and value of a bit is:

Bit at logic 0	->	Output disabled	=	Transistor disabled
Bit at logic 1	->	Output enabled	=	Transistor enabled

OPTOCOUPLED INPUTS

Input register INP is used to perform the management of the 8 optocoupled digital inputs on **JMS 34** board. The 8 bits of this register have the following meaning:

D7	->	IN7
D6	->	IN6
D5	->	IN5
D4	->	IN4
D3	->	IN3
D2	->	IN2
D1	->	IN1
D0	->	IN0

Performing an input operation at the address of IN1, IN2, IN3 or IN4 the corresponding eight optocoupled input signals are acquired.

The correspondance between status of an input and value of a bit is:

Bit at logic 1	->	Input disabled	=	Input contact open
Bit at logic 0	->	Input enabled	=	Input contact closed

D/A CONVERTER

There are 18 specific registers, described in the table of figure 20, for the management of the two on board 12 bit DAC. The devices are controlled performing read or write operations to these registers. Write operations can be done to the following registers:

D1AL	->	Sets the low byte (bit D7÷D0) in the 12 bit combination of channel A input register on DAC installed in socket IC10.
D1AH	->	Sets the high nibble (bit D11÷D8) in the 12 bit combination of channel A input register on DAC installed in socket IC10. The nibble must be written in bit D3÷D0 of the register.
D1BL	->	Sets the low byte (bit D7÷D0) in the 12 bit combination of channel B input register on DAC installed in socket IC10.
D1BH	->	Sets the high nibble (bit D11÷D8) in the 12 bit combination of channel B input register on DAC installed in socket IC10. The nibble must be written in bit D3÷D0 of the register.
D2AL	->	Sets the low byte (bit D7÷D0) in the 12 bit combination of channel A input register on DAC installed in socket IC9.
D2AH	->	Sets the high nibble (bit D11÷D8) in the 12 bit combination of channel A input register on DAC installed in socket IC9. The nibble must be written in bit D3÷D0 of the register.
D2BL	->	Sets the low byte (bit D7÷D0) in the 12 bit combination of channel B input register on DAC installed in socket IC9.
D2BH	->	Sets the high nibble (bit D11÷D8) in the 12 bit combination of channel B input register on DAC installed in socket IC9. The nibble must be written in bit D3÷D0 of the register.

Read operations can be done to the following registers:

D1SET	->	Sets the output voltage of channels A and B of DAC installed on socket IC10 with the voltage specified by the 12 bit values written previously to the 4 write registers.
D2SET	->	Sets the output voltage of channels A and B of DAC installed on socket IC9 with the voltage specified by the 12 bit values written previously to the 4 write registers.

The instructions sequence used to set the output voltage of a specified DAC output channel is the follwing:

- Write to the opportune register the low byte (bit D7÷D0) of the 12 bit combination.
- Write to bit D3÷D0 of the the opportune register the high nibble (bit D11÷D8) of the 12 bit combination.
- Perform a read from register D**n**SET, where **n** can be 1 or 2, to let the **n**-th output of the DAC reach the voltage specified by the 12 bit values written to the 4 write registers.

The output voltage of the DAC is proportional to the 12 bit value written in its write registers according to the following relations:

DAC set for output range 0/10 V:

Combination		Output voltage
4095 = FFF_{HEX}	->	+10 V
2048 = 800_{HEX}	->	+5 V
0	->	0 V

DAC set for output range ±10 V:

Combination		Output voltage
4095 = FFF_{HEX}	->	+10 V
2048 = 800_{HEX}	->	0 V
0	->	-10 V

So, for example, if the User wants to set +6.25 V of output voltage in channel B of DAC installed on IC10, configured for output range 0/10 V, then he/she will have perform the following operations:

- The combination to have +6.25 V, with DAC configured for 0/10 V is 2560 ($A00_{HEX}$).
- Write the value 0 (00_{HEX}) to register D1BL.
- Write the value 10 ($0A_{HEX}$) to register D1BH.
- Read the register D1SET to set the DAC output voltages.

If the User wants to set -1.25 V of output voltage in channel A of DAC installed on IC9, configured for output range ±10 V, then he/she will have perform the following operations:

- The combination to have -1.25 V, with DAC configured for ±10 V is 1792 (700_{HEX}).
- Write the value 0 (00_{HEX}) to register D2AL.
- Write the value 7 (07_{HEX}) to register D2AH.
- Read the register D2SET to set the DAC output voltages.

NOTE

When an external RESET occours (from pin 16c of **ABACO® BUS**) the outputs of the two DAC channels are set to **0 V** while the content of the write registers is set to **0 (000_{HEX})**.
If the **DAC is configured for ±10V** and a read is performed from register DnSET without having set opportunely the write registers, the output voltagewill reach the value of -10 V, which corresponds to the combination 0.
To prevent this the user, before starting to use the DAC, must initialize the write registers with the value **2048 (800_{HEX})**, corresponding to an output voltage of 0 V.
These operations are not required if the DAC is configured for 0/10 V, because in this condition the combination 0 generates an output of 0 V.

EXTERNAL CARDS

JMS 34 can be connected to a wide range of block modules and operator interface system produced by **grifo®**, or to many system of other companies.The on board resources can be expanded with a simple connection to the numerous peripheral **grifo®** boards,both intelligent and not, thanks to its standard **ABACO®** BUS connector. Even cards with **ABACO®** I/O BUS can be connected, by using the proper mother boards.
Hereunder some of these cards are briefly described; ask the detailed information directly to **grifo®**, if required.

MB3 01-MB4 01-MB8 01
Mother Board 3, 4, 8 slots
Motherboard featuring 3, 4 or 8 slots of **ABACO®** industrial BUS; pitch 4 TE; standard power supply connectors; LEDs for visual feed-back of power supply; holes for rack docking.

SPB 04-SPB 08
Switch Power BUS 4-8 slots
Motherboard featuring 4-8 slots of **ABACO®** industrial BUS; pitch 4 TE; standard power supply connectors; termination resistances; connector type F for **SPC xxx** supply ; holes for rack docking.

ABB 03
ABACO® Block BUS 3 slots
3 slots **ABACO®** mother board; 4 TE pitch connectors; **ABACO®** I/O BUS connector; screw terminal for power supply; connection for DIN C type and Ω rails.

ABB 05
ABACO® Block BUS 5 slots
5 slots **ABACO®** mother board with power supply. Double power supply built in; 5Vdc 2,5A section for powering the on board logic; second section at 24Vdc 400mA galvanically coupled, for the optocoupled input lines. Auxiliary connector for **ABACO®** I/O BUS. Connection for DIN Ω rails.

SBP 02-xx
Switch BLOCK Power xx version
Low cost switching power supply able to generate voltage from +5 to +40 Vdc and current up to 2.5 A; Input from 12 to 24 Vac; Connection for DIN C Type and Ω rails.

SPC 03.5S
Switch Power Card +5 Vdc
Europe format switching power supply capable to provide +5 Vdc to a load of 4 A; input voltage 12÷24 Vac; power-failure; connector for back-up battery; standard connector for mother board **SPB 0x**.

SPC 512
Switch Power Card +5 Vdc +12 Vdc
Europe format switching power supply capable to provide +5 Vdc 5A and +12 Vdc 2.5 A; input voltage 12÷24 Vac; power-failure; connector for back-up battery; standard connector for mother board **SPB 0x**.

GPC® 51

General Purpose Controller fam. 51

Microprocessor family 51 INTEL including the masked BASIC chip; the board features: 16 I/O TTL lines; dip switch; 3 timer/counter; RS 232; 4 A/D converter signals resolution 11 bit; buzzer; on board EPROM programmer; RTC and 32K SRAM with Lithium battery back up; controlloer for display and keyboard.

GPC® 68

General Purpose Controller 68000

1 RS 232 line; 1 RS 232 line or RS 422-485 line with settable Baud Rate up to 38K Baud; 3 8 bits parallel ports and 3 timer counter; 10 MHz 68000 CPU; 768 KByte RAM EPROM; disconnectable Watch dog.

GPC® 188F

General Purpose Controller 80C188

80C188 µP 20MHz; 1 RS 232 line; 1 RS 232, RS 422-485 or Current Loop line; 24 TTL I/O lines; 1M EPROM or 512K FLASH; 1M RAM Lithium battery backed; 8K serial EEPROM; RTC; Watch Dog; 8 Dip switch; 3 Timer Counter; 8 13 bit A/D lines; Power failure; activity LEDs; single power supply +5Vdc.

GPC® 150

General Purpose Controller 84C15

Microprocessor Z80 at 16 MHz; implementation completely CMOS; 512K EPROM or FLASH; 512K SRAM; RTC; Back-Up through external Lithium battery; 4M serail FLASH ; 1 serial line RS 232 plus 1 RS 232 or RS 422-485 or current loop; 40 I/O TTL; 2 timer/counter; 2 watch dog; dip switch; EEPROM; A/D converter with resolution 12 bit; activity LED.

GPC® 15R

General Purpose Controller 84C15

84C15 µP, 10÷16 MHz; 1 RS 232 line; 1 RS 232 or RS 422-485 or C. L. line; 16÷24 TTL I/O lines; 16 Opto-in; 8 Relays; 4 Opto Coupled Timers Counters; 512K EPROM or FLASH; 512K RAM and RTC backed; 8K serial EEPROM; 8K Backed RAM modul; Buzzer; 1 Activity LED; Watch dog; 4÷12 readable DIPs; LCD Interface.

GPC® 15A

General Purpose Controller 84C15

Full CMOS card, 10÷20 MHz 84C15 CPU; 512K EPROM or FLASH; 128K RAM; 8K RAM and RTC backed; 8K serial EEPROM; 1 RS 232 line; 1 RS 232 line or RS 422-485 or Current Loop line; 32 or 40 TTL I/O lines; CTC; Watch dog; 2 Dip switches; Buzzer.

GPC® 323

General Purpose Controller 51 family

80C32 µP, 14 MHz; Full CMOS; 1 RS 232 line (software); 1 RS 232 or RS 422-485 or Current Loop line; 24 TTL I/O lines; 11 A/D 12 bits lines; 3 Timers Counters; 64K EPROM; 64K RAM; 32K RAM and RTC backed; 32K DIL EEPROM; 8K serial EEPROM; Buzzer; 2 Activity LED; Watch dog; 5 readable DIPs; LCD Interface.

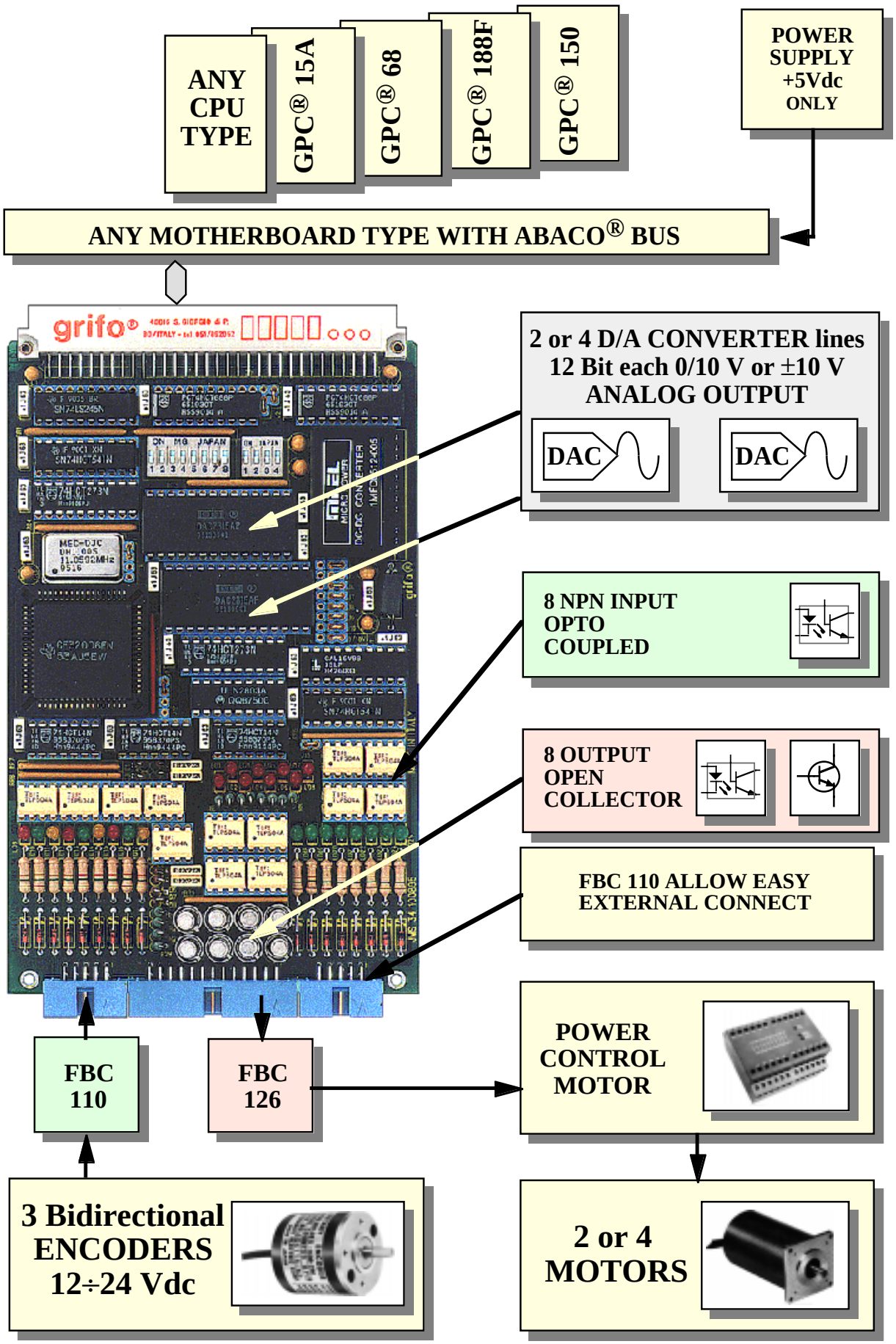


FIGURE 21: POSSIBLE CONNECTIONS DIAGRAM

GPC® 553

General Purpose Controller 80C552

80C552 µP, 22÷33 MHz; 1 RS 232 line (software); 1 RS 232 or RS 422-485 or Current Loop line; 16 TTL I/O lines; 8 A/D 10 bits lines; 3 Timers Counters; 64K EPROM; 64K RAM; 32K RAM and RTC backed; 32K DIL EEPROM; 8K serial EEPROM; 2 PWM lines; 1 Activity LED; Watch dog; 5 readable DIPs; LCD Interface.

GPC® 153

General Purpose Controller Z80

84C15 µP, 10÷16 MHz; Full CMOS; 1 RS 232 line; 1 RS 232 or RS 422-485 or Current Loop line; 16 TTL I/O lines; 8 A/D 12 bits lines; 2÷4 Timers Counters; 512K EPROM or FLASH; 512K RAM and RTC backed; 8K serial EEPROM; Buzzer; 1 Activity LED; Watch dog; 8 readable DIPs; LCD Interface.

GPC® 183

General Purpose Controller Z180

Z180 µP, 10÷16 MHz; Full CMOS; 1 RS 232 line; 1 RS 232 or RS 422-485 or Current Loop line; 24 TTL I/O lines; 11 A/D 12 bits lines; 2 Timers Counters; 512K EPROM or FLASH; 512K RAM and RTC backed; 8K serial EEPROM; Buzzer; 2 Activity LED; Watch dog; 4 readable DIPs; LCD Interface.

GPC® 324/D

"4" Type General Purpose Controller 80C32/320

80C32 or 80C320 µP, 14÷22 MHz; Full CMOS; 1 RS 232 line; 1 RS 232 or RS 422-485 or Current Loop line; 4÷16 TTL I/O lines; 3 Timers Counters; 64K EPROM; 64K RAM; 32K RAM backed; 32K DIL E2; 8K serial EEPROM; Watch dog; 1 readable DIP; LCD Interface; Abaco® I/O BUS; 5Vdc Power supply; Size: 100x50 mm.

GPC® 554

General Purpose Controller 80C552

Microprocessor 80C552 at 22 MHz; implementation completely CMOS; 32K EPROM; 32 K SRAM; 32 K EEPROM or SRAM; EEPROM; 2 RS 232 serial lines; 16 I/O TTL; 2 PWM lines; 16 bits Timer/Counter; Watch Dog; 6 signals A/D converter with resolution 10 bit; interface for **ABACO®** I/O BUS.

GPC® 154

"4" Type General Purpose Controller Z80

84C15 µP, 10÷16 MHz; Full CMOS; 1 RS 232 line; 1 RS 232 or RS 422-485 line; 16 TTL I/O lines; 2÷4 Timers Counters; 512K EPROM or FLASH; 512K RAM and RTC backed; 8K serial EEPROM; Watch dog; 2 readable DIPs; LCD Interface; Abaco® I/O BUS; 5Vdc Power supply; Size: 100x50 mm.

GPC® 884

General Purpose Controller Am188ES

Microprocessor AMD Am188ES up to 40 MHz16 bits; implementation completely CMOS; serie 4 format; 512K EPROM or FLASH; 512K SRAM backed with Lithium battery; RTC; 1 RS 232 serial line + 1 RS 232 or RS 422-485 or current loop; 16 I/O TTL; 3 timer/counter; watch dog; EEPROM; 11 signals A/D converter with 12 bit resolution; interface for **ABACO®** I/O BUS.

GPC® 114

General Purpose Controller 68HC11

Microprocessor 68HC11A1 at 8 MHz; implementation completely CMOS; serie 4 format; 32K EPROM; 32K SRAM backed with Lithium battery; 32K EPROM, SRAM, EEPROM; RTC; 1 serial line RS 232 or RS 422-485; 10 I/O TTL; 3 timer/counter; watch dog; 8 signals A/D converter with resolution 8 bit; 1 asunchronous serial line; extremly low power consumption; interface for **ABACO®** I/O BUS.

MMB 16

Multilayer Mother Board 21 slots **ABACO®**

Mother Board featuring 16 ABACO® BUS slots; type 4 TE; standard connectors for power supply and utility; 3 LEDs to visualize power supply status; termination resistors; holes for rack mounting.

PBI 01

PNP BLOCK Input

Interface for PNP drivers through NPN inputs; 16 inputs for driver PNP, visualized by LEDs; 16 NPN outputs on **ABACO®** standard input connector; Plastic mount for rails DIN 46277-1 and 3.

FBC 20-120

Flat Block Contact 20 vie

Interface for 2 or 1 mounting cable connectors (low profile 20 pins male) and quick release screw terminal connectors; Plastic mount for rails DIN 46277-1 and 3.

FBC 110

Flat Block Contact 10 vie

Interface for 1 mounting cable connectors (low profile 10 pins male) and quick release screw terminal connectors; Plastic mount for rails DIN 46277-1 and 3.

FBC 34

Flat Block Contact 34 vie

Interface for 2 mounting cable connector (low profile 34 pins male) and quick release screw terminal connectors; Plastic mount for rails DIN 46277-1 and 3.

FBC L20

Flat Block Contact LED 20 vie

Interface for 1 mounting cable connector (low profile 20 pins male,featuring **ABACO®** standard Input pin out, and quick release screw terminal connectors; All the signals are visualized through LEDs; Plastic mount for rails DIN 46277-1 and 3.

FBC L34

Flat Block Contact LED 34 vie

Interface for 2 mounting cable connectors (low profile34 and 20 pins male) and quick release screw terminal connectors; featuring **ABACO®** standard Input and Output pin out; All the signals are visualized through LEDs; Plastic mount for rails DIN 46277-1 and 3.

BIBLIOGRAPHY

Here follows a list of manuls thst can be a source of further informations about the devices installed on **JMS 34**.

Manual TEXAS INSTRUMENTES: *The TTL Data Book - SN54/74 Families*
Tech note TEXAS INSTRUMENTS: *THCT12316 triple incremental encored interface - 1Q/88*

Manual BURR-BROWN: *Integrated cicuits data book supplement - Volume 33c*

Manual SGS-THOMSON: *Programmable logic manual - GAL prducts*
Manual SGS-THOMSON: *Motion Control application manual*
Manual SGS-THOMSON: *Small Signal Transistors - Data Book*

Manual TOSHIBA: *Photo Couplers - Data Book*

Tech note MI.EL. MICROPOWER: *DC/DC Converters*

Tech note MICRO-GISCO: *DC/DC Converter 2CCR0515D*

Please connect to the manifactures Web sites to get the latest version of all manuals and data sheets.

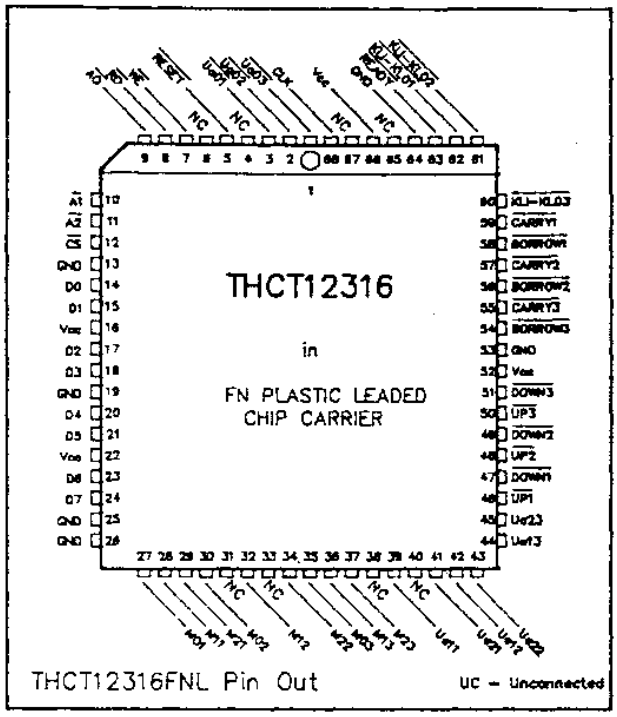
APPENDIX A: ON BOARD COMPONENTS DESCRIPTION

THCT 12316

Smart Part™

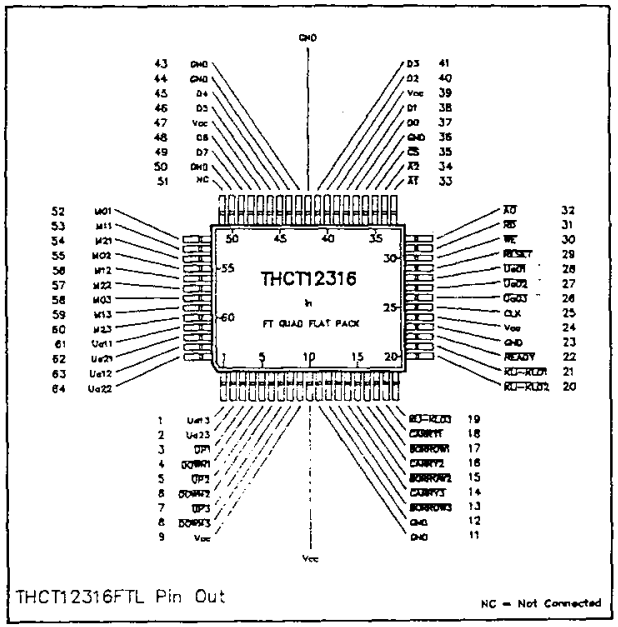
THCT12316 TRIPLE
INCREMENTAL ENCODER INTERFACE

* Three independent channels in one compact surface mount device
* Each channel compatible with the popular THCT2000
* Interfaces three mechanisms/ axes to data bus
* Direction discriminators identify & measure forward/ backward rotation/direction
* Separate zero pulse input
* Pulse width measurement
* Frequency measurement
* Cascadable 16-bit counters
* TTL compatible
* 8-bit parallel 3-state bus
* Simple write/read procedure
* Choice of chip carrier or flat package
* Advanced 1.8um CMOS technology



Description

The THCT12316 INCREMENTAL ENCODER INTERFACE consists of three channels each, of which can independently determine the direction and displacement of a mechanical device or axis based on two input signals from transducers in quadrature. Alternatively, each channel can measure a pulse width using a known clock rate, or a frequency, by counting input pulses over a known time interval. It includes three 16-bit counters which may also be used separately. The THCT12316 may be cascaded between channels on one device or between devices to provide accuracy greater than 16-bits, and is designed for use in many types of microprocessor-based systems.



Applications

The THCT12316 enables mechanical devices to be interfaced with microprocessors. It may be used in many diverse applications, including robotics, tracker balls (or mouse), lathes or tooling machines, automobiles, conveyor belts and transport mechanisms. Since it contains three channels each THCH12316 can support three measurements or axes of motion.

Architecture

Within each channel there are four main elements:-

1. The measurementand mode control logic generates up or down count pulses,internal signals I1 and I2, from :

   - Quadrature signals Ual *,Ua2 * and zero pulse UaOn *
   - Clock input
   - Mode controls MOn *,Mln *,M2n *

Architecture - continued

2. A 16-bit counter made up from two independently loadable 8-bit counters.

3. A 16-bit latch which "freezes" the counter value when required

4. A multiplexer that allows the processor to read either upper or lower byte in the latch.

Supporting the three channels:-

The control logic provides common microprocessor interface signals; the output multiplexer allows the processor to select data from one of the three channels and the three-state buffers place this data on the bus.

(* throughout this data sheet signals suffixed n are repeated for each channel)

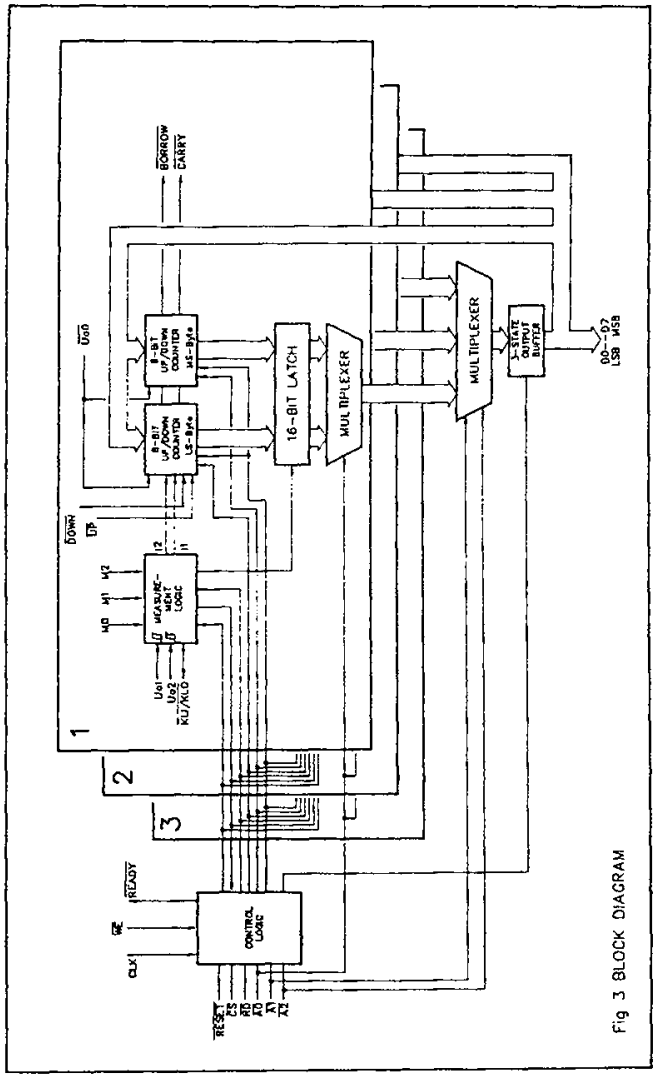


Fig 3 BLOCK DIAGRAM

Operation

The eight modes of operation of the THCT12316 are summarized in Table 1. The modes of the three channels can be selected independently.

MODE	M2n	M1n	M0n	MODE DESCRIPTION
				COUNTER
0	0	0	0	16-bit up/down counter (inhibits direction discriminator).
				DIRECTION DISCRIMINATOR
1	0	0	1	Single count pulse synchronous with Ua1n rising in forward direction and Ua1n falling in backward direction.
2	0	1	0	Single count pulse synchronous with Ua2n rising in forward direction and Ua2n falling in backward direction.
3	0	1	1	Double count pulse synchronous with Ua1n rising and falling.
4	1	0	0	Double count pulse synchronous with Ua2n rising and falling.
5	1	0	1	Quadruple count pulse synchronous with all edges.
				PULSE WIDTH MEASUREMENT
6	1	1	0	Ua1n is the gate signal Ua2n is high for up counting and low for down counting. Count is synchronous with rising clock.
				FREQUENCY MEASUREMENT
7	1	1	1	Ua1n is frequency signal to be measured Ua2n is the gate signal of known time interval. Count is synchronous with rising edge of Ua1n

Table 1

operation – continued

MODE 0: 16-BIT UP/DOWN COUNTER MODE

In this mode the THCT12316 may be used as three fast 16-bit synchronous up-/down counters with cascade capability. This is operated using the /UPn and /DOWNn inputs.

The states of the counter outputs are transferred to a 16-bit latch. The contents of this 16-bit latch are multiplexed on an 8-bit parallel data bus (D0.....D7) and enabled using /RD and /CS.

/A0 is the control input for the byte multiplexer. A high level at this input transfers the least significant byte to the data outputs; and a low level transfers the most significant byte.

The signals /A1 and /A2 select the channel for read or write according to the following table:

channel number	/A1	/A2
1	H	H
2	L	H
3	H	L
no channel selected(1)	L	L

(1) Output buffers still selected if /RD and /CS active – data bus carries invalid data

Table 2

The up/down counters are loaded in individual 8-bit bytes by the /WR and /CS signals, with the byte selected by the /A0 input, and the channel by the /A1 and /A2 inputs. The counters and the control logic may be cleared using the /SRESET signal. The counters are cleared individually using the UaOn signals.

Cascading to 32 bits is possible using the inputs /UPn and /DOWNn the outputs /BORROWn, /CARRYn and the input/outputs /KLI-KLOn.

MODES 1-5: DIRECTION DISCRIMINATOR MODES

The quadrature signals UAln and Ua2n, identify forward or backward directions. If Ualn leads Ua2n, the forward direction is indicated and the counter will count up; if Ualn lags Ua2n, the reverse direction is indicated and the counter will count down.

operation – continued

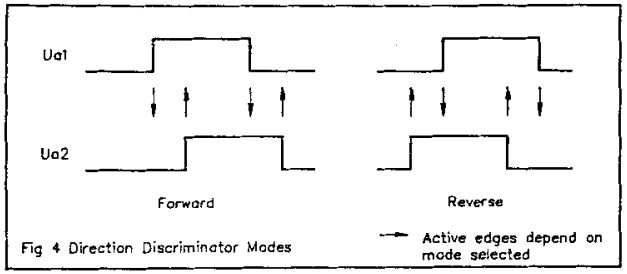


Fig 4 Direction Discriminator Modes

Ualn and Ua2n are both stored in the first of a pair of consecutive D-type flip-flops on the clock falling edge, and transferred to the next on the clock rising edge. By comparing the states of the four flip-flops and checking the mode inputs, the up or down count pulses are generated; see figures 5 and 6.

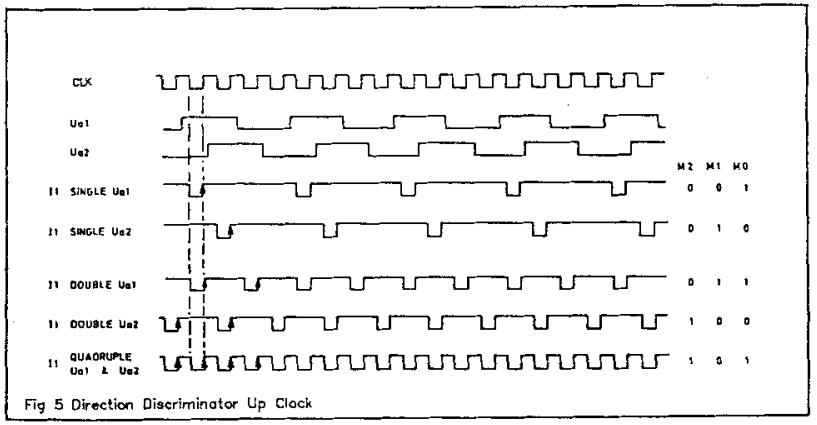


Fig 5 Direction Discriminator Up Clock

operation - continued

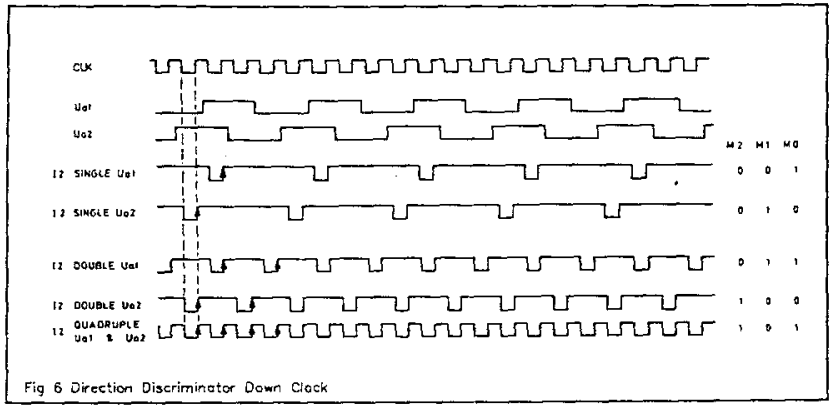


Fig 6 Direction Discriminator Down Clock

MODES 1 to 5 define which edge of the quadrature signals will be counted in accordance with Table 1.

The clock frequency should be at least four times greater than the frequencies of the quadrature signals: this will eliminate problems resulting from timing jitter in the transducer signals and will allow the quadruple counting mode to be used. The frequency of the quadrature signals, Ualn and Ua2n may be calculated from the relationship:

$$F = \frac{\text{shaft speed}}{\text{resolution of transducer}}$$

MODE 6: PULSE WIDTH MEASUREMENT MODE

In this mode, Ualn acts as a gate, and is the pulse width to be measured. Synchronised with the clock edge after a low to high transition in Ualn, count -ing begins at the input clock frequency. Similarly, synchronised with the clock edge after a high to low transition of Ualn, counting is disabled; the value in the counter is loaded in the output register; /KLI-KLOn is pulled low; and then the counter clears. See figure 7. If Ua2n is held high, the counter will count up, and if Ua2n is held low, the counter will count down.

Each counter can be preloaded in two bytes by activating /CS, /WE, and selecting the required byte with /A0, and the required channel with /A1 and /A2. This must be done while Ualn is low. The output register should be read by activating /CS, /RD, and selecting the individual bytes with /A0 after Ualn has fallen and before the next preload takes place.

operation - continued

The /KLI-KLOn signal may be used as an interrupt to indicate to the processor when the output register has been loaded. In both the pulse width and frequency modes, the output register will not be loaded via /CS and /RD, but by the falling edge of Ualn, or by pulling /KLI-KLOn low.

In pulse width mode, the minimum time that can be measured is:

Tmin = 2 (To) (Accuracy is +/- To)

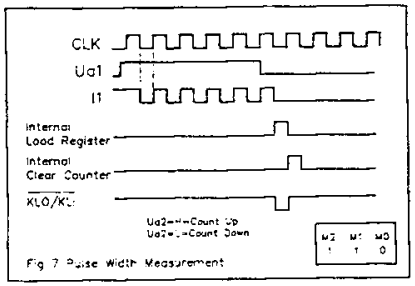


Fig 7 Pulse Width Measurement

MODE 7: FREQUENCY MEASUREMENT MODE

In Mode 7, Ualn is the signal of unknown frequency to be measured; Ua2n is a gate signal of known width. A low to high transition of Ua2n enables counting at the frequency of Ualn. When the gate (Ua2n) goes low, counting is disabled, the value of the counter is loaded into the output register, /KLI-KLOn is pulled low, and the counter is then cleared. See Figure 8.

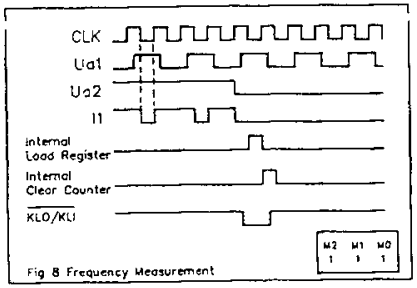


Fig 8 Frequency Measurement

operation - continued

RESET OPERATION

A total reset is initiated by pulling the /RESET pin low. This will clear the counters to zero, reset the D flip-flops at the inputs of the quadrature signals (Ua1n and Ua2n), clear the latches that inhibit the load register pulse, and load zero into the output register. To avoid a spurious count errors (+/- 1) after a reset, the Ua1n and Ua2n inputs should be held to the values indicated in Table 2 during and just after the reset pulse.

MODE	Ua1n	Ua2n
0	X	X
1-5	H	H
6-7	L	L

Table 3

CASCADING DEVICES

The /KLI-KLOn pins of all cascaded THCT12316's should be tied together, so that all of the devices load their output registers at the same time. When the 'master' generates a pulse for the other THCT12316s, /KLI-KLOn on the 'master' works as an output, and /KLI-KLOn on the 'slaves' work as inputs. The /CARRY output of one device should be tied to the /UP input of the next device in the cascade. Similarly, /BORROW should be connected to /DOWN. See 'System Application.'

READ OPERATION

A number may be preloaded into the counter by pulling /CS and /WE low while using /A0 to direct the value on the data bus to the selected byte of the counter and /A1 & /A2 to select the required channel. This will cause /READY to go low on the next falling clock edge, and remain low until /CS and /WE go high. See Figure 12.

WRITE OPERATION

When in MODES 0 to 5 the contents of the counter can be read at any time by pulling /CS and /RD low. The channel is selected by using /A1 & /A2. Within this channel the most significant byte may be selected be setting /A0 to low, and the least significant byte may be read be setting /A0 high. This will cause a load output register pulse to be generated and /KLI-KLOn will go low during the next low clock pulse. /READY will also go low as the clock goes

WRITE OPERATION - continued

low, and will stay low until /CS and/or /RD go high. The load output register pulse stores the current value of the counter in a 16-bit latch register and /A0 directs the selected byte through a multiplexer to the outputs : /CS and /RD also enable the 3-state outputs - see Figure 13. The output register will be loaded immediately if /KLI-KLOn is pulled low externally, this signal normally comes from a cascaded device.

For Modes 6 & 7 see the earlier description of these modes.

Configuration

Special consideration should be paid to the automatic configuration features of the THCT12316. The purpose of these features is to allow for the different order of byte reads (high then low or low then high) of different processors when doing a word read across a byte wide bus and also to configure cascaded devices automatically for correct word read sequence -see below.

Byte order configuration-

After a system reset has occured, the first read operation will store the value of /A0 in a latch within the device. From that time until the next system reset the load output register pulse during a read operation will only be generated if /A0 is this stored value. This means that the internal load output register pulse is correctly generated for word operations regardless of the byte order of the particular processor. Special care should be taken if reading individual bytes to ensure these operations are always done in a consistent order.

Cascaded configuration-

After a system reset the first device and channel to receive a read operation configures itself into "Master" mode and outputs a pulse on /KLI-KLO. In cascaded operation the /KLI-KLO pins of the cascaded channels are connected together and the input pulse on /KLI-KLO of the cascaded channels configures these to "Slave" mode. On all subsequent read operations the load output register pulse is only generated by the "Master" channel (for the appropriate polarity of /A0, as noted above) and this is fed to the "Slave" devices via the /KLI-KLO connection.

Special care should be taken when cascading devices or channels to always read in the same channel order, as well as the byte order already mentioned. To freeze all three channels with a single read cycle (in cascaded or non-cascaded mode) the /KLI-KLO pins of all channels are connected with a pull-up resistor to Vcc (see Systems Application). This ensures that only one channel is operating as the "Master" and all others are "Slaves".

If an external "freeze" of the positioning system is required, and external /KLI-KLO pulse will program all channels as slaves. This is derived by generating an external /KLI-KLO pulse before the first read cycle appears after system reset (See Design Checklist).

Pin Description

Pin Name	Pin Number 68 PLCC	Pin Number 64 QFP	I/O	Description
/CS	12	35	Input	Chip Select. A low enables the device.
/RD	8	31	Input	Read. When this and /CS are active(low), the data from the output register will be present on the data bus.
D0	14	37	Input/ Output	LSB Data Bus Buffer: 8-Bit Bi-directional buffer with 3-state outputs connected to the microprocessor system.
.	15	38		
.	17	40		
.	18	41		
.	20	45		
.	21	46		
.	23	48		
D7	24	49		MSB
/BORROW1	58	17	Output	Counter underflow signal
/BORROW2	56	15		
/BORROW3	54	13		
/CARRY1	59	18	Output	Counter overflow signal
/CARRY2	57	16		
/CARRY3	54	14		
/KLI-KLO1	62	21	Input/ Output	Cascade load input/cascade load output. Open drain output with internal 95uA(nom) pull-up. External pull-up required for full speed operation.
/KLI-KLO2	61	20		
/KLI-KLO3	60	19		
/READY	63	22	Output	When low signal indicates to the MPU that read or write may be completed. /READY falling edge synchronous with CLK Open drain output needs external pull-up.
M21	29	54	Input	Mode select inputs (see Table 1)
M11	28	53	"	
M01	27	52	"	
M22	34	57	"	
M12	32	56	"	
M02	30	55	"	
M23	37	60	"	
M13	36	59	"	
M03	35	58	"	

Pin Description - continued

Pin Name	Pin Number 68 PLCC	Pin Number 64 QFP	I/O	Description
Ua13	44	1	Input	Measuring input signals (Schmitt characteristics)
Ua12	42	63	"	
Ua11	39	61	"	
Ua23	45	2	"	
Ua22	43	64	"	
Ua21	41	62	"	
/Ua01	3	28	Input	Zero pulse. When active (low), the counter in the appropriate channel is cleared. Other logic is not affected.
/Ua02	2	27		
/Ua03	1	26		
CLK	68	25	Input	Clock. Used for internal synchronisation and control timing.
/A0	9	32	Input	Byte select. A high level selects the least significant byte. A low level selects the most significant byte
/A1	10	33	Input	Channel select. See Table 2.
/A2	11	34	Input	
/RESET	5	29	Input	Device reset. When active (low), the control logic is reset to a known state and the counter is cleared.
/WE	7	30	Input	Write enable. When /WE and /CS are active (low), the data that is on the bus is loaded into the counter address -ed by 1A0,1A1 and 1A3.
/DOWN1	47	4	Input	Cascade input for counting down.
/DOWN2	49	6		
/DOWN3	51	8		
/UP1	46	3	Input	Cascade input for counting up.
/UP2	48	5		
/UP3	50	7		
Vcc	16,22, 52,66	9,10, 24,39, 47		Power supply voltage 5V +/- 10%.
GND	13,19,25, 53,64	11,12,23,36 42,43,44,50		Ground.

APPENDIX B: ALPHABETICAL INDEX

E

G

H

I

J

L

M