GPC® R/T63

**General Purpose Controller 6 inputs;
3 Relays/Transistor output**

TECHNICAL MANUAL

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Intelligent **ABACO®** Block module of the **M Serie** with 22,5x82x90 mm dimension. **Housing** for **Omega rail** DIN 46277-1 and DIN 46277-2 types. Available in 3 different versions with the following CPUs:

GPC® R63   with **80C32** 22MHz, 32K RAM.
GPC® R63A   with **Atmel 89S8252** 22MHz; 8K Internal FLASH; 2K internal EEPROM; 32K RAM.
GPC® R63D   with **Dallas 80C320** 22MHz, 32K RAM.

Total memory addressing of **96K** size, divided in: 32K static **RAM** soldered; socket for 32K **EPROM**; socket for 32K RAM, EPROM or **EEPROM**. Compatible code with the famous **51 family** of µP. **Real Time Clock** with 256 Byte of internal RAM. **Back up** circuitery for RTC and RAM, based on **LITHIUM** battery. **6** NPN **digital input lines**, galvanically coupled. External **INT** line, galvanically coupled. 3 **digital output lines** buffered with 5 A **relays** or 4 A darlington **transistor**. Status **LEDs** affording visual check for all the I/O lines. I/O connection through **quick release srew terminal** connectors. **Three** 16 bits **timer counter**. TTL **serial line**. Built in **switching** power supply. Coupled galvanically I/O section powered at **24 Vdc**; on board logic powered at 5 Vdc or 10÷40 Vdc or 10÷24 Vac, protected by **TranZorb**. Wide range of developping software tools such as **C compilers**, **BXC51**, **Assembler**, **Monitor**, **NoICE**, **HTC 51**, **BASCOM 8051**, **PASCAL**, **CMX**, and so on.

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IMPORTANT

Although all the information contained herein have been carefully verified, **grifo®** assumes no responsibility for errors that might appear in this document, or for damage to things or persons resulting from technical errors, omission and improper use of this manual and of the related software and hardware.

grifo® reservs the right to change the contents and form of this document, as well as the features and specification of its products at any time, without prior notice, to obtain always the best product.

For specific informations on the components mounted on the card, please refer to the Data Book of the builder or second sources.

SYMBOLS DESCRIPTION

In the manual could appear the following symbols:

Attention: Generic danger

Attention: High voltage

Trade marks

GENERAL INDEX

FIGURE INDEX

INTRODUCTION

The use of these devices has turned - IN EXCLUSIVE WAY - to specialized personnel.

The purpose of this handbook is to give the necessary information to the cognizant and sure use of the products. They are the result of a continual and systematic elaboration of data and technical tests saved and validated from the manufacturer, related to the inside modes of certainty and quality of the information.

The reported data are destined- IN EXCLUSIVE WAY- to specialized users, that can interact with the devices in safety conditions for the persons, for the machine and for the enviroment, impersonating an elementary diagnostic of breakdowns and of malfunction conditions by performing simple functional verify operations , in the height respect of the actual safety and health norms.

The informations for the installation, the assemblage, the dismantlement, the handling, the adjustment, the reparation and the contingent accessories, devices etc. installation are destined - and then executable - always and in exclusive way from specialized warned and educated personnel, or directly from the TECHNICAL AUTHORIZED ASSISTANCE, in the height respect of the manufacturer recommendations and the actual safety and health norms.

The devices can't be used outside a box. The user must always insert the cards in a container that rispect the actual safety normative. The protection of this container is not threshold to the only atmospheric agents, but specially to mechanic, electric, magnetic, etc. ones.

To be on good terms with the products, is necessary guarantee legibility and conservation of the manual, also for future references. In case of deterioration or more easily for technical updates, consult the AUTHORIZED TECHNICAL ASSISTANCE directly.

To prevent problems during card utilization, it is a good practice to read carefully all the informations of this manual. After this reading, the user can use the general index and the alphabetical index, respectly at the begining and at the end of the manual, to find information in a faster and more easy way.

CARD VERSION

The present handbook is reported to the card release:
- **GPC® R63**   version **101197** and later;
- **GPC® T63**   version **101197** and later;
The validity of the bring informations is subordinate to the number of the card release. The user must always verify the correct correspondence among the two denotations. On the card the release number is present in more points both board printed diagram (serigraph) and printed circuit (for example near the the CN4 connector, under C8 capacitor, on the solder side).

GENERAL FEATURES

The **GPC® R/T63** card, belonging to the CPU M serie with 22,5x82x90 mm overall dimension is a powerfull control module with a low cost, ables to work in an autonomous way as intelligent peripheric and/or remoted in a more wider telecontrol and/or aquisition net.

The **GPC® R/T63** is supplied with a plastic holder equipped with hooks for the Omega rail DIN 46277-1 and DIN 46277-2 types. Thanks to the low cost of this CPU serie, it is possible to successfully solve, also all those small automation problems, which have a limited cost budget. Using the wide range of developing softwar tools, available for the **GPC® R/T63** such as the **BASCOM LT** or the Intel **MCS BASIC 52**, and so on, it is possible to complete the applications in a very short time and with minimum investments. For who wants to work in Assembler there is the very good **Soft-ICE** developping tool, that includes an Assembler and a Debuger for the 8051 CPU family.

The **GPC® R/T63** is also available already programmed with telecontrol program. In this case, thanks to ALB (**ABACO®** Link BUS) comunication protocol, it can be used like an intelligent peripheric, alone or in net by a standard serial line; so even applications with limited number of I/O, driven by a normal PC, could be realized in an easy way.

The card is provided of comfortable connector that simplify the connection with field signals, with no requirements of further modules and further cost. Moreover these connectors reduces times when possible up date and assistance phases must be performed.

- Intelligent **ABACO®** Block module of the **M Serie** with 22,5x82x90 mm dimension
- **Housing** for **Omega rail** DIN 46277-1 and DIN 46277-2 types
- Available in 3 different versions with the following CPUs:
    GPC® R/T63   with **80C32** 22MHz, 32K RAM
    GPC® R/T63A   with **Atmel 89S8252** 22MHz; 8K internal FLASH; 2K internal
                          EEPROM; 32K RAM
    GPC® R/T63D   with **Dallas 80C320** 22MHz, 32K RAM
- Total memory addressing of **96K** size, divided in: 32K static **RAM** soldered; socket for
    32K **EPROM**; socket for 32K RAM, EPROM or **EEPROM**
- Compatible code with the famous **51 family** of µP
- **Real Time Clock** with 256 Byte of internal RAM
- **Back up** circuitery for RTC and RAM, based on **LITHIUM** battery
- **6** NPN **digital input lines**, galvanically coupled
- External **INT** line, galvanically coupled
- 3 digital output lines buffered with: 5 A **relays**   on **GPC® R63**
                          4 A darlington **transistor**   on **GPC® T63**
- Status **LEDs** affording visual check for all the I/O lines
- I/O connection through **quick release srew terminal** connectors
- **Three** 16 bits **timer counter**
- TTL **serial line**
- Built in **switching** power supply
- Coupled galvanically I/O section powered at **24 Vdc**; on board logic powered at 5 Vdc
    or 10÷40 Vdc or 10÷24 Vac, protected by **TranZorb**
- Wide range of developping software tools such as **C compilers**, **BXC51**, **Assembler**,
    Monitor, **NoICE**, **HTC 51**, **BASCOM 8051**, **PASCAL**, **CMX**, and so on.

The following pages describe each section of the card in a more detailed mode and figures 1, 2 illustrate the sections interconnections.

CN3	CN4
TTL **SERIAL LINE** POWER SUPPLY	**POWER SUPPLY**

+5 Vdc

SWITCHING
POWER SUPPLY

USER INPUT

CONTROL
LOGIC

**CPU
51 family**

IC 12
RAM

IC10
RAM, EEPROM,
EPROM

IC 7
EPROM

IC8
SERIAL RAM+RTC

BATTERY

DRIVERS

N.O. RELAYS

OPTO COUPLERS

3 OUTPUT LINES	6 INPUT LINES
CN8	**CN7**

FIGURE 1: GPC® R63 BLOCK DIAGRAM

CPU

The **GPC® R/T63** can use many of '51 microprocessors family. Basically these µP can be divided in three groups that have some common features:

- 8 bit CPU;
- 256 bytes internal RAM;
- 64K + 64K bytes of external code and data memory;
- four 8 bits I/O port;
- 2 standard 16 bits Timer/Counters;
- 16 bits Timer/Counters with Capture and Compare function;
- Idle mode or Power down mode;

and some specific features as below described:
- µP 80C32, 80C52, 87C52, 89C52, etc., manufactured by INTEL and other secound sources:

- 12 clocks system cycle;
- 8K bytes internal EPROM or FLASH EPROM;
- 2 priority level for interrupts and 6 interrupt sources;
- 1 syncronous/asyncronous serial line;

- µP 89S8252 manufactured by ATMEL:

- 12 clocks system cycle;
- 8K bytes internal FLASH EPROM;
- 2K bytes internal EEPROM;
- 2 priority level for interrupts and 6 interrupt sources;
- 1 syncronous/asyncronous serial line;

- µP 80C320, 87C320, etc., manufactured by DALLAS:

- 4 clocks system cycle;
- 8K bytes internal EPROM;
- 3 priority level for interrupts and 13 interrupt sources;
- 2 syncronous/asyncronous serial line;
- power failure section;
- internal watch dog timer.

All these microprocessors are code compatible with the world wide used '51 family and they have an extended instruction set, fast execution time, easy use of all kind of memory and an efficient interrupt management. As previously described the card can be ordered in three different CPU configuration: **GPC® R/T63** with 80C32; **GPC® R/T63A** with 89S8252 and **GPC® R/T63A** with 80C320.

For further information on the listed microprocessor, please refer to specific documentation of the manufacturing company.

CONTROL LOGIC

The addresses of all peripheral device's registers and of memory devices on **GPC® R/T63** are assigned from a specific control logic that allocates all these devices in the microprocessor addressing space.

For further information please refer to "ADDRESSES AND MAPS" chapter.
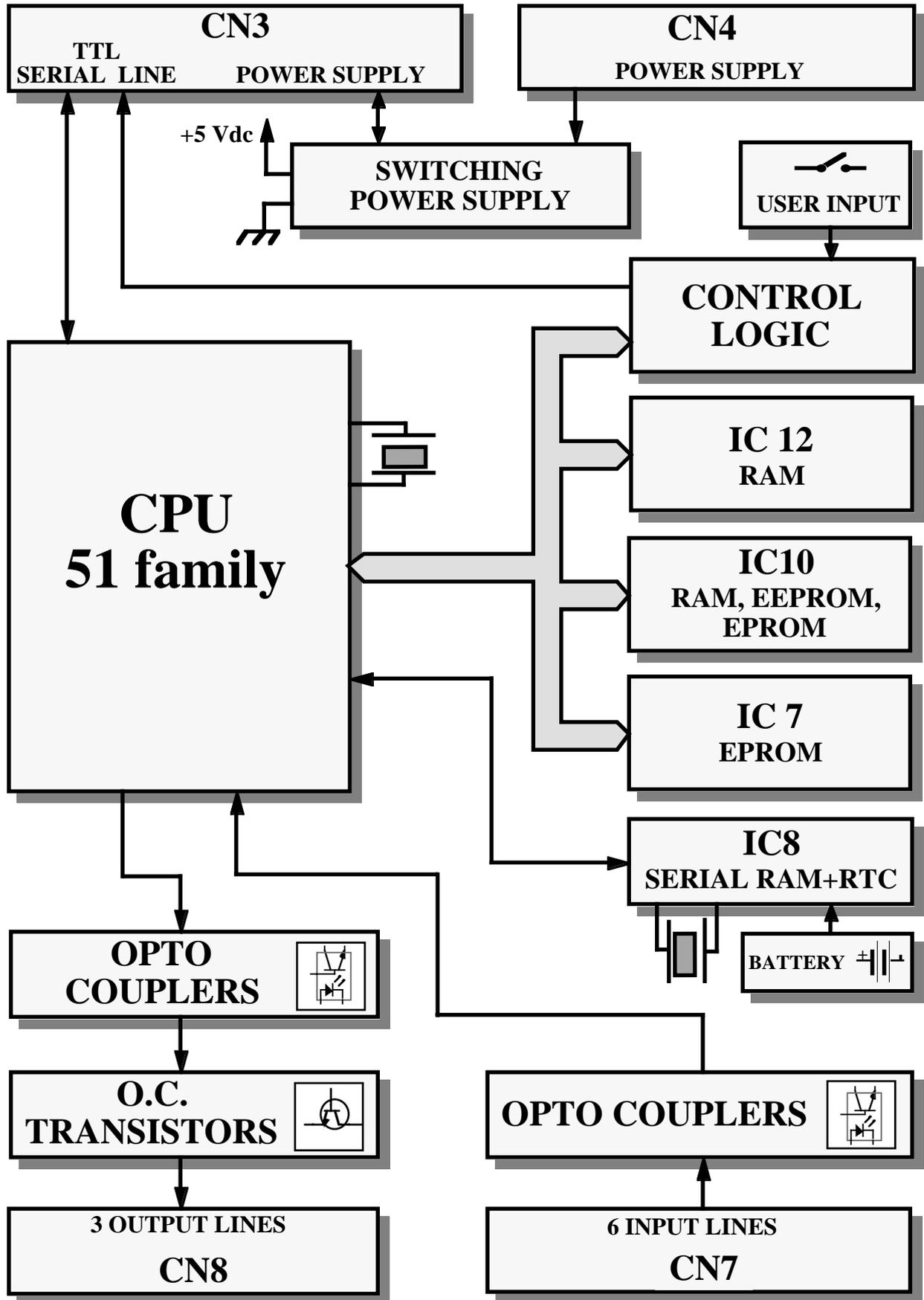
FIGURE 2: GPC® T63 BLOCK DIAGRAM

SERIAL COMMUNICATION

On **GPC® R/T63** it is always available an hardware serial line that is completely software configurable for physical protocol and by simply programming some microprocessor registers, the user can set the baud rate, stop bits number, lenght of character and parity. The serial line is connected to CN3 connector at TTL level, so when the card must be connected in a network or at long distance or with other systems that use standard electric protocol, the user must provide external drivers (RS 232,RS 422, RS 485, current loop, etc.). Please remember that on CN3 connectors more than standard receive and transmit signals it is available also another output signal that can be driven by software. This signals can be used to define the RS 485 line direction, to enable the RS 422 transmit drive or to generate an RS 232 handshake.
Please read APPENDIX A of this manual or contact directly **grifo®** technician for further explanation or any other necessary information.

MEMORY DEVICES

On the card can be mounted 96,256K of memory divided with a maximum of **32K** EPROM, **32K** RAM, **32K** EEPROM, RAM or EPROM and 256 bytes of serial RAM. The **GPC® R/T63** memory configuration must be chosen considering the application to realize or the specific requirements of the user. Normally the card is equipped with 32K byte of static RAM plus the 256 bytes of serial RAM and all different configurations must be specified from the user, at the moment of the order.
With the on board back up circuit there is the possibility to mantain the value of the 256 bytes serial RAM and to keep the real time clock counting, also when power supply is failed; in this way the card is always able to maintain parameters, logged data, system status and configuration, etc. without using expensive external UPS. The back up circuit is based on the on board battery that ensures a very long data retention time. By mounting the backed RAM module or the EEPROM module option on IC10 the user can improve the on board RAM capacity. The addressing of memory devices is controlled by control logic, that provides to allocate the devices in the microprocessor address space; this control logic automatically manages the different addressing mode and it satisfy the requests of each **GPC® R/T63** software tools.
For further information about memory configuration, sockets description and jumpers connection, please refer to chapter "ADDRESSES AND MAPS", "PERIPHERAL SOFTWARE DESCRIPTION" and to the paragraph "MEMORY SELECTION".

CLOCK DEVICES

On **GPC® R/T63** there are two separate circuits with crystal to generate the clock signal for the microprocessor (22.1184 MHz) and the clock signal for Real Time Clock (32.768 KHz). The choice of using two circuits and two separated crystals, has the advantage to change the microprocessor working speed (when best performances are required) without additional changes in software, firmware, etc.
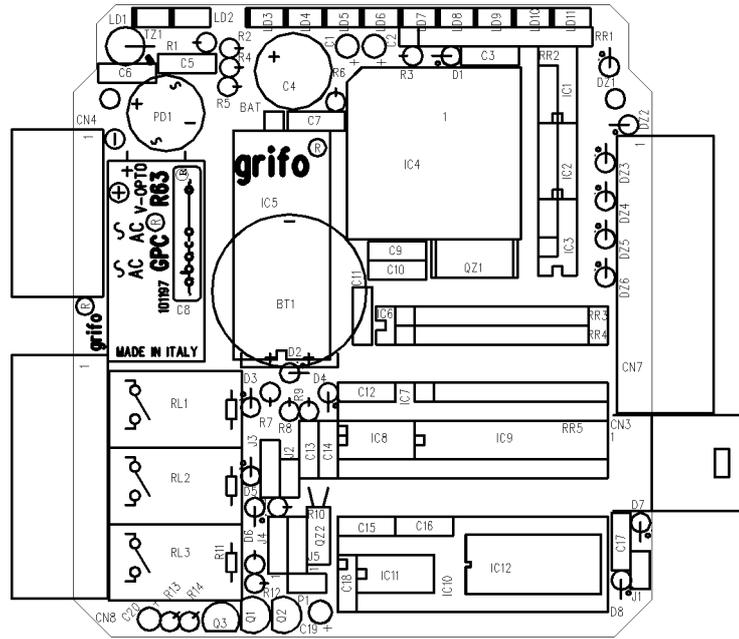
FIGURE 3: GPC® R63 COMPONENTS MAP (COMPONENT SIDE)
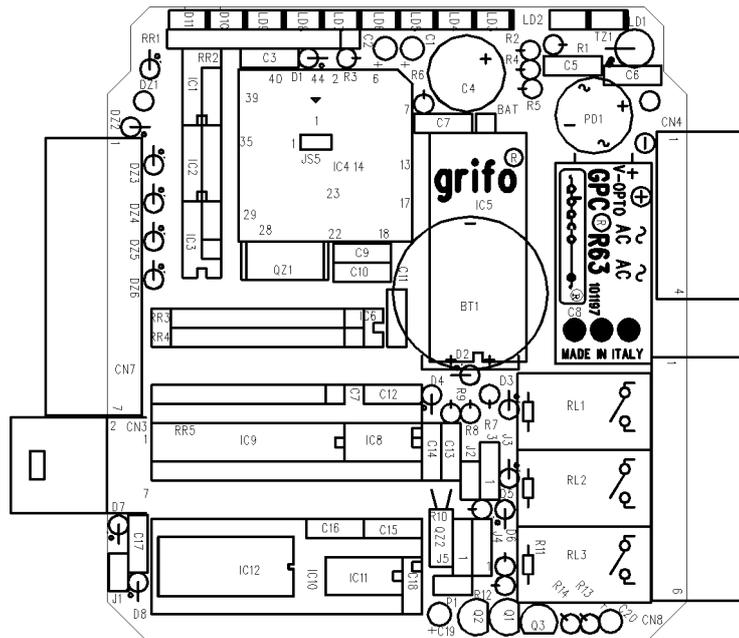
FIGURE 4: GPC® R63 COMPONENTS MAP (SOLDER SIDE)

PERIPHERAL DEVICES

GPC® R/T63 is the right card to solve many control problems in automation fields, in fact it is equipped with some peripheral components that facilitate the connection and the management to external system. These devices are:

Real Time Clock:	the IC 8 module includes a serial RAM and a serial RTC, which manages time (hours, minutes, seconds) and date (day, month, year, day of the week). The RTC is also capable to generate programmable periodic alarms that are connected to one of the microprocessor interrupt pin.
NPN digital inputs:	throught this section the user can acquire, by software, the status of the 6 card input lines. Each NPN input lines is optcoupled and its state is shown by a proper LED. The optocoupled section is powered by a specific +Vopto voltage that must be provided externally. Two of the inputs are connected to microprocessor interrupt pins.
Relay digital outputs:	throught this section the user can set, by software, the status of the relays outputs. Each output has an own LED that shows the line status and it drives a 5 A normally open relay. This section is available only on **GPC® R63** card.
Transistor digital outputs:	throught this section the user can set, by software, the status of the transistor outputs. Each output is galvanically isolated by optocoupler, it has an own LED that shows the line status and it drives a 4 A darlington, open collector transistor. This section is available only on **GPC® T63** card.

For further information about described resources, please refer to "PERIPHERAL DEVICES SOFTWARE DESCRIPTION" chapter.

POWER SUPPLY

One of the most important features of **GPC® R/T63** is its on board power supply circuit. The card requires two different power signal: one for the optocoupled I/O and the other for on board logic. For further information please refer to "ELECTRIC FEATURES" and "POWER SUPPLY SELECTION" chapters.
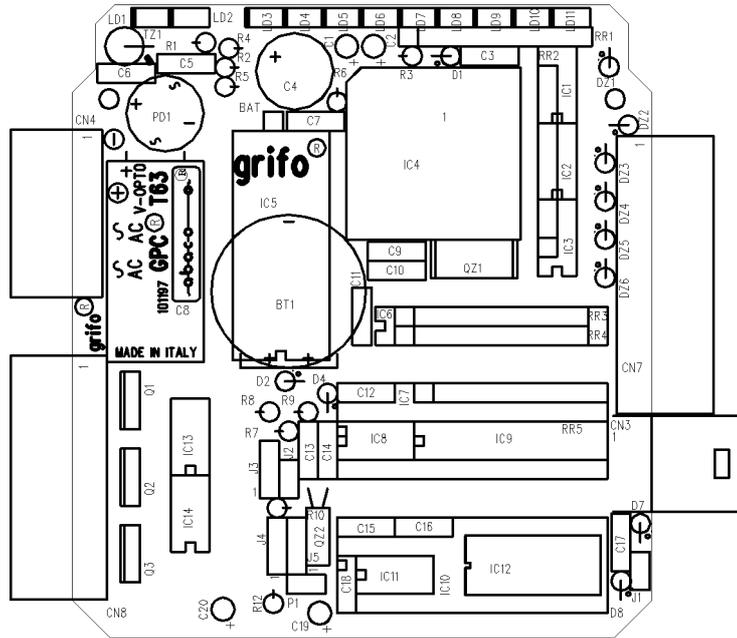
FIGURE 5: GPC® T63 COMPONENTS MAP (COMPONENT SIDE)
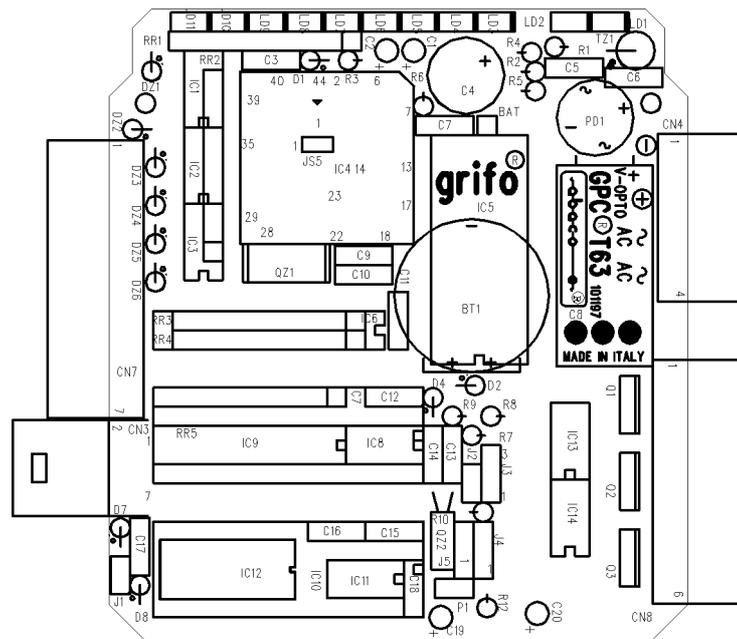
FIGURE 6: GPC® T63 COMPONENTS MAP (SOLDER SIDE)

TECHNICAL FEATURES

GENERAL FEATURES

Devices:	6 NPN optocoupled digital inputs.
(without µP resources)	3 digital outputs buffered with relays. (**GPC® R63**)
	buffered with transistor. (**GPC® T63**)
	1 bidirectional TTL serial line.
	1 local contact for reset.
	1 software readable user inputs.
	1 backed real time clock.

Memory:	IC 7:	32K x 8 EPROM.
	IC 12:	32K x 8 RAM.
	IC 10:	32K x 8 RAM, EEPROM, EPROM.
	IC 8:	serial RAM 256 bytes.

CPU:	INTEL 80C32 and compatible ones. (**GPC® R/T63**)
	ATMEL 89S8252 and compatible ones. (**GPC® R/T63A**)
	DALLAS 80C320 and compatible ones. (**GPC® R/T63D**)

Clock Frequency:	22.1184 MHz

PHYSICAL FEATURES

Size:	22,5 x 82 x 90 mm
	22,5 x 82 x 102 mm (including Ω rail hook)
Mounting:	On Ω rail DIN 46277-1 and DIN 46277-2 types
Weight:	180 g (**GPC® R63**)
	170 g (**GPC® T63**)
Connectors:	CN3: 4+4 pins, AMP Mod II 90°
	CN4: 4 pins, quick release screw terminal connector
	CN7: 7 pins, quick release screw terminal connectors
	CN8: 6 pins, quick release screw terminal connector
Temperature range:	0÷50 °C
Relative humidity:	20%÷90% (without condense)

ELECTRIC FEATURES

Version without power supply section:

Power supply voltage:	+5 Vdc	(control logic)
	+24 Vdc	(+V opto)

Version with switching power supply section:

Power supply voltage inputs:	+10÷40 Vdc or 10÷24 Vac	(control logic)
	+24 Vdc	(+V opto)

Power supply voltage outputs:	+5 Vdc;	1000 mA - Consumption
	+V opto;	100 mA

Consumption:	345 mA max	(**GPC® R63**	+5 Vdc)
	340 mA max	(**GPC® R63A**	+5 Vdc)
	360 mA max	(**GPC® R63D**	+5 Vdc)
	170 mA max	(**GPC® T63**	+5 Vdc)
	165 mA max	(**GPC® T63A**	+5 Vdc)
	185 mA max	(**GPC® T63D**	+5 Vdc)
	17 mA max		(+V opto)

Back up current:	3,6 μ A

Min current for optocoupled input:	1 mA

Relay max current:	5 A

Relay max voltage:	30 Vdc / 250 Vac

Transistor max current:	4 A, not continuative	(*)
Transistor max voltage:	45 Vdc	(*)
Transistor max power:	1.25 W	(*)

(*) The value are referred to a 20° C work temperature.

INSTALLATION

In this chapter there are the information for a right installation and correct use of the card. The user can find the location and functions of each connectors, jumpers and some explanatory diagrams.

CONNECTIONS

The **GPC® R/T63** module has 4 connectors that can be linkeded to other devices or directly to the field, according to system requirements. In this paragraph there are connectors pin out, a short signals description (including the signals direction) and connectors location (see figure ??).

CN3 - AUXILIARY POWER SUPPLY AND SERIAL LINE CONNECTOR

CN3 is a 4+4 pins, AMP Mod II connector with 2,54mm pitch.
On CN3 connector are available the TTL serial line signals and the power supply voltages. If the card has the switching power section mounted, trough CN3 the user can draw the two galvanically isolated voltages and can use them for external loads supply. Viceversa (power supply not present) trough CN3 the user must give the two voltages (+5 Vdc and +V opto) for card power supply. All the signals are placed in order to reduce interference and electrical noise.

+5 Vdc		1 2		+V opto
TxD TTL		3 4		DIR
RxD TTL		5 6		N.C.
GND		7 8		GND opto
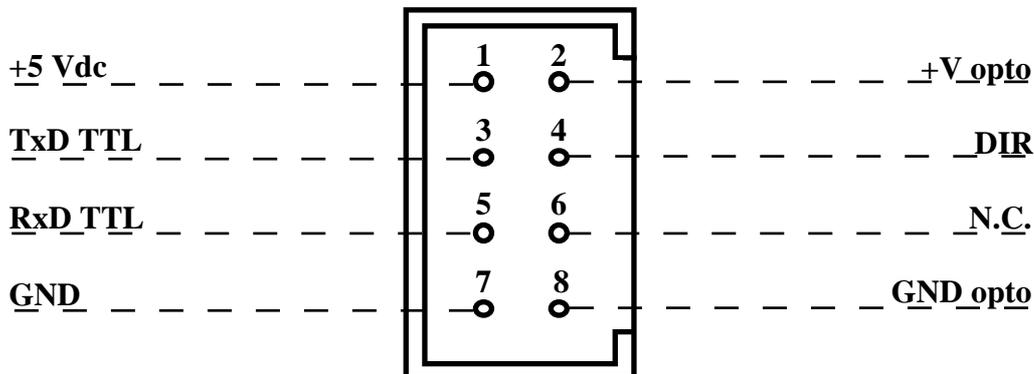
FIGURE 7: CN3 - AUXILIARY POWER SUPPLY AND SERIAL LINE CONNECTOR

Signals description:

TxD TTL	=	O	- Transmit data signal of TTL serial line.
RxD TTL	=	I	- Receive data signal of TTL serial line.
DIR	=	O	- Direction or handshake signal of TTL serial line.
+5 Vdc	=	I/O	- +5 Vdc power supply signal.
GND	=		- Digital ground signal.
+V opto	=	I/O	- +Vopto power supply signal.
GND opto	=		- Opto ground signal.
N.C.	=		- Not connected.
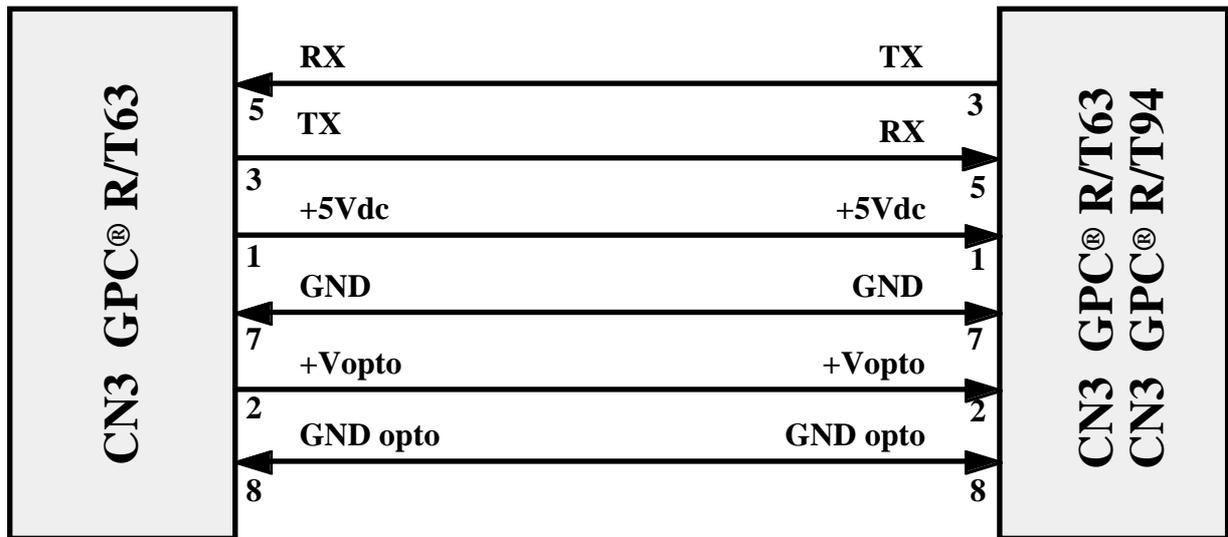
FIGURE 8: SERIAL LINE E POWER SUPPLY CONNECTION EXAMPLE

CN4 - POWER SUPPLY CONNECTOR

CN4 is a 4 pins, quick release, screw terminal connector.
CN4 is used to power the card when on **GPC® R/T9** there is the switching power supply section. If switching power supply section is not present the card must be powered through CN3 connector. Please remember that the two required voltages must be galvanically isolated.
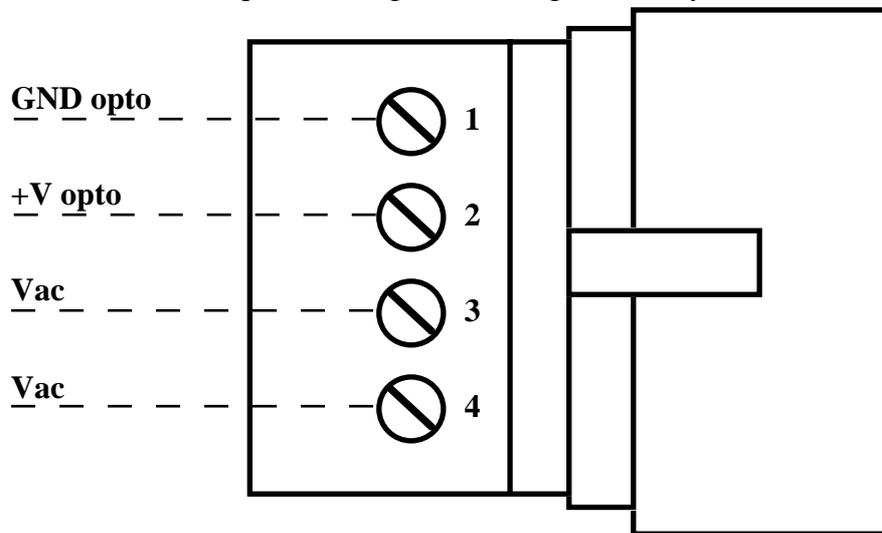
FIGURE 9: CN4 - POWER SUPPLY CONNETTOR

Signals description:

+V opto	=	I	- +V opto power supply signal.
GND opto	=		- Opto ground signal.
Vac	=	I	- Control logic power supply signal (+10÷40 Vdc or 10÷24Vac).
Vac	=	I	- Control logic power supply signal (+10÷40 Vdc or 10÷24Vac).

Please read carefully the "POWER SUPPLY SELECTION" chapter to obtain all the necessary information on power supply configuration and connection.

CN7 - OPTOCOUPLED INPUTS CONNECTOR

CN7 is a 7 pins, quick release, screw terminal connector.
CN7 is used to connect the 6 optocoupled NPN input signals that the card manages. The inputs lines are indirectly connected to some microcontroller I/O pins that have been carefully selected to simplify the software management; in fact these digital inputs can generate interrupt, can be counted through the timer counter, etc. (for further information please read the "PERIPHERAL DEVICES SOFTWARE DESCRIPTION" chapter). On the connector are available the open collector inputs signals and the Opto ground signal.


```
1  ⊘ ─ ─ ─ ─ ─  IN0 (P1.0)

2  ⊘ ─ ─ ─ ─ ─  IN1 (P1.1)

3  ⊘ ─ ─ ─ ─ ─  IN2 (P3.2)

4  ⊘ ─ ─ ─ ─ ─  IN3 (P3.3)

5  ⊘ ─ ─ ─ ─ ─  IN4 (P3.4)

6  ⊘ ─ ─ ─ ─ ─  IN5 (P3.5)

7  ⊘ ─ ─ ─ ─ ─  GND opto
```
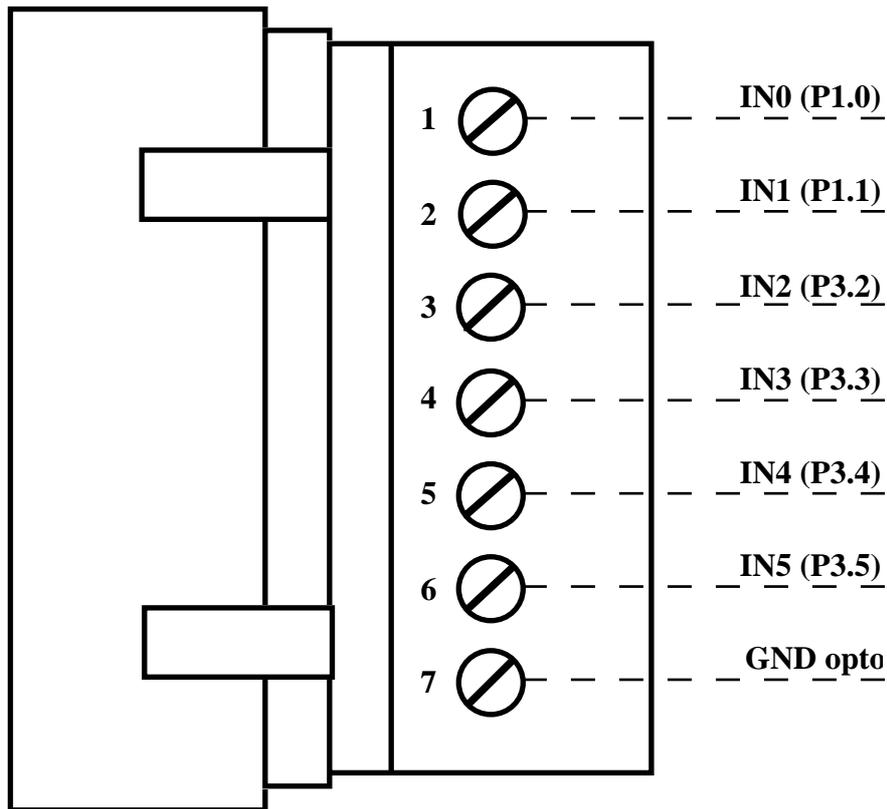
FIGURE 10: CN7 - OPTOCOUPLED INPUTS CONNECTOR

Signals description:

INn (Px.y) = I - NPN input signal n, connected to microprocessor Px.y pin.
GND opto = - Opto ground signal.
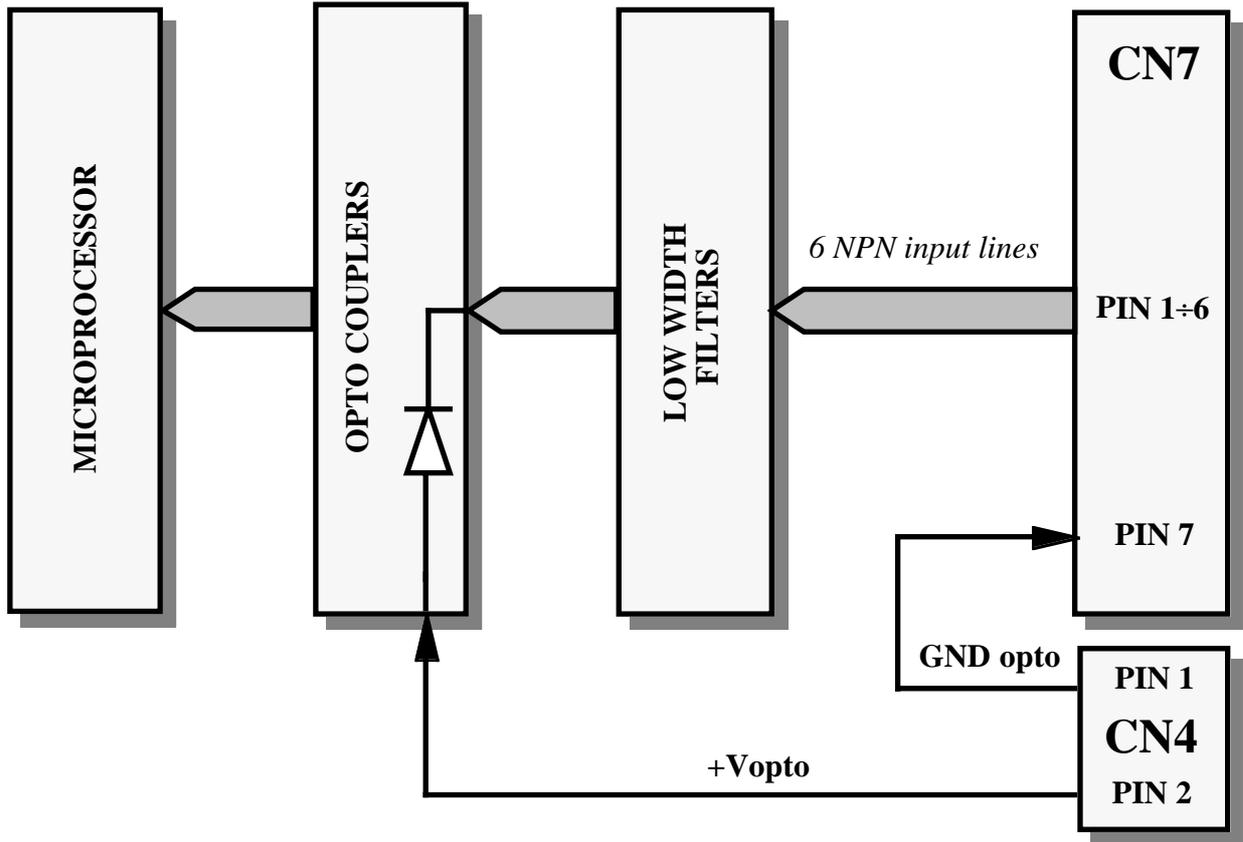
FIGURE 11: OPTOCOUPLED INPUTS DIAGRAM

The low width filters ensure that the optocoupled inputs always work in the best electric conditions, starting from an external +V opto of +24 Vcc.

CN8 - GPC® R63 RELAYS OUTPUTS CONNECTOR

CN8 is a 6 pins, quick release, screw terminal connector.
On CN8 are available three normally open relays outputs and their relative commons. The maximum external load for each line is **5 A** with a maximum voltage of **30 Vdc** or **250 Vac** and each relay output has an own LED that shows the line status (the LED is turned ON when the contact is closed). The outputs lines are indirectly connected to some microcontroller I/O pins that have been carefully selected to simplify the software management (for further information please read the "PERIPHERAL DEVICES SOFTWARE DESCRIPTION" chapter).
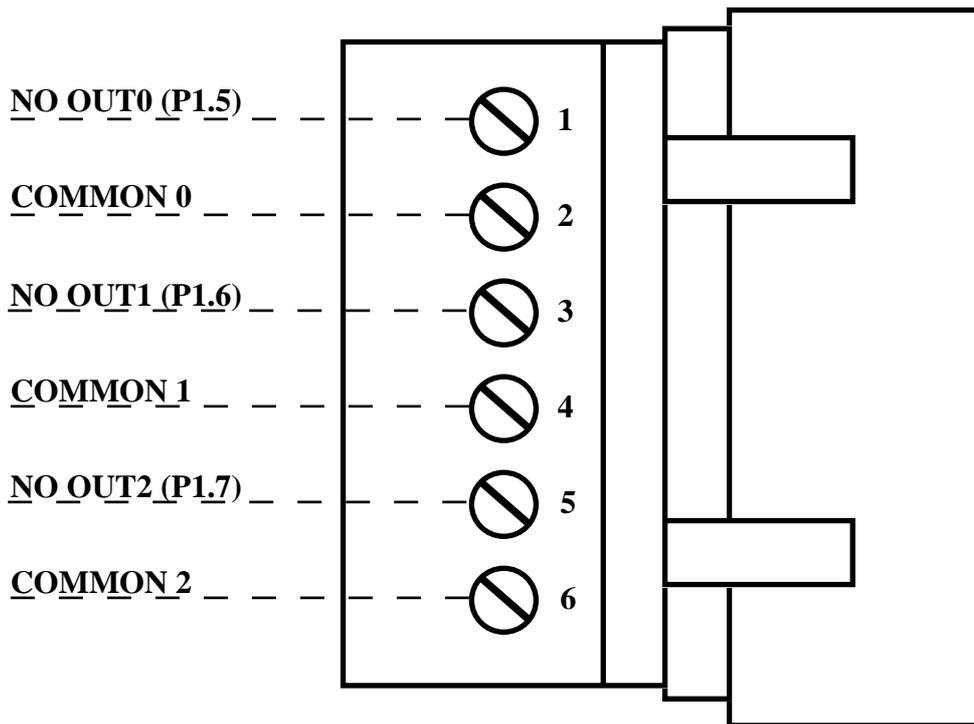
FIGURE 12: CN8 - GPC® R63 RELAYS OUTPUTS CONNECTOR

Signals description:

NO OUTn (Px.y) = O - Normally open relay n output signal, driven by microprocessor Px.y pin.

COMMON n = - Relay n common line.
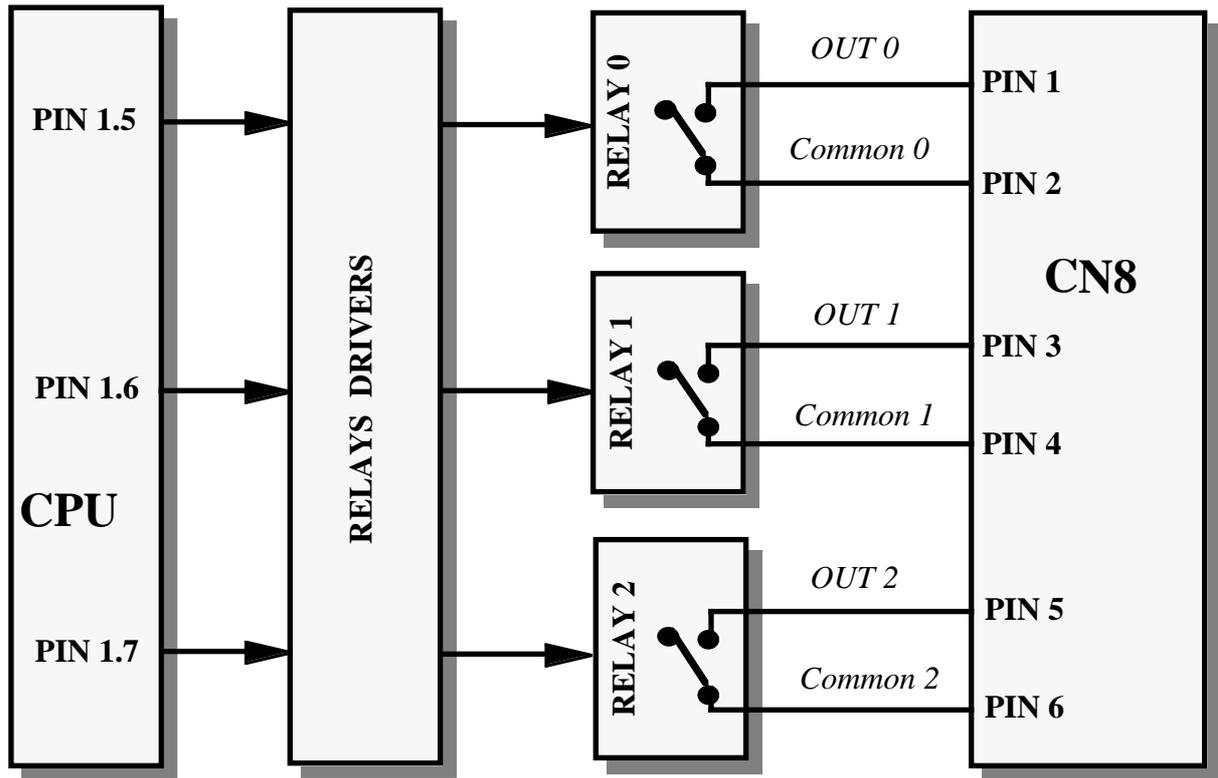
FIGURE 13: RELAYS OUTPUTS DIAGRAM
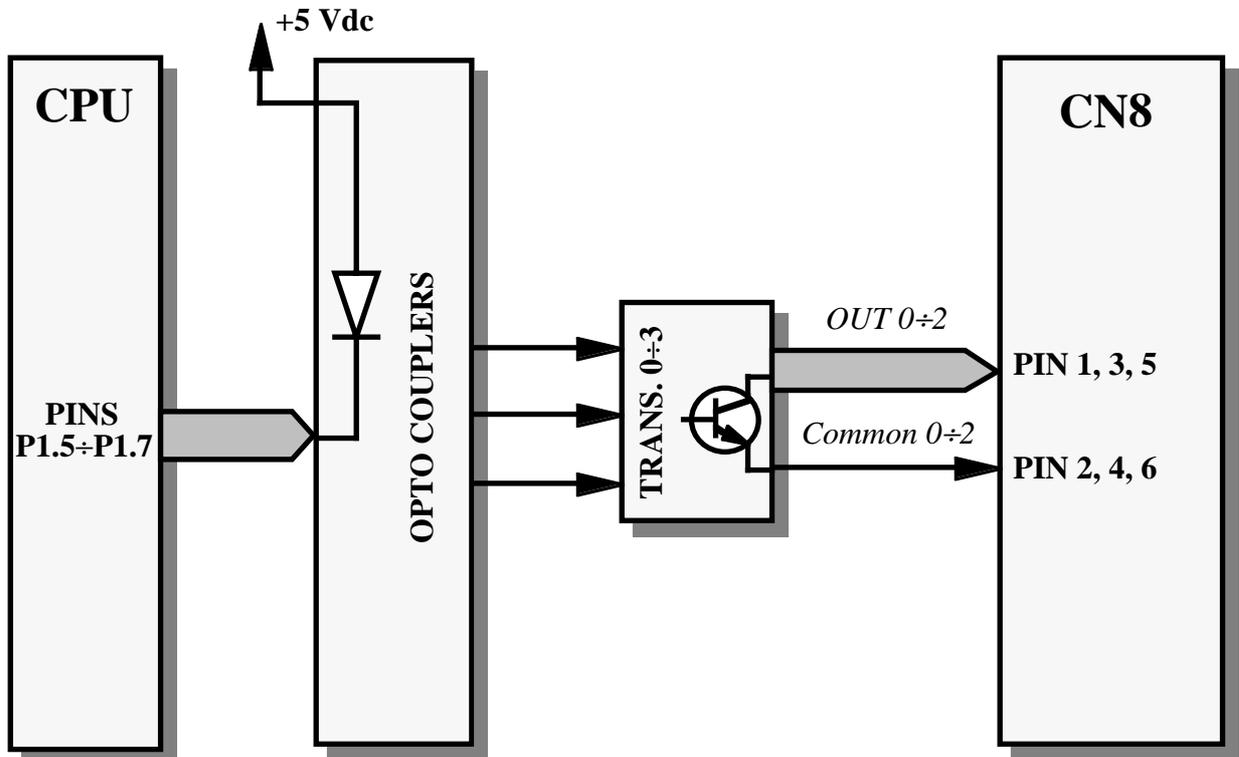
FIGURE 14: TRANSISTORS OUTPUTS DIAGRAM

CN8 - GPC® T63 TRANSISTOR OUTPUTS CONNECTOR

CN8 is a 6 pins, quick release, screw terminal connector.

On CN8 are available the 3 open collector Darlington transistor outputs and their relative common signals. Each output is optocoupled and it has a own LED that shows the line status (the LED is turned ON when the transistor is in conduction). Each NPN open collector Darlington transistor allows a maximum current of **4A**, not continuative, with a voltage of **+45 Vdc**. The transistor haven't radiator so for example they can continuosly drive an external load supplied with +24Vdc and with a maximum current consumption of 600 mA, at a work temperature of about 20 C°. When the transistor outputs are used to drive inductive loads (i.e. power relays, solenoids, electric valve) the user must also connect an external protection diode for reverse voltage. The outputs lines are indirectly connected to some microcontroller I/O pins that have been carefully selected to simplify the software management (for further information please read the "PERIPHERAL DEVICES SOFTWARE DESCRIPTION" chapter).

Signal	Pin
OC OUT0 (P1.5)	1
COMMON 0	2
OC OUT1 (P1.6)	3
COMMON 1	4
OC OUT2 (P1.7)	5
COMMON 2	6
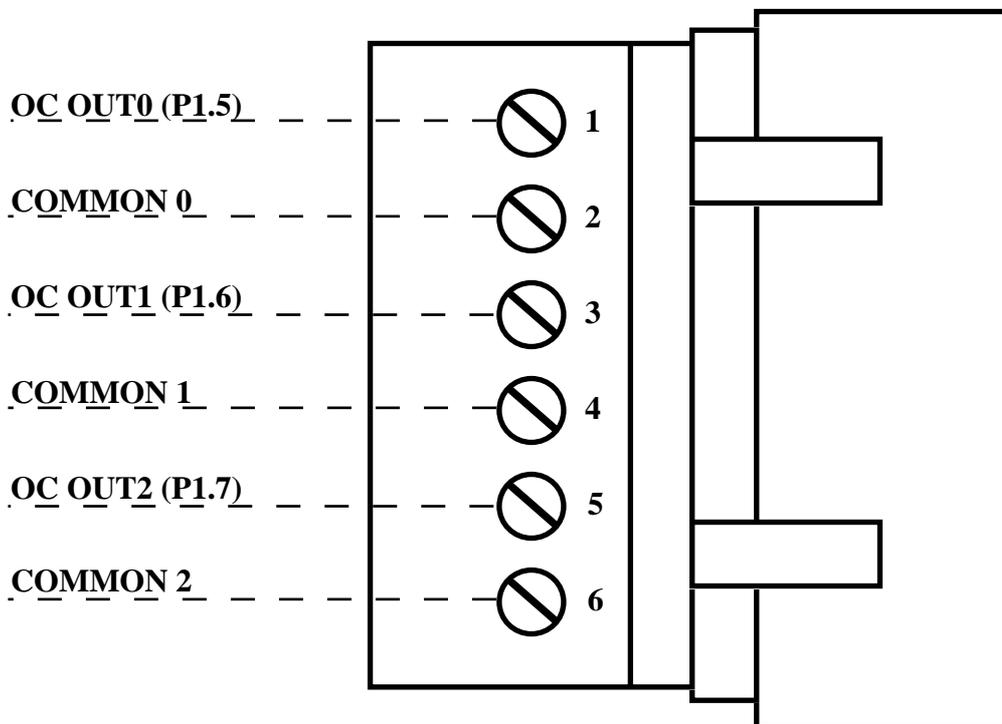
FIGURE 15: CN8 - GPC® T63 TRANSISTORS OUTPUTS CONNECTOR

Signals description:

OC OUTn (Px.y)	=	O	- Open collector transistor n output signal, driven by microprocessor Px.y pin.
COMMON n	=		- Transistor n common line.
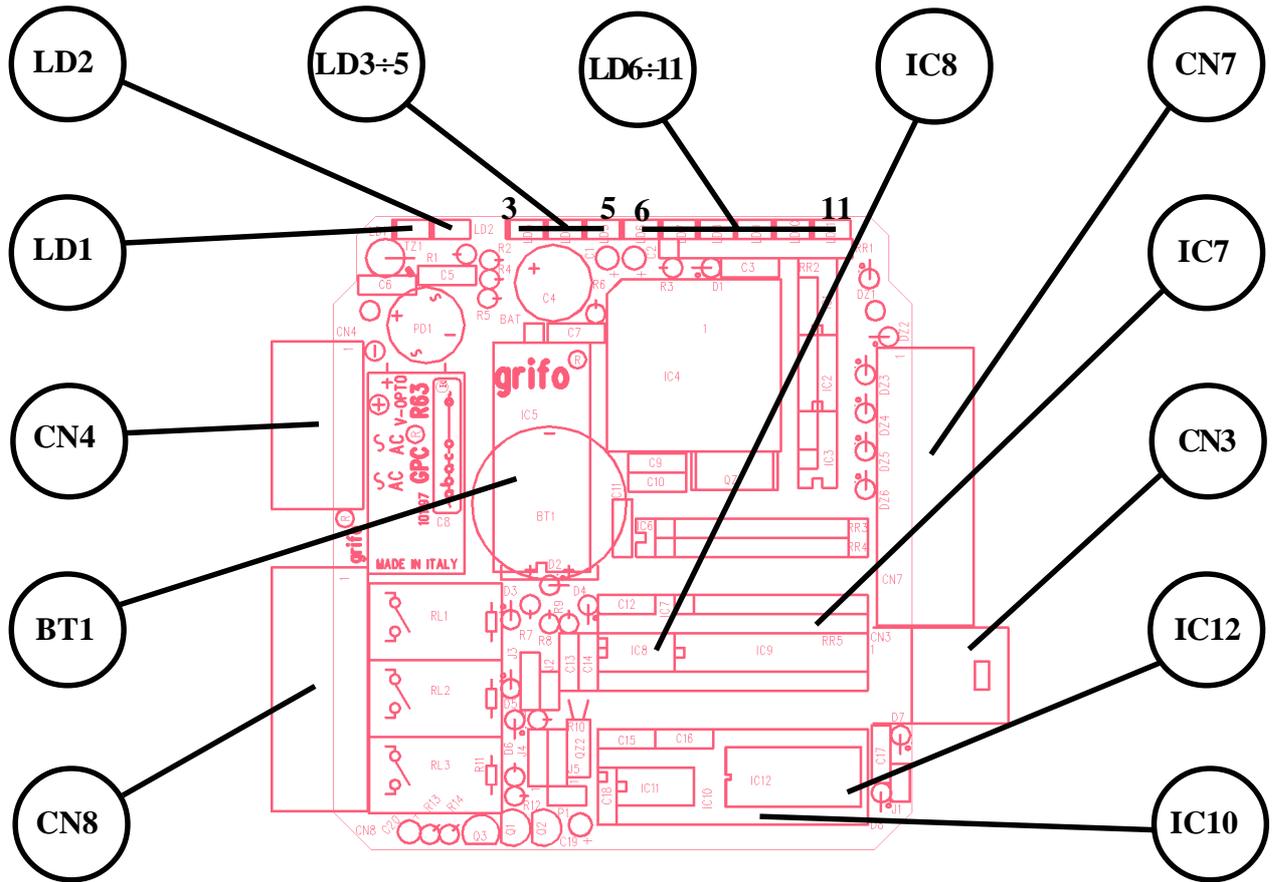
FIGURE 16: MEMORIES, CONNECTORS, LED, ETC. LOCATION ON GPC® R63
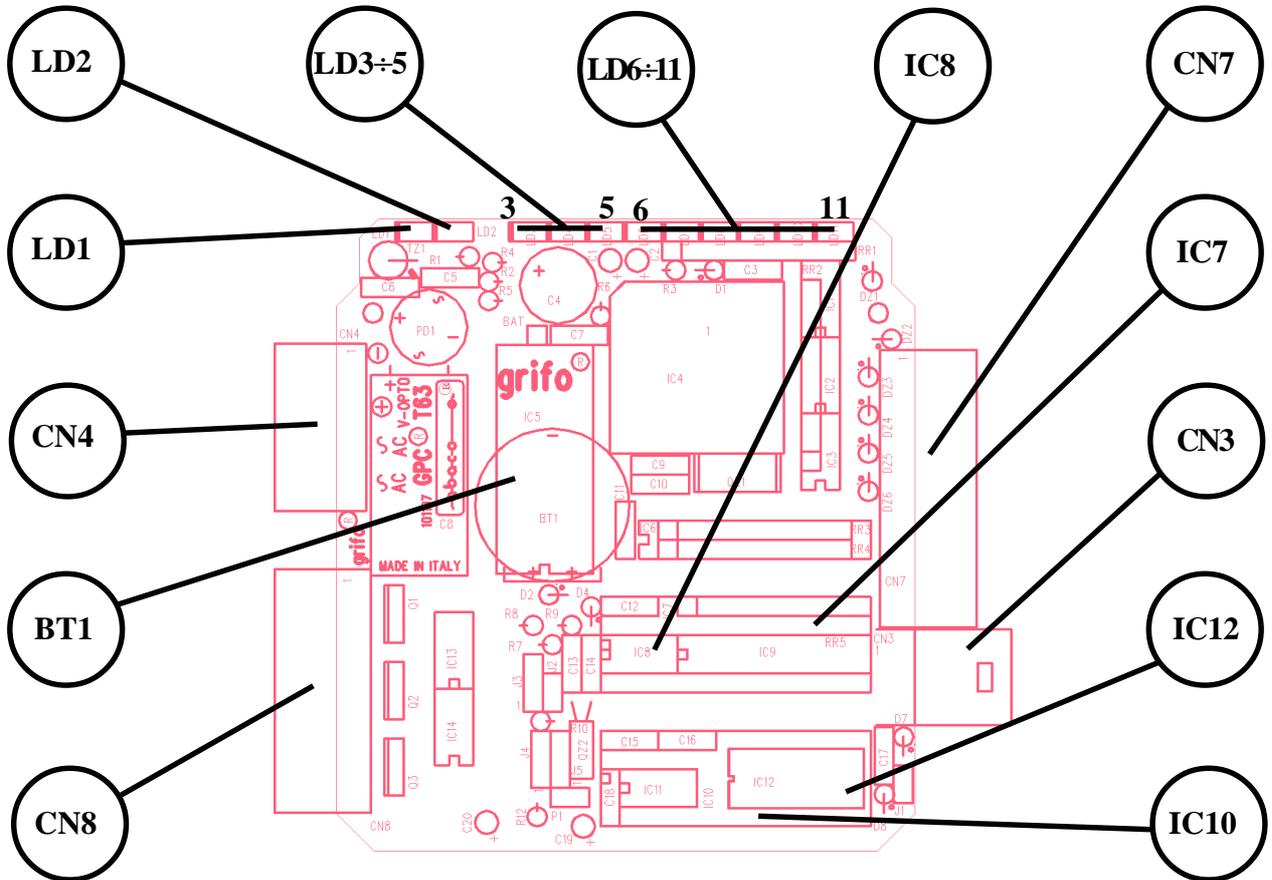
FIGURE 17: MEMORIES, CONNECTORS, LED, ETC. LOCATION ON GPC® T63

INTERRUPTS MANAGEMENT

One of the most important **GPC® R/T63** features is the powerfull interrupts management. Following there is a brief description on interrupt hardware signals management of the card:

Optocoupled input **IN2**   ->   generates an interrupt signal on /INT0 = P3.2 of CPU
Optocoupled input **IN3**   ->   generates an interrupt signal on /INT1 = P3.3 of CPU
Real Time Clock   ->   generates an interrupt signal on /INT1 = P3.3 of CPU

For software information about all internal interrupts and the interrupt mangement by the CPU, please refer to specific documentation of the manufacturing company.

POWER SUPPLY SELECTION

One of the most important features of **GPC® R/T63** is its on board power supply circuitery. The card has two different power supply configurations as below described:

without power supply:
+V opto: it supplies the opto coupled input section of the card and it is a +24 Vdc voltage that must be connected to pins 1 and 2 of CN4 or pins 2 and 8 of CN3.
control logic: it supplies all the electronic of the card and it is a +5 Vdc voltage that must be connected to pins 1 and 7 of CN3.

with switching power supply:
+V opto: it supplies the opto coupled input section of the card and it is a +24 Vdc voltage that must be connected to pins 1 and 2 of CN4 or pins 2 and 8 of CN3.
control logic: it supplies all the electronic of the card and it is a +10÷40 Vdc, or 10÷24 Vac, voltage that must be connected to pins 3 and 4 of CN4. The power supply circuit generates the necessary voltages for the card, starting from all the standard industrial source like mains, power transformer, battery, solar cell, etc. If the user must supply external loads, he can draw the on board generated voltage from pins 1 and 7 of CN3.
                    Please remember that the on board switching power supply have a bridge rectifier, so when DC power supply is furnished, the card GND signal is at a different voltage from power supply ground signal.

The power supply circuit was designed for reducing the consumption (the microprocessor power down and idle mode is available) and for increasing the electrical noise immunity. To ensure this immunity against noisy, variation, etc., the two required external power supply signals that must be galvanically isolated, while to safeguard the card from accidental voltage peaks, on board there is a protection circuit by **TransZorb**™.
The power supply type must be specified at the moment of the order (in fact this configuration requires an hardware modification that must be performed by specialized **grifo®** technicians) and if not stated, the switching power supply is provide as default.
For detailed power supply technical information, please refer to "ELECTRIC FEATURES" paragraphs.
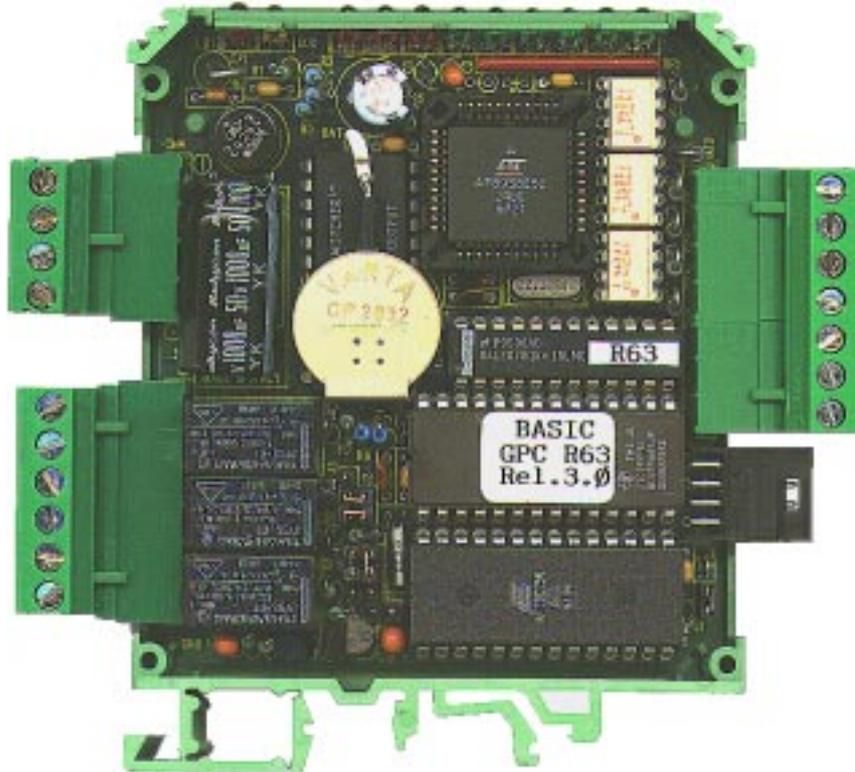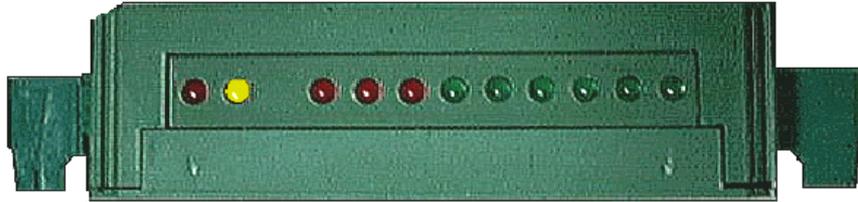
FIGURE 18: GPC® R63 PHOTO

LEDS

On **GPC® R/T94** there are 11 LEDs that show the card status, as described in the following table:

LED	COLOR	FUNCTION
LD1	Red	It signals the presence of +5 Vdc power supply voltage for control logic.
LD2	Yellow	It signals the presence of +V opto power supply voltage for optocoupled inputs.
LD3÷LD5	Red	They signal the status of digital output 0÷3. The LED is turned on when the output OUTn is connected to COMMON n.
LD6÷LD11	Green	They signal the status of digital input 0÷5. The LED is turned on when the input INPn is connected to GND opto.

FIGURE 19: LEDS TABLE

All the LEDs are visible on the front side of the card. The main function of LEDs is to inform the user about card status, with a simple visual indication and in addition to this, LEDs make easier the debug and test operations of the complete system. To recognize LEDs location on the card, please refer to figures 16 and 17.

BACK UP BATTERY

On **GPC® R/T94** there is a lithium battery BT1 that can be used to back up the on board serial RAM+RTC. The user can connect or disconnect the battery from back up circuitry through a simple female strip connected to a flying wire, in fact this strip can be manually inserted in the near battery pin. The card is furnished with the battery not connect to prevent useless discharge and the user can connect it when the real time clock counting and RAM value must be mantained, also in absence of power supply. To recognize battery location on the card, please refer to figures 16 and 17.

JUMPERS

On **GPC® R/T63** there are 7 jumpers for card configuration. Connecting these jumpers, the user can define for example the memory type and size, the peripheral devices functionality and so on. Here below is the jumpers list, location and function:

NAME	PIN N°	FUNCTION
J1	2	It selects the connection for RUN/DEBUG user input.
J2	2	It selects memories maps.
J3	3	Selects memories maps.
J4	3	It selects IC10 memory devices type.
J5	3	Selects IC10 memory devices size.
JS5	2	It enables/disables optional microprocessor internal ROM.
P1	2	It enables/disables the on board RESET circuitry

FIGURE 20: JUMPERS SUMMARIZING TABLE

The following tables describe all the right connections of **GPC® R/T63** jumpers with their relative functions. To recognize these valid connections, please refer to the board printed diagram (serigraph) or to figure 3÷6 of this manual, where the pins numeration is listed; for recognizing jumpers location, please refer to figure 21 and 22.
The "*" used in the following tables, denotes the default connection, or on the other hand the connection set up at the end of testing phase, that is the configuration the user receives.

2 PINS JUMPERS

JUMPER	CONNECTION	USE	DEF.
P1	not connected	It disables the on board RESET circuitry.	*
	connected	It enables the on board RESET circuitry.	
JS5	not connected	It enables the eventual internal ROM of the CPU.	
	connected	It disables the eventual internal ROM of the CPU.	*
J1	not connected	It sets RUN/DEBUG user input at logic level 1 (RUN mode).	*
	connected	It sets RUN/DEBUG user input at logic level 0 (DEBUG mode).	
J2	not connected	This jumper is used with J3 for memory addresses selection. For further information please refer to	*
	connected	chapter "MEMORY MAPS".	

FIGURE 21: 2 PINS JUMPERS TABLE

3 PINS JUMPERS

JUMPER	CONNECTION	USE	DEF.
J3	not connected 1-2 2-3	This jumper is used with J2 for memory addresses selection. For further information please refer to chapter "MEMORY MAPS".	*
J4	1-2 2-3	It configures IC10 for EPROM. It configures IC10 for RAM or EEPROM.	 *
J5	1-2 2-3	It configures IC10 for 32K EPROM. It configures IC10 for 32K RAM or EEPROM.	 *

FIGURE 22: 3 PINS JUMPERS TABLE

POWER ON AND RESET

On **GPC® R/T63** there is a reset and power on circuit that manages the always hard phase of card power up and start. This circuit has the following features:
- Fixed power on time, defined by a proper on board RC circuit;
- reset source from on board P1 contact;
- reset circuit output connected to all the card's section;

The P1 contact can enable the card reset circuitry by connecting the two jumpers pins to a normally open contact (i.e. a button), when the contact is closed (two pins short circuited) the card restarts execution of the program saved in the code area and all the on board peripheral devices are reset at the same time. P1 is commonly used to exit from endless loopespecially during debug phase. To recognize P1 location on the board, please refer to figures 23 and 24.

ON BOARD INPUT

GPC® R/T63 card is equipped with one jumper (J1) that can be read by software. It is normally used for system configuration (operating mode selection, card number programmation inside a network system, fimware configuration, etc.). The J1 status ("0" = CONNECTED; "1" = NOT CONNECTED) can be acquired by reading the RUN/DEBUG register that is allocated in the microprocessor addressing space by the control logic, as described in the paragraph "I/O ADDRESSES". Many software tools available for the **GPC® R/T63** use this jumper for RUN or DEBUG mode selection, as described in the previous table, but the jumper can still be acquired by the user. For recognizing J1 location, please refer to figures 23 and 24.
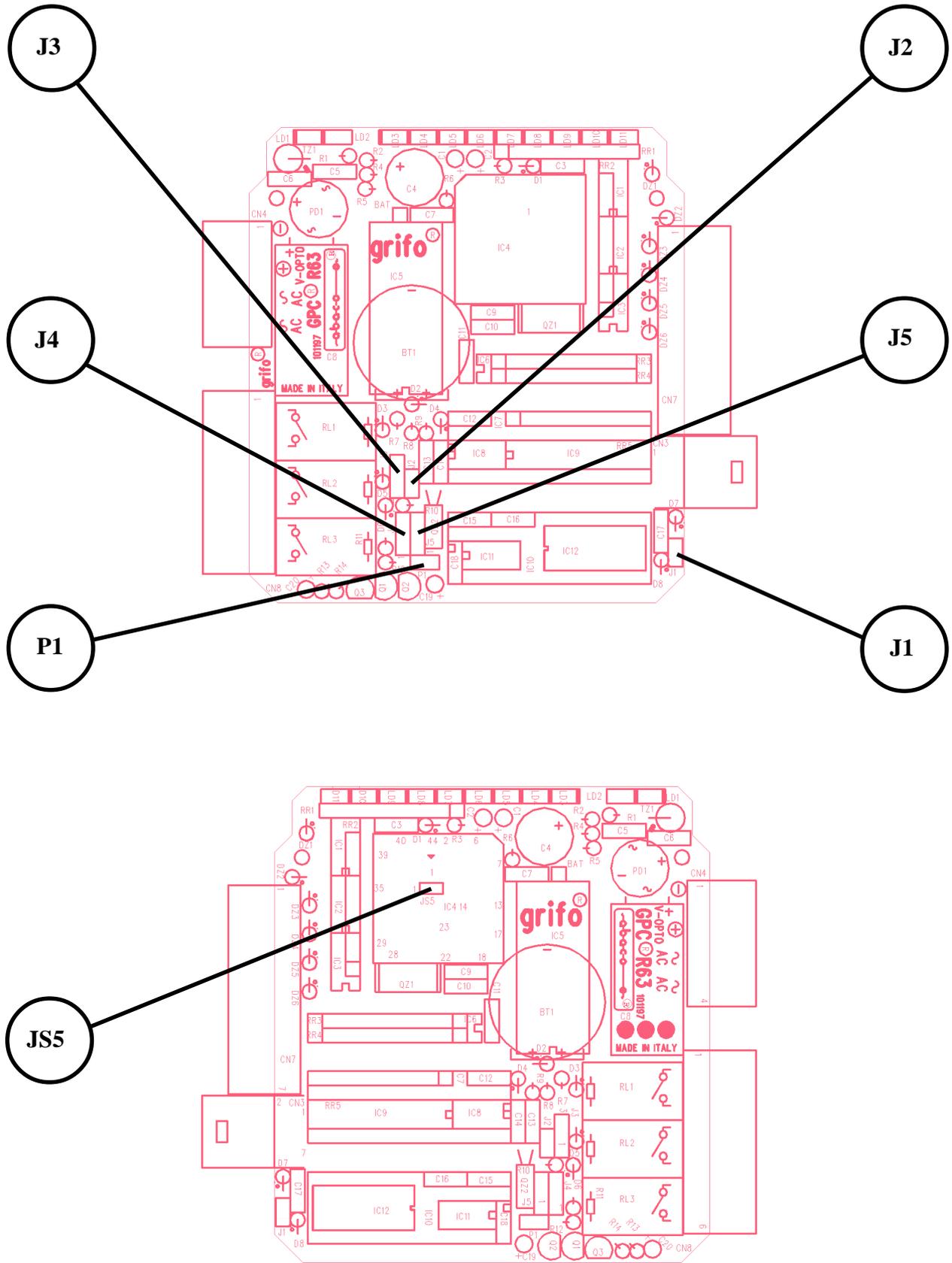
FIGURE 23: GPC® R63 JUMPERS LOCATION (COMPONENT AND SOLDER SIDE)

MEMORY SELECTION

On **GPC® R/T63** can be mounted 96,256 Kbytes of memory divided in several configurations, as described in the following table:

IC	DEVICE	SIZE	JUMPERS CONFIGURATION
10	RAM, EEPROM	32K Bytes	J4, J5 in position 2-3
	EPROM	32K Bytes	J4, J5 in position 1-2
12	RAM	32K Bytes	-
7	EPROM	32K Bytes	-
8	RAM+RTC	256 Bytes	-

FIGURE 24: MEMORY SELECTION TABLE

The sockets IC 7 and IC 10 follow the JEDEC standard, so the mounted memory devices must have JEDEC pin outs; instead IC 8 is a serial memory device that can be mounted only by **grifo®** technicians. The jumpers configurations described on figure 24 only set the sockets for the indicated memory device, but there are some other jumpers that set the memory addressing map; for this information, please refer to "MEMORY MAPS" paragraph.

Normally **GPC® R/T63** is supplied in its default configuration with 32K RAM on IC 12 and 256 byte RAM on IC 8; each different configurations can be defined during order phase or self mounted by the user. Below are reported the abbrevation code of the possible memory options:

.32K	->	32K x 8 RAM
.32KMOD	->	32K x 8 backed RAM
.32EE	->	32K x 8 parallel EEPROM

For further information and prices please contact directly **grifo®**.

SOLDER JUMPERS

The default setting of the solder jumpers, named **JSxx**, is performed with a small track on the solder side, so if this setting must be changed, first cut the default connection track with a sharp cutter and then connect the required position with a low power solder .

FIGURE 25: GPC® T63 JUMPERS LOCATION (COMPONENT AND SOLDER SIDE)

SOFTWARE

A wide selection of software development tools can be obtained, allowing use of the module as a system for its own development, both in assembler and in other high level languages; in this way the user can easily develop all the requested application programs in a very short time. Generally all software packages available for the mounted microprocessor, or for the 51 family, can be used.

**MCS BASIC R/T63**: complete development tools for MCS BASIC (interpreted BASIC language for industrial application). It needs a P.C. for console and program saving operations, while the debug, test and program operations are performed on the card. Special instructions which manage the on board peripheral devices have been added.

BXC51: cross compiler for source files written in MCS BASIC R/T63. It allows a considerable speed increment of the starting MCS BASIC program and it is completely executed on external P.C.

XPAS51: cross compiler for PASCAL source program , executable on P.C. with MS-DOS.

FORTH: complete software development tools to program the card with FORTH high level language. It needs a P.C. for user interface and it is really interesting for its fast execution and small size, of the generated code.

MCC 51: integer cross compiler for source files in standard ANSI C. It produces a source assembly file compatible with MCA 51 or with Intel macro relocatable assembler MCS 51.

MCA 51: macro cross assembler available for MS-DOS operating system in absolute and relocatable version. In this relocatable version is supplied with a linker and a library manager.

MCS 51: source level debugger and simulator. It is executed on P.C. without any additional hardware and it allows loading of HEX and SYMBOLIC files, breakpoint setting, instruction execution in trace mode, registers and memory dump, etc.

MCK 51: it is the sum of MCC 51 and MCA 51 and it is a complete C compiler with an output file type compatible with MCS 51.

HI TECH C 51: cross compiler for C source program. It is a powerful software tool that includes editor, C compiler, assembler, optimizer, linker, library, and remote symbolic debugger, in one easy to use integrated development environment.

SYS51CW: cross compiler for C source program. It is a powerful software tool that includes editor, C compiler, assembler, optimizer, linker, library, simulator and remote symbolic debugger, included in an easy to use integrated development environment for Windows.

SYS51PW: cross compiler for PASCAL source program. It is a powerful software tool that includes editor, PASCAL compiler, assembler, optimizer, linker, library, simulator and remote symbolic debugger, included in an easy to use integrated development environment for Windows.

MDP: monitor debugger program able to load and debug each HEX Intel files for 51 microprocessor family. It is provided of the standard commands available on in circuit emulator and requires only an external P.C. connected through a serial line.
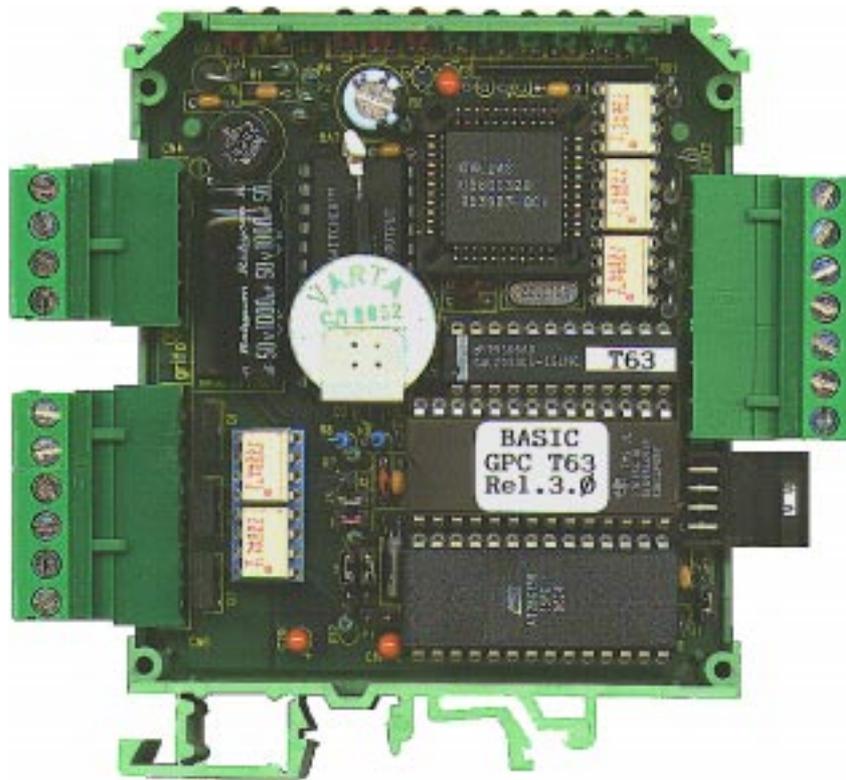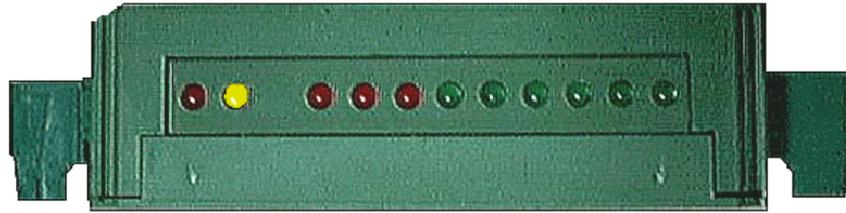
FIGURE 26: GPC® T63 PHOTO

DDS MICRO C 51: low cost ross compiler for C source program. It is a powerful software tool that includes editor, C compiler (integer), assembler, optimizer, linker, library, and remote debugger, in one easy to use integrated development environment. There are also included the library sources and many utilities programs.

SOFTICE: It is a remote symbolic debugger with cross assembler. It is provided of the standard commands available on in circuit emulator and requires only an external P.C. connected through a serial line. There is an high level user interface that can visualize all the processor status in a multiwindow visualization.

NOICE 51: It is a PC hosted debugger consists of a target specific DOS program, NOICExxx.EXE, and a target resident monitor program. The two programs comunicate via RS 232. NOICE includes: source level debug; a disassembler; a file viewer; memory display and editing; a virtually unlimited number of breakpoints; hardware free single step; definition of symbols; the ability to record and play back files of commands; on line help.

OPEN 51/UNI: in circuit emulator for the 51 family. It is a powerfull hardware and software tool that includes: source level debugging and symbolic debugging; project management; built-in multi-file editor; execution of external compilers; debugging of several modules at the same time; built-in disassembler; source level step and trace functions; animate functions; inserting and deleting of breakpoints on the source level; watching and modifying variables on symbol and absolute level.

EMBEDDED PASCAL 51: cross compiler for PASCAL source program. It is a powerful software tool that includes editor, PASCAL compiler, assembler, optimizer, library, included in an easy to use integrated development environment for Windows 95 and NT. Many memory models and data types are supported and sources of library are provided too.

BASCOM 8051: cross compiler for BASIC source program. It is a powerful software tool that includes editor, BASIC compiler and simulator included in an easy to use integrated development environment for Windows. Many memory models, data types and direct use of hardware resource instructions are available.

GET 51: it is a complete program with editor, communication driver and mass memory management for all '51 family cards. This program developed by **grifo®** allows to operate in the best conditions when MCS BASIC, BXC51, MDP software tools are used.

M052: monitor debugger program able to load and debug each HEX Intel files for 51 microprocessor family. It is provided of the standard commands available on in circuit emulator and requires only an external P.C. connected through a serial line. It is preconfigured to work directly with BASCOM 8051 and GET51 software tools.

ADDRESSES AND MAPS

INTRODUCTION

In this chapter are reported all information about card use, related to hardware and software. For example, the registers addresses and the memory allocation are described below.

ADDRESSES

The card devices addresses are managed by a specific control logic, realized with programmable array logic. This control logic allocates memory and peripheral devices in a confortable mode for the user. The available microprocessors addresses 64K bytes of code memory and 64K bytes of data memory and the control logic maps the on board memories and peripheral devices, inside these address spaces. Control logic sets size, type and addresses of memory devices through jumpers J2, J3, J4 and J5; at the same time it allocates I/O addresses always in the upper 256 bytes of microprocessor data memory. Summarizing the control logic allocates:

- 32K bytes of EPROM on IC 7;
- 32K bytes of RAM on IC 12;
- 32K bytes of RAM, EEPROM, EPROM on IC 10;
- RUN/DEBUG selector (J1 status);
- DIR signal for serial communication;

The addresses of all these devices are described in the following paragraphs and can't be set with different value. The other device serial RAM+RTC of IC 8, is managed always by control logic but it is not allocated in memory space, in fact this device is driven through CPU I/O lines with a syncronous communication.

I/O ADDRESSES

I/O addresses are located in the last 256 bytes of the 64K bytes data microprocessor addressing space. Next table shows addresses, meanings and direction of peripheral devices registers (only the external ones to microprocessor):

DEVICES	REG.	ADDRESS	R/W	FUNCTION
RUN/DEBUG	RUNDEB	FF00H÷FF7FH	R	J1 status reading register.
DIR signal	RESDIR	FF00H÷FF7FH	R	Reset DIR signal register.
	SETDIR	FF80H÷FFFFH	R	Set DIR signal register.

FIGURE 27: I/O ADDRESSES TABLE

For further information about register meanings, please refer to next chapter called "PERIPHERAL DEVICES SOFTWARE DESCRIPTION".

MEMORY MAPS

On the **GPC® R/T63** three different memory configurations can be used. The configuration must be selected, with J2 and J3, both according to used software tools and user requests and/or application features. The following figures describe available memory configurations, with proper J2 and J3 setting.

MEMORY CONFIGURATION 0
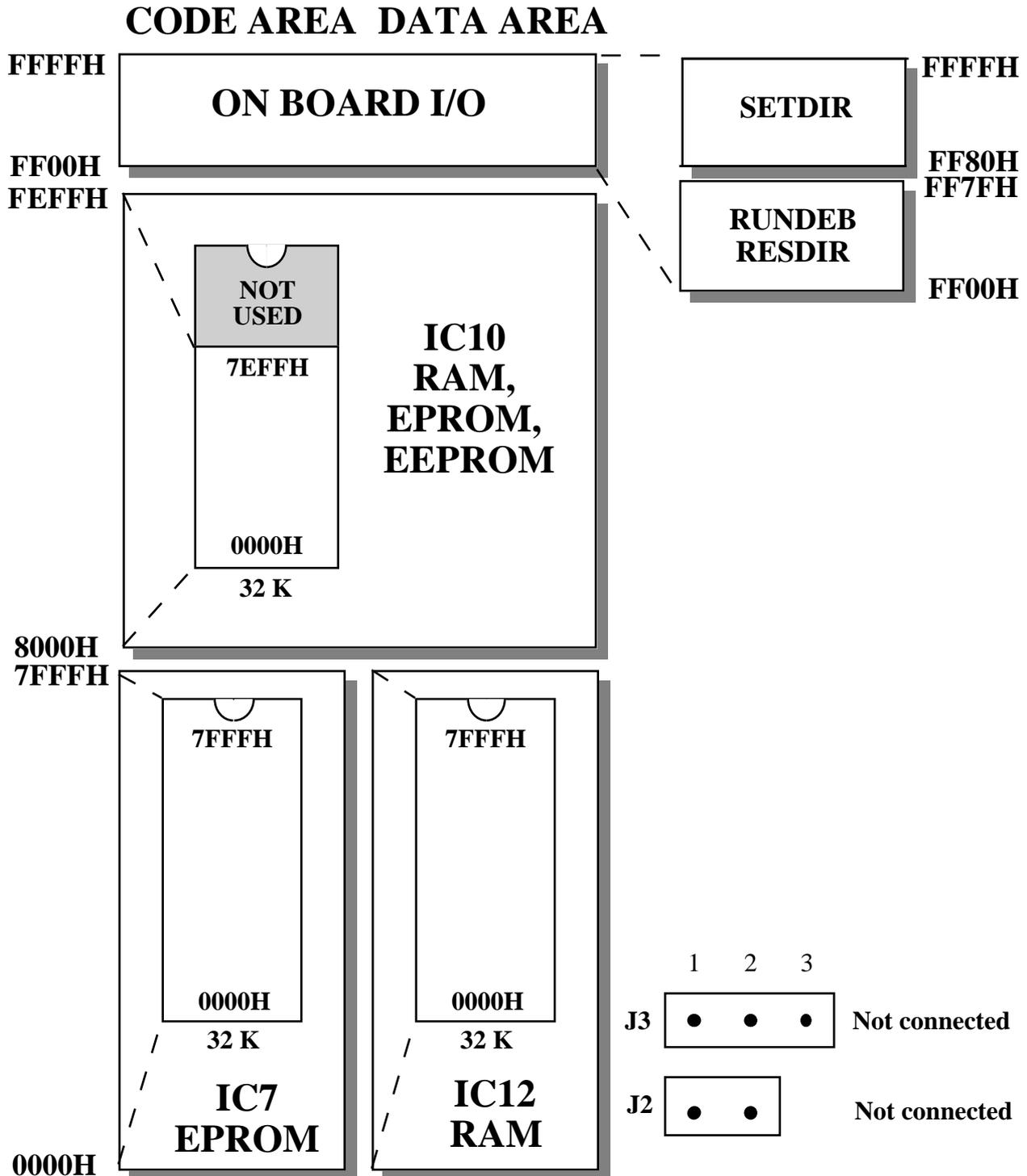
FIGURE 28: MODE 0 MEMORY CONFIGURATION (BASIC+DEBUG)

Used by software tools as: BASIC R/T63; BXC51; HI TECH C; DDS C; SOFTICE (**J3 in 1-2**); etc.

MEMORY CONFIGURATION 1

CODE AREA DATA AREA

FFFFH	**ON BOARD I/O**
FF00H	
FEFFH	

FFFFH **SETDIR** FF80H
FF7FH **RUNDEB RESDIR** FF00H

NOT USED

7EFFH

IC12 RAM

0000H

32 K

8000H
7FFFH

7FFFH

IC7 EPROM

0000H

32 K

0000H

1   2   3

J3 • • • Not connected

J2 ▮ Connected
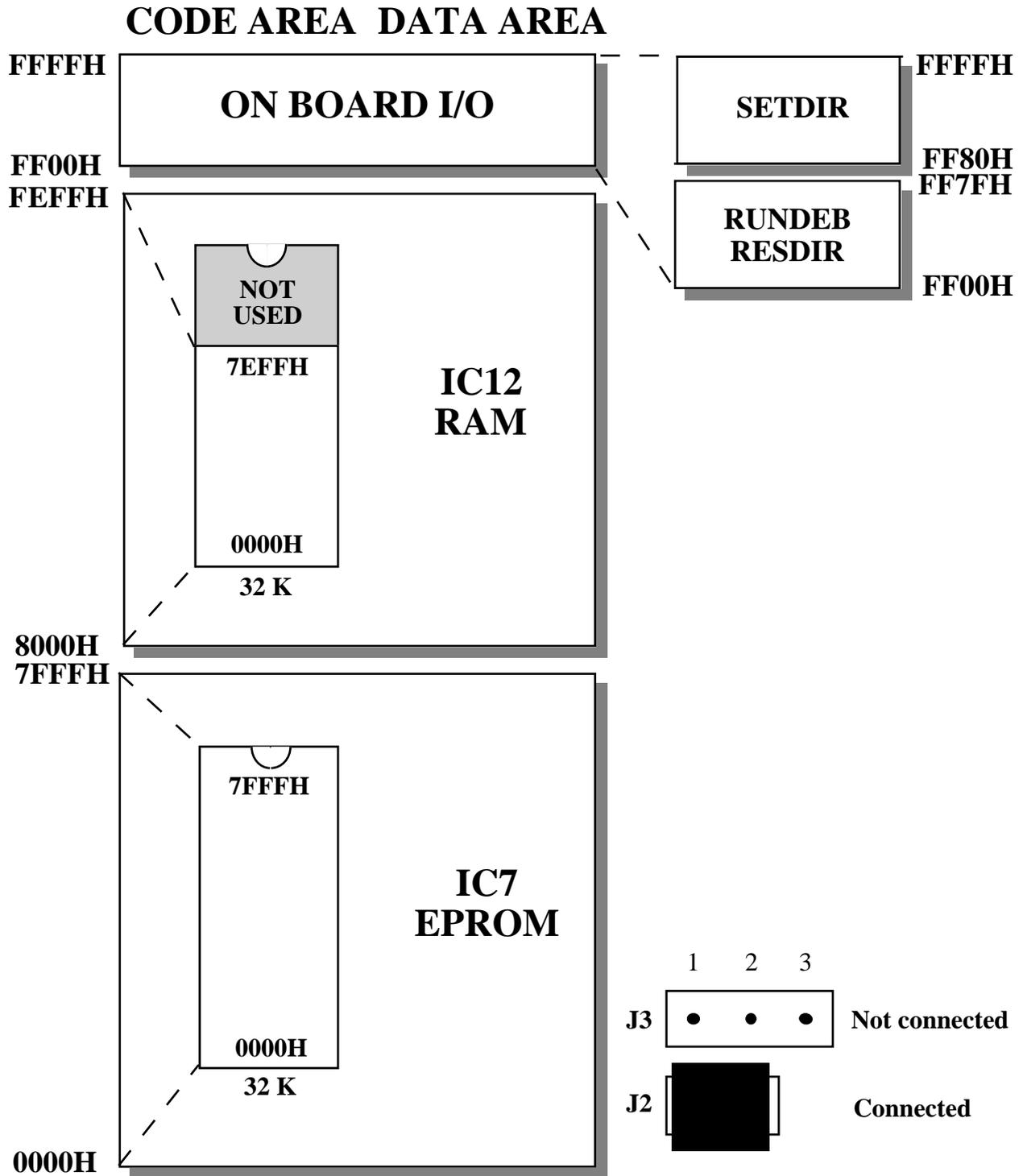
FIGURE 29: MODE 1 MEMORY CONFIGURATION (ASM)
Used by software tools as: HI TECH C; DDS MICRO C; MO52; etc.

MEMORY CONFIGURATION 3

CODE AREA DATA AREA

FFFFH — ON BOARD I/O — FF00H

FEFFH
NOT USED
7EFFH
IC10 RAM, EPROM, EEPROM
0000H
32 K
8000H

7FFFH
7FFFH
2000H
IC12 RAM
NOT USED
32 K
2000H

1FFFH
NOT USED
1FFFH
IC7 EPROM
0000H
32 K
0000H

FFFFH — SETDIR — FF80H
FF7FH — RUNDEB RESDIR — FF00H

J3   1 2 3   Position 2-3
J2   Connected
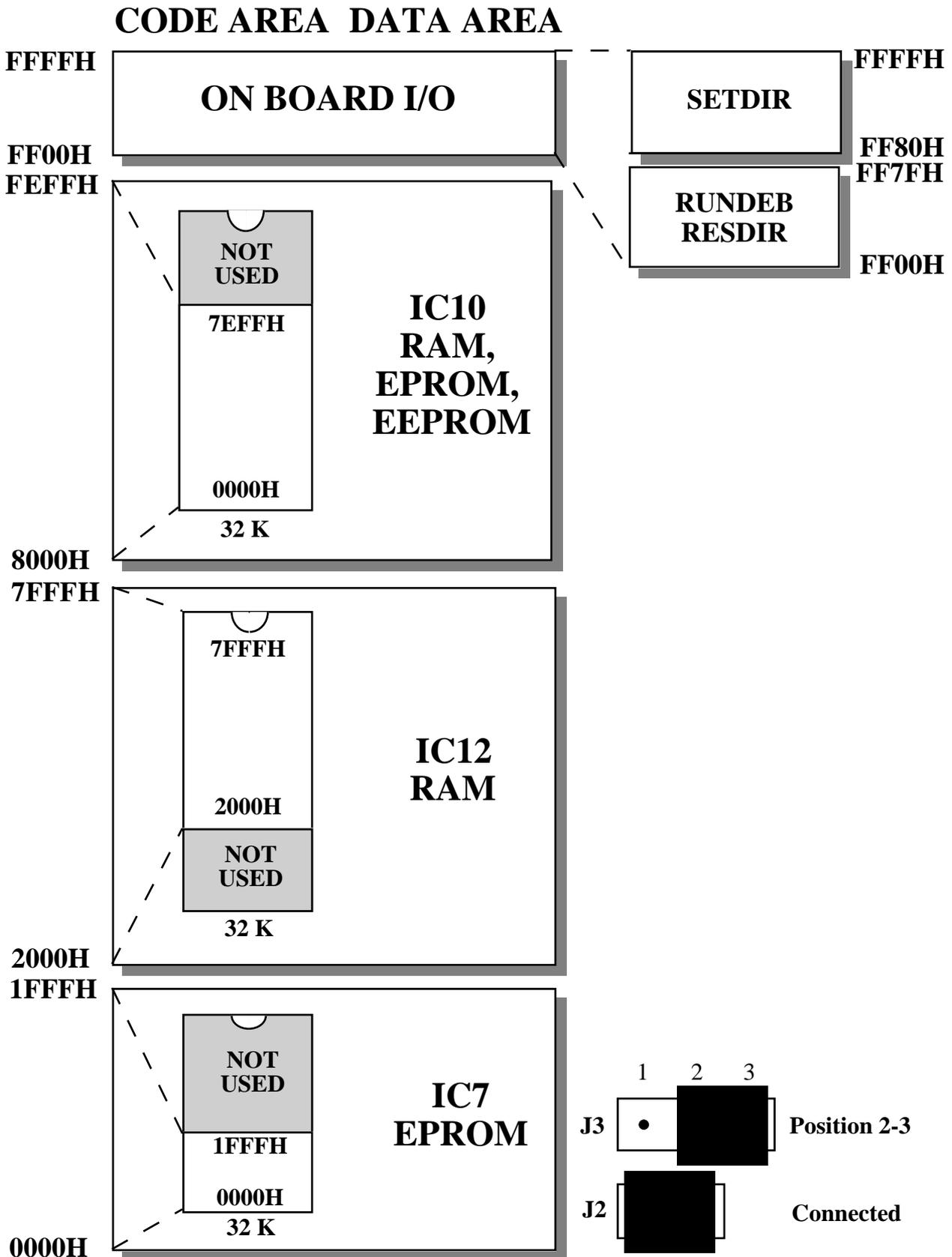
FIGURE 30: MODE 3 MEMORY CONFIGURATION (ASM)
Used by software tools as: MDP; LUCIFER HI TECH C; DDS MICRO C; NO ICE; etc.

PERIPHERAL DEVICES SOFTWARE DESCRIPTION

In the previous paragraphes are described the external registers addresses, while in this one there is a specific description of registers meaning and function (please refer to figure 24, for the registers name). For microprocessor internal peripheral devices, not described in this paragraph, or for further information, please refer to manufacturing company documentation.

SERIAL RAM+RTC

For software management of serial RAM+RTC module PCF8583, please refer to specific documentation or to demo programs supplied with the card. The user must realize a serial communication with I²C bus standard protocol, through two I/O microprocessor pins. The only necessary information is the electric connection:

Data line	(SDA)	->	pin 4 of the CPU =	P1.2
Clock line	(SCL)	->	pin 5 of the CPU =	P1.3
Interrupt line	(INT)	->	pin 15 of the CPU =	P3.3 = /INT1
Address line	(A0)	->	GND (0 logic state)	

The RAM+RTC interrupt line shares the same microprocessor signal of IN3 optocoupled input, so the user must correctly manage this condition, when both the resources are contemporaneously used. After a **GPC® R/T63** reset or power on, the RTC drives the interrupt line with an 1 Hz square wave signal for calibration. This functionality can be disabled by software, setting the real time clock interrupt management (alarm and count mode) and connecting the back up battery.

DIGITAL INPUTS

As previously described, the 6 optocoupled inputs status can be acquired by software, through a simple read operation of the indirectly connected microprocessor pins. The corrispondence between inputs and pins is as follows:

IN0	->	pin 2 of the CPU =	P1.0 = T2
IN1	->	pin 3 of the CPU =	P1.1 = T2EX
IN2	->	pin 14 of the CPU =	P3.2 = /INT0
IN3	->	pin 15 of the CPU =	P3.3 = /INT1
IN4	->	pin 16 of the CPU =	P3.4 = T0
IN5	->	pin 17 of the CPU =	P3.5 = T1

When the inputs INn is connected to GND opto, the relative LED is turned on and the CPU pin is set at logic status **0**. Viceversa when the inputs INn is open, the relative LED is turned off and the CPU pin is set at logic status **1**.

The used CPU pins have been carefully selected to simplify the software management; in fact they can generate interrupts, they can be counted through the counters or they can be simply acquired with input instructions. This feature is really important , in fact optocoupled digital signals can be counted or they can generate interrupt for a fast event response. The RAM+RTC interrupt line shares the same microprocessor signal of IN3 optocoupled input, so the user must correctly manage this condition, when both the resources are contemporaneously used.

DIGITAL OUTPUTS

The 3 relays or transistor outputs status can be defined by software, through a simple write operation of the indirectly connected microprocessor pins. The corrispondence between inputs and pins is as follows:

OUT0   ->   pin 7 of the CPU =   P1.5
OUT1   ->   pin 8 of the CPU =   P1.6
OUT2   ->   pin 9 of the CPU =   P1.7

When the CPU pin is set low (logic status **0**) the relative LED is turned on and the output OUTn is connected to COMMONn. Viceversa when the CPU pin is set high (logic status **1**) the relative LED is turned off and the output OUTn is not connected to COMMONn.
Output CPU pins are set (1) after a reset or power on of the card, to mantain the digital outputs not connected.

ON BOARD INPUTS: J1 (RUN/DEBUG)

The on board J1 status can be obtained by software, through a simple read operation at the RUNDEB register address. The corrispondence between register bits and J1 status is as follows:

D0÷D6   ->   Reserved
D7   ->   J1 status (RUN/DEBUG)

Remember that if the jumper is connected the read logic status is **0** and if the jumper is not connected the read logic status is **1**.

DIR SIGNAL

On CN3 connector of **GPC® R/T63** is available a TTL digital output signal named DIR that can be driven by software and can be used to define the RS 485 line direction, to enable the RS 422 transmit drive or to generate an RS 232 handshake (remember that possible RS 485, RS 422 RS 232 drivers must be externally connected). The DIR line is driven by software as below described:

Read operation at the RESDIR register address   ->   DIR = 0
Read operation at the SETDIR register address   ->   DIR = 1

Both the reading operations return an 8 bits data with no meaning for the DIR signal status. Please note that the RUNDEB register shares the same addresses of RESDIR register; for this reason an acquire operation of J1 (RUN/DEBUG) user inputs will reset the DIR signal, too.
DIR signal is reset (0) after a reset or power on of the card, to avoid any possible conflict.

UART; TIMER/COUNTER; INTERNAL WATCH DOG

For further information, please refer to specific documentation of the microprocessor manufacturing company.
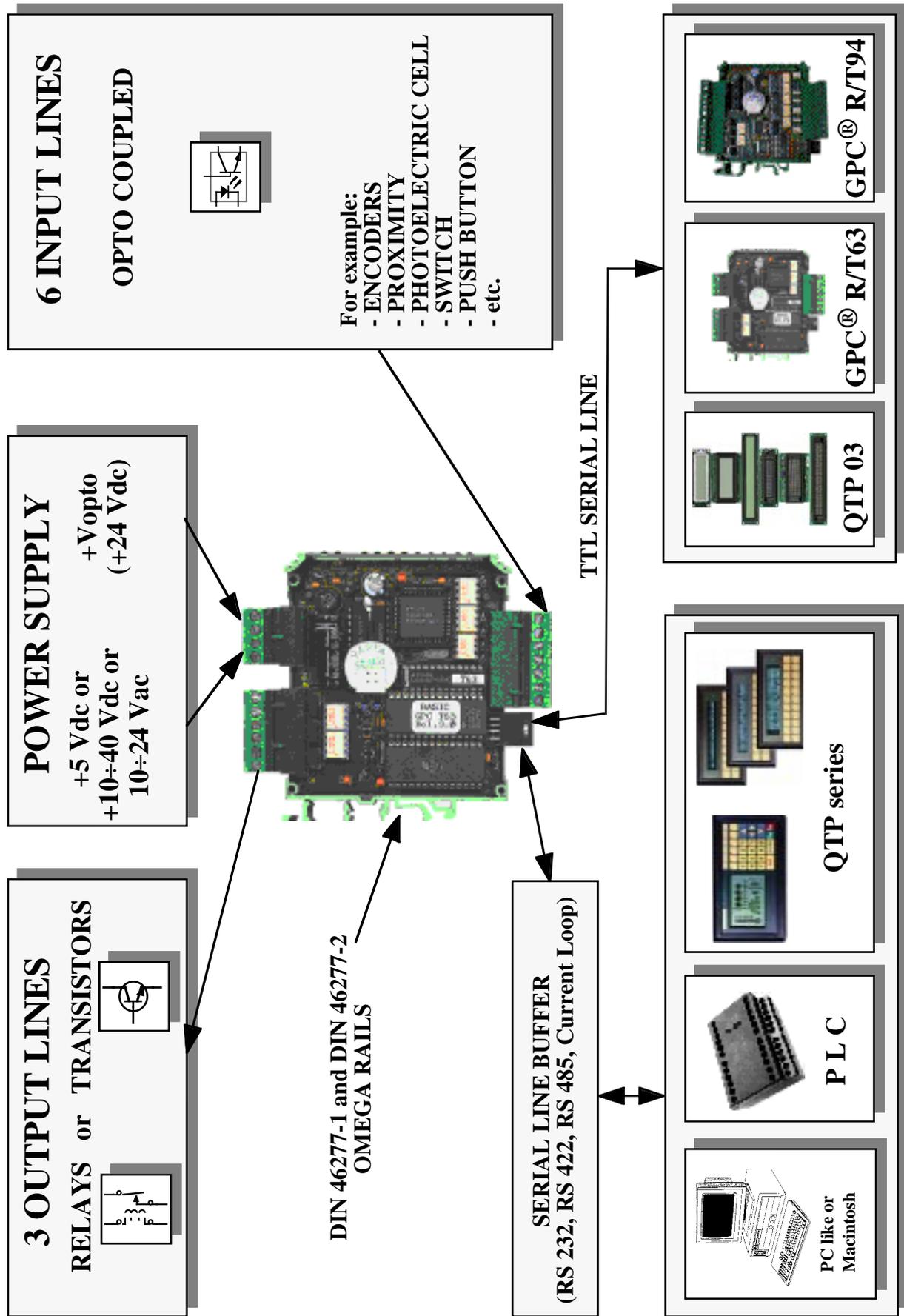
FIGURE 31: GPC® R/T63 AVAILABLE CONNECTIONS DIAGRAM

BIBLIOGRAPHY

In this chapter there is a complete list of technical books, where the user can find all the necessary documentations on the components mounted on **GPC® R/T63**.

Data book TEXAS INSTRUMENTS: *The TTL Data Book - SN54/74 Families*
Data book TEXAS INSTRUMENTS: *Linear Circuits Data Book - Vol. 1 and 3*

Data book NEC: *Memory Products*

Data book PHILIPS: *80C51 - Based 8 Bit Microcontrollers*
Data book PHILIPS: *I²C-bus compatible ICs*

Data book DALLAS SEMICONDUCTOR: *1992-1993 Product Data Book Supplement*

Data book INTEL: *8 Bit Embedded Microcontrollers*

Data book ATMEL: *Microcontrollers - AT89S series*

Data book TOSHIBA: *Mos Memory Products*
Data book TOSHIBA: *Photo couplers - Data Book*

Data book MOTOROLA: *Bipolar Power Transistor Data*

Data book NATIONAL SEMICONDUCTOR   *Programmable Logic Design Guide*

For further information and upgrades please refer to specific internet web pages of the manufacturing companies.

APPENDIX A: SERIAL LINE BUFFER

IC1 = SN 75176 driver
IC2 = SN 75176 driver
J1 = 5 pins jumper
J2,J3,J4,J5 = 2 pins jumpers
C1 = 100 nF multi layered capacitor
R1,R3,R4,R6 = 3,3KΩ, 1/4 W resistor

IC1
SN 75176
Gnd Vcc

J1
DIR

C1 +5V

IC2
75176
SN
Gnd Vcc

+5V R1 J2 RX+ 422 TX+RX+ 485
R2 RX- 422 TX-RX- 485
J3 R3

+5V R4 J4 TX- 422
R5 TX+ 422
J5 R6

IC3 = HP 4200 driver
IC4 = HP 4100 driver
C2 = 100 nF multi layered capacitor

RxD
+5V IC3 RX 4200 RX+ CL
C2 RX- CL
TxD TX 4100 IC4 TX+ CL
TX- CL

IC5 = MAX 232 driver
C3,C4,C5,C6,C7 = 22μF 16V tantalum capacitor

+5V C3 C4 IC5
MAX232
TIN ROUT TX 232
TOUT RIN
TIN ROUT RX 232
TOUT RIN
C+ C+
C- C-
C5 C7
C6

| Titolo: BUFSER	**grifo®**
Data: 26-03-1999	Rel. 1.1
Pagina : 1 of 1	

FIGURE A-1: SERIAL LINE BUFFER ELECTRIC DIAGRAM

In previous page is reported an electric circuit diagram that can be used to buffer the **GPC® R/T63** TTL serial line. The diagram shows the most used standard electric protocol, as RS 232, RS 422, RS 485 and current loop. In details:

- SERIAL LINE CONFIGURED IN RS 232

			IC 1	=	no component
J1	=	not connected	IC 2	=	no component
J2, J3	=	not connected	IC 3	=	no component
J4, J5	=	not connected	IC 4	=	no component
			IC 5	=	MAX 232 driver

- SERIAL LINE CONFIGURED IN CURRENT LOOP

			IC 1	=	no component
J1	=	not connected	IC 2	=	no component
J2, J3	=	not connected	IC 3	=	HCPL 4200 driver
J4, J5	=	not connected	IC 4	=	HCPL 4100 driver
			IC 5	=	no component

The current loop serial line is a passive line, so during connection the user must provide an external power supply.

- SERIAL LINE CONFIGURED IN RS 422

			IC 1	=	SN 75176 driver
J1	=	position 1-2 and 3-4	IC 2	=	SN 75176 driver
J2, J3	=	(*)	IC 3	=	no component
J4, J5	=	(*)	IC 4	=	no component
			IC 5	=	no component

With DIR signal the user enables or disables the transmitter driver:

> DIR = low level = 0 logic state   -> transmitter driver disabled
> DIR = high level = 1 logic state   -> transmitter driver enabled

allowing either point to point (driver can be mantained always enabled) or network (driver is enabled only when the unit can hold the line) connection.

- SERIAL LINE CONFIGURED IN RS 485

			IC 1	=	SN 75176 driver
J1	=	position 2-3 and 4-5	IC 2	=	no component
J2, J3	=	(*)	IC 3	=	no component
J4, J5	=	not connected	IC 4	=	no component
			IC 5	=	no component

With DIR signal the user defines the RS 485 line direction:

> DIR = low level = 0 logic state   -> RS 485 line receiving
> DIR = high level = 1 logic state   -> RS 485 line transmitting

allowing network connection in a master multi slave system and multi master system. All the transmitted characters are at the same time received when the user select RS 485; in this way the line conflict can be immediately recognized simply testing the received character after each transmission.

(*) With jumper J2, J3 and J4, J5 the RS 422 receiving line or the RS 485 line can be terminated and forced with a suitable resistor circuit. The line termination must be added only at the beginning and at the end of the physical line, connecting both the jumpers. Normally these jumper must be connected in point to point network, or on the farther cards in multipoint network.
For further information please contact directly **grifo®** technicians.

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