GPC® 884

General Purpose Controller Am188ES 4 type

TECHNICAL MANUAL

Intelligent Abaco® BLOCK module, 4 serie, 100x50 mm size; optional plastic mount for connection to DIN 46277-1 and DIN 46277-3 Ω rails; 26÷40 MHz 80C188ES CPU; 512K EPROM or FLASH and 512K RAM. Back up circuitry for RAM and RTC through internal and external lithium battery; serial EEPROM up to 8K; jumper readable from software. 2 serial lines in RS232, one configurable in RS422, RS485, with programmable Baud Rate up to 115 Kbaud. 2 independent DMA channels completely software programmable. 16 I/O TTL lines, managed via software (some lines have duplicate function); 11 lines of 12 bits A/D converter, 0÷2,5 or 0÷5 V input range; 4 lines are provided of filter capacitors. Three 16 bits Timer Counter capable to generate pulse defined by software; Real Time Clock able to display day, month, year, week day, seconds, minutes and hours. It can be programmed to issue a INT at software programmed intervals. 26 pins connector for Abaco® I/O BUS; Watch dog resettable by software and power failure circuit that generates interrupt. Very low consumption (160mA) on single 5Vdc power supply; on board protection against voltage peaks by TransZorb™. Wide range of base software and development tools that allow card use with only a standard PC, connected through serial line. Among these: GDOS 188; PASCAL 188; Monitor Debugger; GCTR 884; ROM-DOS; HI TECH C 86; GET 188; FLASH WRITER; DDS MICROC 86; etc.
IMPORTANT

Although all the information contained herein have been carefully verified, grifo® assumes no responsibility for errors that might appear in this document, or for damage to things or persons resulting from technical errors, omission and improper use of this manual and of the related software and hardware.

grifò resves the right to change the contents and form of this document, as well as the features and specification of its products at any time, without prior notice, to obtain always the best product.

For specific informations on the components mounted on the card, please refer to the Data Book of the builder or second sources.

SYMBOLS DESCRIPTION

In the manual could appear the following symbols:

⚠️ Attention: Generic danger

⚡️ Attention: High voltage

Trade marks

GPC®, grifo®: are trade marks of grifo®.
Other Product and Company names listed, are trade marks of their respective companies.
GENERAL INDEX

INTRODUCTION ................................................................................................................... ..... 1
CARD VERSION ..................................................................................................................... 1

GENERAL FEATURES .......................................................................................................... 2
CPU .......................................................................................................................................... 3
MEMORY DEVICES .................................................................................................................. 3
SERIAL COMMUNICATION ..................................................................................................... 4
POWER SUPPLY .................................................................................................................... 4
CLOCK ....................................................................................................................................... 4
ABACO® I/O BUS ..................................................................................................................... 4
DIGITAL I/O LINES .................................................................................................................. 6
REAL TIME CLOCK .................................................................................................................. 6
WATCH DOG ............................................................................................................................ 6
A/D CONVERTER ..................................................................................................................... 6

TECHNICAL FEATURES ......................................................................................................... 8
GENERAL FEATURES ............................................................................................................. 8
PHYSICAL FEATURES ........................................................................................................... 8
ELECTRIC FEATURES ............................................................................................................. 9

INSTALLATION .................................................................................................................... 10
CONNECTIONS .................................................................................................................... 10
CN2 - EXTERNAL BACK UP BATTERY CONNECTOR ................................................................. 10
CN1 - ABACO® I/O BUS CONNECTOR .................................................................................... 11
CN3A - SERIAL LINE A CONNECTOR ...................................................................................... 12
CN3B - SERIAL LINE B CONNECTOR ...................................................................................... 14
CN5 - PIO I/O AND A/D CONVERTER CONNECTOR ............................................................... 18
CN5A - A/D CONVERTER CONNECTOR .................................................................................. 20
DIGITAL I/O INTERFACES ..................................................................................................... 22
RESET CONTACT ................................................................................................................... 22
I/O CONNECTION .................................................................................................................... 23
TRIMMERS AND CALIBRATION ............................................................................................. 23
JUMPERS .................................................................................................................................. 24
2 PINS JUMPERS .................................................................................................................... 26
5 PINS JUMPERS .................................................................................................................... 26
3 PINS JUMPERS .................................................................................................................... 27
BACK UP .................................................................................................................................. 27
RESET AND WATCH DOG ...................................................................................................... 28
INTERRUPTS ............................................................................................................................ 28
SERIAL COMMUNICATION SELECTION .............................................................................. 29
MEMORY SELECTION ............................................................................................................ 30
SOLDER JUMPERS ................................................................................................................... 31
MULTIPLEXED PINS ............................................................................................................... 31
POWER FAILURE ..................................................................................................................... 32
FIGURE INDEX

FIGURE 1: BLOCK DIAGRAM ............................................................................................................. 5
FIGURE 2: CARD PHOTO .................................................................................................................. 7
FIGURE 3: COMPONENTS MAPS (SOLDERING SIDE AND COMPONENTS SIDE) ........................................... 7
FIGURE 4: CN2 - EXTERNAL BACK UP BATTERY CONNECTOR ........................................................... 10
FIGURE 5 CN1 - ABACO® I/O BUS CONNECTOR ........................................................................ 11
FIGURE 6: CN3A- SERIAL line A Connector ....................................................................................... 12
FIGURE 7: SERIAL COMMUNICATION DIAGRAM ................................................................................. 13
FIGURE 8: CN3B- SERIAL line B Connector .......................................................................................... 14
FIGURE 9: RS 232 PIN OUT AND CONNECTION EXAMPLE .......................................................... 15
FIGURE 10: RS 422 PIN OUT AND POINT TO POINT CONNECTION EXAMPLE ......................................... 15
FIGURE 11: RS 485 PIN OUT AND POINT TO POINT CONNECTION EXAMPLE ......................................... 15
FIGURE 12: RS 485 PIN OUT AND NETWORK CONNECTION EXAMPLE ................................................ 16
FIGURE 13: CONNECTORS, MEMORIES, TRIMMER, BATTERY, ETC. LOCATION ...................................... 17
FIGURE 14: CN5 - PIO I/O AND A/D CONVERTER CONNECTOR ......................................................... 18
FIGURE 15: PIO I/O SIGNALS CONNECTION DIAGRAM ..................................................................... 19
FIGURE 16: CN5A - A/D CONVERTER CONNECTOR ............................................................................ 20
FIGURE 17: A/D CONVERTER INPUTS DIAGRAM ................................................................................ 21
FIGURE 18: JUMPERS SUMMARIZING TABLE ..................................................................................... 24
FIGURE 19: JUMPERS LOCATION ........................................................................................................ 25
FIGURE 20: 2 PINS JUMPERS TABLE ................................................................................................. 26
FIGURE 21: 5 PINS JUMPERS TABLE .................................................................................................. 26
FIGURE 22: 3 PINS JUMPERS TABLE .................................................................................................. 27
FIGURE 23: MEMORY SELECTION TABLE .......................................................................................... 30
FIGURE 24: MULTIPLEXED PIN TABLE ............................................................................................... 31
FIGURE 25: STATUS OF CN5 SIGNALS DURING POWER ON OR RESET ............................................... 32
FIGURE 26: DEVICES HARDWARE CONNECTION TABLE ..................................................................... 35
FIGURE 27: I/O ADDRESSES TABLE .................................................................................................. 36
FIGURE 28: MEMORY ALLOCATION .................................................................................................... 38
FIGURE 29: AVAILABLE CONNECTIONS DIAGRAM .......................................................................... 43
FIGURE A1: MEMORY JUMPERS LOCATION ...................................................................................... A-1
FIGURE A2: SERIAL COMMUNICATION JUMPERS LOCATION ............................................................... A-1
FIGURE A3: SERIAL COMMUNICATION DRIVERS LOCATION ............................................................... A-2
FIGURE C1: MODULE DIMENSION FOR PIGGY BACK MOUNTING ................................................... C-1
FIGURE C2: PIGGY BACK MOUNTING ............................................................................................... C-2
FIGURE C3: WEIDMULLER RAIL MOUNTING ..................................................................................... C-3
FIGURE D1: PPI EXPANSION ELECTRIC DIAGRAM ........................................................................... D-1
FIGURE D2: SPA 03 ELECTRIC DIAGRAM .......................................................................................... D-2
FIGURE D3: QTP 16P ELECTRIC DIAGRAM ....................................................................................... D-3
FIGURE D4: QTP 24P ELECTRIC DIAGRAM (1 OF 2) .......................................................................... D-4
FIGURE D5: QTP 24P ELECTRIC DIAGRAM (2 OF 2) .......................................................................... D-5
FIGURE D6: IAC 01 ELECTRIC DIAGRAM .......................................................................................... D-6
FIGURE D7: ABACO® I/O BUS INPUT OUTPUT ELECTRIC DIAGRAM ............................................. D-7
FIGURE D8: BUS INTERFACE ELECTRIC DIAGRAM .......................................................................... D-8
INTRODUCTION

The use of these devices has turned - IN EXCLUSIVE WAY - to specialized personnel.

The purpose of this handbook is to give the necessary information to the cognizant and sure use of the products. They are the result of a continual and systematic elaboration of data and technical tests saved and validated from the manufacturer, related to the inside modes of certainty and quality of the information.

The reported data are destined- IN EXCLUSIVE WAY- to specialized users, that can interact with the devices in safety conditions for the persons, for the machine and for the environment, impersonating an elementary diagnostic of breakdowns and of malfunction conditions by performing simple functional verify operations, in the height respect of the actual safety and health norms.

The informations for the installation, the assemblage, the dismantlement, the handling, the adjustment, the reparation and the contingent accessories, devices etc. installation are destined - and then executable - always and in exclusive way from specialized warned and educated personnel, or directly from the TECHNICAL AUTHORIZED ASSISTANCE, in the height respect of the manufacturer recommendations and the actual safety and health norms.

The devices can't be used outside a box. The user must always insert the cards in a container that respect the actual safety normative. The protection of this container is not threshold to the only atmospheric agents, but specially to mechanic, electric, magnetic, etc. ones.

To be on good terms with the products, is necessary guarantee legibility and conservation of the manual, also for future references. In case of deterioration or more easily for technical updates, consult the AUTHORIZED TECHNICAL ASSISTANCE directly.

To prevent problems during card utilization, it is a good practice to read carefully all the informations of this manual. After this reading, the user can use the general index and the alphabetical index, respectly at the begining and at the end of the manual, to find information in a faster and more easy way.

CARD VERSION

The present handbook is reported to the GPC® 884 card release 250699 and later. The validity of the bring informations is subordinate to the number of the card release. The user must always verify the correct correspondence among the two denotations. On the card the release number is present in more points both board printed diagram (serigraph) and printed circuit (for example between the CPU an the memory devices on the component side).
GENERAL FEATURES

The GPC® 884 belongs to the CPUs 4 Serie 100x50 mm. size, and it is a powerful control low cost module capable of operating in stand alone mode or as an intelligent peripheral, and/or remoted, in a wider telecontrol or acquisition network. The GPC® 884 module is secured in a plastic mount for connection to Omega rails DIN 46277-1 and DIN 46277-3, thereby dispensing with the need of rack and allowing a cheaper mounting direct to the electrical control panel. Thanks to its small size, the GPC® 884 can be inserted into the same plastic rails that contains the peripheral I/O, i.e ZBR 168, forming in this way an unique BLOCK element. Another application of this GPC® 884 is that when it is used as CPU it can be mounted in Piggy Back, on the peripheral cards of the end user. The GPC® 884 is based on the powerful and notorious CPU 80C188ES AMD, code compatible with any PC that includes considerable hardware resources. The 11 lines of 12 bits high performances A/D converter are particularly interesting. Its modularity and the remarkable hardware resources allow this card to easily solve even complex applications. The card use is simplified by a wide range of software development tools with high level languages which, in an efficient and friendly environment, allow to work at the best using a standard PC. Noteworthy among these tools is the operating system GDOS 188 in conjunction with an efficient PASCAL romated compiler and the tools that allow to romate what has been developed by the standard Borland C compiler, available on the PC. Special care has been devoted to the difficult operation of develop and debugger, by programs which allow the remote symbolic debugger directly on the card, with almost the same characteristics as Borland Turbo Debugger.

For getting a quick prototype it is possible to use SPA 03 and SPA 04 cards on which it is possible to mount, in Piggy Back mode, the GPC® 884 card. The Abaco® I/O BUS connector allows to drive directly the ZBR xxx and ZBT xxx cards and through ABB 03, ABB 05 and so on, it is possible to run all peripheral cards available on Abaco® BUS.

- Intelligent Abaco® BLOCK module, 4 serie, 100x50 mm size.
- Optional plastic mount for connection to DIN 46277-1 and DIN 46277-3 Ω rails.
- 26÷40 MHz 80C188ES CPU; 512K EPROM or FLASH and 512K RAM.
- Back up circuitry for RAM and RTC through internal and external lithium battery.
- Serial EEPROM up to 8K. Jumper readable from software.
- 2 serial lines in RS232, one configurable in RS422, RS485, with programmable Baud Rate up to 115 Kbaud.
- 2 independent DMA channels completely software programmable.
- 16 I/O TTL lines, managed via software (some lines have duplicate function).
- 11 lines of 12 bits A/D converter, 0÷2,5 or 0÷5 V input range; 4 lines are provided of filter capacitors.
- Three 16 bits Timer Counter capable to generate pulse defined by software.
- Real Time Clock able to display day, month, year, week day, seconds, minutes and hours. It can be programmed to issue a INT at software programmed intervals.
- 26 pins connector for Abaco® I/O BUS.
- Watch dog resettable by software and power failure circuit that generates interrupt.
- Very low consumption (160mA) on single 5Vdc power supply.
- On board protection against voltage peaks by TransZorb™.
- Wide range of base software and development tools that allow card use with only a standard PC, connected through serial line. Among these: GDOS 188; PASCAL 188; Monitor Debugger: GCTR 884; ROM-DOS; HI TECH C 86; GET 188; FLASH WRITER; DDS MICROC 86; etc.
Here follows a description of the board's functional blocks, with an indication of the operations performed by each one. To easily locate these blocks and verify their connections please refer to figure 1.

**CPU**

**GPC® 884** board is designed to employ the **Am 188ES** microcontroller manufactured by **AMD**. This 16 bits CPU is code compatible with Intel 86 family so it features: an extended instructions set, high speed of execution, efficient vectored interrupts management, wide range of addressing modes and interesting data manipulation techniques. Remarkable is the presence of these peripherals inside the CPU:

- Two 16 bits timers counter and one 16 bits timer (TCU), capable to generate and to measure (PWD) pulse with modulation signals;
- Two asynchronous serial lines provided of handshake signals (ASP);
- Two DMA channels for high speed data transfers (DMAU);
- One interrupt controller (ICU);
- One power management section (CPMU);
- One section that generates control signal for peripheral devices management (CSU), with programmable wait states generator;
- 32 I/O lines driven by software (PIO);
- Idle and Stop modes, to reduce power consumption;

For further informations about this component please refer to the manufacturer documentation, or see appendix B of this manual.

**MEMORY DEVICES**

On the card can be mounted 1032K bytes of memory divided with a maximum of 512K EPROM or FLASH EPROM, 512K static RAM and 8K serial EEPROM. The **GPC® 884** memory configuration must be chosen considering the application to realize or the specific requirements of the user. Normally the card is equipped with 128K bytes of static RAM plus 512 bytes of serial EEPROM and all different configurations must be specified from the user, at the moment of the order.

With the on board back up circuit there is the possibility to keep data, also when power supply is failed; in this way the card is always able to maintain parameters, logged data, system status and configuration, etc. without using expensive external UPS. The back up circuit is supplied by a on board lithium battery or an external battery to be connected to a specific connector.

The addressing of memory devices is controlled by a specific microprocessor section (Chip Select Unit), that provides to allocate the devices in the microprocessor address space; this CSU automatically manages the different addressing mode and it satisfies the requests of each **GPC® 884** software tools.

For further information about memory configuration, sockets description and jumpers connection, please refer to "Addresses and Maps" chapter and to "Memory Selection" paragraph.
SERIAL COMMUNICATION

Serial communication is completely software settable for protocol and for speed (which ranges from 50 to as high as 115,2K Baud with both the available clock frequency) in a separate manner for each one of the two lines. These settings are performed programming the ASP inside the microprocessor, so for further informations, please refer to the manufactuer documentation or to appendix B of this manual. By hardware it is possible to select, through some on board jumpers, the electric communication protocol. In detail, one line is always buffered as RS 232, while the other line can be buffered in three different electrical protocols: RS 232, RS 485 or RS 422; in this last cases also directionality and line activation is programmable.

POWER SUPPLY

The card must be powered only with +5 Vdc through the pin 25 (GND) and pin 26 (+5Vdc) of the CN1 connector. The power supply circuit generates all the necessary voltages for the card and it is designed for reducing the consumption (the microprocessor power down modes are available) and for increasing the electrical noise immunity. In fact, as low as 160 mA of consumption for the normal working mode, allow the user to supply the board by batteries, solar panels, small power supplies, etc. An interesting power failure circuitry capable to detect the imminent power black out is installed on the board, so it can start a software intervent routine by generating an interrupt. Please remember that on board there is a protection circuit against voltage peaks by TransZorb™.

CLOCK

GPC® 884 is provided with a circuitry that generates the CPU clock frequency; this frequency is used also to generate the frequencies needed to the other sections of the board (Timer, serial lines, DMA etc.). The default clock value is 26,045 MHz but if the user needs to run very fast applications the clock frequency can be increased up to 40,665 MHz. The clock frequency selection must be specified during the order phase of the card, in fact it requires an hardware intervent on the proper circuit (for more informations please contact grifo®). We would remark that the CPU clock frequency normally coincides with the crystal oscillation frequency and it can also be divided by software through the power management section.

ABACO® I/O BUS

One of the most important features of GPC® 884 is its possibility to be interfaced to industrial ABACO® I/O BUS. Thanks to this standard connector, the card can be connected to some of the numerous grifo® boards, both intelligent and not. For example the user can directly use cards for analog signals acquisition, cards for analog signals generation (D/A), cards for digital I/O signals management, cards with timers and counters, cards for temperature controls, etc. also custom boards designed to satisfy specific needs of the end user.

Using ABB 03 or ABB 05 mother boards it is possible manage even all the BUS ABACO® single EURO cards. So GPC® 884 becomes the right component for each industrial automation system, in fact ABACO® I/O BUS makes the card easily expandable with the best price/performance ratio.
**Figure 1: Block Diagram**

- **CN3A** Serial Line A
- **CN3B** Serial Line B
- **CN2** External Lithium
- **IC4** Watch-Dog Reset
- **CPU** AM188ES
- **PIO, ICU, TCU, DMA**
- **IC11** Serial EEPROM
- **IC10** A/D TLC 2543
- **CN5** 16 I/O Lines 4 A/D Lines
- **CN5A** 7 Auxiliary A/D Lines
- **CN1** ABACO® I/O Bus
- **IC12** RTC
- **IC13** RAM
- **IC5** EEPROM Flash
- **CN2** External Lithium On Board
- **3V Lithium On Board**
- **CN3A**, **CN3B**, **CN2**, **IC4**, **IC11**, **IC10**, **IC12**, **IC13**, **IC5**, **CN5**, **CN5A**, **CN1**

**Figure 1: Block diagram**
DIGITAL I/O LINES

On the board are available 16 digital I/O signals at TTL level with direction settable for each line, directly managed by the microprocessor. These signals are connected to a 26 pins connector that is compatible with the standard I/O ABACO® 20 pins connector, so the GPC® 884 card can be connected to any of the numerous grifo® boards compliant to the same pinout. By software the functions of these lines can be defined thanks to 6 registers allocated in the microprocessor I/O space. Please remember that the I/O lines can also be connected and used in conjunction with some internal peripheral device, as DMA, Timers Counters, Interrupts, etc.

REAL TIME CLOCK

GPC® 884 board is provided with a complete Real Time Clock device capable to manage hours, minutes, seconds, day of month, month, year and day of week in stand alone mode. The component is supplied by the back up circuitry to warrant data integrity in every working condition and is completely software programmable acting on 16 registers addressable in the CPU I/O space by a specific control logic (CSU). The RTC section can generate interrupts at software programmable rates, for diverting the CPU from its normal tasks or awakening it from one of its low consumption working modes.

WATCH DOG

GPC® 884 board is provided with a watch dog circuitry that, if used, allows to exit from infinite loop or abnormal conditions not managed by the application program. This circuitry is made by an astable section with 1400 msec intervent time, it is completely software managed (by accessing a register addressed in the CPU addressing space) and gives the board an exterme degree of safety.

A/D CONVERTER

The A/D section of GPC® 884 is based on a converter with 11 input channels with 12 bits max resolution. By software the user selects the channel to convert, starts and stops the conversion, defines the returned data format, reduce power consumption, etc., through the management of a synchronous communication with the device. It is possible to simplify the management of A/D conversion in all its parts by using software tools already designed for this purpose. The analog voltage input can be in the range 0÷2,490V or 0÷5,000 V as specified in "TRIMMER AND CALIBRATION" paragraph.

Four of the eleven input analog lines are provided of a filter capacitor that increases the noisy immunity and data stability.
Figure 2: Card Photo

Figure 3: Components Maps (soldering side and components side)
TECHNICAL FEATURES

GENERAL FEATURES

Devices:
- 16 digital TTL input output lines (PIO)
- Two 16 bit timers counter (TCU)
- One 16 bits timers (TCU)
- 2 DMA channels (DMAU)
- 1 RS 232 serial line (ASP 1=A)
- 1 RS 232, RS 422, RS 485 serial line (ASP 0 =B)
- 11 A/D converter lines
- 1 reset contact
- 1 astable hardware watch dog
- 1 real time clock
- 1 configuration jumper
- 1 **ABACO®** I/O BUS interface
- 1 power failure circuitry

Memory:
- IC 5: EPROM from 128K x 8 to 512K x 8
- FLASH EPROM from 128K x 8 to 512K x 8
- IC 13: RAM from 128K x 8 to 512K x 8
- IC 11: serial EEPROM from 256 to 8K

CPU:
- AMD Am188ES

Clock frequency:
- 26,045 or 40,665 MHz

A/D resolution:
- 12 bits

A/D conversion time:
- 10 µsec

Watch dog intervent time:
- from 940 to 2060 msec (typical 1420 msec)

PHYSICAL FEATURES

Size (W x H x D):
- 100 x 50 x 25 mm (without container)
- 110 x 60 x 60 mm (with DIN rails container)

Weight:
- 66 g (without container)
- 126 g (with DIN rails container)

Connectors:
- CN1: 26 pins, male, vertical, low profile connector
- CN2: 2 pins, male, vertical, low profile connector
- CN3A: 6 pins, Plug, female
- CN3B: 6 pins, Plug, female
- CN5: 26 pins, male, vertical, low profile connector
- CN5A: 4+4 pins, male, vertical, strip connector
Temperature range: from 0 to 50 Centigrade degrees

Relative humidity: 20% up to 90% (without condens)

ELECTRIC FEATURES

Power Supply: +5 Vdc

Consumption on 5 Vdc: 160 mA in default configuration (26,045 MHz)
220 mA in default configuration (40,665 MHz)

On board back up battery: 3,0 Vdc; 180 mAh

External back up battery: 3,6±5 Vdc

Back up current: 3,5 µA (on board battery)
4,5 µA (external 3,6V battery)

Analog inputs: 0±2,490 V or 0±5,000 V

Analog inputs impedance: 1 KΩ

RS 422, RS 485 line termination: Line termination resistance= 120 Ω
Positive pull-up resistance= 3,3 KΩ
Negative pull-up resistance= 3,3 KΩ

Power failure intervent threshold: 52 mV before reset activation
INSTALLATION

In this chapter there are the information for a right installation and correct use of the card. The user can find the location and functions of each connectors, trimmers, jumpers and some explanatory diagrams.

CONNECTIONS

The GPC®884 module has 6 connectors that can be linkeded to other devices or directly to the field, according to system requirements. In this paragraph there are connectors pin outs, a short signals description (including the signals direction) and connectors location (see figure 13), plus some figures that describe how the interface signals are connected on the card.

CN2 - EXTERNAL BACK UP BATTERY CONNECTOR

CN2 is a 2 pins, vertical, male connector with 2,54mm pitch. Through CN2 the user can connect an external battery for RAM and RTC back up when the power supply is switched off (for further information please refer to "BACK UP" and "ELECTRIC FEATURES" paragraphs).

Signals description:

<table>
<thead>
<tr>
<th>Signal</th>
<th>Pin</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>+Vbat</td>
<td>1</td>
<td>Positive pin of external back up battery</td>
</tr>
<tr>
<td>GND</td>
<td>2</td>
<td>Negative pin of external back up battery</td>
</tr>
</tbody>
</table>
CN1 - ABACO® I/O BUS CONNECTOR

CN1 is a 26 pins, male, vertical, low profile connector with 2.54 mm pitch. Through CN1 the card can be connected to external expansion modules developed by the user or to the numerous grifo® boards, both intelligent and not. All this connector signals are at TTL level and follows the ABACO® I/O BUS standard.

Signals description:

<table>
<thead>
<tr>
<th>Signal</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A0-A7</td>
<td>O</td>
<td>Address BUS.</td>
</tr>
<tr>
<td>D0-D7</td>
<td>I/O</td>
<td>Data BUS.</td>
</tr>
<tr>
<td>/INT BUS</td>
<td>I</td>
<td>Interrupt request (open collector type).</td>
</tr>
<tr>
<td>/NMI BUS</td>
<td>I</td>
<td>Non maskable interrupt (open collector type).</td>
</tr>
<tr>
<td>/IORQ</td>
<td>O</td>
<td>Input output request.</td>
</tr>
<tr>
<td>/RD</td>
<td>O</td>
<td>Read cycle status.</td>
</tr>
<tr>
<td>/WR</td>
<td>O</td>
<td>Write cycle status.</td>
</tr>
<tr>
<td>/RESET</td>
<td>O</td>
<td>Reset.</td>
</tr>
<tr>
<td>+5 Vdc</td>
<td>I/O</td>
<td>+5 Vdc power supply.</td>
</tr>
<tr>
<td>GND</td>
<td></td>
<td>Ground signal.</td>
</tr>
<tr>
<td>N.C.</td>
<td></td>
<td>Not connected</td>
</tr>
</tbody>
</table>

FIGURE 5 CN1 - ABACO® I/O BUS CONNECTOR
CN3A - SERIAL LINE A CONNECTOR

CN3A is a 6 pins, female PLUG connector for serial communication. Physically, serial line A of GPC® 884 board is connected to the ASP 1 serial line of the CPU. Placing of the signal has been designed to reduce interference and electrical noise and to simplify connections with other systems, while the electric protocol follows the CCITT normative.

Signals description:

RXA RS 232 = I - Serial line A=ASP 1 RS 232 Receive Data.
TXA RS 232 = O - Serial line A=ASP 1 RS 232 Transmit Data.
CTSA RS 232 = I - Serial line A=ASP 1 RS 232 Clear To Send (*1).
RTSA RS 232 = O - Serial line A=ASP 1 RS 232 Request To Send (*1).
+5 Vdc/GND = I - +5 Vdc power supply or ground signal
GND = Ground signal

*1: The handshake signals RTSA and CTSA are connected to the proper microprocessor signals with two jumpers. For further information please refer to serial communication selection paragraph.
FIGURE 7: SERIAL COMMUNICATION DIAGRAM
CN3B - SERIAL LINE B CONNECTOR

CN3B is a 6 pins, female PLUG connector for serial line B, that can be buffered as RS 232, RS 422 or RS 485. Physically, serial line B of GPC® 884 board is connected to the ASP 0 serial line of the CPU. Placing of the signal has been designed to reduce interference and electrical noise and to simplify connections with other systems, while the electric protocol follows the CCITT normative.

.signals description:

RXB RS 232  =  I - Serial line B=ASP 0 RS 232 Receive Data.
TXB RS 232  =  O - Serial line B=ASP 0 RS 232 Transmit Data.
CTSB RS 232 =  I - Serial line B=ASP 0 RS 232 Clear To Send.
RTSB RS 232 =  O - Serial line B=ASP 0 RS 232 Request To Send.
RXB- RS 422 =  I - Receive Data Negative: Serial line B=ASP 0 negative signal for RS 422 serial differential receive.
RXB+ RS 422 =  I - Receive Data Positive: Serial line B=ASP 0 positive signal for RS 422 serial differential receive.
TXB- RS 422 =  O - Transmit Data Negative: Serial line B=ASP 0 negative signal for RS 422 serial differential transmit.
TXB+ RS 422 =  O - Transmit Data Positive: Serial line B=ASP 0 positive signal for RS 422 serial differential transmit.
RXTXB- RS 485 =I/O- Receive Transmit Data Negative: Serial line B=ASP 0 negative signal for RS 485 serial differential receive and transmit.

FIGURE 8: CN3B- SERIAL LINE B CONNECTOR
RXTXB+ RS 485 = I/O- Receive Transmit Data Positive: Serial line B=ASP 0 positive signal for RS 485 serial differential receive and transmit.

+5 Vdc/GND = I - +5 Vdc or ground signal.
GND = - Ground signal.

**Figure 9: RS 232 Pin Out and Connection Example**

**Figure 10: RS 422 Pin Out and Point to Point Connection Example**

**Figure 11: RS 485 Pin Out and Point to Point Connection Example**
An RS 485 network must be forced with a suitable pair of resistors connected on a single point and it must be terminated only at the beginning and at the end of the physical line, near the master unit and near the farther slave unit.

On GPC® 884 there are both the force and termination circuits that can be connected or disconnected through two specific jumpers, as described in the following paragraphs.

Please remember to connect the termination resistor near the master unit, if only it is not already available inside the same unit. In fact many RS 422 and RS 485 interfaces have this feature.

For further informations please refer to “RS 422 and RS 485 Interface Circuits” data book, by TEXAS INSTRUMENTS.
FIGURE 13: CONNECTORS, MEMORIES, TRIMMER, BATTERY, ETC. LOCATION
CN5 - PIO I/O AND A/D CONVERTER CONNECTOR

CN5 is a 26 pins, male, vertical, low profile connector with 2.54 mm pitch. CN5 connects the 16 PIO digital I/O lines (and pertinent internal peripheral devices), plus 4 of the 11 A/D converter lines, to the external field signals. All the PIO signals are at TTL level and follows the standard I/O ABACO® pin out, while the A/D lines are voltage analog signals (0±2.490 V or 0±5.000 V) provided of filter capacitors. The lay out of this connector is designed to prevent noise and interference problems and it ensures an excellent signal transmission.

Signals description:

PA.n = I/O - PIO port A digital line n (see "MULTIPLEXED PIN" paragraph).
PC.n = I/O - PIO port C digital line n (see "MULTIPLEXED PIN" paragraph).
ADCn = I - A/D converter analog input n.
AGND = - Analog ground signal.
+5 Vdc = O - +5 Vdc power supply.
GND = - Ground signal.

Figure 14: CN5 - PIO I/O and A/D converter connector
FIGURE 15: PIO i/o SIGNALS CONNECTION DIAGRAM
CN5A - A/D CONVERTER CONNECTOR

CN5A is a 4+4 pins, male, vertical, strip connector with 2.54 mm pitch. CN5A connects 7 of the 11 A/D converter lines, to the external field signals. The A/D lines are voltage analog signals (0÷2,490 V or 0÷5,000 V) not provided of filter capacitors.

Signals description:

\[
\begin{align*}
\text{ADC}_n & \quad = \quad I \quad - \quad \text{A/D converter analog input } n. \\
\text{AGND} & \quad = \quad - \quad \text{Analog ground signal.}
\end{align*}
\]
**Figure 17: A/D Converter Inputs Diagram**

- **IC10 TLC 2543**
- **VRef.**
- **RV1**
- **AN. GND**
- **CN5**
- **CN5A**

Connectors and Channels:
- CH0
- CH1
- CH2
- CH3
- CH4
- CH5
- CH6
- CH7
- CH8
- CH9
- CH10
- CH11
- CH12
- CH13
- VRef.
- RV1

Connections:
- CN5: Connects to CH0, CH1, CH2, CH3
- CN5A: Connects to CH4, CH5, CH6, CH7, CH8, CH9, CH10

**Diagram Details**
- Pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 11, 12, 13 are connected to specific channels as shown.
- CN5 and CN5A are likely connectors for the input channels.
DIGITAL I/O INTERFACES

With CN5 (compatible with standard I/O ABACO® connector) the GPC® 884 can be connected to some of the numerous grifo® boards modules that have the same pin out. The connection of all these external modules is really simple in fact only a 18 ways flat cable, crimped with 20 and 26 pins connector, is necessary. This flat cable connect the power supply too and the user can make it himself or he can order it with the order code FLT.26+20. About software the use of digital I/O interfaces is likewise easy in fact GPC® 884 software tools include proper drivers, library, example, etc. Below there is a brief description of the supported interfaces:

- **QTP 16P, QTP 24P, KDx x24, DEB 01, etc.:** they are usefull local operator panels. These boards already have all the resources (alphanumeric displays, matrix keyboards, LEDs etc) necessary to solve the common man machine communication problems at a short distance from GPC® 884. For software the programmer can use the relative procedure contained in all the GPC® 884 software tools. These procedures normally are software drivers added to the language and they use directly its console instructions (for example WRITE and READ for PASCAL, PRINTF and SCNF for C etc.), so for the user is very simple to write on displays and to get data from keyboards.

- **MCI 64:** it a large mass memory support that can directly manage the PCMCIA memory cards (RAM, FLASH, ROM, etc.) in their available sizes. About software the developed drivers provide an high level managements based on a file system where data are read and write on a memory card disk.

- **IAC 01, DEB 01:** it is an interface for CENTRONICS parallel printer that can be connected with a standard printer cable. The printer is managed by software through the high level instructions of the selected programming language (LPRINT for BASIC, PRINTF for C, WRITE(LST,..) for PASCAL, etc.).

- **RBO xx, TBO xx, XBI xx, OBI xx:** these are buffer interfaces for I/O TTL signals. With these modules the TTL input signals are converted in NPN or PNP optoisolated inputs and the TTL output signals are converted in relays or transistor optoisolated outputs.

For further information about the digital I/O interfaces please read "EXTERNAL CARD" chapter and the software tools documentation.

RESET CONTACT

P1 reset contact of the GPC® 884 board allows the user to reset the board and restarting it in a general clearing condition. The two pins of P1 can be connected to a normally open contact (i.e. a push button) and when the contact is closed (shortcut of the two pins) the reset circuit is enabled. The main purpose of this contact is to come out of infinite loop conditions, useful especially during debug and develop phases, or to ensure a particular initial status. Please see figure 13 for an easy localization of this contact.
I/O CONNECTION

To prevent possible connecting problems between GPC® 884 and the external systems, the user has to read carefully the information of the previous paragraphs and he must follow these instructions:

- For RS 232, RS 422 or RS 485 communication signals the user must follow the standard rules of these protocols.

- For all TTL signals the user must follow the rules of this electric standard. The connected digital signal must be always referred to card digital ground (GND). For TTL signals, the 0 Vdc level corresponds to logic state "0", while 5Vdc level corresponds to logic state "1".

- The analog inputs (A/D section) must be connected to low impedance signals in the following ranges: 0±2,490 V or 0±5,000 V according to selected voltage reference (Vref). Remember that the four analog inputs available on CN5 are provided of filter capacitors that ensure an higher stability of the acquired signals, but reduce at the same time the bandwidth frequency.

TRIMMERS AND CALIBRATION

On GPC® 884 is available a trimmer, named RV1, that calibrates the Vref voltage of the A/D converter section. The GPC® 884 is subjected to a carefull test that verifies and calibrates all the card sections. The calibration is executed in laboratory, with a controlled +20°C room temperature, following these steps:

- The A/D voltage reference (Vref) is calibrated through RV1 trimmer, by using a 5 digits precision multimeter, to a value of +2,4900 Vdc or +5,0000 Vdc. The reference voltage is measured between the pin 14 (Vref) and pin 13 (GND), of IC10 A/D converter.

- The correspondence between the analog input signal and the combination read from A/D is verified. This check is performed with a reference signal connected to A/D inputs and testing that the A/D combination and the theoric combination differ at maximum of the A/D section errors sum.

- The trimmer is blocked with paint.

The analog interfaces use high precision components that are selected during mounting phase to avoid complicate and long calibration procedures. After the calibration, the on board trimmer is blocked with paint to maintain calibration also in presence of mechanic stresses (vibrations, movings, delivery, etc.).

The reference voltage generation circuit defines the full scale value for all the 8 analog inputs, between the two available ranges: 0±2,490 V or 0±5,000 V. The full scale value must be specified at the moment of the order, in fact it requires different components and different calibration. If not stated, the default configuration with a 2,490 V full scale is provided.

The user must not modify the card calibration, but if thermic drifts, time drifts and so on, make necessary a new calibration, the user must strictly follow the previous described procedure.

To recognize trimmer location on GPC® 884, please refer to figure 13.
JUMPERS

On GPC® 884 there are 13 jumpers for card configuration, 10 of them are solder jumpers. Thanks to these jumpers, the user can define for example the memory type and size, the peripheral devices functionality and so on. Below there is the jumpers list, location and function.

<table>
<thead>
<tr>
<th>JUMPERS</th>
<th>PIN N°</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>J1</td>
<td>2</td>
<td>It selects the connection for RUN DEBUG user input.</td>
</tr>
<tr>
<td>J2</td>
<td>5</td>
<td>It selects the device type (EPROM or FLASH EPROM) on IC5.</td>
</tr>
<tr>
<td>J3</td>
<td>2</td>
<td>It selects the size of the RAM device mounted on IC13.</td>
</tr>
<tr>
<td>JS1, JS2</td>
<td>2</td>
<td>They connect the termination and force circuit to RS 422 and RS 485 serial line.</td>
</tr>
<tr>
<td>JS3</td>
<td>3</td>
<td>It selects the connection for pin 1 of CN3A.</td>
</tr>
<tr>
<td>JS4</td>
<td>3</td>
<td>It selects the connection for pin 1 of CN3B.</td>
</tr>
<tr>
<td>JS10</td>
<td>2</td>
<td>It enables the watch dog circuit.</td>
</tr>
<tr>
<td>JS14</td>
<td>2</td>
<td>It connects the on board battery BT1, to back up circuit.</td>
</tr>
<tr>
<td>JS15</td>
<td>3</td>
<td>It selects the serial line B configuration between RS 422 and RS 485 standards.</td>
</tr>
<tr>
<td>JS17</td>
<td>3</td>
<td>It defines the function of CPU pin 63 (/CTS1-PIO18).</td>
</tr>
<tr>
<td>JS18</td>
<td>3</td>
<td>It defines the function of CPU pin 62 (/RTS1-PIO19).</td>
</tr>
<tr>
<td>JS19</td>
<td>3</td>
<td>It connects the power failure circuit.</td>
</tr>
</tbody>
</table>

**Figure 18: JUMPERS summarizing table**

The following tables describe all the right connections of GPC® 884 jumpers with their relative functions. To recognize these valid connections, please refer to the board printed diagram (serigraph) or to figure 3 of this manual, where the pins numeration is listed; for recognizing jumpers location, please refer to figure 19. The "*" used in the following tables, denotes the default connection, or on the other hand the connection set up at the end of testing phase, that is the configuration the user receives.
**Figure 19: Jumpers Location**

- J1
- J2
- J3
- JS1
- JS2
- JS3
- JS4
- JS10
- JS14
- JS15
- JS17
- JS18
- JS19
2 PINS JUMPERS

<table>
<thead>
<tr>
<th>JUMPERS</th>
<th>CONNECTION</th>
<th>FUNCTION</th>
<th>DEF.</th>
</tr>
</thead>
<tbody>
<tr>
<td>J1</td>
<td>not connected</td>
<td>It connects user input to +5Vdc, and it selects the RUN mode.</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>connected</td>
<td>It connects user input to GND, and it selects the DEBUG mode.</td>
<td></td>
</tr>
<tr>
<td>J3</td>
<td>not connected</td>
<td>It configures IC13 socket for 128K Byte RAM.</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>connected</td>
<td>It configures IC13 socket for 512K Byte RAM.</td>
<td></td>
</tr>
<tr>
<td>JS1, JS2</td>
<td>not connected</td>
<td>The termination and force circuit is not connected to RS 422 or RS 485 serial line B.</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>connected</td>
<td>The termination and force circuit is connected to RS 422 or RS 485 serial line B.</td>
<td></td>
</tr>
<tr>
<td>JS10</td>
<td>not connected</td>
<td>It disables the watch dog circuit by hardware.</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>connected</td>
<td>It enables the watch dog circuit by hardware.</td>
<td></td>
</tr>
<tr>
<td>JS14</td>
<td>not connected</td>
<td>The on board battery BT1 is not connected to back up circuit.</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>connected</td>
<td>The on board battery BT1 is connected to back up circuit.</td>
<td></td>
</tr>
</tbody>
</table>

**Figure 20: 2 pins jumpers table**

5 PINS JUMPERS

<table>
<thead>
<tr>
<th>JUMPERS</th>
<th>CONNECTION</th>
<th>FUNCTION</th>
<th>DEF.</th>
</tr>
</thead>
<tbody>
<tr>
<td>J2</td>
<td>position 1-2 and 3-4</td>
<td>It configures IC5 for EPROM.</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>position 2-3 and 4-5</td>
<td>It configures IC5 for FLASH EPROM.</td>
<td></td>
</tr>
</tbody>
</table>

**Figure 21: 5 pins jumpers table**
3 PINS JUMPERS

<table>
<thead>
<tr>
<th>JUMPERS</th>
<th>CONNECTION</th>
<th>FUNCTION</th>
<th>DEF.</th>
</tr>
</thead>
<tbody>
<tr>
<td>JS3</td>
<td>position 1-2</td>
<td>It connects pin 1 of CN3A to GND.</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>position 2-3</td>
<td>It connects pin 1 of CN3A to +5 Vcc.</td>
<td></td>
</tr>
<tr>
<td>JS4</td>
<td>position 1-2</td>
<td>It connects pin 1 of CN3B to GND.</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>position 2-3</td>
<td>It connects pin 1 of CN3B to +5 Vcc.</td>
<td></td>
</tr>
<tr>
<td>JS15</td>
<td>position 1-2</td>
<td>It configures the serial line B for RS 485 (half duplex on 2 wires).</td>
<td></td>
</tr>
<tr>
<td></td>
<td>position 2-3</td>
<td>It configures the serial line B for RS 422 (full duplex or half duplex on 4 wires).</td>
<td></td>
</tr>
<tr>
<td>JS17</td>
<td>position 1-2</td>
<td>It connects pin 63 of the CPU (/CTS1-PIO18) to /CTSA signal.</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>position 2-3</td>
<td>It connects pin 63 of the CPU (/CTS1-PIO18) to pin 9 of CN5 (PC.6).</td>
<td></td>
</tr>
<tr>
<td>JS18</td>
<td>position 1-2</td>
<td>It connects pin 62 of the CPU (/RTS1-PIO19) to /RTSA signal.</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>position 2-3</td>
<td>It connects pin 62 of the CPU (/RTS1-PIO19) to pin 10 of CN5 (PC.7).</td>
<td></td>
</tr>
<tr>
<td>JS19</td>
<td>not connected</td>
<td>The power failure circuit is not connected.</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>position 1-2</td>
<td>The power failure circuit is connected to NMI signal of the CPU.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>position 2-3</td>
<td>The power failure circuit is connected to INT0 signal of the CPU</td>
<td></td>
</tr>
</tbody>
</table>

**Figure 22: 3 pins jumpers table**

BACK UP

GPC® 884 has an on board lithium battery BT1 for the back up of RAM and RTC content when power supply is switched off. Jumper JS14 connects physically the battery so it can be disconnected to save its charge whenever back up is not needed (delivery, stockage, etc.). By CN2 connector it is possible to connect an external battery; configuration of jumper JS14 does not affect the working of this battery and it can replace BT1 completely. Please refer to the paragraph “ELECTRIC FEATURES” to choose the type of the external back up battery, while to easily find the back up components location see figure 9.
RESET AND WATCH DOG

The watch dog circuit of GPC® 884 is really efficient and provided of easy software management. In details the most important features of this circuit are:

- astable functionality;
- intervent time of about 1400 msec;
- hardware enable;
- software retrigger;

With the astable mode when the intervent time elapses, the circuit becomes active, it stay active till the end of reset time (about 200 msec) and after it is deactivated. Jumper JS10 connects the watch dog circuit to reset circuit so when it is connected the watch dog is enabled and viceversa. The watch dog retrigger operation is described in chapter "WATCH DOG".

In addition to watch dog the card /RESET signal is activated also by P1 contact and power good circuit; it is also connected on homonymous pin of CN1 to allow reset condition of the external card too. After an activation and following deactivation of /RESET signal, the card resumes execution of the program saved on IC5 (at address FFFFF0H) starting from a global reset status of all the on board peripheral devices.

INTERRUPTS

One of the most important GPC® 884 features is the powerful interrupts management. Here is a short description of how the board's hardware interrupt signals can be managed; a more complete description of the hardware interrupts can be found in the microprocessor data sheets or in appendix B of this manual.

- **ABACO® I/O BUS** -> It generates an NMI interrupt, by the /NMI BUS signal of CN1 connector.
  It generates an INT0 interrupt, by the /INT BUS signal of CN1 connector.

- **Power failure** -> It generates an NMI or an INT0 interrupt according with JS19 connection.

- **Real Time Clock** -> It generates an INT1 interrupt.

- **A/D converter** -> It generates an INT2, by the PC.5 signal of CN5.
  It generates an INT4, by the PC.4 signal of CN5.

- **PIO** ->

- **CPU inside devices** -> They generate a vectored interrupt. Possible sources of internal interrupt events are: TCU 0, TCU 1, TCU 2, DMAU 0, DMAU 1, ASP 0, ASP 1, software interrupts.

The board has an unit (ICU) that enables, disables, masks and defines priority of all the interrupt sources. The addresses of the interrupt service routines can be software programmed by the user acting on microprocessor memory and inside registers. So the user program has always the possibility to react promptly to every external event, also when more sources are simultaneously active.
SERIAL COMMUNICATION SELECTION

The communication serial line A is always buffered in RS 232 while the serial line B can be buffered in RS 232, RS 422 or RS 485 electric standard. By hardware can be selected which one of these electric standard is used, through jumpers connection (as described in the previous tables). By software the serial lines can be programmed to operate with 7, 8, 9 bits per character, parity, between 1 and 2 stop bits at standard or no standard baud rates, through some CPU internal registers setting.

Some components necessary for RS 422 and RS 485 communication are not mounted and not tested on the default configuration card, so the first not standard configuration must always be executed by grifo® technician; then the user can change himself the configuration, following the below description:

- SERIAL LINE A=ASP 1 CONFIGURED IN RS 232
  With the JS17 and JS18 jumpers in 2-3 position the serial line has only three wires (TXA, RXA, GND) while by connecting the same jumpers in 1-2 position, the serial line A has five wires (TXA, RXA, CTSA, RTSA, GND) in fact two handshake signals, driven by proper microcontroller lines, are added. In details the two handshake signals of CN3A are connected as below described:
  
  | JS17 and JS18 | CTSA | RTSA |
  | 1-2 position | PIO 18, /CTS1 CPU signal | PIO 19, /RTS1 CPU signal |
  | 2-3 position | not acquired | continuously disabled = -10 Vdc |

  If the last condition is incompatible with the system to be connected, perform the connection without the RTSA signal.

- SERIAL LINE B=ASP 0 CONFIGURED IN RS 232 (default configuration)
  
  | IC6 | IC7 | IC8 |
  | MAX 202 driver | no component | no component |

  JS15 = not connected
  JS1, JS2 = not connected

- SERIAL LINE B=ASP 0 CONFIGURED IN RS 422 (.RS422 option)
  
  | IC6 | IC7 | IC8 |
  | no component | SN 75176 driver | SN 75176 driver |

  JS15 = position 2-3
  JS1, JS2 = (*)

  With /RTSB=/RTS0=PIO 20 signal (managed by software with ASP 0 or PIO registers) the user enables or disables the transmitter driver:
  
  /RTS0 = low level = 0 logic state -> transmitter driver enabled
  /RTS0 = high level = 1 logic state -> transmitter driver disabled

  allowing either point to point (driver can be mantained always enabled) or network (driver is enabled only when the unit can hold the line) connection.

- SERIAL LINE B=ASP 0 CONFIGURED IN RS 485 (.RS485 option)
  
  | IC6 | IC7 | IC8 |
  | no component | no component | SN 75176 driver |

  JS15 = position 1-2
  JS1, JS2 = (*)

  With /RTSB=/RTS0=PIO20 signal (managed by software with ASP 0 or PIO registers) the user defines the RS 485 line direction:
  
  /RTS0 = low level = 0 logic state -> RS 485 line transmitting
  /RTS0 = high level = 1 logic state -> RS 485 line receiving

  allowing network connection in a master multi slave system and multi master system. With RS
485 communication line, on CN3B the pins 4 and 5 have the double function of reception and transmission signals. All the transmitted characters are at the same time received when the user select RS 485 on GPC® 884; in this way the line conflicts can be immediately recognized by simply testing the received character after each transmission.

(*) With jumper JS1 and JS2 the RS 422 receiving line or the RS 485 line can be terminated and forced with a suitable resistors circuit. The line termination must be added only at the beginning and at the end of the physical line, connecting both the jumpers. Normally these jumper must be connected in point to point network, or on the farther cards in multipoints network.

After reset or power on phase, the /RTS0 signal is forced to high level that maintain the RS 485 driver receiving and that disables the RS 422 transmitter driver; this condition eliminates any conflict on the communication line.

For further information about serial communication, please refer to connection examples described in figures 9÷12 and to appendix A.

MEMORY SELECTION

On GPC® 884 can be mounted up to 1032K bytes of memory divided in several configurations, as described in the following table:

<table>
<thead>
<tr>
<th>IC</th>
<th>DEVICE</th>
<th>SIZE</th>
<th>JUMPERS CONFIGURATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>EPROM</td>
<td>128K Byte</td>
<td>J2 in position 1-2 and 3-4</td>
</tr>
<tr>
<td></td>
<td>EPROM</td>
<td>256K Byte</td>
<td>J2 in position 1-2 and 3-4</td>
</tr>
<tr>
<td></td>
<td>EPROM</td>
<td>512K Byte</td>
<td>J2 in position 1-2 and 3-4</td>
</tr>
<tr>
<td></td>
<td>FLASH EPROM</td>
<td>128K Byte</td>
<td>J2 in position 2-3 and 4-5</td>
</tr>
<tr>
<td></td>
<td>FLASH EPROM</td>
<td>256K Byte</td>
<td>J2 in position 2-3 and 4-5</td>
</tr>
<tr>
<td></td>
<td>FLASH EPROM</td>
<td>512K Byte</td>
<td>J2 in position 2-3 and 4-5</td>
</tr>
<tr>
<td>13</td>
<td>RAM</td>
<td>128K Byte</td>
<td>J3 not connected</td>
</tr>
<tr>
<td></td>
<td>RAM</td>
<td>512K Byte</td>
<td>J3 connected</td>
</tr>
<tr>
<td>11</td>
<td>EEPROM</td>
<td>256±8K Byte</td>
<td>-</td>
</tr>
</tbody>
</table>

Figure 23: Memory selection table

The sockets IC 5 and IC 13 follow the JEDEC standard, so the mounted memory devices must have JEDEC pin outs. IC 11 is a serial memory device with I²C BUS. The jumpers configurations described on figure 23 only set the sockets for the indicated memory device, but they don't define the addressing map; for this information, please refer to "MEMORY ADDRESSES" paragraph. To easily locate the memory devices on the board, please refer to figure 13.

Normally GPC® 884 is supplied in its default configuration with 128K RAM on IC13 and 512 byte EEPROM on IC11; each different configurations can be defined during order phase or self mounted by the user. Below are reported the code of the possible memory options: the ordering phase. Here follow the codes to order the optional memory configurations:

.512 -> 512K RAM

For further informations about prices and options please contact grifo®.
SOLDER JUMPERS

The solder jumpers called JSxx are connected by a thin copper connection on the solder side. So, if one of their configurations has to be changed, the user must first cut this connection using a sharpened cutter, then make the new connection using a low power soldering tool and some non-corrosive tin.

MULTIPLEXED PINS

The microcontroller used on the GPC® 884 includes two 16 bits ports equal to 32 general purpose input output lines. Many of these lines are internally multiplexed and they assume different functions according with the performed software programmation. In the below table are described all the signals that have a multiplexed function on the card:

<table>
<thead>
<tr>
<th>PIO SIGNAL</th>
<th>MPX FUNCTIONS</th>
<th>USE ON GPC® 884</th>
</tr>
</thead>
<tbody>
<tr>
<td>PIO 00</td>
<td>PIO 00 ; TMR IN 1</td>
<td>PA.0 on CN5</td>
</tr>
<tr>
<td>PIO 01</td>
<td>PIO 01 ; TMR OUT 1</td>
<td>PA.1 on CN5</td>
</tr>
<tr>
<td>PIO 03</td>
<td>PIO 03</td>
<td>PA.2 on CN5</td>
</tr>
<tr>
<td>PIO 10</td>
<td>PIO 10 ; TMR OUT 0</td>
<td>PA.3 on CN5</td>
</tr>
<tr>
<td>PIO 11</td>
<td>PIO 11 ; TMR IN 0</td>
<td>PA.4 on CN5</td>
</tr>
<tr>
<td>PIO 12</td>
<td>PIO 12 ; DRQ 0</td>
<td>PA.5 on CN5</td>
</tr>
<tr>
<td>PIO 13</td>
<td>PIO 13 ; DRQ 1</td>
<td>PA.6 on CN5</td>
</tr>
<tr>
<td>PIO 14</td>
<td>PIO 14</td>
<td>PA.7 on CN5</td>
</tr>
<tr>
<td>PIO 15</td>
<td>PIO 15</td>
<td>PC.0 on CN5</td>
</tr>
<tr>
<td>PIO 24</td>
<td>PIO 24</td>
<td>PC.1 on CN5</td>
</tr>
<tr>
<td>PIO 25</td>
<td>PIO 25</td>
<td>PC.2 on CN5</td>
</tr>
<tr>
<td>PIO 26</td>
<td>PIO 26</td>
<td>PC.3 on CN5</td>
</tr>
<tr>
<td>PIO 30</td>
<td>PIO 30 ; INT4</td>
<td>PC.4 on CN5</td>
</tr>
<tr>
<td>PIO 31</td>
<td>PIO 31 ; INT2 ; PWD</td>
<td>PC.5 on CN5</td>
</tr>
<tr>
<td>PIO 18</td>
<td>PIO 18 ; /CTS1</td>
<td>PC.6 on CN5 ; /CTSA</td>
</tr>
<tr>
<td>PIO 19</td>
<td>PIO 19 ; /RTS1</td>
<td>PC.7 on CN5 ; /RTSA</td>
</tr>
<tr>
<td>PIO 04</td>
<td>PIO 04 ; DTR</td>
<td>serial EEPROM SDA; A/D converter DIN</td>
</tr>
<tr>
<td>PIO 06</td>
<td>PIO 06 ; SRDY</td>
<td>serial EEPROM SCL</td>
</tr>
<tr>
<td>PIO 05</td>
<td>PIO 05 ; /DEN</td>
<td>A/D converter CLK</td>
</tr>
<tr>
<td>PIO 09</td>
<td>PIO 09 ; A19</td>
<td>A/D converter DOUT</td>
</tr>
<tr>
<td>PIO 29</td>
<td>PIO 29 ; /CLKDIV2</td>
<td>A/D converter /CS</td>
</tr>
</tbody>
</table>

Figure 24: Multiplexed pin table

The user can arbitrarily decide the function of the CN5 connected signals but he must take care of the A/D converter, EEPROM and not described PIO signals setting. The software tools developed for the card provide the right configuration of each multiplexed PIO pins, so the user can simply acquire the old setting, change the allowed signals functions and then set the new configuration. The following table shows the CN5 I/O lines status during the power on and reset phase:
The internal pull up and pull down resistor value is about 10 KΩ, thus if the CN5 lines are not connected to low impedance external loads, during the power on or reset they will assume respectively the logic status 1 and 0.

### POWER FAILURE

Together with the power management circuit of the CPU, it is also available an interesting power failure circuit, that can be connected to two different interrupt signals (NMI or INT0). The power failure circuit checks the power supply voltage of the card and whenever it reaches the threshold intervent value (52 mV before reset activation value), it enables its output and it captures CPU attention, if JS19 is connected. The time delay between the power failure activation and the reset circuit activation depends on the used power supply and on the developed system configuration; normally this delay is about 100 µsec and it is sufficient to execute only a fast interrupt service routine (i.e. save a flag in the backed memory). The common use of this circuit is to inform application program of the imminent power supply failure, so as to save the necessary status information by taking advantage of the residue capacitor charge.
SOFTWARE

A wide selection of software development tools can be obtained, allowing use of the module as a system for its own development, both in assembler and in other high level languages; in this way the user can easily develop all the requested application programs in a very short time. Generally all software packages available for the mounted microprocessor, or for the 8086 and derived ones, can be used. Even many of the P.C. softwares could be used on GPC® 884 but the numerous hardware difference make it really difficult. Below is described a brief list of the available software tools:

GET 188
It is a complete program with Editor, Communication driver, and Mass Memory management for all 80188 family cards. This program, developed by grifo®, allows to operate in the best conditions when GDOS, FGDOS or FWR software tools are used; GET 188 is supplied when one of these tools is ordered and it is personalized with name and general data of the customer. A useful list of pull down menus and the possibility of using mouse, make program use very comfortable. GET 188 program can be executed both on MS-DOS system and on MACINTOSH computers too, through SOFT-PC program. It is supplied on MS-DOS 3”1/2 floppy disk with the documentation on GDOS 188 manual.

GDOS 884
It is a complete development tool for GPC® 884 card. It is supplied together with GET 188 program to allow an easy and immediate use of this powerful development system. GDOS is divided in two different structures: the first one works on PC maintaining serial communication with the second one. The second structure is on EPROM, it works on board of the card and it is an efficient operating system that executes many low level functions and, at the same time, it allows high level language use. The combination of the said structures results in a complete machine, in fact the card uses PC resources (like floppy disk, hard disk, printer, keyboard, monitor, etc.) as its own peripheral devices. This resulting “virtual machine” performs operation in a transparent way for the user, so this latter can operate with the same modality of standard PC languages. Moreover, GDOS can manage a portion of the on board memory as RAM disk. The on board RAM devices can directly be used performing data read and write operations with the confortable high level file system mode. This software tools is supplied on EPROM with MS-DOS GET 188 floppy disk, some examples, utilities and the operating system documentation.

FGDOS 884
It is really similar to GDOS, but it can program and erase the on board FLASH EPROM with the application program developed from the user. In this way the external EPROM programmer is not necessary to store definitely the program and it is possible to modify or to add code directly on the installed machine, through a portable PC. This software tools is supplied on FLASH EPROM with MS-DOS GET 188 floppy disk, some examples, utilities and the operating system documentation.

PASCAL 188
It is an efficient and complete PASCAL Compiler for 8086 family cards, with features similar to Release 3.0 of Borland Turbo PASCAL. It must work together with any GDOS version and it can
take advantage of its RAM disk management in fact all the high level instructions for file system can be directly used. This compiler generates an optimized code that is saved and executed on EPROM or FLASH EPROM and it requires very small RAM data area.

The terminal emulation of GET 80 program support the typical full screen PASCAL Editor, including the attributes management.

This program is supplied saved on GDOS EPROM or FLASH EPROM and on MS-DOS floppy disk with some examples and manual.

GCTR 884
Complete software tools for GPC® 884 cards that allows application program development by using a standard Borland C, C++ compiler and an external P.C. A very powerful remote symbolic and source debugger let the user download and test the compiled program with the same comfortable manners of an in circuit emulator, through a simple serial connection. At the end of debug phase the generated code can be saved in EPROM or FLASH EPROM, reducing the RAM usage.

This program is supplied saved on EPROM or FLASH EPROM and on MS-DOS floppy disks with some examples and a user manual.

FWR884
It is a really interesting utility program capable to save files saved on P.C. disks on the FLASH EPROM installed on the board. It is sufficient a serial connection with an external P.C., where GET188 is executed, and the card is capable to burn its FLASH EPROM with the user selected code, data, configuration, etc. file.

This program is supplied saved on FLASH EPROM and on MS-DOS floppy disks with GET188 program.

HI TECH C 86
Professional C Cross Compiler of Hi-Tech Software Inc. This Compiler is terribly fast and it generates a small quantity of code. This result is due to advanced techniques in optimizing the generated code based on Artificial Intelligence techniques which allow to get a very compact and very fast code. The package includes: IDE, Compiler, Code optimizer, Assembler, Linker, Remote Debugger and so on. This tool is Full ANSI/ISO Standard and Full Library Source Code. Once the porting of the Remote-Debugger module is done, this tool allows the user the software debugging directly on the hardware that he is experimenting. This type of specialization of the Remote Debugger is available from now and it is supplied with all grifo® CPU cards. This software package is on 3” 1/2 diskettes under MS-DOS format along with user manual. This version supports these following CPUs: 8088, 8086, 80186, 80188, 80286, V20, V30, V25, etc.

DDS MICRO C 86: low cost cross compiler for C source program. It is a powerful software tool that includes editor, C compiler (integer), assembler, optimizer, linker, library, and remote debugger, in one easy to use integrated development environment. There are also included the library sources and many utilities programs.
DEVICES MAP AND ADDRESSES

INTRODUCTION

In this chapter are reported all informations about card use, related to software programmation of GPC® 884. For example the registers addresses, the memory and peripheral devices allocation are described below.

ON BOARD DEVICES ADDRESSES

The on board devices addresses are managed from a microcontroller internal section (CSU) that generates the required control signals. This section allocates memory (RAM, EPROM or FLASH EPROM) and peripheral devices with a very simple software management.

The CSU has been designed to control the memory and the I/O peripherals addresses in a separate manner. The Am188ES CPU directly addresses 1 M bytes of memory and 64 K I/O registers and the chip select unit provides on board memory and peripheral devices allocation inside these addresses spaces. The maps management is completely driven by software through the CSU circuit programmation: the chip selects of the on board devices are enabled in different addresses range according with CSU registers setting.

Thanks to this feature the the maps and addresses of the card are defined by software and for the user are sufficient only the hardware connection performed on the board. Summarizing the on board device list and the pertinent connection with the CPU signals, are described in the following table:

<table>
<thead>
<tr>
<th>DEVICE</th>
<th>SOCKET</th>
<th>SIGNALS</th>
<th>ADDRESS</th>
</tr>
</thead>
<tbody>
<tr>
<td>EPROM</td>
<td>IC5</td>
<td>/UCS</td>
<td></td>
</tr>
<tr>
<td>FLASH EPROM</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RAM</td>
<td>IC13</td>
<td>/LCS</td>
<td></td>
</tr>
<tr>
<td>EEPROM</td>
<td>IC11</td>
<td>PIO4 ; PIO6</td>
<td></td>
</tr>
<tr>
<td>A/D TLC2543</td>
<td>IC10</td>
<td>PIO4 ; PIO5 ; PIO9 ; PIO29</td>
<td></td>
</tr>
<tr>
<td>ABACO® I/O BUS</td>
<td>-</td>
<td>/PCS0</td>
<td>PCS0ADDR</td>
</tr>
<tr>
<td>RTC 72421</td>
<td>IC12</td>
<td>/PCS1</td>
<td>PCS1ADDR</td>
</tr>
<tr>
<td>J1 JUMPER</td>
<td>-</td>
<td>/PCS1</td>
<td>PCS1ADDR</td>
</tr>
<tr>
<td>WATCH DOG</td>
<td>IC4</td>
<td>/PCS6</td>
<td>PCS6ADDR</td>
</tr>
</tbody>
</table>

**FIGURE 26: DEVICES HARDWARE CONNECTION TABLE**

The connection of all these devices are described in the following paragraphs and can't be changed by the user. If some different specific maps are required, please contact directly grifo®.

Normally the software package tools developed for GPC® 884 attend to correctly initialize the CSU section, as described in the user manuals of the same software tools.
I/O ADDRESSES

The on board CSU manages the allocation of all the peripheral devices registers in the microprocessor I/O space, that is 64K bytes long. Next table shows names, addresses, meanings and directions of peripheral device registers (excluding the internal microprocessor ones). For a detailed description of the registers function, please refer to next chapter "PERIPHERAL DEVICES SOFTWARE DESCRIPTION".

<table>
<thead>
<tr>
<th>DEVICE</th>
<th>REG.</th>
<th>ADDRESS</th>
<th>R/W</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>ABACO® I/O BUS</td>
<td>I/OBUS</td>
<td>PCS0ADDR+00H … PCS0ADDR+FFH</td>
<td>R/W</td>
<td>ABACO® I/O BUS addresses</td>
</tr>
<tr>
<td>J1</td>
<td>RUNDEB</td>
<td>PCS1ADDR+00H</td>
<td>R</td>
<td>Register for configuration jumper acquisition</td>
</tr>
<tr>
<td>Real Time Clock</td>
<td>SEC1</td>
<td>PCS1ADDR+00H</td>
<td>R/W</td>
<td>Data register for seconds units</td>
</tr>
<tr>
<td></td>
<td>SEC10</td>
<td>PCS1ADDR+01H</td>
<td>R/W</td>
<td>Data register for seconds decines</td>
</tr>
<tr>
<td></td>
<td>MIN1</td>
<td>PCS1ADDR+02H</td>
<td>R/W</td>
<td>Data register for minutes units</td>
</tr>
<tr>
<td></td>
<td>MIN10</td>
<td>PCS1ADDR+03H</td>
<td>R/W</td>
<td>Data register for minutes decines</td>
</tr>
<tr>
<td></td>
<td>HOU1</td>
<td>PCS1ADDR+04H</td>
<td>R/W</td>
<td>Data register for hours units</td>
</tr>
<tr>
<td></td>
<td>HOU10</td>
<td>PCS1ADDR+05H</td>
<td>R/W</td>
<td>Data register for hours decines and AM/PM</td>
</tr>
<tr>
<td></td>
<td>DAY1</td>
<td>PCS1ADDR+06H</td>
<td>R/W</td>
<td>Data register for day units</td>
</tr>
<tr>
<td></td>
<td>DAY10</td>
<td>PCS1ADDR+07H</td>
<td>R/W</td>
<td>Data register for day decines</td>
</tr>
<tr>
<td></td>
<td>MON1</td>
<td>PCS1ADDR+08H</td>
<td>R/W</td>
<td>Data register for month units</td>
</tr>
<tr>
<td></td>
<td>MON10</td>
<td>PCS1ADDR+09H</td>
<td>R/W</td>
<td>Data register for month decines</td>
</tr>
<tr>
<td></td>
<td>YEA1</td>
<td>PCS1ADDR+0AH</td>
<td>R/W</td>
<td>Data register for year units</td>
</tr>
<tr>
<td></td>
<td>YEA10</td>
<td>PCS1ADDR+0BH</td>
<td>R/W</td>
<td>Data register for year decines</td>
</tr>
<tr>
<td></td>
<td>WEE</td>
<td>PCS1ADDR+0CH</td>
<td>R/W</td>
<td>Data register for week day</td>
</tr>
<tr>
<td></td>
<td>REGD</td>
<td>PCS1ADDR+0DH</td>
<td>R/W</td>
<td>Control register D</td>
</tr>
<tr>
<td></td>
<td>REGE</td>
<td>PCS1ADDR+0EH</td>
<td>R/W</td>
<td>Control register E</td>
</tr>
<tr>
<td></td>
<td>REGF</td>
<td>PCS1ADDR+0FH</td>
<td>R/W</td>
<td>Control register F</td>
</tr>
<tr>
<td>Watch dog</td>
<td>RWD</td>
<td>PCS6ADDR+00H</td>
<td>R/W</td>
<td>Register for watch dog retrigger</td>
</tr>
</tbody>
</table>

**FIGURE 27: I/O ADDRESSES TABLE**

The addresses value used in figure 27 (PCS0ADDR, PCS1ADDR, etc.) are defined by software setting of CSU section. The previous table shows only the registers of the peripheral devices external to microprocessor; for the internal registers please refer to specific documentation of the manufacturing company or to appendix B of this manual. About I/O maps the CSU avoids every conflicts problems between CPU internal and external peripherals.
ABACO® I/O BUS ADDRESSES

The GPC® 884 CSU manages the ABACO® I/O BUS and it defines the allocation addresses of this BUS. As described in the previous "I/O ADDRESSES" table, the BUS uses the /PCS0 addresses with a 256 bytes extension. Any I/O operations at each one of these addresses enables the /IORQ signal and the other control signals of CN1 connector. Please remember that ABACO® I/O BUS has only 8 address bits and 8 data bits, so when the peripheral card is mapped by hardware, only the least significant byte of the 16 bits I/O address is meaningful.

MEMORY ADDRESSES

The maximum 1032K bytes of memory, are allocated on the board as below described:

- Up to 512K bytes of EPROM or FLASH EPROM allocated in memory space.
- Up to 512K bytes of RAM allocated in memory space.
- Up to 8K bytes of serial EEPROM allocated in I/O space.

GPC® 884 can directly manage no more than 1M bytes of memory that is the microprocessor physical addressable space. On the board this physical space can be divided in two separated segments: each ones of these segment have software programmable dimension and start/end address. The CPU internal CSU circuit divides the space directly managed by the microprocessor into these segments and it allocates them in the physical memory devices space. The CSU circuit is software programmable with I/O operations to five specific registers in a fast and comfortable manner. So CSU allows software managements of all the IC5 and IC13 memory sizes, with the possibility to define the timing and access modality.

The following figure describe available memory configurations; for further informations on CSU use and segments meaning (/UCS, /LCS), please refer to appendix B, while for memory devices location and configuration refer to figures 13.

After power on or reset phase, the CSU circuit allocates a 64K segment at the end of the CPU physical space, therefore the card starts execution of code saved at address FFFF0H of IC5 EPROM or FLASH EPROM, that always is the address the last 16 bytes of the device.

The memory size and type configurations must be selected both according to used software tools and user requests and/or application features. The card configuration for the selected memory device types and sizes on IC5 and IC13 sockets, is performed with some comfortable jumpers, as described in "MEMORY SELECTION" chapter.

Some software tools, i.e. GDOS, GCTR, self manage the CSU circuit to use all the available memories at high level without user intervention.
**Figure 28: Memory Allocation**

- **RAM**
  - IC 13
  - Address range: $00000H$ to $E0000H$

- **EPROM / FLASH**
  - IC 5
  - Address range: $7FFFFH$ to $1FFFFH$

- **RAM**
  - IC 13
  - Address range: $E0000H$ to $FFFFFH$
PERIPHERAL DEVICES SOFTWARE DESCRIPTION

In the previous paragraphs are described the external registers addresses, while in this one there is a specific description of registers meaning and function (please refer to I/O addresses table, for the registers names and addresses values). For a more detailed description of the devices, please refer to manufacturing company documentation; for microprocessor internal peripheral devices, not described in this paragraph, refer to appendix B. In the following paragraphs the $D_7 \div D_0$ indication denotes the eight bits of the combination used in I/O operations.

WATCH DOG

Retrigger operation of GPC® 884 watch dog circuit is performed with a simple input and/or output operation at the address of register RWD. The input or output data has no meaning so it can be discharged or setted with any value. To avoid watch dog activation it is necessary to retrigger its circuit at regular time periods and the duration of these periods must be smaller than intervent time. If retrigger doesn't happen as before described and JS10 is connected, when intervention time is elapsed, the card is reset. The default intervention time is about 1.4 sec.

CONFIGURATION JUMPER INPUT

The J1 configuration jumper installed on the GPC® 884 board can be acquired simply by performing an input operation from RUNDEB registers and masking bit D7. The value is in complemented logic, this means that the connected jumper gives a logic value "0" while if the jumper is not connected the acquired logic value will be "1". The mostly implemented applications for this feature are: working conditions setting, selection of some on board firmware parameters, language selection, etc. This jumper switches between the RUN (not connected) or the DEBUG (connected) mode, a feature used by some grifo® software tools, as described in the manuals of the tools themselves.

SERIAL EEPROM

For software management of serial EEPROM module of IC 11, please refer to specific documentation or to demo programs supplied with the card. The user must realize a serial communication with I2C bus standard protocol, through two I/O microprocessor pins. The only necessary information is the electric connection:

- DATA line (SDA) -> PIO 04 (input/output) of the CPU
- CLOCK line (SCL) -> PIO 06 (output) of the CPU
- A2 address line -> GND (0 logic state)
- A1 address line -> GND (0 logic state)
- A0 address line -> GND (0 logic state)

The first 32 bytes of serial EEPROM (0:31) are reserved for software tools use, so they can't be neither read nor written by user program. The PIO logic state "0" corresponds to low level (0 V), while logic state "1" corresponds to high level (5 V).
A/D CONVERTER

For software management of the eleven A/D converter channel, please refer to specific documentation of the component or to demo programs supplied with the card. The user must realize a serial synchronous communication standard protocol, through four I/O microprocessor pins. The only necessary information is the electric connection:

- DATA IN line -> PIO 04 (output) of the CPU
- DATA OUT line -> PIO 09 (input) of the CPU
- I/O CLOCK line -> PIO 05 (output) of the CPU
- /CS line -> PIO 29 (output) of the CPU

The PIO logic state "0" corresponds to low level (0 V), while logic state "1" corresponds to high level (5 V).

REAL TIME CLOCK

This peripheral is allocated in 16 consecutive I/O addresses, 3 of which correspond to status registers while the remaining 13 are for datas. Data registers are used both for read operations (of the current time and date) and write operations (to initialize the time and date) just like the status registers which are used in write operations (to program the operative mode) and in read operations (to acquire the RTC status). Here follows a list of the RTC data registers' meanings:

- SEC1 - Units of seconds - 4 least significant bits of SEC1.3÷SEC1.0
- SEC10 - Deciles of seconds - 3 least significant bits of SEC10.2÷SEC10.0
- MIN1 - Units of minutes - 4 least significant bits of MIN1.3÷MIN1.0
- MIN10 - Deciles of minutes - 3 least significant bits of MIN10.2÷MIN10.0
- HOU1 - Units of hours - 4 least significant bits of HOU1.3÷HOU1.0
- DAY1 - Units of day number - 4 least significant bits of DAY1.3÷DAY1.0
- DAY10 - Deciles of day number - 2 least significant bits of DAY10.1÷DAY10.0
- MON1 - Units of month - 4 least significant bits of MON1.3÷MON1.0
- MON10 - Deciles of month - 1 least significant bit of MON10.0
- YEA1 - Units of year - 4 least significant bits of YEA1.3÷YEA1.0
- YEA10 - Deciles of year - 4 least significant bits of YEA10.3÷YEA10.0
- WEE - Day of the week - 3 least significant bits of WEE.2÷WEE.0

For this last register the three least significant bits mean:

<table>
<thead>
<tr>
<th>WEE.2</th>
<th>WEE.1</th>
<th>WEE.0</th>
<th>Day of the week</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Sunday</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Monday</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Tuesday</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>Wednesday</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Thursday</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>Friday</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>Saturday</td>
</tr>
</tbody>
</table>

While, the meaning of the three control registers is:
bit 7 6 5 4 3 2 1 0
REG D = NU NU NU NU 30S IF B H
NU = Not used.
30S = If high (1) it allows a 30 seconds correction of the time. Once set the RTC seconds are
reset and the minutes increased, if the previous seconds was equal or greater than 30.
IF = It manages the RTC interrupt status. When read it shows the current interrupt status (1
active and vice versa), when reset to 0 it disables the RTC interrupt signal if the interrupt
mode is selected.
B = Indicates whether R/W operations can be performed on the registers:
   1 -> operations are not allowed and vice versa.
H = If high (1) it stores the written time and date.

bit 7 6 5 4 3 2 1 0
REG E = NU NU NU NU T1 T0 I M
NU = Not used.
T1 T0 = Determine the duration of the internal counters interrupt cycle.
0 0 -> 1/64 second
0 1 -> 1 second
1 0 -> 1 minute
1 1 -> 1 hour
I = It defines the interrupt operating mode:
   1 -> it selects interrupt mode: when the selected duration elapses the interrupt is
   enabled and then disabled only with a reset of bit IF of control register D;
   0 -> it selects the standard mode: when the selected duration elapses the interrupt
   is enabled and then disabled only after 7.8 msec.
M = It masks the interrupt status:
   1 -> interrupt masked: the RTC interrupt signal is always disabled;
   0 -> interrupt not masked: the RTC interrupt signal reflects interrupt status.

bit 7 6 5 4 3 2 1 0
REG F = NU NU NU NU T 24/12 S R
NU = Not used.
T = It determines from which internal counter to take the counting signal:
   1 -> main counter (fast counter for test);
   0 -> 15th counter.
24/12 = It determines the hours counting mode:
   1 -> 0-23;
   0 -> 1-12 with AM/PM.
S = If high (1) it stops the clock time counting until the next enabling (0).
R = If high (1) it resets all the internal counters.

CPU INTERNAL PERIPHERALS

The descriptions of the registers that manages the CPU internal peripheral devices (ASP, TCU, DMA,
ICU, CSU, etc) is available in the appendix B. Whenever this information is still insufficient,
please refer to specific documentation of the manufacturing company.
EXTERNAL CARDS

GPC® 884 can be connected to a wide range of block modules and operator interface system produced by grifo®, or to many system of other companies. The on board resources can be expanded with a simple connection to the numerous peripheral grifo® boards, both intelligent and not, thanks to its standard ABACO® I/O BUS connector. Even single EURO cards with BUS ABACO® can be connected, by using the proper mother boards.

Hereunder some of these cards are briefly described; ask the detailed information directly to grifo®, if required.

KDL xxx - KDF xxx
Keyboard Display interface - LCD or Fluorescent
Interface with Fluorescent or LCD display, LEDs backlit, 20x2 or 20x4 characters; up to 24 keys matrix keyboard connector. It is directly driven by 16 TTL I/O lines; High level languages supported.

QTP 24 - QTP 24P
Quick Terminal Panel 24 keys - Parallel interface
Intelligent user panel equipped with Fluorescent or LCD display, LEDs backlit, 20x2 or 20x4 characters; RS 232, RS 422, RS 485 or current loop serial line; serial E² for set up and message. Possibility of re-naming keys, LEDs and panel name by inserting label with new name into the proper slot; 24 Keys and 16 LEDs with blinking attribute and buzzer manageable by software; built in power supply; RTC option, reader of magnetic badge and relay. The QTP 24P is low cost no intelligent (passive) version. It is directly driven from 16 TTL I/O lines; high level languages supported.

QTP G26
Quick Terminal Panel - LCD Graphic, 26 keys
Intelligent user panel equipped with graphic LCD display 240x128 pixel, CFC backlit; optocoupled RS 232 line and additional RS 232, RS 422, RS 485 or current loop serial line. Indepndent optional CAN line controller; serial E² for set up; RTC and RAM Lithium backed; primary graphic objects; possibility of renaming keys, LEDs and panel name by inserting label with new name into the proper slot; 26 Keys and 16 LEDs with blinking attribute and buzzer manageable by software; built in power supply; reader of magnetic badge, smart card and relay option.

MCI 64
Memory Cards Interfaces 64 MBytes
Interfacing card for managing 68 pins PCMCIA memory cards, it is directly driven from any ABACO® I/O standard connector; availability of high level drivers for programming languages.

IBC 01
Interface Block Comunication
Conversion card for serial communication, 2 RS 232 lines; 1 RS 422-485 line; 1 optical fibre line; selectable DTE/DCE interface; quick connection for DIN 46277-1 and 3 rails.

ADC 812
Analog to Digital Converter, 12 bits, multi range
DAS (Data Acquisition System) multi range 8 channels 12 bit A/D conversion lines; track and hold; 6µs conversion time; range ±10, ±5, +10, +5Vdc or 0÷20, 4÷20mA; analog inputs connections through quick terminal screw connectors; ABACO® I/O BUS interface; direct mounting for DIN 247277-1 and 3 rails; 4 type dimension.
Figure 29: Available Connections Diagram

- PC like or Macintosh
- PLC
- QTP G26
- PC like or Macintosh
- PLC

- Serial Line RS-232
- Serial Line RS-232, RS 422 e RS 485

- External Lithium Battery 3.6 V to RAM Back up
- Serial Line RS-232, RS 422 e RS 485

- DIRECT CONNECTION TO QTP xxP TYPE
- DIGITAL TTL INPUT/OUTPUT to XBI-01, OBI-01, RBO-08 etc.
- RELAY
- TRANS.
- COUPLED

- 2 COUNTER/TIMER, 2 DMA, 2 INT

- 12 Bits ANALOG INPUT.
  VOLTAGE: 0±2.490V opt. 0±5V

- ANY I/O TYPE
- C/O R16-T16, etc.
- IPC 52, UAR 24, etc.

- ABACO® BUS
- ABB 03 or ABB 05, etc.

- ABACO® I/O BUS
- ZBx series
DAC 212
Digital to Analog Converter 12 bits, multi range
Digital to Analog converter; multi range 2 channels 12 bits ±10, +10 Vdc output; analog outputs connections through quick terminal screw connectors; **ABACO**® I/O BUS interface; direct mounting for DIN 247277-1 and 3 rails; 4 type dimension.

CAN 14
Control Area Network, 1 channel, galvanically insulated
UART CAN SJA1000; 1 serial channels galvanically insulated; **ABACO**® I/O BUS interface; 4 type dimension; support of CAN 2.0B protocol; transfer rate up to 1M bit/sec; direct mounting for DIN 247277-1 and 3 rails.

ETI 324
Encoder Timer I/O, 3 counters, 24 I/O
Three timers counters driven by 82C54; bidirectional optocoupled encoder input; direction identifier; phases multiplier; 24 digital lines driven by 82C55 on two standard I/O **ABACO**® connectors; **ABACO**® I/O BUS interface; direct mounting for DIN 247277-1 and 3 rails.

OBI 01 - OBI 02
Osblo BLOCK Input NPN-PNP
Interface between 16 NPN, PNP optocoupled and displayed input lines, with screw terminal and **ABACO**® standard I/O 20 pins connector; power supply section; connection for DIN Ω rails.

OBI N8 - OBI P8
Opto BLOCK Input NPN-PNP
Interface between 8 NPN, PNP optocoupled and displayed input lines, with screw terminal and **ABACO**® standard I/O 20 pins connector; power supply section; connection for DIN Ω rails.

TBO 01 - TBO 08
Transistor BLOCK Output
Interface for **ABACO**® standard I/O 20 pins connector; 16 or 8 transistor output lines 45 Vdc 3 A open collector; screw terminal; optocoupled and displayed lines; connection for DIN 247277-1 and 3 rails.

RBO 01
Relé BLOCK Output
Interface for **ABACO**® standard I/O 20 pins connector; 8 displayed 5A or 10A relays; screw terminal; connection for DIN Ω rails.

RBO 08 - RBO 16
Relé BLOCK Output
Interface for **ABACO**® standard I/O 20 pins connector; 8 or 16 displayed Relays 3A with MOV; screw terminal; connection for DIN Ctype and Ω rails.

XBI 01
miXed BLOCK Input Output
Interface for **ABACO**® standard I/O 20 pins connector; 8 transistor output lines 45 Vdc 3A; 8 input lines; screw terminal; optocoupled and displayed I/O lines; connection for DIN 247277-1 and 3 rails.
**XBI R4 - XBI T4**

miXed BLOCK Input-Output

Interface for ABACO® standard I/O 20 pins connector; 4 Relays 3A with MOV or 4 opticcoupled Transistors 3A open collectors; 4 input lines opticcoupled; screw terminal; connection for DIN C type and Ω rails.

**FBC xxx**

Flat Block Contactxxx pins

This interconnection system "wire to board" allows the connection to many type of flat cable connectors to terminal for external connections. Connection for DIN Ω rails.

**ABB 05**

ABACO® Block BUS 5 slots

5 slots ABACO® mother board with power supply. Double power supply built in; 5Vdc 2,5A section for powering the on board logic; second section at 24Vdc 400mA galvanically coupled, for the opticcoupled input lines. Auxiliary connector for ABACO® I/O BUS. Connection for DIN Ω rails.

**ABB 03**

ABACO® Block BUS 3 slots

3 slots ABACO® mother board; 4 TE pitch connectors; ABACO® I/O BUS connector; screw terminal for power supply; connection for DIN C type and Ω rails.

**ZBR xxx**

Zipped BLOCK Relays xx Input + xx Output

Peripheral cards family, relays outputs, equipped with housing for Ω rails mounting. Double power supply built in; 5Vdc section for powering the on board logic and an external CPU cards; second section, galvanically coupled, for the opticcoupled input lines. All I/O lines are displayed by LEDs. Relays contacts are 3A and are MOV protected. All I/O connections are availables on quick terminal connectors. 1 connector interface to ABACO® I/O BUS. The ZBR serie represent the ideal complement for cards 3 and 4 type. The ZBR cards can be directly driven, through the PC parallel port, by using the PCC A26 low cost interface card. ZBR 324 -> 32 opto in, 24 relays; ZBR 246 -> 24 opto in, 16 relays; ZBR 168 -> 16 opto in, 8 relays; ZBR 84 -> 8 opto in, 4 relays.

**ZBT xxx**

Zipped BLOCK Transistors xx Input + xx Output

Peripheral cards family having opticcoupled outputs and 3A transistor in open collector. Cards are equipped with housing for Ω rails mounting. Double power supply built in; 5Vdc section for powering the on board logic and an external CPU cards; second section, galvanically coupled, for the opticcoupled input lines. All I/O lines are displayed by LEDs. All output transistors are equipped with protection against inductive loads. All I/O connections are availables on easy quick terminal connectors. Connector interface to ABACO® I/O BUS. The ZBT serie represent the ideal complement for cards 3 and 4 type. The ZBT cards can be directly driven, through the PC parallel port, by using the PCC A26 low cost interface card. ZBT 324 -> 32 opto in, 24 transistors; ZBT 246 -> 24 opto in, 16 transistors; ZBT 168 -> 16 opto in, 8 transistors; ZBT 84 -> 8 opto in, 4 transistors.
In this chapter there is a complete list of technical books, where the user can find all the necessary documentations on the components mounted on GPC® 884.

Data book Manuale TEXAS INSTRUMENTS: The TTL Data Book - SN54/74 Families
Data book Manuale TEXAS INSTRUMENTS: RS-422 and RS-485 Interface Circuits
Data book Manuale TEXAS INSTRUMENTS: Data Acquisition Circuits Data Book

Data book NEC: Memory Products
Data book MAXIM: New Releases Data Book - Volume IV
Data book MAXIM: New Releases Data Book - Volume V
Data book XICOR: Data Book
Data book NATIONAL SEMICONDUCTOR: Linear Data Book - Volume 1
Data sheets SEIKO EPSON: REAL TIME CLOCK MODULE RTC-62421 Application manual

For further information and upgrades please refer also to specific internet web pages of the manufacturing companies.
APPENDIX A: JUMPERS AND SERIAL DRIVERS LOCATION

**Figure A1: Memory Jumpers Location**

**Figure A2: Serial Communication Jumpers Location**
Serial A = ASP 1 in RS 232
Serial B = ASP 0 in RS 422

Serial A = ASP 1 in RS 232
Serial B = ASP 0 in RS 485

Figure A3: Serial Communication Drivers Location
DISTINCTIVE CHARACTERISTICS

- E86 family 80C186-/188- and 80L186-/188-compatible microcontrollers with enhanced bus interface
  - Lower system cost with higher performance
  - 3.3-V ±0.3-V operation (Am186ESLV and Am188ESLV microcontrollers)
- High performance
  - 20-, 25-, 33-, and 40-MHz operating frequencies
  - Supports zero-wait-state operation at 25 MHz with 100-ns static memory (Am186ESLV and Am188ESLV microcontrollers) and 40 MHz with 70-ns static memory (Am186ES and Am188ES microcontrollers)
  - 1-Mbyte memory address space
  - 64-Kbyte I/O space
- Enhanced features provide improved memory access and remove the requirement for a 2x clock input
  - Nonmultiplexed address bus
  - Processor operates at the clock input frequency
  - On the Am186ES/ESLV microcontroller, 8-bit or 16-bit memory and I/O static bus option
- Enhanced integrated peripherals provide increased functionality, while reducing system cost
  - Thirty-two programmable I/O (PIO) pins
  - Two full-featured asynchronous serial ports allow full-duplex, 7-bit, 8-bit, or 9-bit data transfers
  - Serial port hardware handshaking with CTS, RTS, ENRX, and RTR selectable for each port
- Multidrop 9-bit serial port protocol
- Independent serial port baud rate generators
- DMA to and from the serial ports
- Watchdog timer can generate NMI or reset
- A pulse-width demodulation option
- A data strobe, true asynchronous bus interface option included for DEN
- Pseudo static RAM (PSRAM) controller includes auto refresh capability
- Reset configuration register
- Familiar 80C186/80L186 peripherals
  - Two independent DMA channels
  - Programmable interrupt controller with up to eight external and eight internal interrupts
  - Three programmable 16-bit timers
  - Programmable memory and peripheral chip-select logic
  - Programmable wait state generator
  - Power-save clock divider
- Software-compatible with the 80C186/80L186 and 80C188/80L188 microcontrollers with widely available native development tools, applications, and system software
- A compatible evolution of the Am186™EM and Am188™EM microcontrollers
- Available in the following packages:
  - 100-pin, thin quad flat pack (TQFP)
  - 100-pin, plastic quad flat pack (PQFP)

GENERAL DESCRIPTION

The Am186™ES/ESLV and Am188™ES/ESLV microcontrollers are an ideal upgrade for 80C186/188 and 80L186/188 microcontroller designs requiring 80C186/188 and 80L186/188 compatibility, increased performance, serial communications, and a direct bus interface.

The Am186ES/ESLV and Am188ES/ESLV microcontrollers are part of the AMD E86 family of embedded microcontrollers and microprocessors based on the x86 architecture. The E86 family includes the 16- and 32-bit microcontrollers and microprocessors described on page 8.

The Am186ES/ESLV and Am188ES/ESLV microcontrollers have been designed to meet the most common requirements of embedded products developed for the office automation, mass storage, and communications markets. Specific applications include disk drives, hand-held and desktop terminals, set-top controllers, fax machines, printers, photocopiers, feature phones, cellular phones, PBXs, multiplexers, modems, and industrial controls.
**Am188ES MICROCONTROLLER BLOCK DIAGRAM**

- **Clock and Power Management Unit**
- **Interrupt Control Unit**
- **Asynchronous Serial Port 0**
- **Asynchronous Serial Port 1**
- **DMA Unit**
- **Execution Unit**
- **Chip-Select Unit**
- **Cache Control Registers**
- **Control Registers**
- **Program Control Unit**
- **Timer Control Unit**
- **Max Count B Registers**
- **Max Count A Registers**
- **16-Bit Count Registers**
- **20-Bit Destination Pointers**
- **20-Bit Source Pointers**
- **Refresh Control Unit**
- **Control Registers**

**Notes:**
- *All PIO signals are shared with other physical pins. See the pin descriptions beginning on page 27 and Table 2 on page 34 for information on shared functions.*
- **PWD, INT5, INT6, RTS, CTS, TMRIN0, TMRIN1, DRQ0, DRQ1, MCS0, A2, A1,** and **A0** are multiplexed with **INT2/INTA, DRQ0, DRQ1, UCS1/ONCE, MCS0, A2, A1, A0** respectively. See the pin descriptions beginning on page 27.

---

**Am188ES Microcontroller**

- **Connection Diagram**
- **Top Side View—100-Pin Plastic Quad Flat Pack (PQFP)**

**Note:**
- Pin 1 is marked for orientation.
### Peripheral Control Block Register Map

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Offset</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>Processor Control Registers: Chapters 4 &amp; 6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Peripheral control block relocation register</td>
<td>F6h</td>
<td>4-3</td>
</tr>
<tr>
<td>Reset configuration register</td>
<td>F6h</td>
<td>4-4</td>
</tr>
<tr>
<td>Processor release level register</td>
<td>F4h</td>
<td>4-5</td>
</tr>
<tr>
<td>Auxiliary configuration register</td>
<td>F2h</td>
<td>4-6</td>
</tr>
<tr>
<td>System configuration register</td>
<td>F0h</td>
<td>4-7</td>
</tr>
<tr>
<td>Enable RCU register</td>
<td>E4h</td>
<td>6-2</td>
</tr>
<tr>
<td>Clock prescaler register</td>
<td>E2h</td>
<td>6-2</td>
</tr>
<tr>
<td>Memory partition register</td>
<td>E0h</td>
<td>6-1</td>
</tr>
<tr>
<td>DMA Registers: Chapter 9</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DMA 1 control register</td>
<td>DAh</td>
<td>9-3</td>
</tr>
<tr>
<td>DMA 1 transfer count register</td>
<td>DBh</td>
<td>9-6</td>
</tr>
<tr>
<td>DMA 1 destination address low register</td>
<td>D4h</td>
<td>9-8</td>
</tr>
<tr>
<td>DMA 1 source address low register</td>
<td>D6h</td>
<td>9-9</td>
</tr>
<tr>
<td>DMA 1 source address high register</td>
<td>D8h</td>
<td>9-10</td>
</tr>
<tr>
<td>DMA 0 transfer count register</td>
<td>C6h</td>
<td>9-6</td>
</tr>
<tr>
<td>DMA 0 destination address high register</td>
<td>C8h</td>
<td>9-7</td>
</tr>
<tr>
<td>DMA 0 destination address low register</td>
<td>C4h</td>
<td>9-8</td>
</tr>
<tr>
<td>DMA 0 source address high register</td>
<td>C2h</td>
<td>9-9</td>
</tr>
<tr>
<td>DMA 0 source address low register</td>
<td>C0h</td>
<td>9-10</td>
</tr>
<tr>
<td>Chip-Select Registers: Chapter 5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PCS and MCS auxiliary register</td>
<td>A8h</td>
<td>5-10</td>
</tr>
<tr>
<td>Midrange memory chip-select register</td>
<td>A6h</td>
<td>5-8</td>
</tr>
<tr>
<td>Low memory chip-select register</td>
<td>A4h</td>
<td>5-12</td>
</tr>
<tr>
<td>Upper memory chip-select register</td>
<td>A2h</td>
<td>5-6</td>
</tr>
<tr>
<td>Serial Port 0 Registers: Chapter 10</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Serial port 0 baud rate divisor register</td>
<td>8Ah</td>
<td>10-13</td>
</tr>
<tr>
<td>Serial port 0 receive register</td>
<td>88h</td>
<td>10-12</td>
</tr>
<tr>
<td>Serial port 0 transmit register</td>
<td>84h</td>
<td>10-11</td>
</tr>
<tr>
<td>Serial port 0 status register</td>
<td>82h</td>
<td>10-9</td>
</tr>
<tr>
<td>Serial port 0 control register</td>
<td>80h</td>
<td>10-5</td>
</tr>
<tr>
<td>PIO Registers: Chapter 11</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PIO data 1 register</td>
<td>74h</td>
<td>11-5</td>
</tr>
<tr>
<td>PIO direction 1 register</td>
<td>73h</td>
<td>11-4</td>
</tr>
<tr>
<td>PIO mode 1 register</td>
<td>76h</td>
<td>11-3</td>
</tr>
<tr>
<td>PIO data 0 register</td>
<td>74h</td>
<td>11-5</td>
</tr>
<tr>
<td>PIO direction 0 register</td>
<td>72h</td>
<td>11-4</td>
</tr>
<tr>
<td>PIO mode 0 register</td>
<td>70h</td>
<td>11-3</td>
</tr>
</tbody>
</table>

### Peripheral Control Block Relocation Register (RELREG, Offset FEh)

The peripheral control block is mapped into either memory or I/O space by programming the Peripheral Control Block Relocation (RELREG) register (see Figure 4-1). This register is a 16-bit register at offset FEh from the control block base address. The Peripheral Control Block Relocation register provides the upper 12 bits of the base address of the control block. The control block is effectively an internal chip select range.

Other chip selects can overlap the control block only if they are programmed to zero wait states and ignore external ready. If the control register block is mapped into I/O space, the upper four bits of the base address must be programmed as 0000b (since I/O addresses are only 16 bits wide).

In addition to providing relocation information for the control block, the Peripheral Control Block Relocation register contains a bit that places the interrupt controller into either slave mode or master mode.

At reset, the Peripheral Control Block Relocation register is set to 20FFh, which maps the control block to start at FF00h in I/O space. An offset map of the 256-byte peripheral control block register is shown in Table 4-1.

#### Figure 4-1 Peripheral Control Block Relocation Register

The value of the RELREG register is 20FFh at reset.

Bit 15: Reserved

Bit 14: Slave/Master (S/M)—Configures the interrupt controller for slave mode when set to 1 and for master mode when set to 0.

Bit 13: Reserved

Bit 12: Memory/Io Space (M/I)—When set to 1, the peripheral control block (PCB) is located in memory space. When set to 0, the PCB is located in I/O space.

Bits 11–0: Relocation Address Bits (R19–R0)—R19–R0 define the upper address bits of the PCB base address. The lower 8 bits (R7–R0) default to 00h. R19–R16 are ignored when the PCB is mapped to I/O space.
4.1.2 Reset Configuration Register (RESCON, Offset F6h)

The Reset Configuration (RESCON) register (see Figure 4-2) in the peripheral control block latches system configuration information that is presented to the processor on the address/data bus (AD15–AD0 for the 186 or AO15–AO8 and AD7–AD1 for the 188) during the rising edge of reset. The interpretation of this information is system-specific. The processor does not impose any predetermined interpretation, but simply provides a means for communicating this information to software.

When the RES input is asserted Low, the contents of the address/data bus are written into the Reset Configuration register. The system can place configuration information on the address/data bus using weak external pullup or pulldown resistors, or using an external driver that is enabled during reset. The processor does not drive the address/data bus during reset.

For example, the Reset Configuration register could be used to provide the software with the position of a configuration switch in the system. Using weak external pullup and pulldown resistors on the address and data bus, the system could provide the microcontroller with a value corresponding to the position of a jumper during a reset.

The value of the RESCON register is system-dependent.

Bits 15-0: Reset Configuration (RC)—There is a one-to-one correspondence between address/data bus signals during the reset and the Reset Configuration register's bits. On the Am186ES microcontroller, AD15 corresponds to bit 15 of the Reset Configuration register, and so on. On the Am188ES microcontroller, AO15 corresponds to register bit 15 and AD7 corresponds to bit 7. Once RES is deasserted, the Reset Configuration register holds its value. This value can be read by software to determine the configuration information.

The contents of the Reset Configuration register are read-only and remain valid until the next processor reset.

---

4.1.3 Processor Release Level Register (PRL, Offset F4h)

The Processor Release Level register (Figure 4-3) is a read-only register that specifies the processor version.

**Figure 4-3 Processor Release Level Register**

Bits 15-8: Processor Release Level (PRL)—This byte returns the current release level of the processor, as well as the identification of the family member. The Am186ES and Am188ES microcontrollers' revision A PRL is 10h.

Bits 7-0: Reserved

**Table 4-2 Processor Release Level (PRL) Values**

<table>
<thead>
<tr>
<th>PRL Value</th>
<th>Processor Release Level</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>A</td>
</tr>
<tr>
<td>0x1</td>
<td>B</td>
</tr>
<tr>
<td>0x2</td>
<td>C</td>
</tr>
<tr>
<td>0x3</td>
<td>D</td>
</tr>
<tr>
<td>0x4</td>
<td>E</td>
</tr>
</tbody>
</table>
4.1.4 Auxiliary Configuration Register (AUXCON, Offset F2h)

The auxiliary configuration register is used to configure the asynchronous serial port flow-control signals and to configure the data bus width for memory and I/O accesses. The format of the auxiliary configuration register is shown in Figure 4-4.

The reset value of this register is 0000h.

Bits 15-7: Reserved

Bit 6: Serial Port 1 Enable Receiver Request (ENRX1) — When this bit is 1, the CTS1/ENRX1 pin is configured as ENRX1. When this bit is 0, the CTS1/ENRX1 pin is configured as CTS1. This bit is 0 after processor reset.

Bit 5: Serial Port 1 Request to Send (RTS1) — When this bit is 1, the RTS1/RTS1 pin is configured as RTS1. When this bit is 0, the RTS1/RTS1 pin is configured as RTS1. This bit is 0 after processor reset.

Bit 4: Serial Port 0 Enable Receiver Request (ENRX0) — When this bit is 1, the CTS0/ENRX0 pin is configured as ENRX0. When this bit is 0, the CTS0/ENRX0 pin is configured as CTS0. This bit is 0 after processor reset.

Bit 3: Serial Port 0 Request to Send (RTS0) — When this bit is 1, the RTS0/RTS0 pin is configured as RTS0. When this bit is 0, the RTS0/RTS0 pin is configured as RTS0. This bit is 0 after processor reset.

Bit 2: LCS Data Bus Size (LSIZ) — (Am186ES microcontroller only) This bit determines the width of the data bus for access to LCS space. If this bit is 1, 8-bit accesses are performed. If this bit is 0, 16-bit accesses are performed. This bit should not be modified while executing from LCS space or while the PCB is overlaid with LCS space. This bit is 0 after processor or reset.

Bit 1: Midrange Data Bus Size (MSIZ) — (Am186ES microcontroller only) This bit determines the width of the data bus for memory accesses which do not fall into the UCS or LCS address spaces, including MCS address space and PCS address space, if mapped to memory. If this bit is 1, 8-bit accesses are performed. If this bit is 0, 16-bit accesses are performed. This bit should not be modified while executing from the associated address space or while the PCB is overlaid on this address space. This bit is 0 after processor or reset.

Bit 0: I/O Space Data Bus Size (IOSIZ) — (Am186ES microcontroller only) This bit determines the width of the data bus for all I/O space accesses. If this bit is 1, 8-bit accesses are performed. If this bit is 0, 16-bit accesses are performed. This bit is 0 after processor reset. This bit should not be modified while the PCS is located in I/O space.

4.1.5 System Configuration Register (SYSCON, Offset F0h)

The format of the system configuration register is shown in Figure 4-5.

The value of the SYSCON register at reset is 0000h.

Bit 15: Enable Power-Save Mode (PSEN) — When set to 1, enables power-save mode and divides the internal operating clock by the value in F2–F0. PSEN is automatically cleared when an external interrupt, including those generated by on-chip peripheral devices, occurs. The value of the PSEN bit is not restored by the execution of an IRET instruction. Software interrupts (INT instruction) and exceptions do not clear the PSEN bit, and interrupt service routines for these conditions should do so, if desired. This bit is 0 after processor reset.

Bit 14: MCS0 Only Mode Bit (MCSBIT) — This bit controls the MCS0 only mode. When set to 0, the middle chip selects operate normally. When set to 1, MCS0 is active over the entire MCS range. This bit is 0 after processor reset.

Bit 13: Data Strobe Mode of DEN Enable (DSDEN) — This bit enables the data strobe timings on the DEN pin. When this bit is set to 1, data strobe bus mode is enabled, and the TS timing for reads and writes is identical to the normal write cycle DEN timing. When this bit is set to 0, the TS timing for both reads and writes is normal. The DEN pin is renamed TS in data strobe bus mode. This bit is 0 after processor reset.

During the bus cycle in which the DSDEN bit of the SYSCON register is written, the timing of the DEN/TS pin is slightly different from normal. When a 1 is written to the DSDEN bit (which previously contained a 0), the falling edge of DEN/TS occurs during PH2 of T1 as it does during a normal write cycle, but the rising edge occurs during PH1 of T1 in conformance with the data strobe timing. All writes after this have the normal data strobe timing until the DSDEN bit is reset.

When a 0 is written to the DSDEN bit (which previously contained a 1), the falling edge of DEN/TS occurs during PH2 of T1 as it does with the data strobe timing, but the rising edge occurs during PH1 of T1 in conformance with the normal write cycle timing. All writes after this have the normal write cycle timing until the DSDEN bit is set again.

Bit 12: Pulse Width Demodulation Mode Enable (PWE) — This bit enables pulse width modulation mode. When this bit is set to 1, pulse width modulation is enabled. When this bit is set to 0, pulse width modulation is disabled. This bit is 0 after processor reset.

Bit 11: CLKOUTB Output Frequency (CBF) — When set to 1, CLKOUTB is enabled and follows the crystal input (PLL) frequency. When set to 0, CLKOUTB follows the internal processor frequency (after the clock divider). This bit is 0 after processor reset.
CLKOUTB can be used as a full-speed clock source in power-save mode.

Bit 10: CLKOUTB Drive Disable (CBD)—When set to 1, CBD three-states the clock output driver for CLKOUTB. When set to 0, CLKOUTB is driven as an output. This bit is 0 after processor reset.

Bit 9: CLKOUTA Output Frequency (CAF)—When set to 1, CLKOUTA follows the crystal input (PLL) frequency. When set to 0, CLKOUTA follows the internal processor frequency (after the clock divider). This bit is 0 after processor reset.

CLKOUTA can be used as a full-speed clock source in power-save mode.

Bit 8: CLKOUTA Drive Disable (CAD)—When set to 1, CAD three-states the clock output driver for CLKOUTA. When set to 0, CLKOUTA is driven as an output. This bit is 0 after processor reset.

Bits 7–3: Reserved—Read back as 0.

Bits 2–0: Clock Divider Select (F2–F0)—Controls the division factor when Power-Save mode is enabled. F2—F0 is 000b after processor reset. Allowable values are as follows:

<table>
<thead>
<tr>
<th>F2</th>
<th>F1</th>
<th>F0</th>
<th>Divider Factor</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Divide by 1 (2^0)</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Divide by 2 (2^1)</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Divide by 4 (2^2)</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>Divide by 8 (2^3)</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Divide by 16 (2^4)</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>Divide by 32 (2^5)</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>Divide by 64 (2^6)</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>Divide by 128 (2^7)</td>
</tr>
</tbody>
</table>

4.2 INITIALIZATION AND PROCESSOR RESET

Processor initialization or startup is accomplished by driving the RES input pin Low. RES must be Low during power-up to ensure proper device initialization. RES forces the Am186ES and Am188ES microcontrollers to terminate all execution and local bus activity. No instruction or bus activity occurs as long as RES is active.

After RES is deasserted and an internal processing interval elapses, the microcontroller begins execution with the instruction at physical location FFFF0h. RES also sets some registers to predefined values as shown in Table 4-3.

5.5.1 Upper Memory Chip Select Register (UMCS, Offset A0h)

The Am186ES and Am188ES microcontrollers provide the UCS chip select pin for the top of memory. On reset, the microcontroller begins fetching and executing instructions starting at memory location FFFF0h, so upper memory is usually used as instruction memory. To facilitate this usage, UCS defaults to active on reset with a default memory range of 64 Kbytes from F0000h to FFFFFh, with external ready required and three wait states automatically inserted.

The UCS memory range always ends at FFFFFh. The lower boundary is programmable. The Upper Memory Chip Select is configured through the UMCS register (Figure 5-1).

![Figure 5-1 Upper Memory Chip Select Register](image)

The value of the UMCS register at reset is F03Bh.

Bit 15: Reserved—Set to 1.

Bits 14–12: Lower Boundary (LB2–LB0)—The LB2–LB0 bits define the lower bound of the memory access through the UCS chip selects. The number of programmable bits has been reduced from the eight bits in the 80C186 and 80C188 microcontrollers to three bits in the Am186ES and Am188ES microcontrollers.

The Am186ES and Am188ES microcontrollers provide an additional block size of 512K, which is not available on the 80C186 or 80C188 microcontrollers. Table 5-2 outlines the possible configurations and differences with the 80C186 and 80C188 microcontrollers.

<table>
<thead>
<tr>
<th>Memory Block Size</th>
<th>Starting Address</th>
<th>LB2–LB0</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>64K</td>
<td>F0000h</td>
<td>111b</td>
<td>Default</td>
</tr>
<tr>
<td>128K</td>
<td>E0000h</td>
<td>110b</td>
<td></td>
</tr>
<tr>
<td>256K</td>
<td>C0000h</td>
<td>100b</td>
<td></td>
</tr>
<tr>
<td>512K</td>
<td>80000h</td>
<td>000b</td>
<td>Not available on the 80C186 or 80C188 microcontrollers</td>
</tr>
</tbody>
</table>
Bits 11–8: Reserved

Bit 7: Disable Address (DA)—The DA bit enables or disables the AD15–AD0 bus during the address phase of a bus cycle when UCS is asserted. If DA is set to 1, AD15–AD0 is not driven during the address phase of a bus cycle when UCS is asserted. If DA is set to 0, AD15–AD0 is driven during the address phase of a bus cycle. Disabling AD15–AD0 reduces power consumption. DA defaults to 0 at power-on reset.

Note: On the Am188ES microcontroller, the AO15–AO8 address pins are driven during the data phase of the bus cycles, even when DA is set to 1 in either the Upper Memory Chip Select register (UMCS) or the Low Memory Chip Select register (LMCS).

If BHE/ADEN (on the 186) or RFSH2/ADEN (on the 188) is held Low on the rising edge of RES, then AD15–AD0 is always driven regardless of the DA setting. This configures AD15–AD0 to be enabled regardless of the setting of DA.

If BHE/ADEN (on the 186) or RFSH2/ADEN (on the 188) is High on the rising edge of RES, then DA in the Upper Memory Chip Select (UMCS) register and DA in the Low Memory Chip Select (LMCS) register control the AD15–AD0 disabling.

See the descriptions of the BHE/ADEN and RFSH2/ADEN pins in Chapter 3.

Bit 6: Reserved—Set to 0.

Bits 5–3: Reserved—Set to 1.

Bit 2: Ready Mode (R2)—The R2 bit is used to configure the ready mode for the UCS chip select. If R2 is set to 0, external ready is required. If R2 is set to 1, external ready is ignored. In each case, the processor also uses the value of the R1–R0 bits to determine the number of wait states to insert. R2 defaults to 0 at reset.

Bits 1–0: Wait-State Value (R1–R0)—The value of R1–R0 determines the number of wait states inserted into an access to the UCS memory area. From zero to three wait states can be inserted (R1–R0 = 00b to 11b). R1–R0 default to 11b at reset.

5.5.2 Low Memory Chip Select Register (LMCS, Offset A2h)

The Am186ES and Am188ES microcontrollers provide the UCS chip select pin for the bottom of memory. Since the interrupt vector table is located at 00000h at the bottom of memory, the UCS pin has been provided to facilitate this usage. The UCS pin is not active on reset, but any write access to the LMCS register activates this pin.

Before activating the UCS chip select, the width of the data bus for UCS space should be configured in the AUXCON register.

The Low Memory Chip Select is configured through the LMCS register (see Figure 5-2).

Figure 5-2 Low Memory Chip Select Register

The value of the LMCS register at reset is undefined except DA is set to 0.

Bit 15: Reserved—Set to 0.

Bits 14–12: Upper Boundary (UB2–UB0)—The UB2–UB0 bits define the upper boundary of the memory accessed through the UCS chip select. Because of the timing requirements of the UCS output and the nonmultiplexed address bus, the number of programmable memory sizes for the LMCS register is reduced compared to the 80C186 and 80C188 microcontrollers. Consequently, the number of programmable bits has been reduced from eight bits in the 80C186 and 80C188 microcontrollers to three bits in the Am186ES and Am188ES microcontrollers.

The Am186ES and Am188ES microcontrollers have a block size of 512 Kbytes, which is not available on the 80C186 and 80C188 microcontrollers. Table 5-3 outlines the possible configurations.

Table 5-3 LMCS Block Size Programming Values

<table>
<thead>
<tr>
<th>Memory Block Size</th>
<th>Ending Address</th>
<th>UB2–UB0</th>
</tr>
</thead>
<tbody>
<tr>
<td>64K</td>
<td>0FFFFh</td>
<td>00b</td>
</tr>
<tr>
<td>128K</td>
<td>1FFFFh</td>
<td>00b</td>
</tr>
<tr>
<td>256K</td>
<td>3FFFFh</td>
<td>01b</td>
</tr>
<tr>
<td>512K</td>
<td>7FFFFh</td>
<td>11b</td>
</tr>
</tbody>
</table>
The Am186ES and Am188ES microcontrollers provide four chip select pins, MCS0–MCS3, for use within a user-locatable memory block. The base address of the memory block can be located anywhere within the 1-Mbyte memory address space, exclusive of the areas associated with the UCS and LCS chip selects (and, if they are mapped to memory, the address range of the Peripheral Chip Selects, PCS0–PCS3 and RFSH–RFSH3). The LCS address range can overlap the PCS address range if the PCS chip selects are mapped to I/O space.

The Midrange Memory Chip Selects are programmed through two registers. The Midrange Memory Chip Select (MMCS) register (see Figure 5-3) determines the base address and the ready condition and wait states of the memory block accessed through the MCS chip select. If BHE is set to 1, external Ready is required. If BHE is set to 0, external Ready is ignored. In each case, the processor also uses the value of the R1–R0 bits to determine the number of wait states inserted into an access to the LCS memory area. From zero to three wait states can be inserted (R1–R0 = 00b to 11b).

Contrary to earlier timing of the A19–A0 bus, the A19–A0 bus can still be used for address selection, but the timing is delayed for a half cycle later than that for UCS and LCS.

The value of the MMCS register at reset is undefined.

Bits 15–9: Base Address (BA19–BA13)—The base address of the memory block that is addressed by the MCS chip select pins is determined by the value of BA19–BA13. These bits correspond to bits A19–A13 of the 20-bit memory address. Bits A12–A0 of the base address are always 0.

The base address can be set to any integer multiple of the size of the memory block size selected in the MPCS register. For example, if the midrange block is 32 Kbytes, the block could be located at 10000h or 18000h but not at 14000h.

The base address of the midrange chip selects can be set to 00000h or any other address within the 1-Mbyte memory address space, exclusive of the areas associated with the UCS and LCS chip selects (and, if they are mapped to memory, the address range of the Peripheral Chip Selects, PCS0–PCS3 and RFSH–RFSH3). The LCS address range can overlap the PCS address range if the PCS chip selects are mapped to I/O space.

The Midrange Memory Chip Selects are configured by the MMCS register (Figure 5-3).
Bits 8–3: Reserved—Set to 1.

Bit 2: Ready Mode (R2)—The R2 bit is used to configure the ready mode for the MCS chip selects. If R2 is set to 0, external ready is required. If R2 is set to 1, external ready is ignored. In each case, the processor also uses the value of the R1–R0 bits to determine the number of wait states to insert.

Bits 1–0: Wait-State Value (R1–R0)—The value of R1–R0 determines the number of wait states inserted into an access to the MCS memory area. From zero to three wait states can be inserted (R1–R0 = 00b to 11b).

5.5.4 PCS and MCS Auxiliary Register (MPCS, Offset A8h)

The PCS and MCS Auxiliary (MPCS) register (see Figure 5-4) differs from the other chip select control registers in that it contains fields that pertain to more than one type of chip select. The MPCS register fields provide program information for MCS0–MCS3 as well as PCS5–PCS0.

In addition to its function as a chip select control register, the MPCS register contains a field that configures the PCS6–PCS5 pins as either chip selects or as alternate sources for the A2 and A1 address bits. When programmed to provide address bits A1 and A2, PCS6–PCS5 cannot be used as peripheral chip selects. These outputs can be used to provide latched address bits for A2 and A1.

On reset, PCS6–PCS5 are not active. If PCS6–PCS5 are configured as address pins, an access to the MPCS register causes the pins to activate. No corresponding access to the PACS register is required to activate the PCS6–PCS5 pins as addresses.

Figure 5-4 PCS and MCS Auxiliary Register

The value of the MPCS register at reset is undefined.

Bit 15: Reserved—Set to 1.

Bits 14–8: MCS Block Size (M6–M0)—This field determines the total block size for the MCS3–MCS0 chip selects. Each individual chip select is active for one quarter of the total block size. The size of the memory block defined is shown in Table 5-4.

Only one of the bits M6–M0 can be set at any time. If more than one of the M6–M0 bits is set, unpredictable operation of the MCS lines occurs.

If the MCSBIT in the SYSCON register is set, MCS0 asserts over the entire programmed block size. MCS3–MCS1 will continue to assert over their programmed range but are typically used as PIO's in the configuration.

Table 5-4 MCS Block Size Programming

<table>
<thead>
<tr>
<th>Total Block Size</th>
<th>Individual Select Size</th>
<th>M6–M0</th>
</tr>
</thead>
<tbody>
<tr>
<td>8K</td>
<td>2K</td>
<td>0000001b</td>
</tr>
<tr>
<td>16K</td>
<td>4K</td>
<td>0000010b</td>
</tr>
<tr>
<td>32K</td>
<td>8K</td>
<td>0000100b</td>
</tr>
<tr>
<td>64K</td>
<td>16K</td>
<td>0001000b</td>
</tr>
<tr>
<td>128K</td>
<td>32K</td>
<td>0010000b</td>
</tr>
<tr>
<td>256K</td>
<td>64K</td>
<td>0100000b</td>
</tr>
<tr>
<td>512K</td>
<td>128K</td>
<td>1000000b</td>
</tr>
</tbody>
</table>
Bit 7: Pin Selector (EX)—This bit determines whether the PCS6–PCS5 pins are configured as chip selects or as alternate outputs for A2–A1. When this bit is set to 1, PCS6–PCS5 are configured as peripheral chip select pins. When EX is set to 0, PCS5 becomes address bit A1 and PCS6 becomes address bit A2.

Bit 6: Memory/I/O Space Selector (MS)—This bit determines whether the PCS pins are active during memory bus cycles or I/O bus cycles. When MS is set to 1, the PCS outputs are active for memory bus cycles. When MS is set to 0, the PCS outputs are active for I/O bus cycles.

Bits 5–3: Reserved—Set to 1.

Bit 2: Ready Mode (R2)—This bit applies only to the PCS6–PCS5 chip selects. If R2 is set to 0, external ready is required. If R2 is set to 1, external ready is ignored. In each case, the processor also uses the value of the R1–R0 bits to determine the number of wait states to insert.

Bits 1–0: Wait-State Value (R1–R0)—These bits apply only to the PCS6–PCS5 chip selects. The value of R1–R0 determines the number of wait states inserted into an access to the PCS memory or I/O area. From zero to three wait states can be inserted (R1–R0 = 00b to 11b).

5.5.5 Peripheral Chip Select Register (PACS, Offset A4h)

Unlike the UCS and LCS chip selects, the PCS outputs assert with the same timing as the multiplexed AD address bus. Also, each peripheral chip select asserts over a 256-byte address range, which is twice the address range covered by peripheral chip selects in the 80C186 and 80C188 microcontrollers.

The Am186ES and Am188ES microcontrollers provide six chip selects, PCS6–PCS5, for use within a user-locatable memory or I/O block. PCS4 is not implemented on the Am186ES and Am188ES microcontrollers. The base address of the memory block can be located anywhere within the 1-Mbyte memory address space, exclusive of the areas associated with the UCS, LCS, and MCS chip selects, or they can be configured to access the 64-Kbyte I/O space.

The Peripheral Chip Selects are programmed through two registers—the Peripheral Chip Select (PACS) register and the PCS and MCS Auxiliary (MPCS) register. The Peripheral Chip Select (PACS) register (Figure 5-5) determines the base address, the ready condition, and the wait states for the PCS6–PCS5 outputs.

The MPCS register (Figure 5-4) contains bits that configure the PCS6–PCS5 pins as either chip selects or address pins A1 and A2. When the PCS6–PCS5 pins are chip selects, the MPCS register also determines whether PCS chip selects are active during memory or I/O bus cycles and specifies the ready and wait states for the PCS6–PCS5 outputs.

The PCS pins are not active on reset. The PCS pins are activated as chip selects by writing to the PACS and MPCS registers.

PCS6–PCS5 can be configured and activated as address pins by writing only the MPCS register. No corresponding access to the PACS register is required in this case.

PCS3–PCS0 can be configured for zero wait states to 15 wait states. PCS6–PCS5 can be configured for zero wait states to three wait states.

Figure 5-5 Peripheral Chip Select Register

The value of the PACS register at reset is undefined.

Bits 15–7: Base Address (BA19–BA11)—The base address of the peripheral chip select block is defined by BA19–BA11 of the PACS register. BA19–BA11 correspond to bits 19–11 of the 20-bit programmable base address of the peripheral chip select block. Bit 6 of the PACS register corresponds to bit 10 of the base address in the original 80C186 and 80C188 microcontrollers and is not implemented. Thus, code previously written for the 80C186 microcontroller in which bit 6 was set with a meaningful value would not produce the address expected on the Am186ES microcontroller.

When the PCS chip selects are mapped to I/O space, BA19–16 must be programmed to 0000b because the I/O address bus is only 16 bits wide.
Table 5-5  PCS Address Ranges

<table>
<thead>
<tr>
<th>PCS Line</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCS0</td>
<td>Base Address</td>
</tr>
<tr>
<td></td>
<td>+255</td>
</tr>
<tr>
<td>PCS1</td>
<td>Base Address +256</td>
</tr>
<tr>
<td></td>
<td>+511</td>
</tr>
<tr>
<td>PCS2</td>
<td>Base Address +512</td>
</tr>
<tr>
<td></td>
<td>+767</td>
</tr>
<tr>
<td>PCS3</td>
<td>Base Address +768</td>
</tr>
<tr>
<td></td>
<td>+1023</td>
</tr>
<tr>
<td>Reserved</td>
<td>N/A</td>
</tr>
<tr>
<td>PCS5</td>
<td>Base Address +1280</td>
</tr>
<tr>
<td></td>
<td>+1535</td>
</tr>
<tr>
<td>PCS6</td>
<td>Base Address +1536</td>
</tr>
<tr>
<td></td>
<td>+1791</td>
</tr>
</tbody>
</table>

Bits 6–4: Reserved—Set to 1.

Bit 3: Wait-State Value (R3)—If this bit is set to 0, the number of wait states from zero to three is encoded in the R1–R0 bits. In this case, R1–R0 encodes from zero (00b) to three (11b) wait states.

When R3 is set to 1, the four possible values of R1–R0 encode four additional wait-state values as follows: 00b = 5 wait states, 01b = 7 wait states, 10b = 9 wait states, and 11b = 15 wait states. Table 5-6 shows the wait-state encoding.

Table 5-6  PCS3–PCS5 Wait-State Encoding

<table>
<thead>
<tr>
<th>R3</th>
<th>R1</th>
<th>R0</th>
<th>Wait States</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>2</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>3</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>5</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>7</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>9</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>15</td>
</tr>
</tbody>
</table>

Bit 2: Ready Mode (R2)—The R2 bit is used to configure the ready mode for the PCS3–PCS5 chip selects. If R2 is set to 0, external ready is required. External ready is ignored when R2 is set to 1. In each case, the processor also uses the value of the R3 and R1–R0 bits to determine the number of wait states to insert. The ready modes for PCS5–PCS6 is configured through the MPC5 register.

Bits 1–0: Wait-State Value (R1–R0)—The value of R3 and R1–R0 determines the number of wait states inserted into a PCS3–PCS5 access. Up to 15 wait states can be inserted. See the discussion of bit 3 (R3) for the wait-state encoding of R1–R0.

From zero to three wait states for the PCS6–PCS5 outputs are programmed through the R1–R0 bits in the MPC5 register.

Table 7-1  Am186ES and Am188ES Microcontroller Interrupt Types

<table>
<thead>
<tr>
<th>Interrupt Name</th>
<th>Interrupt Type</th>
<th>Vector Table Address</th>
<th>EOI Type</th>
<th>Overall Priority</th>
<th>Related Instructions</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Divide Error Exception</td>
<td>00h</td>
<td>00h</td>
<td>N/A</td>
<td>1</td>
<td>DIV, DIV</td>
<td>1</td>
</tr>
<tr>
<td>Trace Interrupt</td>
<td>01h</td>
<td>04h</td>
<td>N/A</td>
<td>1A</td>
<td>All</td>
<td>2</td>
</tr>
<tr>
<td>Nonmaskable Interrupt (NMI)</td>
<td>02h</td>
<td>08h</td>
<td>N/A</td>
<td>1B</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Breakpoint Interrupt</td>
<td>03h</td>
<td>0Ch</td>
<td>N/A</td>
<td>1</td>
<td>INTO</td>
<td>1</td>
</tr>
<tr>
<td>INT0 Detected Overflow Exception</td>
<td>04h</td>
<td>10h</td>
<td>N/A</td>
<td>1</td>
<td>INTO</td>
<td>1</td>
</tr>
<tr>
<td>Array Bounds Exception</td>
<td>05h</td>
<td>14h</td>
<td>N/A</td>
<td>1</td>
<td>BOUND</td>
<td>1</td>
</tr>
<tr>
<td>Unused Opcode Exception</td>
<td>06h</td>
<td>18h</td>
<td>N/A</td>
<td>1</td>
<td>Undefined Opcodes</td>
<td>1</td>
</tr>
<tr>
<td>ESC Opcode Exception</td>
<td>07h</td>
<td>1Ch</td>
<td>N/A</td>
<td>1</td>
<td>ESC Opcodes</td>
<td>1, 3</td>
</tr>
<tr>
<td>Timer 0 Interrupt</td>
<td>08h</td>
<td>20h</td>
<td>08h</td>
<td>2A</td>
<td>4</td>
<td>5</td>
</tr>
<tr>
<td>Timer 1 Interrupt</td>
<td>09h</td>
<td>24h</td>
<td>08h</td>
<td>2B</td>
<td>4</td>
<td>5</td>
</tr>
<tr>
<td>Timer 2 Interrupt</td>
<td>0Ah</td>
<td>28h</td>
<td>0Ch</td>
<td>2C</td>
<td>4</td>
<td>5</td>
</tr>
<tr>
<td>Reserved for AMD Use</td>
<td>0Bh</td>
<td>2Ch</td>
<td>0Bh</td>
<td>3</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td>DMA 0 Interrupt/INT5</td>
<td>0Ch</td>
<td>30h</td>
<td>0Ch</td>
<td>5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DMA 1 Interrupt/INT6</td>
<td>0Dh</td>
<td>32h</td>
<td>0Ch</td>
<td>6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>INT0 Interrupt</td>
<td>0Fh</td>
<td>34h</td>
<td>0Ch</td>
<td>7</td>
<td></td>
<td></td>
</tr>
<tr>
<td>INT1 Interrupt</td>
<td>10h</td>
<td>36h</td>
<td>0Ch</td>
<td>8</td>
<td></td>
<td></td>
</tr>
<tr>
<td>INT2 Interrupt</td>
<td>11h</td>
<td>38h</td>
<td>0Ch</td>
<td>9</td>
<td></td>
<td></td>
</tr>
<tr>
<td>INT3 Interrupt</td>
<td>12h</td>
<td>3Ah</td>
<td>0Ch</td>
<td>10</td>
<td></td>
<td></td>
</tr>
<tr>
<td>INT4 Interrupt</td>
<td>13h</td>
<td>3Ch</td>
<td>0Ch</td>
<td>11</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Asynchronous Serial Port1 Interface</td>
<td>14h</td>
<td>42h</td>
<td>14h</td>
<td>12</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Asynchronous Serial Port0 Interrupt</td>
<td>15h</td>
<td>44h</td>
<td>14h</td>
<td>13</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reserved for AMD Use</td>
<td>16h–1Fh</td>
<td>54h–7Ch</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Notes:
1. Default priorities for the interrupt sources are used if the user does not reprogram priority levels.
2. Trace is performed in the same manner as 8086 and 8088.
3. An ESC opcode causes a trap.
4. All three timers constitute one source of request to the interrupt controller. As such, they share the same priority level with respect to other interrupt sources. However, the timers have a defined priority order among themselves (2A > 2B > 2C).
5. The interrupt types of these sources are programmable in slave mode.
6. Not available in slave mode.
### 7.3 MASTER MODE INTERRUPT CONTROLLER REGISTERS

The interrupt controller registers for master mode are shown in Table 7-2. All the registers can be read and written unless otherwise specified.

Registers can be redefined in slave mode. See Section 7.4 on page 7-28 for detailed information regarding slave mode register usage. On reset, the microcontroller is in master mode. Bit 14 of the Peripheral Control Block Relocation register (see Figure 4-1) must be set to initiate slave mode operation.

#### Table 7-2 Interrupt Controller Registers in Master Mode

<table>
<thead>
<tr>
<th>Offset</th>
<th>Register</th>
<th>Mnemonic</th>
<th>Register Name</th>
<th>Associated Pins</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>38h</td>
<td>I0CON</td>
<td>INT0 Control</td>
<td>INT0</td>
<td>INT0</td>
<td></td>
</tr>
<tr>
<td>3Ah</td>
<td>I1CON</td>
<td>INT1 Control</td>
<td>INT1</td>
<td>INT1</td>
<td></td>
</tr>
<tr>
<td>3Ch</td>
<td>I2CON</td>
<td>INT2 Control</td>
<td>INT2</td>
<td>INT2</td>
<td></td>
</tr>
<tr>
<td>3Eh</td>
<td>I3CON</td>
<td>INT3 Control</td>
<td>INT3</td>
<td>INT3</td>
<td></td>
</tr>
<tr>
<td>40h</td>
<td>I4CON</td>
<td>INT4 Control</td>
<td>INT4</td>
<td>INT4</td>
<td></td>
</tr>
<tr>
<td>44h</td>
<td>DMA0CON</td>
<td>DMA0 Interrupt Control/INT5</td>
<td>INT5</td>
<td>INT5</td>
<td></td>
</tr>
<tr>
<td>42h</td>
<td>DMA1CON</td>
<td>DMA1 Interrupt Control/INT6</td>
<td>INT6</td>
<td>INT6</td>
<td></td>
</tr>
<tr>
<td>44h</td>
<td>TCUCON</td>
<td>Timer Interrupt Control</td>
<td>TMRIN1</td>
<td>TMRIN1</td>
<td>TMROUT1</td>
</tr>
<tr>
<td>46h</td>
<td>SP0CON</td>
<td>Serial Port 0 Interrupt Control</td>
<td>SP0</td>
<td>SP0</td>
<td></td>
</tr>
<tr>
<td>48h</td>
<td>SP1CON</td>
<td>Serial Port 1 Interrupt Control</td>
<td>SP1</td>
<td>SP1</td>
<td></td>
</tr>
<tr>
<td>2Eh</td>
<td>REQST</td>
<td>Interrupt Request</td>
<td>INT6–INT0</td>
<td>Read-only register</td>
<td></td>
</tr>
<tr>
<td>2Ch</td>
<td>INSERV</td>
<td>In-Service</td>
<td>INT6–INT0</td>
<td>Read-only register</td>
<td></td>
</tr>
<tr>
<td>26h</td>
<td>IMASK</td>
<td>Interrupt Mask</td>
<td>INT6–INT0</td>
<td>Write-only register</td>
<td></td>
</tr>
<tr>
<td>24h</td>
<td>POOLLST</td>
<td>Poll Status</td>
<td>INT6–INT0</td>
<td>Read-only register</td>
<td></td>
</tr>
<tr>
<td>22h</td>
<td>EOI</td>
<td>End of Interrupt</td>
<td>INT6–INT0</td>
<td>Write-only register</td>
<td></td>
</tr>
</tbody>
</table>

#### 7.3.1 INT0 and INT1 Control Registers

**(I0CON, Offset 38h, I1CON, Offset 3Ah)** *(Master Mode)*

The INT0 interrupt is assigned to interrupt type 0Ch. The INT1 interrupt is assigned to interrupt type 0Dh.

When cascade mode is enabled for INT0 by setting the C bit of I0CON to 1, the INT2 pin becomes INTA0, the interrupt acknowledge for INT0.

When cascade mode is enabled for INT1 by setting the C bit of I1CON to 1, the INT3 pin becomes INTA1, the interrupt acknowledge for INT1.

<table>
<thead>
<tr>
<th>Offset</th>
<th>Register</th>
<th>Mnemonic</th>
<th>Register Name</th>
<th>Associated Pins</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>38h</td>
<td>I0CON</td>
<td>INT0 Control</td>
<td>INT0</td>
<td>INT0</td>
<td></td>
</tr>
<tr>
<td>3Ah</td>
<td>I1CON</td>
<td>INT1 Control</td>
<td>INT1</td>
<td>INT1</td>
<td></td>
</tr>
<tr>
<td>3Ch</td>
<td>I2CON</td>
<td>INT2 Control</td>
<td>INT2</td>
<td>INT2</td>
<td></td>
</tr>
<tr>
<td>3Eh</td>
<td>I3CON</td>
<td>INT3 Control</td>
<td>INT3</td>
<td>INT3</td>
<td></td>
</tr>
<tr>
<td>40h</td>
<td>I4CON</td>
<td>INT4 Control</td>
<td>INT4</td>
<td>INT4</td>
<td></td>
</tr>
<tr>
<td>44h</td>
<td>DMA0CON</td>
<td>DMA0 Interrupt Control/INT5</td>
<td>INT5</td>
<td>INT5</td>
<td></td>
</tr>
<tr>
<td>42h</td>
<td>DMA1CON</td>
<td>DMA1 Interrupt Control/INT6</td>
<td>INT6</td>
<td>INT6</td>
<td></td>
</tr>
<tr>
<td>44h</td>
<td>TCUCON</td>
<td>Timer Interrupt Control</td>
<td>TMRIN1</td>
<td>TMRIN1</td>
<td>TMROUT1</td>
</tr>
<tr>
<td>46h</td>
<td>SP0CON</td>
<td>Serial Port 0 Interrupt Control</td>
<td>SP0</td>
<td>SP0</td>
<td></td>
</tr>
<tr>
<td>48h</td>
<td>SP1CON</td>
<td>Serial Port 1 Interrupt Control</td>
<td>SP1</td>
<td>SP1</td>
<td></td>
</tr>
<tr>
<td>2Eh</td>
<td>REQST</td>
<td>Interrupt Request</td>
<td>INT6–INT0</td>
<td>Read-only register</td>
<td></td>
</tr>
<tr>
<td>2Ch</td>
<td>INSERV</td>
<td>In-Service</td>
<td>INT6–INT0</td>
<td>Read-only register</td>
<td></td>
</tr>
<tr>
<td>26h</td>
<td>IMASK</td>
<td>Interrupt Mask</td>
<td>INT6–INT0</td>
<td>Write-only register</td>
<td></td>
</tr>
<tr>
<td>24h</td>
<td>POOLLST</td>
<td>Poll Status</td>
<td>INT6–INT0</td>
<td>Read-only register</td>
<td></td>
</tr>
<tr>
<td>22h</td>
<td>EOI</td>
<td>End of Interrupt</td>
<td>INT6–INT0</td>
<td>Write-only register</td>
<td></td>
</tr>
</tbody>
</table>

The value of I0CON and I1CON at reset is 000Fh.

- **Bits 15–7:** Reserved—Set to 0.
- **Bit 6:** Special Fully Nested Mode (SFNM)—When set to 1, enables special fully nested mode for INT0 or INT1.
- **Bit 5:** Cascade Mode (C)—When set to 1, enables cascade mode for INT0 or INT1.
- **Bit 4:** Level-Triggered Mode (LT) —When set to 1, enables edge-sensitive interrupts. A 0 in this bit enables INT0 or INT1 as a Low-to-High, edge-triggered interrupt. In either case, INT0 or INT1 must remain High until they are acknowledged.
- **Bit 3:** Mask (MSK)—When set to 1, INT0 or INT1 signal can cause an interrupt. A 0 in this bit disables INT0 or INT1 interrupts. This bit is duplicated in the Interrupt Mask register. See the Interrupt Mask register in Section 7.3.10 on page 7-24.
- **Bits 2–0:** Priority Level (PR2–PR0)—This field determines the priority of INT0 or INT1 relative to the other interrupt signals, as shown in Table 7-3 on page 7-18.
7.3.2 INT2 and INT3 Control Registers
(I2CON, Offset 3Ch, I3CON, Offset 3Eh)
(Master Mode)

The INT2 interrupt is assigned to interrupt type OEh. The INT3 interrupt is assigned to interrupt type 0Fh.

The INT2 and INT3 pins can be configured as interrupt acknowledge pins INTA0 and INTA1 when cascade mode is implemented.

Figure 7-5 INT2 and INT3 Control Registers

<table>
<thead>
<tr>
<th>Reserved</th>
<th>LTM</th>
<th>PR2</th>
<th>PR1</th>
<th>PR0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

The value of I2CON and I3CON at reset is 000Fh.

Bits 15–5: Reserved—Set to 0.

Bit 4: Level-Triggered Mode (LTM)—This bit determines whether the microcontroller interprets an INT2 or INT3 interrupt request as edge- or level-sensitive. A 1 in this bit configures INT2 or INT3 as an active High, level-sensitive interrupt. A 0 in this bit configures INT2 or INT3 as a Low-to-High, edge-triggered interrupt. In either case, INT2 or INT3 must remain High until they are acknowledged.

Bit 3: Mask (MSK)—This bit determines whether the INT2 or INT3 signal can cause an interrupt. A 1 in this bit masks this interrupt source, preventing INT2 or INT3 from causing an interrupt. A 0 in this bit enables INT2 or INT3 interrupts.

This bit is duplicated in the Interrupt Mask register. See the Interrupt Mask register in Section 7.3.10 on page 7-24.

Bits 2–0: Priority Level (PR2–PR0)—This field determines the priority of INT2 or INT3 relative to the other interrupt signals, as shown in Table 7-3 on page 7-18.

7.3.3 INT4 Control Register
(I4CON, Offset 40h)
(Master Mode)

The Am186ES and Am188ES microcontrollers provide INT4, an additional external interrupt pin. This input behaves like INT3–INT0 on the 80C186 microcontroller with the exception that INT4 is only intended for use as a fully nested-mode interrupt source. INT4 is not available in cascade mode.

This interrupt is assigned to interrupt type 10h. The Interrupt 4 Control register (see Figure 7-6) controls the operation of the INT4 signal.

Figure 7-6 INT4 Control Register

<table>
<thead>
<tr>
<th>Reserved</th>
<th>LTM</th>
<th>PR2</th>
<th>PR1</th>
<th>PR0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

The value of I4CON at reset is 000Fh.

Bits 15–5: Reserved—Set to 0.

Bit 4: Level-Triggered Mode (LTM)—This bit determines whether the microcontroller interprets an INT4 interrupt request as edge- or level-sensitive. A 1 in this bit configures INT4 as an active High, level-sensitive interrupt. A 0 in this bit configures INT4 as a Low-to-High, edge-triggered interrupt. In either case, INT4 must remain High until it is acknowledged.

Bit 3: Mask (MSK)—This bit determines whether the INT4 signal can cause an interrupt. A 1 in this bit masks this interrupt source, preventing INT4 from causing an interrupt. A 0 in this bit enables INT4 interrupts.

This bit is duplicated in the Interrupt Mask register. See the Interrupt Mask register in Section 7.3.10 on page 7-24.

Bits 2–0: Priority (PR)—This field determines the priority of INT4 relative to the other interrupt signals, as shown in Table 7-3 on page 7-18.
7.3.4 Timer and DMA Interrupt Control Registers
(TCUCON, Offset 32h, DMA0CON/INT5CON, Offset 34h, DMA1CON/INT6CON, Offset 36h)
(Master Mode)
The three timer interrupts are assigned to interrupt type 08h, 12h, and 13h. All three timer
interrupts are configured through TCUCON, offset 32h. The DMA0 interrupt is assigned to
interrupt type 0Ah. The DMA1 interrupt is assigned to interrupt type 0Bh. See the DMA
control registers for how to configure these pins as DMA requests or external interrupts.

The value of TCUCON, DMA0CON, and DMA1CON at reset is 000Fh.

- Bits 15–4: Reserved—Set to 0.
- Bit 3: Interrupt Mask (MSK)—This bit determines whether the corresponding signal can
generate an interrupt. A 1 masks this interrupt source. A 0 enables the corresponding
interrupt.

This bit is duplicated in the Interrupt Mask register. See the Interrupt Mask register in Section
7.3.10 on page 7-24.

- Bits 2–0: Priority Level (PR2–PR0)—Sets the priority level for its corresponding source.
  See Table 7-3 on page 7-18.

7.3.5 Serial Port 0/1 Interrupt Control Registers
(SPOCON/SPICON, Offset 44h/42h)
(Master Mode)
The serial port interrupt control registers control the operation of the serial ports' interrupt
source (SP1 and SP0, bits 10–9 in the interrupt request register). Serial port 0 is assigned
to interrupt type 14h and serial port 1 is assigned to interrupt type 11h. The control register
format is shown in Figure 7-8.

The value of SPOCON and SPICON at reset is 001Fh.

- Bits 15–6: Reserved—Set to 0.
- Bit 5: Reserved—Set to 1.
- Bit 4: Mask (MSK)—This bit determines whether the serial port can cause an interrupt. A
  1 in this bit masks this interrupt source, preventing the serial port from causing an interrupt.
  A 0 in this bit enables serial port interrupts.

This bit is duplicated in the Interrupt Mask register. See the Interrupt Mask register in Section
7.3.10 on page 7-24.

- Bits 2–0: Priority (PR2–PR0)—This field determines the priority of the serial port relative
to the other interrupt signals. After a reset, the priority is 7. See Table 7-3.

<table>
<thead>
<tr>
<th>Priority</th>
<th>PR2–PR0</th>
</tr>
</thead>
<tbody>
<tr>
<td>(High)</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>0 0 0b</td>
</tr>
<tr>
<td>1</td>
<td>0 0 1b</td>
</tr>
<tr>
<td>2</td>
<td>0 1 0b</td>
</tr>
<tr>
<td>3</td>
<td>0 1 1b</td>
</tr>
<tr>
<td>4</td>
<td>1 0 0b</td>
</tr>
<tr>
<td>5</td>
<td>1 0 1b</td>
</tr>
<tr>
<td>6</td>
<td>1 1 0b</td>
</tr>
<tr>
<td>(Low)</td>
<td>7</td>
</tr>
<tr>
<td></td>
<td>1 1 1b</td>
</tr>
</tbody>
</table>
### 7.3.6 Interrupt Status Register (INTSTS, Offset 30h) (Master Mode)

The interrupt status register indicates the interrupt request status of the three timers.

**Figure 7-9 Interrupt Status Register**

<table>
<thead>
<tr>
<th>Bit 15: DMA Halt (DHLT)</th>
<th>— When set to 1, halts any DMA activity. This bit is automatically set to 1 when nonmaskable interrupts occur and is reset when an IRET instruction is executed. Time critical software, such as interrupt handlers, can modify this bit directly to inhibit DMA transfers. Because of the function of this register as an interrupt request register for the timers, the DHLT bit should not be modified by software when timer interrupts are enabled.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bits 14–3: Reserved</td>
<td>— Reserved</td>
</tr>
<tr>
<td>Bits 2–0: Timer Interrupt Request (TMR2–TMR0)</td>
<td>— When set to 1, these bits indicate that the corresponding timer has an interrupt request pending. (Note that the timer TMR bit in the REGST register is the logical OR of these timer interrupt requests.)</td>
</tr>
</tbody>
</table>

### 7.3.7 Interrupt Request Register (REQST, Offset 2Eh) (Master Mode)

The hardware interrupt sources have interrupt request bits inside the interrupt controller. A read from this register yields the status of these bits. The Interrupt Request register is a read-only register. The format of the Interrupt Request register is shown in Figure 7-10.

For internal interrupts (SP0, SP1, D1/I6, D0/I5, and TMR), the corresponding bit is set to 1 when the device requests an interrupt. The bit is reset during the internally generated interrupt acknowledge.

For INT6–INT0 external interrupts, the corresponding bit (INT4–INT0) reflects the current value of the external signal. The device must hold this signal high until the interrupt is serviced.

Generally the interrupt service routine signals the external device to remove the interrupt request.

**Figure 7-10 Interrupt Request Register**

<table>
<thead>
<tr>
<th>Bit 15–11: Reserved</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit 10: Serial Port 0 Interrupt Request (SP0)</td>
</tr>
<tr>
<td>Bit 9: Serial Port 1 Interrupt Request (SP1)</td>
</tr>
<tr>
<td>Bits 8–4: Interrupt Requests (INT4–INT0)</td>
</tr>
<tr>
<td>Bit 3: DMA Channel 1 Interrupt 6 Request (D1/6)</td>
</tr>
<tr>
<td>Bit 2: DMA Channel 0 Interrupt 5 Request (D0/5)</td>
</tr>
<tr>
<td>Bit 1: Reserved</td>
</tr>
</tbody>
</table>

---

**Interrupt Control Unit**

Page B-15
**Bit 0: Timer Interrupt Request (TMR)—** This bit indicates the state of the timer interrupts. This bit is the logical OR of the timer interrupt requests. When set to a 1, this bit indicates that the timer control unit has an interrupt pending.

The interrupt status register indicates the specific timer that is requesting an interrupt. See Section 7.3.6.

---

**7.3.8 Interrupt In-Service Register**

(INSERV, Offset 2Ch) (Master Mode)

The bits in the In-Service register are set by the interrupt controller when the interrupt is taken. Each bit in the register is cleared by writing the corresponding interrupt type to the End-of-Interrupt (EOI) register.

**Figure 7-11 Interrupt In-Service Register**

![Interrupt In-Service Register Diagram](image)

The INSERV register is set to 0000h on reset.

**Bits 15–11: Reserved**

**Bit 10: Serial Port 0 Interrupt In-Service (SP0)—** This bit indicates the in-service state of serial port 0.

**Bit 9: Serial Port 1 Interrupt In-Service (SP1)—** This bit indicates the in-service state of the serial port 1.

**Bits 8–4: Interrupt In-Service (INT4–INT0)—** These bits indicate the in-service state of the corresponding INT pin.

**Bit 3: DMA Channel 1/Interrupt 6 In-Service (D1/I6)—** This bit indicates the in-service state of DMA channel 1 or INT6.

**Bit 2: DMA Channel 0/Interrupt 5 In-Service (D0/I5)—** This bit indicates the in-service state of DMA channel 0 or INT5.

**Bit 1: Reserved**

**Bit 0: Timer Interrupt In-Service (TMR)—** This bit indicates the state of the in-service timer interrupts. When set to a 1, this bit indicates that the corresponding timer interrupt request is in-service.
### 7.3.9 Priority Mask Register
**(PRIMSK, Offset 2Ah) (Master Mode)**

The Priority Mask register provides the value that determines the minimum priority level at which maskable interrupts can generate an interrupt.

The value of PRIMSK at reset is 0007h.

**Bits 15–3: Reserved** — Set to 0.

**Bits 2–0: Priority Field Mask (PRM2–PRM0)** — This field determines the minimum priority that is required for a maskable interrupt source to generate an interrupt. Maskable interrupts with programmable priority values that are numerically higher than this field are masked. The possible values are zero (000b) to seven (111b). A value of seven (111b) allows all interrupt sources that are not masked to generate interrupts. A value of five (101b) allows only unmasked interrupt sources with a programmable priority of zero to five (000b to 101b) to generate interrupts.

#### Table 7-4 Priority Level

<table>
<thead>
<tr>
<th>Priority</th>
<th>PR2–PR0</th>
</tr>
</thead>
<tbody>
<tr>
<td>(High) 0</td>
<td>0 0 0 0</td>
</tr>
<tr>
<td>1</td>
<td>0 0 1 0</td>
</tr>
<tr>
<td>2</td>
<td>0 1 0 0</td>
</tr>
<tr>
<td>3</td>
<td>0 1 1 0</td>
</tr>
<tr>
<td>4</td>
<td>1 0 0 0</td>
</tr>
<tr>
<td>5</td>
<td>1 0 1 0</td>
</tr>
<tr>
<td>6</td>
<td>1 1 0 0</td>
</tr>
<tr>
<td>(Low) 7</td>
<td>1 1 1 0</td>
</tr>
</tbody>
</table>

### 7.3.10 Interrupt Mask Register
***(IMASK, Offset 28h) (Master Mode)***

The Interrupt Mask register is a read/write register. Programming a bit in the Interrupt Mask register has the effect of programming the MSK bit in the associated interrupt control register. The format of the Interrupt Mask register is shown in Figure 7-13.

When a bit is set to 1 in this register, the corresponding interrupt source is masked. When the bit is set to 0, the interrupt source is enabled to generate an interrupt request.

The IMASK register is set to 07FDh on reset.

**Bits 15–11: Reserved**

**Bit 10: Serial Port 0 Interrupt Mask (SP0)** — When set to 1, this bit indicates that the serial port 0 interrupt is masked.

**Bit 9: Serial Port 1 Interrupt Mask (SP1)** — When set to 1, this bit indicates that the serial port 1 interrupt is masked.

**Bits 8–4: Interrupt Mask (INT4–INT0)** — When set to 1, an INT4–INT0 bit indicates that the corresponding interrupt is masked.

**Bits 3–2: DMA Channel Interrupt Masks (D1/I6–D0/I5)** — When set to 1, a D1/I6–D0/I5 bit indicates that the corresponding DMA or INT6/INT5 channel interrupt is masked.

**Bit 1: Reserved**

**Bit 0: Timer Interrupt Mask (TMR)** — When set to 1, this bit indicates that interrupt requests from the timer control unit are masked.
7.3.11 Poll Status Register
(POLLST, Offset 26h)
(Master Mode)

The Poll Status register mirrors the current state of the Poll register. The Poll Status register can be read without affecting the current interrupt request. But when the Poll register is read, the current interrupt is acknowledged and the next interrupt takes its place in the Poll register. This is a read-only register.

**Figure 7-14 Poll Status Register**

<table>
<thead>
<tr>
<th>Bit 15: Interrupt Request (IREQ)</th>
<th>Set to 1 if an interrupt is pending. When this bit is set to 1, the S4–S0 field contains valid data.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bits 14–5: Reserved</td>
<td>Set to 0.</td>
</tr>
<tr>
<td>Bits 4–0: Poll Status (S4–S0)</td>
<td>Indicates the interrupt type of the highest priority pending interrupt (see Table 7-1 on page 7-4).</td>
</tr>
</tbody>
</table>

7.3.12 Poll Register
(POLL, Offset 24h)
(Master Mode)

When the Poll register is read, the current interrupt is acknowledged and the next interrupt takes its place in the Poll register.

The Poll Status register mirrors the current state of the Poll register, but the Poll Status register can be read without affecting the current interrupt request. This is a read-only register.

**Figure 7-15 Poll Register**

<table>
<thead>
<tr>
<th>Bit 15: Interrupt Request (IREQ)</th>
<th>Set to 1 if an interrupt is pending. When this bit is set to 1, the S4–S0 field contains valid data.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bits 14–5: Reserved</td>
<td>Set to 0.</td>
</tr>
<tr>
<td>Bits 4–0: Poll Status (S4–S0)</td>
<td>Indicates the interrupt type of the highest priority pending interrupt (see Table 7-1). Reading the Poll register acknowledges the highest pending interrupt and allows the next interrupt to advance into the register. Although the IS bit is set, the interrupt service routine does not begin execution automatically. The application software must execute the appropriate ISR.</td>
</tr>
</tbody>
</table>
7.3.13 End-of-Interrupt Register (EOI, Offset 22h) (Master Mode)

The End-of-interrupt (EOI) register is a write-only register. The in-service flags in the In-Service register (see Section 7.3.8 on page 7-22) are reset by writing to the EOI register. Before executing the IRET instruction that ends an interrupt service routine (ISR), the ISR should write to the EOI register to reset the IS bit for the interrupt.

The specific EOI reset is the most secure method to use for resetting IS bits. Figure 7-16 shows an example code for a specific EOI reset. See Table 7-1 on page 7-4 for specific EOI values.

Figure 7-16 Example EOI Assembly Code

```
... ;ISR code
exit: mov ax,int_type ;load the interrupt type in ax
       mov dx, 0ff22h ;write the interrupt type to EOI
       out dx,ax
       popa
       iret ;return from interrupt
```

8.3.2 Timer 0 and Timer 1 Mode and Control Registers (T0CON, Offset 56h, T1CON, Offset 5Eh)

These registers control the functionality of timer 0 and timer 1. See Figure 8-2.

Figure 8-2 Timer 0 and Timer 1 Mode and Control Registers

The value of T0CON and T1CON at reset is 0000h.

Bit 15: Enable Bit (EN)—When set to 1, the timer is enabled. When set to 0, the timer is inhibited from counting. This bit can only be written with the INH bit set at the same time.

Bit 14: Inhibit Bit (INH)—Allows selective updating of enable (EN) bit. When set to 1 during a write, EN can also be modified. When set to 0 during a write, writes to EN are ignored. This bit is not stored and is always read as 0.

Bit 13: Interrupt Bit (INT)—When set to 1, an interrupt request is generated when the count register equals a maximum count. If the timer is configured in dual maxcount mode, an interrupt is generated each time the count reaches maxcount A or maxcount B. When INT is set to 0, the timer will not issue interrupt requests. If the enable bit is cleared after an interrupt request has been generated but before the pending interrupt is serviced, the interrupt request will still be present.

Bit 12: Register in Use Bit (RIU)—When the maxcount compare A register is being used for comparison to the timer count value, this bit is set to 0. When the maxcount compare B register is being used, this bit is set to 1.

Bits 11–6: Reserved—Set to 0.

Bit 5: Maximum Count Bit (MC)—The MC bit is set to 1 when the timer reaches a maximum count. In dual maxcount mode, the bit is set each time either maxcount A or maxcount B is reached. This bit is set regardless of the timer interrupt-enable bit. The MC bit can be used to monitor timer status through software polling instead of through interrupts.

Bit 4: Retrigger Bit (RTG)—Determines the control function provided by the timer input pin. When set to 1, a 0 to 1 edge transition on TMRIN0 or TMRIN1 resets the count. When set to 0, a Low input enables counting and a Low input holds the timer value. This bit is ignored when external clocking (EXT=1) is selected.

Bit 3: Prescaler Bit (P)—When set to 1, the timer is prescaled by timer 2. When set to 0, the timer counts up every fourth CLKOUT period. This bit is ignored when external clocking (EXT=1) is selected.

Bit 2: External Clock Bit (EXT)—When set to 1, an external clock is used. When set to 0, the internal clock is used.
8.3.3 Timer 2 Mode and Control Register

(T2CON, Offset 66h)

This register controls the functionality of timer 2. See Figure 8-3.

**Figure 8-3 Timer 2 Mode and Control Register**

- **Bit 15: Enable Bit (EN)** — When set to 1, the timer is enabled. When set to 0, the timer is inhibited from counting. This bit cannot be written to unless the INH bit is set to 1 during the same write.

- **Bit 14: Inhibit Bit (INH)** — Allows selective updating of enable (EN) bit. When INH is set to 1 during a write, EN can be modified on the same write. When INH is set to 0 during a write, writes to EN are ignored. This bit is not stored and is always read as 0.

- **Bit 13: Interrupt Bit (INT)** — When INT is set to 1, an interrupt request is generated when the count register equals a maximum count. When INT is set to 0, the timer will not issue interrupt requests. If the EN enable bit is cleared after an interrupt request has been generated but before the pending interrupt is serviced, the interrupt request remains active.

- **Bits 12–6: Reserved** — Set to 0.

- **Bit 5: Maximum Count Bit (MC)** — The MC bit is set to 1 when the timer reaches its maximum count. This bit is set regardless of the timer interrupt enable bit. The MC bit can be used to monitor timer status through software polling instead of through interrupts.

- **Bits 4–1: Reserved** — Set to 0.

- **Bit 0: Continuous Mode Bit (CONT)** — When set to 1, it causes the associated timer to run continuously. When set to 0, EN is cleared after each timer count sequence and the timer halts on reaching the maximum count.

---

**Bit 1: Alternate Compare Bit (ALT)** — When set to 1, the timer counts to maxcount compare A, then resets the count register to 0. Then the timer counts to maxcount compare B, resets the count register to zero, and starts over with maxcount compare A.

If ALT is clear, the timer counts to maxcount compare A and then resets the count register to zero and starts counting again against maxcount compare A. In this case, maxcount compare B is not used.

**Bit 0: Continuous Mode Bit (CONT)** — When set to 1, CONT causes the associated timer to run in the normal continuous mode.

When CONT is set to 0, EN is cleared after each timer count sequence and the timer clears and then halts on reaching the maximum count. If CONT=0 and ALT=1, the timer counts to the maxcount compare A register value and resets, then it counts to the B register value and resets and halts.

The value of T2CON at reset is 0000h.
8.3.4 Timer Count Registers (T0CNT, Offset 50h, T1CNT, Offset 58h, T2CNT, Offset 60h)

These registers can be incremented by one every four internal processor clocks. Timer 0 and timer 1 can also be configured to increment based on the TMRIN0 and TMRIN1 external signals, or they can be prescaled by timer 2. See Figure 8-4.

The count registers are compared to maximum count registers, and various actions are triggered based on reaching a maximum count.

Figure 8-4 Timer Count Registers

The value of these registers at reset is undefined.

Bits 15–0: Timer Count Value (TC15–TC0)—This register contains the current count of the associated timer. The count is incremented every fourth processor clock in internal clocked mode, or each time the timer 2 maxcount is reached if prescaled by timer 2. Timer 0 and timer 1 can be configured for external clocking based on the TMRIN0 and TMRIN1 signals.

8.3.5 Timer Maxcount Compare Registers (T0CMPA, Offset 52h, T0CMPB, Offset 54h, T1CMPA, Offset 5Ah, T1CMPB, Offset 5Ch, T2CMPA, Offset 62h)

These registers serve as comparators for their associated count registers. Timer 0 and timer 1 each have two maximum count compare registers. See Figure 8-5.

Timer 0 and timer 1 can be configured to count and compare to register A and then count and compare to register B. Using this method, the TMROUT0 or TMROUT1 signals can be used to generate wave forms of various duty cycles.

Timer 2 has one compare register, T2CMPA.

If a maximum count compare register is set to 0000h, the timer associated with that compare register will count from 0000h to FFFFh before requesting an interrupt. With a 40-MHz clock, a timer configured this way interrupts every 6.5536 ms.

Figure 8-5 Timer Maxcount Compare Registers

The value of these registers at reset is undefined.

Bits 15–0: Timer Compare Value (TC15–TC0)—This register contains the maximum value a timer will count to before resetting its count register to 0.
9.3 PROGRAMMABLE DMA REGISTERS

The following sections describe the control registers that are used to configure and operate the two DMA channels.

9.3.1 DMA Control Registers (D0CON, Offset CAh, D1CON, Offset DAh)

The DMA control registers (see Figure 9-2) determine the mode of operation for the DMA channels. These registers specify the following options:

- Whether the destination address is memory or I/O space
- Whether the destination address is incremented, decremented, or maintained constant after each transfer
- Whether the source address is memory or I/O space
- Whether the source address is incremented, decremented, or maintained constant after each transfer
- If DMA activity ceases after a programmed number of DMA cycles
- If an interrupt is generated with the last transfer
- The mode of synchronization
- The relative priority of the DMA channel with respect to the other DMA channel
- Whether timer 2 DMA requests are enabled or disabled
- Whether bytes or words are transferred (on the Am186 microcontroller only)
- Whether the DRQ pin is used for external interrupts

The DMA channel control registers can be changed while the channel is operating. Any changes made during DMA operations affect the current DMA transfer.

Figure 9-2 DMA Control Registers

```
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>DM/IO Select</td>
<td>Source Decrement</td>
<td>Destination Increment</td>
<td>Source Increment</td>
<td>Source Address Space Select</td>
<td>Terminal Count</td>
<td>Interrupt</td>
<td>Synchronization Type</td>
<td></td>
<td>Change Start Bit</td>
</tr>
</tbody>
</table>
```

The value of D0CON and D1CON at reset is undefined except ST is set to 0.

- Bit 15: Destination Address Space Select (DM/IO) — Selects memory or I/O space for the destination address. When DM/IO is set to 1, the destination address is in memory space. When set to 0, the destination address is in I/O space.
- Bit 14: Destination Decrement (DDEC) — When DDEC is set to 1, the destination address is automatically decremented after each transfer. The address decrements by 1 or 2 depending on the byte/word bit (BW, bit 0). The address remains constant if the increment and decrement bits are set to the same value (00b or 11b).
- Bit 13: Destination Increment (DINC) — When DINC is set to 1, the destination address is automatically incremented after each transfer. The address increments by 1 or 2 depending on the byte/word bit (BW, bit 0). The address remains constant if the increment and decrement bits are set to the same value (00b or 11b).
- Bit 12: Source Address Space Select (SM/IO) — When SM/IO is set to 1, the source address is in memory space. When set to 0, the source address is in I/O space.
- Bit 11: Source Decrement (SDEC) — When SDEC is set to 1, the source address is automatically decremented after each transfer. The address decrements by 1 or 2 depending on the byte/word bit (BW, bit 0). The address remains constant if the increment and decrement bits are set to the same value (00b or 11b).
- Bit 10: Source Increment (SINC) — When SINC is set to 1, the source address is automatically incremented after each transfer. The address increments by 1 or 2 depending on the byte/word bit (BW, bit 0). The address remains constant if the increment and decrement bits are set to the same value (00b or 11b).
- Bit 9: Terminal Count (TC) — The DMA decrements the transfer count for each DMA transfer. When TC is set to 1, source or destination synchronized DMA transfers terminate when the count reaches 0. When TC is set to 0, source or destination synchronized DMA transfers do not terminate when the count reaches 0. Unsynchronized DMA transfers always terminate when the count reaches 0, regardless of the setting of this bit.
- Bit 8: Interrupt (INT) — When INT is set to 1, the DMA channel generates an interrupt request on completion of the transfer count. The TC bit must also be set to generate an interrupt.
- Bit 7–6: Synchronization Type (SYN1–SYN0) — The SYN1–SYN0 bits select channel synchronization as shown in Table 9-2. The value of this field is ignored if TDRQ (bit 4) is set to 1. For more information on DMA synchronization, see Section 9.4 on page 9-11. This field is 11b after processor reset.

<table>
<thead>
<tr>
<th>SYN1</th>
<th>SYN0</th>
<th>Sync Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Unsynchronized</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Source Synch</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Destination Synch</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

- Bit 5: Relative Priority (P) — When P is set to 1, it selects high priority for this channel relative to the other channel during simultaneous transfers.
- Bit 4: Timer 2 Synchronization (TDRQ) — When TDRQ is set to 1, it enables DMA requests from timer 2. When set to 0, TDRQ disables DMA requests from timer 2.
- Bit 3: External Interrupt Enable Bit (EXT) — This bit enables the external interrupt functionality of the corresponding DRQ pin. If this bit is set to 1, the external pin is an INT pin and requests on the pin are processed by the interrupt controller; the associated DMA channel does not respond to changes on the DRQ pin. When this bit is set to 0, the pin functions as a DRQ pin.
- Bit 2: Change Start Bit (CHG) — This bit must be set to 1 during a write to allow modification of the ST bit. When CHG is set to 0 during a write, ST is not altered when writing the control word. This bit always reads as 0.
9.3.2 Serial Port/DMA Transfers

The Am186ES and Am188ES microcontrollers have the added feature of being able to DMA to and from the serial ports. This is accomplished by programming the DMA controller to perform transfers between a data buffer (located either in memory or I/O space) and a serial port peripheral control register (SP0TD, SP1TD, SP0RD, or SP1RD). It is important to note that when a DMA channel is in use by a serial port, the corresponding external DMA request signal is deactivated.

For DMA to the serial port, the transmit data register address, either I/O mapped or memory mapped, should be specified as a byte destination for the DMA by writing the address of the register into the DMA destination low and DMA destination high registers. The destination address (the address of the transmit data register) should be configured as a constant throughout the DMA operation. The serial port transmitter acts as the synchronizing device so the DMA channel should be configured as destination synchronized.

For DMA from the serial port, the receive data register address, either I/O mapped or memory mapped, should be specified as a byte source for the DMA by writing the address of the register into the DMA Source and DMA Source High registers. The source address (the address of the receive data register) should be configured as a constant throughout the DMA. The serial port receiver acts as the synchronizing device so the DMA channel should be configured as source synchronized.

9.3.3 DMA Transfer Count Registers

Each DMA channel maintains a 16-bit DMA Transfer Count register (DTC). This register is decremented after each DMA cycle, regardless of the state of the TC bit in the DMA control register. However, if the TC bit in the DMA control word is set or if unsynchronized transfers are programmed, DMA activity terminates when the transfer count register reaches 0.

The value of D0TC and D1TC at reset is undefined.

Bits 15–0: DMA Transfer Count (TC15–TC0)—Contains the transfer count for a DMA channel. Value is decremented by 1 after each transfer.
9.3.4 DMA Destination Address High Register (High Order Bits)  
(D0DSTH, Offset C6h, D1DSTH, Offset D6h)

Each DMA channel maintains a 20-bit destination and a 20-bit source register. Each 20-bit address takes up two full 16-bit registers (the high register and the low register) in the peripheral control block. For each DMA channel to be used, all four address registers for that channel must be initialized. These addresses can be individually incremented or decremented after each transfer. If word transfers are performed, the address is incremented or decremented by 2 after each transfer. If byte transfers are performed, the address is incremented or decremented by 1.

Each register can point into either memory or I/O space. The user must program the upper four bits to 0000b in order to address the normal 64K I/O space. Since the DMA channels can perform transfers to or from odd addresses, there is no restriction on values for the destination and source address registers. Higher transfer rates can be achieved on the Am186ES microcontroller if all word transfers are performed to or from even addresses so that accesses occur in single 16-bit bus cycles.

Figure 9-4 DMA Destination Address High Register

![Diagram of DMA Destination Address High Register](image)

Bits 15–4: Reserved

Bits 3–0: DMA Destination Address High (DDA19–DDA16)—These bits are driven onto A19–A16 during the write phase of a DMA transfer.

---

9.3.5 DMA Destination Address Low Register (Low Order Bits)  
(D0DSTL, Offset C4h, D1DSTL, Offset D4h)

Figure 9-5 shows the DMA Destination Address Low register. The sixteen bits of this register are combined with the four bits of the DMA Destination Address High register (see Figure 9-4) to produce a 20-bit destination address.

Figure 9-5 DMA Destination Address Low Register

![Diagram of DMA Destination Address Low Register](image)

The value of D0DSTL and D1DSTL at reset is undefined.

Bits 15–0: DMA Destination Address Low (DDA15–DDA0)—These bits are driven onto A15–A0 during the write phase of a DMA transfer.

Bits 15–4: Reserved

Bits 3–0: DMA Destination Address Low (DDA19–DDA16)—These bits are driven onto A19–A16 during the write phase of a DMA transfer.
9.3.6 DMA Source Address High Register (High Order Bits)  
(D0SRCH, Offset C2h, D1SRCH, Offset D2h)

Each DMA channel maintains a 20-bit destination and a 20-bit source register. Each 20-bit address takes up two full 16-bit registers (the high register and the low register) in the peripheral control block. For each DMA channel to be used, all four address registers for that channel must be initialized. These addresses can be individually incremented or decremented after each transfer. If word transfers are performed, the address is incremented or decremented by 2 after each transfer. If byte transfers are performed, the address is incremented or decremented by 1.

Each register can point into either memory or I/O space. The user must program the upper four bits to 0000b in order to address the normal 64K I/O space. Since the DMA channels can perform transfers to or from odd addresses, there is no restriction on values for the destination and source address registers. Higher transfer rates can be achieved on the Am186ES microcontroller if all word transfers are performed to or from even addresses so that accesses occur in single 16-bit bus cycles.

Figure 9-6 DMA Source Address High Register

The value of D0SRCH and D1SRCH at reset is undefined.

Bits 15–4: Reserved

Bits 3–0: DMA Source Address High (DSA19–DSA16)—These bits are driven onto A19–A16 during the read phase of a DMA transfer.

9.3.7 DMA Source Address Low Register (Low Order Bits)  
(D0SRCL, Offset C0h, D1SRCL, Offset D0h)

Figure 9-7 shows the DMA Source Address Low register. The sixteen bits of this register are combined with the four bits of the DMA Source Address High register (see Figure 9-6) to produce a 20-bit source address.

Figure 9-7 DMA Source Address Low Register

The value of D0SRCL and D1SRCL at reset is undefined.

Bits 15–0: DMA Source Address Low (DSA15–DSA0)—These bits are driven onto A15–A0 during the read phase of a DMA transfer.

Bits 15–4: Reserved

Bits 3–0: DMA Source Address High (DSA19–DSA16)—These bits are driven onto A19–A16 during the read phase of a DMA transfer.
When a DMA channel is being used for serial port transmits or receives, the DMA request is generated internally. The corresponding external DMA request signals, DRQ0 or DRQ1, are not active for serial port DMA transfers.

Bit 12: Receive Status Interrupt Enable (RSIE)—This bit enables the serial port to generate an interrupt request when an exception occurs during data reception. When this bit is set, interrupt requests are generated for the error conditions reported in the serial port status register (BRK0, BRK1, OER, PER, FER).

Bit 11: Send Break (BRK)—When this bit is set, the TXD pin is driven Low regardless of the data being shifted out of the transmit register. A short break, as reported by the BRK0 bit in the status register, is a continuous Low on the TXD output for a duration of more than one frame transmission time M, where M = start bit + data bits (+ parity bit) + stop bit. The transmitter can be used to time the break by setting the BRK bit when the transmitter is empty (indicated by the TEMT bit of the serial port status register), writing the serial port transmit register with data, then waiting until the TEMT bit is again set before resetting the BRK bit.

A long break, as reported by the BRK1 bit in the status register, is a continuous Low on the TXD output for a duration of more than two frame transmission times plus the transmission time for three additional bits (2M+3). The transmitter can be used to time the break as follows:

1. Wait for the TEMT bit in the status register to be set.
2. Set the BRK bit.
3. Perform two sequential writes to the transmit register.
4. Wait for the TEMT bit in the status register to be set again.
5. Write a character with the low nibble zeroed and the high nibble High (for example, F0h).
6. Clear the BRK bit. The character being transmitted continues to hold the TXD pin Low for the required additional 3-bit transmission time.

Note: The transmitter can only be used to time the break if hardware flow control is disabled. If flow control is enabled, setting the BRK bit will still force the TXD line Low, but the receiving device may deassert the CTS input, inhibiting the clocking out of the character in the transmit data register.

Bit 10: Transmit Bit 8 (TB8)—This bit is transmitted as the ninth data bit in modes 2 and 3 (see the mode field description). This bit is not buffered and is cleared after every transmission. To transmit a character with the 8th data bit High, the following protocol should be followed:

1. Wait for the TEMT bit in the status register to become set.
2. Write the control register with this bit set.
3. Write the character to be transmitted.
4. Write character to be transmitted.

Bit 9: Flow Control Enable (FC)—When this bit is 1, hardware flow control is enabled for the associated serial port. When this bit is 0, hardware flow control is disabled for the associated serial port. The nature of the flow control signals is determined by the setting of the ENRX0/ENRX1 and RTS0/RTS1 bits in the AUXCON register. See the discussion of the AUXCON register and Section 10.1.1 on page 10-4 for more information. If this bit is 1 for serial port 0, the associated pins are used as flow control signals, overiding their function as Peripheral Chip Select signals. This bit is 0 after processor reset.
Bit 8: Transmitter Ready Interrupt Enable (TXIE)—When this bit is set, the serial port generates an interrupt request whenever the transmit holding register is empty (THRE bit in the status register is set), indicating that the transmitter is available to accept a new character for transmission. When this bit is reset, the serial port does not generate transmit interrupt requests. Interrupt requests continue to be generated as long as the TXIE bit is set and the transmitter does not contain valid data to transmit, i.e., the THRE bit in the status register remains set.

Bit 7: Receive Data Ready Interrupt Enable (RXIE)—When this bit is set, the serial port generates an interrupt request whenever the receive register contains valid data (RDR bit in the status register is set). When this bit is reset, the serial port does not generate receive interrupt requests. Interrupt requests continue to be generated as long as the RXIE bit is set and the receiver contains unread data (the RDR bit in the status register is set).

Bit 6: Transmit Mode (TMODE)—When this bit is set, the transmit section of the serial port is enabled. When this bit is reset, the transmitter and transmit interrupt requests are disabled.

Bit 5: Receive Mode (RMODE)—When this bit is set, the receive section of the serial port is enabled. When this bit is reset, the receiver is disabled.

Bit 4: Even Parity (EVN)—This bit determines the parity sense. When EVN is set, even parity checking is enforced (even number of 1s in frame). When EVN is reset, odd parity checking is enforced (odd number of 1s in frame).

Note: This bit is valid only when the PE bit is set (parity enabled).

Bit 3: Parity Enable (PE)—When this bit is set, parity checking is enabled. When this bit is reset, parity checking is disabled.

Bits 2–0: Mode of Operation (MODE)—This field determines the operating mode for the serial port. The valid modes and their descriptions are shown in Table 10-4.

Mode 1 supports 7 data bits when parity is enabled or 8 data bits with parity disabled. When using parity, the eighth bit becomes the parity bit and is generated for transmits, or checked for receives automatically by the processor.

Mode 2—When configured in this mode, the serial port receiver will not complete a data reception unless the ninth data bit is set (High). Any character received with the ninth data bit reset (Low) is ignored. The transmit portion of the port behaves identically with mode 3 operation.

This mode can be used in conjunction with mode 3 to allow for multidrop communications over a common serial link. In this case, the serial port is configured as mode 2 initially. Each time data is received with the ninth bit set, the data is compared by software against a unique ID for this receiver. If the received data does not match the port ID, the port is left in mode 2. If the received data matches the port ID, software should reconfigure the serial port to mode 3, allowing it to receive 9-bit data with the ninth bit reset.

In a serial multidrop configuration, multiple serial ports are attached to the same serial line. The master serial port is configured in mode 3 while the slave serial ports are configured in mode 2. The master polls the other devices by sending out status request packets. Each of these status request packets begins with an address byte (i.e., ninth data bit is set). The slave ports report a receive character for the address byte since the ninth bit is set. Each port then attempts to match the address against its own address. If the addresses do not match, the port remains in mode 2 and ignores the remainder of the message. If the addresses match, software reconfigures the port into mode 3. The two mode 3 ports are able to exchange data freely.

It should be noted that only ports which are actively exchanging data (i.e., ports in mode 3) should have hardware handshaking enabled. If this is not the case, multiple devices may be driving the hardware handshaking lines. For this reason, hardware handshaking is not supported for the mode 2 configuration and should not be enabled. In addition, if it is possible for more than two devices to be configured as mode 3 at any one time, hardware handshaking should not be enabled.

Mode 3 supports 8 data bits when parity is enabled or 9 data bits with parity disabled. When not using parity, the ninth bit (bit 8) for transmission is set by writing a 1 to the TB8 field in the serial port control register. The ninth data bit for a receive can be read in the RB8 field of the serial port status register. See the discussion of the TB8 and RB8 fields for more information.

This mode can be used in conjunction with mode 2 (see above) to allow for multidrop communications over a common serial link. In this case, parity must be disabled. In this configuration, software interprets receive characters as data as long as the ninth data bit is reset (Low). When a character is received with the ninth bit set, software should compare the lower eight bits against the port ID. If the port ID matches the receive data, the port should remain in mode 3. If the port ID does not match the receive data, the port should be reconfigured to mode 2.

Mode 4—In this mode, each frame consists of 7 data bits, a start bit, and a stop bit. Parity is not available in this mode.

<table>
<thead>
<tr>
<th>MODE</th>
<th>Description</th>
<th>Data Bits</th>
<th>Parity Bits</th>
<th>Stop Bits</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Reserved</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Data Mode 1</td>
<td>7 or 8</td>
<td>1 or 0</td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>Data Mode 2</td>
<td>9</td>
<td>N/A</td>
<td>1</td>
</tr>
<tr>
<td>3</td>
<td>Data Mode 3</td>
<td>8 or 9</td>
<td>1 or 0</td>
<td>1</td>
</tr>
<tr>
<td>4</td>
<td>Data Mode 4</td>
<td>7</td>
<td>N/A</td>
<td>1</td>
</tr>
<tr>
<td>5</td>
<td>Reserved</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>Reserved</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>Reserved</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### 10.2.2 Serial Port 0/1 Status Registers (SP0STS/SP1STS, Offset 82h/12h)

The Serial Port Status Registers provide information about the current status of the associated serial port. The THRE and TEMT fields provide the software with information about the state of the transmitter. The THRE and TEMT fields provide information about the receiver. The HS0 bit reflects the value of the serial port's associated CTS/ENRX signal. The THRE, TEMT, and HS0 bits are updated during each processor cycle. The format of the Serial Port Status Register is shown in Figure 10-4.

#### Figure 10-4 Serial Port 0/1 Status Register

![Serial Port 0/1 Status Register](image)

**Bits 15-11: Reserved**

**Bit 10: Long Break Detected (BRK1)** — This bit is set when a long break is detected on the asynchronous serial interface. A long break is defined as a Low signal on the RXD pin for greater than 2M+3 bit times, where M = (start bit + # data bits + # parity bits + stop bit).

If the serial port is receiving a character when the break begins, the reception of the character will be completed (generating a framing error) before timing for the break begins. To guarantee detection with the specified 2M+3 bit times, the break must begin outside of a frame.

*Note:* This bit should be reset by software.

**Bit 9: Short Break Detected (BRK0)** — This bit is set when a short break is detected on the asynchronous serial interface. A short break is defined as a Low signal on the RXD pin for greater than M bit times, where M = (start bit + # data bits + # parity bits + stop bit).

If the serial port is receiving a character when the break begins, the reception of the character will be completed (generating a framing error) before timing for the break begins. To guarantee detection with the specified M bit times, the break must begin outside of a frame.

*Note:* This bit should be reset by software.

**Bit 8: Received Bit 8 (RB8)** — This bit contains the ninth data bit received in modes 2 and 3. (See Serial Port Control register definition.)

*Note:* This bit should be reset by software.

**Bit 7: Receive Data Ready (RDR)** — When this bit is set, the associated Receive Data register contains valid data. This field is read-only. The RDR bit can only be reset by reading the associated SP0RD/SP1RD register.

**Bit 6: Transmit Holding Register Empty (THRE)** — When this bit is set, the transmit holding register is ready to accept data for transmission. This field is read-only.

**Bit 5: Framing Error Detected (FER)** — When this bit is set, the serial port has detected a framing error. Framing errors are generated when the receiver samples the RXD line as Low when it expected the stop bit.

*Note:* This bit should be reset by software.

**Bit 4: Overrun Error Detected (OER)** — This bit is set when the processor detects an overrun error. An overrun error occurs when the serial port overwrites valid, unread data in the receive register, resulting in loss of data.

*Note:* This bit should be reset by software.

**Bit 3: Parity Error Detected (PER)** — This bit is set when the processor detects a parity error (modes 1 and 3).

*Note:* This bit should be reset by software.

**Bit 2: Transmitter Empty (TEMT)** — When this bit is set, the transmitter has no data to transmit and the transmit shift register is empty. This indicates to software that it is safe to disable the transmit section. This bit is read-only.

**Bit 1: Handshake Signal 0 (HS0)** — This bit reflects the value of the serial port's associated CTS/ENRX signal. The THRE, TEMT, and HS0 bits are updated during each processor cycle. The format of the Serial Port Status Register is shown in Figure 10-4.

**Bit 0: Reserved**
10.2.4 Serial Port 0/1 Receive Registers
(SP0RD/SP1RD, Offset 86h/16h)

These registers (Figure 10-6) contain data received over the serial port. The receiver is double-buffered; the receive section can be receiving a subsequent frame of data in the receive shift register (which is not accessible to software) while the receive data register is being read.

The Receive-Data-Ready (RDR) bit in the serial port status register reports the current state of this register. When the RDR bit is set, the receive register contains valid unread data. The RDR bit is automatically cleared when the receive register is read.

When hardware handshaking is enabled, the CTS/ENRX signals are deasserted while the receive register contains valid unread data. Reading the receive register causes the CTS/ENRX signals to be asserted. This behavior prevents overrun errors, but may result in delays between character transmissions.

Figure 10-6 Serial Port Receive 0/1 Registers

The value of SPRD at reset is undefined.

Bits 15-8: Reserved

Bits 7-0: Receive Data (RDATA)—This field contains valid data received over the serial line only when the RDR bit in the associated Serial Port Control register is set.
10.2.5 Serial Port 0/1 Baud Rate Divisor Registers (SP0BAUD/SP1BAUD, Offset 88h/18h)

Each of the asynchronous serial ports has a baud rate divisor register, so the two ports can operate at different rates.

These registers (Figure 10-7) specify a clock divisor for the generation of the serial clock that controls the associated serial port. The baud rate divisor register specifies the number of internal processor cycles in one phase (half period) of the 16x serial clock.

If power-save mode is in effect, the baud rate divisor must be reprogrammed to reflect the new processor clock frequency. Since power-save mode is automatically exited when an interrupt is taken, serial port transmits and receives may be corrupted if the serial port is in use and interrupts are enabled during power-save mode.

A general formula for the baud rate divisor is:

\[ \text{BAUDDIV} = \frac{\text{Processor Frequency}}{(16 \cdot \text{baud rate})} \]

The maximum baud rate is 1/16 of the internal processor clock and is achieved by setting BAUDDIV=0001h. This results in a baud rate of 2500 Kb at 20 MHz, 1562.5 Kb at 25 MHz, 2062.5 Kb at 33 MHz, and 1250 Kb at 40 MHz. A BAUDDIV setting of zero results in no transmission or reception of data.

The serial port receiver can tolerate a 3.0% overspeed and 2.5% underspeed baud rate deviation.

Table 10-5 Common Baud Rates

<table>
<thead>
<tr>
<th>Baud Rate</th>
<th>20 MHz</th>
<th>25 MHz</th>
<th>33 MHz</th>
<th>40 MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>300</td>
<td>4166</td>
<td>5208</td>
<td>6875</td>
<td>8333</td>
</tr>
<tr>
<td>600</td>
<td>2083</td>
<td>2604</td>
<td>3437</td>
<td>4166</td>
</tr>
<tr>
<td>1050</td>
<td>1190</td>
<td>1488</td>
<td>1964</td>
<td>2380</td>
</tr>
<tr>
<td>1200</td>
<td>1041</td>
<td>1302</td>
<td>1718</td>
<td>2083</td>
</tr>
<tr>
<td>1800</td>
<td>694</td>
<td>868</td>
<td>1145</td>
<td>1388</td>
</tr>
<tr>
<td>2400</td>
<td>520</td>
<td>651</td>
<td>859</td>
<td>1041</td>
</tr>
<tr>
<td>4800</td>
<td>260</td>
<td>325</td>
<td>429</td>
<td>520</td>
</tr>
<tr>
<td>7200</td>
<td>173</td>
<td>217</td>
<td>286</td>
<td>347</td>
</tr>
<tr>
<td>9600</td>
<td>130</td>
<td>162</td>
<td>214</td>
<td>260</td>
</tr>
<tr>
<td>19200</td>
<td>65</td>
<td>81</td>
<td>107</td>
<td>130</td>
</tr>
<tr>
<td>28800</td>
<td>43</td>
<td>54</td>
<td>71</td>
<td>86</td>
</tr>
<tr>
<td>38400</td>
<td>33</td>
<td>40</td>
<td>53</td>
<td>65</td>
</tr>
<tr>
<td>56000</td>
<td>22</td>
<td>28</td>
<td>36</td>
<td>45</td>
</tr>
<tr>
<td>57600</td>
<td>22</td>
<td>27</td>
<td>35</td>
<td>43</td>
</tr>
<tr>
<td>76800</td>
<td>16</td>
<td>20</td>
<td>26</td>
<td>32</td>
</tr>
<tr>
<td>115200</td>
<td>10</td>
<td>13</td>
<td>18</td>
<td>22</td>
</tr>
</tbody>
</table>

Note: A 1% error applies to all values in the above tables.
11.2 PIO MODE REGISTERS

Table 11-2 shows the possible settings for the PIO Mode and PIO Direction bits. The Am186ES and Am188ES microcontrollers default the 32 PIO pins to either 00b (normal operation) or 01b (PIO input with weak internal pullup or pulldown enabled).

Pins that default to active High outputs at reset are pulled down. All other pins are pulled up or are normal operation. See Table 11-2. The column titled Power-On Reset State in Table 11-1 lists the defaults for the PIOs.

The internal pullup resistor has a value of approximately 10 Kohms. The internal pulldown resistor has a value of approximately 10 Kohms.

<table>
<thead>
<tr>
<th>PIO Mode</th>
<th>PIO Direction</th>
<th>Pin Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Normal operation</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>PIO input with pullup/pulldown</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>PIO output</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>PIO input w/o pullup/pulldown</td>
</tr>
</tbody>
</table>

Table 11-2 PIO Mode and PIO Direction Settings

11.2.1 PIO Mode 1 Register (PIOMODE1, offset 76h)

The value of PIOMODE1 at reset is 0000h.

<table>
<thead>
<tr>
<th>Bit 15–0</th>
<th>PIN FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>0–15</td>
<td>PMODE1–0</td>
</tr>
</tbody>
</table>

11.2.2 PIO Mode 0 Register (PIOMODE0, offset 70h)

The value of PIOMODE0 at reset is 0000h.

<table>
<thead>
<tr>
<th>Bit 15–0</th>
<th>PIN FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>0–15</td>
<td>PMODE0–15</td>
</tr>
</tbody>
</table>

Figure 11-2 PIO Mode 1 Register (PIOMODE1, offset 76h) Figure 11-3 PIO Mode 0 Register (PIOMODE0, offset 70h)

11.2.1 PIO Mode 1 Register (PIOMODE1, Offset 76h)

The value of PIOMODE1 at reset is 0000h.

Bits 15–0: PIO Mode Bits (PMODE1–PMODE0)—This field, along with the PIO direction registers, determines whether each PIO pin performs its preassigned function or is enabled as a custom PIO signal. The most significant bit of the PMODE field determines whether PIO31 is enabled, the next bit determines whether PIO30 is enabled, and so on.

Table 11-2 shows the values that the PIO mode bits and the PIO direction bits can encode.

11.2.2 PIO Mode 0 Register (PIOMODE0, Offset 70h)

The value of PIOMODE0 at reset is 0000h.

Bits 15–0: PIO Mode Bits (PMODE15–PMODE0)—This field is a continuation of the PMODE field in the PIO Mode 1 register.
11.3 PIO DIRECTION REGISTERS

Each PIO is individually programmed as an input or output by a bit in one of the PIO Direction registers (see Figure 11-4 and Figure 11-5). Table 11-2 on page 11-3 shows the values that the PIO mode bits and the PIO direction bits can encode. The column titled Power-On Reset Status in Table 11-1 lists the reset default values for the PIOs. Bits in the PIO Direction registers have the same correspondence to pins as bits in the PIO Mode registers.

11.3.1 PIO Direction 1 Register
(PDIR1, Offset 78h)

The value of PDIR1 at reset is FFFFh.

Bits 15–0: PIO Direction Bits (PDIR31–PDIR16)—This field determines whether each PIO pin acts as an input or an output. The most significant bit of the PDIR field determines the direction of PIO31, the next bit determines the direction of PIO30, and so on. A 1 in the bit configures the PIO signal as an input and a 0 in the bit configures it as an output or as normal pin function.

11.3.2 PIO Direction 0 Register
(PDIR0, Offset 72h)

The value of PDIR0 at reset is FC0Fh.

Bits 15–0: PIO Direction Bits (PDIR15–PDIR0)—This field is a continuation of the PDIR field in the PIO Direction 1 register.

11.4 PIO DATA REGISTERS

If a PIO pin is enabled as an output, the value in the corresponding bit in one of the PIO Data registers (see Figure 11-6 and Figure 11-7) is driven on the pin with no inversion (Low=0, High=1). If a PIO pin is enabled as an input, the value on the PIO pin is reflected in the value of the corresponding bit in the PIO Data register, with no inversion. Bits in the PIO Data registers have the same correspondence to pins as bits in the PIO Mode registers and PIO Direction registers.

11.4.1 PIO Data Register 1
(PDATA1, Offset 7Ah)

Bits 7–0: PIO Data Bits (PDATA31–PDATA16)—This field determines the level driven on each PIO pin or reflects the external level of the pin, depending upon whether the pin is configured as an output or an input in the PIO Direction registers. The most significant bit of the PDATA field indicates the level of PIO31, the next bit indicates the level of PIO30, and so on.

The value of PDATA1 at reset is undefined.

11.4.2 PIO Data Register 0
(PDATA0, Offset 74h)

Bits 15–0: PIO Data Bits (PDATA15–PDATA0)—This field is a continuation of the PDATA field in the PIO Data 1 register.

The value of PDATA0 at reset is undefined.

11.5 OPEN-DRAIN OUTPUTS

The PIO Data registers permit the PIO signals to be operated as open-drain outputs. This is accomplished by keeping the appropriate PDATA bits constant in the PIO Data register and writing the data value into its associated bit position in the PIO Direction register, so the output is either driving Low or is disabled, depending on the data.
APPENDIX C: CARD MECHANICAL MOUNTING

The GPC® 884 can be physically mounted in two different manner. The first is the piggy back mounting (stack trough mode) that use the three connectors CN1, CN5 and CN5A for the interface with a user developed board. This connectors lead out of 7 mm on solder side and the user board must have proper female strip connectors (2,54 mm pitch) where the card can be plugged in, obtaining a single system.

The second mode expect a mounting inside a proper plastic container for a direct mounting on DIN 247277-1 and 3 Ω rails; if the card is used with some other peripheral cards (i.e. ZBR xxx or ZBT xxx), a single longer container can be used obtaining a single module. The described plastic container code is 414487 type RS/100 by Weidmuller and it can be ordered to grifo® as WM.Ill options, where Ill is the required length. By selecting this mounting the electric connection between GPC® 884 and other peripheral cards is performed with a flat cable that must be really short.

In the following figures are described the module dimensions with the connector positions and some immages that illustrate the connection modes.

![Figure C1: Module dimension for piggy back mounting](image-url)
FIGURE C2: PIGGY BACK MOUNTING

FIGURE C3: WEIDMULLER RAIL MOUNTING
APPENDIX D: ELECTRIC DIAGRAMS

In this appendix are available some electric diagrams of the most frequently used GPC® 884 interfaces. All these interfaces can be yourself produced and some of them are standard grifo® cards and, if required, they can be directly ordered.

**FIGURE D1: PPI EXPANSION ELECTRIC DIAGRAM**
**Figure D2: SPA 03 Electrical Diagram**

- **Title:** SPA-03
- **Date:** 16/11/98
- **Rel.:** 1.1
- **Page:** 1 of 1
FIGURE D3: QTP 16P ELECTRIC DIAGRAM
**Figure D4: QTP 24P Electric Diagram (1 of 2)**
FIGURE D5: QTP 24P ELECTRIC DIAGRAM (2 OF 2)
FIGURE D6: IAC 01 ELECTRIC DIAGRAM
**Figure D7: ABACO® I/O BUS input output electric diagram**
Figure D8: BUS Interface Electric Diagram
## APPENDIX E: ALPHABETICAL INDEX

### A
- A/D converter: 6, 8, 18, 20, 28, 31, 40
- ABACO® I/O BUS: 4, 11, 28, 37, D-7
- Address BUS: 11
- Addresses: 35
- Analog inputs: 9, 18, 20, 23
- ASP: 4, 12, 14, 29
- Assistance: 1

### B
- Back up: 9, 10, 26, 27
- Battery: 9, 10, 17, 27
- Bibliography: 46
- Block diagram: 5
- BUS interface: D-8

### C
- Calibration: 23
- Clock: 4, 8
- Components maps: 7
- Configuration jumper: 26, 36, 39
- Connectors: 8, 10, 17, 43
  - CN1: 11, 37
  - CN2: 10
  - CN3A: 12, 27
  - CN3B: 14, 27
  - CN5: 18, 22, 31
  - CN5A: 20
- Consumption: 9
- Container: 1, 8, C-1
- CPU: 3, 8, 28, 41, B-1
- CSU: 35
- Current: 9

### D
- Data BUS: 11
- Date: 40
- DEBUG: 39
- Default configuration: 24, 29, 30
- Devices: 8, 35, 39, B-1
- Digital I/O: 6, 18, D-1
- Digital I/O interfaces: 22
- Dimension: C-1
- DIN rails: 8, C-1
E
EEPROM  3, 30, 31, 37, 39
Electric diagram  D-1
EPROM  3, 17, 30, 37
Expansion  4, 22, 42, D-1
External cards  4, 22, 42

F
Features
  electric  9
  general  2, 8
  physical  8
  technical  8
FLASH EPROM  3, 17, 37
Frequency  4, 8
Full scale  23

H
Handshake  12, 27, 29
Humidity  9

I
I/O addresses  36
I/O connection  23
I2C bus  39
Impedance  9
Installation  10
Interfaces  22
Interrupts  6, 11, 28, 32
Intervent time  8, 39

J
Jumpers  24, 25
  2 pins  26
  3 pins  27
  5 pins  26

M
Map  35
Memory  3, 8, 17, 22, 26, 30, 35, 37, A-1
Memory allocation  38
Mounting  C-1
Multiplexed pins  31
N
Network 16

O
Operator panel 22, 42, D-3, D-4
Options 29, 30, C-1

P
Peripherals 3, 8, 35, 39, B-1
Photo 7
Piggy back C-1
PIO 18, 28, 31, 39, 40, D-4
PIO signals connection 19
Power failure 9, 27, 28, 32
Power on 28, 32
Power supply 4, 9, 11
Printer 22, D-6

R
RAM 3, 17, 27, 30, 37
Real Time Clock 6, 27, 28, 36, 40
Reference voltage 21, 23
Registers 36, 39
Reset 11, 22, 28, 32
Reset contact 22
RS 232 4, 12, 14, 23, 29, A-2
RS 422 4, 9, 14, 23, 29, A-2
RS 485 4, 9, 14, 16, 23, 29, A-2
RUN 39

S
Serial drivers A-2
Serial line A 12, 29
Serial line B 14, 26, 29
Serial lines 4, 13, 29, A-1
Size 8
Software 22, 33
Solder jumpers 31

T
Temperature 9
Termination circuit 9, 16, 30
Time 40
TransZorb™ 4
Trimmer 17, 23
TTL signals  6, 23

V
Version  1

W
Warranty  1
Watch dog  6, 8, 26, 28, 36, 39
Weight  8