

# GPC<sup>®</sup> 554

General Purpose Controller 80C552 Philips

## TECHNICAL MANUAL



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GPC<sup>®</sup> 554

Edition 5.10 Rel. 27 February 1998

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# GPC<sup>®</sup> 554

**General Purpose Controller 80C552 Philips**

## TECHNICAL MANUAL

Intelligent module of the **Abaco<sup>®</sup> BLOCK 4 Serie**, 100x50 mm size; Optional plastic mount for connection to **DIN 46277-1** and **DIN 46277-2**  $\Omega$  rails; **CPU 80C552, 22MHz**, with maximum address 96KBytes; 32KRAM and socket for 32K EPROM, 32K EEPROM, RAM or EPROM; **Back-up** circuit for **32K RAM**, through external **LITHIUM** battery; Serial **E<sup>2</sup>**, from 128 to 2048Bytes; **Watch-Dog** settable vi software; 2 **RS 232** serial lines one of which software with Baud-Rate settable via software; 6/8 **A/D** Converter lines of **10 Bits**, +2,5V full scale; conversion time **27 $\mu$ s**; 16 TTL **I/O** lines settable via softwar; 2 **PWM** independent outputs of 8 bits; 2 software-readable Dip Switches, and Dip for **RUN/DEBUG Mode**; 16 bits Timer-Counter having 4 Capture registers and 3 Comparable registers; 6 outputs Set-Reset connected to the Comparator T2, plus 2 Toggle outputs ; 26 ways connector for **Abaco<sup>®</sup> I/O BUS** and 26 ways connector for **I/O, A/D, PWM**; Facility of operation in **Idle-Mode or Power-Down Mode**; External supply from mains at 5Vdc, 110 mA and **TransZorb<sup>™</sup>** protected; Wide range of developement software such as: **Monitor, Debugger, Assembler, GET 51** and **BASIC Interpreter, BASIC Compiler, FORTH, C Compiler, HTC-51, CMX-RTX, PLM 51, PASCAL Compiler** etc.

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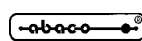
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For specific informations on the components mounted on the card, please refer to the Data Book of the builder or second sources.

### SYMBOLS DESCRIPTION

In the manual could appear the following symbols:

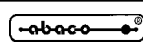


Attention: Generic danger



Attention: High voltage

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## INTRODUCTION

The use of these devices has turned - IN EXCLUSIVE WAY - to specialized personnel.

The purpose of this handbook is to give the necessary information to the cognizant and sure use of the products. They are the result of a continual and systematic elaboration of data and technical tests saved and validated from the Builder, related to the inside modes of certainty and quality of the information.

The reported data are destined- IN EXCLUSIVE WAY- to specialized users, that can interact with the devices in safety conditions for the persons, for the machine and for the environment, impersonating an elementary diagnostic of breakdowns and of malfunction conditions by performing simple functional verify operations , in the height respect of the actual safety and health norms.

The informations for the installation, the assemblage, the dismantlement, the handling, the adjustment, the reparation and the contingent accessories, devices etc. installation are destined - and then executable - always and in exclusive way from specialized warned and educated personnel, or directly from the TECHNICAL AUTHORIZED ASSISTANCE, in the height respect of the builder recommendations and the actual safety and health norms.

The devices can't be used outside a box. The User must always insert the cards in a container that respect the actual safety normative. The protection of this container is not threshold to the only atmospheric agents, but specially to mechanic, electric, magnetic, etc. ones.

To be on good terms with the products, is necessary guarantee legibility and conservation of the manual, also for future references. In case of deterioration or more easily for technical updates, consult the AUTHORIZED TECHNICAL ASSISTANCE directly.

To prevent problems during card utilization, it is a good practice to read carefully all the informations of this manual. After this reading, the User can use the general index and the alphabetical index, respectly at the begining and at the end of the manual, to find information in a faster and more easy way.

## CARD VERSION

The present handbook is reported to the GPC® 554 card release **100997** and later. The validity of the bring informations is subordinate to the number of the card release. The user must always verify the correct correspondence among the two denotations. On the card the release number is present in more points both board printed diagram (serigraph) and printed circuit (for example near the CN2 connector in the component side).



## GENERAL FEATURES

The **GPC<sup>®</sup> 554** is a powerful control **Low-Cost** module capable of operating in stand-alone mode or as an intelligent peripheral, and/or remoted, in a wider telecontrol or acquisition network. It belongs to the CPUs **4 Serie** 100x50 mm.size **BLOCK** family. The **GPC<sup>®</sup> 554** module can be supplied with its plastic mount for connection to **Omega** rails **DIN 46277-1** and **DIN 46277-2**, thereby dispensing with the need of **rack** and allowing a less costly mounting direct to the electrical control panel. Thanks to this small size, the **GPC<sup>®</sup> 554** can be put into the same plastic rails that contains the Peripheral I/O, i.e **ZBR 168**, forming in this way an unique **BLOCK** element. Another application of this **GPC<sup>®</sup> 554** is that when it is used as CPU it can be mounted in **Piggy-Back**, on the peripheral cards of the end user. The **GPC<sup>®</sup> 554** card supports the different versions of **80C552** and **87C552** chips all of them software compatible with the **8051 INTEL**. At present are available many developing software Tools which allow the card to be used as developing system of itself both in Assembler and evolved languages. Special attention is due to development Tools as **C Compilers**, the **FORTH** and the handy **BASIC 554**. This latter is compatible with the widespread **MCS<sup>®</sup> BASIC-52** of **INTEL** to which have been added new commands. Some of these ones need a special mention i.e the **A/D**, **I<sup>2</sup>C-BUS**, **RTC**, **Serial EEPROM**, direct managing of **LCD** or **Fluorescent Displays** and of a Matrix Keyboard etc. For an immediate use of this new command, **KDL-224** boards are available, or if you need a finished object, there is the Operator Panel **QTP 24P**. This Operator Panel, offered in the open frame version, bears the same aesthetic as **QTP 24**, but, as the local intelligence is not furnished, it is driven directly by **GPC<sup>®</sup> 554**, allowing a notable cost reduction. The **BASIC 554** affords truly notable debug facilities, and allows to program directly on board a **EEPROM** with the user program. To speed the applicative system, or to make it unreadable to intrusive eyes, the **BASIC Compiler BXC51**, provided with libraries that accept as source what has been generated and debugged with **BASIC 554**, is available. The **GPC<sup>®</sup> 554** is equipped with a series of standard **Abaco<sup>®</sup>** connectors allowing immediate use of the many **BLOCK I/O** modules available, or enabling a simple and inexpensive means of connections to equipment interfaces made by the user or by third parties. For getting a quick prototype, cards such as **SPA 03** and **SPA 04** on which it is possible to mount the **GPC<sup>®</sup> 554** in **Piggy Back**, are used. The presence on board of the **Abaco<sup>®</sup> I/O BUS** connector, allows to drive directly **I/O** cards as: **ZBR 84**, **ZBR 168**, **ZBR 246**, **ZBR 324**, **ZBT 84**, **ZBT 168**, **ZBT 246**, **ZBT 324**, and through **ABB 03**, **ABB 05** and so on.. it is possible to manage all the peripheral cards available on **Abaco<sup>®</sup> BUS**.

- Intelligent module of the **Abaco<sup>®</sup> BLOCK 4 Serie**, 100x50 mm size
- Optional plastic mount for connection to **DIN 46277-1** and **DIN 46277-2**  $\Omega$  rails
- CPU **80C552**, **22MHz**, with maximum address 96KBytes
- 32KRAM and socket for 32K EPROM, 32K EEPROM, RAM or EPROM
- **Back-up** circuit for **32K RAM**, through external **LITHIUM** battery
- Serial **E<sup>2</sup>**, from 128 to 2048Bytes; **Watch-Dog** settable vi software
- 2 **RS 232** serial lines one of which software with Baud-Rate settable via software
- 6/8 **A/D** Converter lines of **10 Bits**, +2,5V full scale; conversion time **27 $\mu$ s**
- 16 TTL **I/O** lines settable via software; 2 **PWM** independent outputs of 8 bits
- 2 software-readable Dip Switches, and Dip for **RUN/DEBUG Mode**
- 16 bits Timer-Counter having 4 Capture registers and 3 Comparable registers
- 6 outputs Set-Reset connected to the Comparator T2, plus 2 Toggle outputs
- 26 ways connector for **Abaco<sup>®</sup> I/O BUS** and 26 ways connector for **I/O**, **A/D**, **PWM**
- Facility of operation in **Idle-Mode** or **Power-Down Mode**
- External supply from mains at 5Vdc, 110 mA and **TransZorb<sup>TM</sup>** protected
- Wide range of development software such as: **Monitor**, **Debugger**, **Assembler**, **GET 51** and **BASIC Interpreter**, **BASIC Compiler**, **FORTH**, **C Compiler**, **HTC-51**, **CMX-RTX**, **PLM 51**, **PASCAL Compiler** etc.

## CPU

The **GPC® 554** can use all version of microprocessors namely 80C552, 87C552, 80C562, 87C562. These 8 bit microprocessors are code compatible with the 8051 INTEL and so they have an extended instruction set, fast execution time, easy use of all kind of memory and an efficient interrupt management. The most important features of the described 80C552 microprocessor, are:

- 8k bytes EPROM, 256 bytes RAM;
- 6 independent 8 bits I/O ports;
- 2 standard 16 bits Timer/Counters;
- 16 bits Timer/Counters with Capture and Compare function;
- 2 priority level for interrupts;
- 8 lines 10 bits A/D converter;
- 2 independent 8 bits PWM outputs;
- 1 synchronous/asynchronous serial line;
- 1 I<sup>2</sup>C bus line;
- Watch Dog Timer;
- Idle mode or Power down mode;

For further information, please refer to specific documentation of the manufacturing company.

## MEMORY DEVICES

On the card can be mounted 98 K and 256 bytes of memory divided with a maximum of **32K** EPROM, **32K** RAM, **32K** EEPROM/RAM/EPROM and **2K** of serial EEPROM. The **GPC® 554** memory configuration must be chosen considering the application to realize or the specific requirements of the User. Normally the card is equipped with 32K byte of RAM and 512 bytes of serial EEPROM and all different configurations must be specified from the User, at the moment of the order. With the on board back up circuit there is the possibility to keep the 32K RAM data (IC8), also when power supply is failed; in this way the card is always able to maintain parameters, logged data, system status and configuration, etc. without using expensive external UPS. The back up circuit is based on an external battery that the user must connect through CN2 connector. By selecting the backed RAM module or the EEPROM module on IC6 the user can improve the on board RAM capacity. The addressing of memory devices is controlled by a specific on board circuit, that provides to allocate the devices in the microprocessor address space. For further information about memory configuration, sockets description and jumpers connection, please refer to chapter "HARDWARE DESCRIPTION", "PERIPHERAL SOFTWARE DESCRIPTION" and to the paragraph "MEMORY SELECTION".

## POWER SUPPLY

The card must be powered only with +5 Vdc through the pin 25 (GND) and pin 26 (+5Vdc) of the CN1 connector. The power supply circuit generates all the necessary voltages for the card and it was designed for reducing the consumption (the microprocessor power down and idle mode is available) and for increasing the electrical noise immunity. Remember that on board there is a protection circuit against voltage peaks by **TransZorb™**.

## SERIAL COMMUNICATION

The serial communication line is completely software configurable for protocol and speed while it is hardware configurable for electric standard interface. Simply programming the microprocessor SIO, the User can set the baud rate, stop bits number, length of character, parity and handshake.

The card supports only RS 232 interface. **GPC® 554** has an additional serial communication line with the I<sup>2</sup>C BUS or ACCESS bus™ standard, that can be directly used to communicate with other intelligent systems with the same interface. Alternatively, networks made up exclusively of **GPC® 554** modules provide a simple and economic solution. Some software tools (**BASIC 554**, etc.) have a RS232 software serial line that is available on the CN3B connector if JS12 and JS13 are in 2-3 position. For further information about serial communication please refer to appendix A of this manual or to the technical documentation of the manufacturing company.

## ABACO® I/O BUS

One of the most important features of **GPC® 554** is its possibility to be interfaced to industrial **ABACO® I/O BUS**. Thanks to its standard **ABACO® I/O BUS** connector, the card can be connected to some of the numerous **Grifo®** boards, both intelligent and not. For example the user can directly use cards for analog signals acquisition (A/D), cards for analog signals generation (D/A), cards for digital I/O signals management, cards with timers and counters, cards for temperature controls, etc. Using **ABB 03** or **ABB 05** mother boards it is possible manage all the **BUS ABACO®** single EURO cards. So **GPC® 553** becomes the right component for each industrial automation system, in fact **ABACO® I/O BUS** makes the card easily expandable with the best price/performance ratio.

## CONTROL LOGIC

The addresses of all peripheral device's registers and of memory devices on **GPC® 554** are assigned from a specific control logic that allocates all these devices in the microprocessor addressing space. For further information please refer to paragraph "I/O ADDRESSES" of this manual.

## RESET CONTACT

P1 reset contact of **GPC® 554** allows the activation of /RESET card signal. By connecting P1, the card restarts execution of the program saved in EPROM and all the on board peripheral devices are reset at the same time. P1 is commonly used to exit from endless loop, especially during debug phase. To recognize reset contact location on **GPC® 554**, please refer to figure 11.

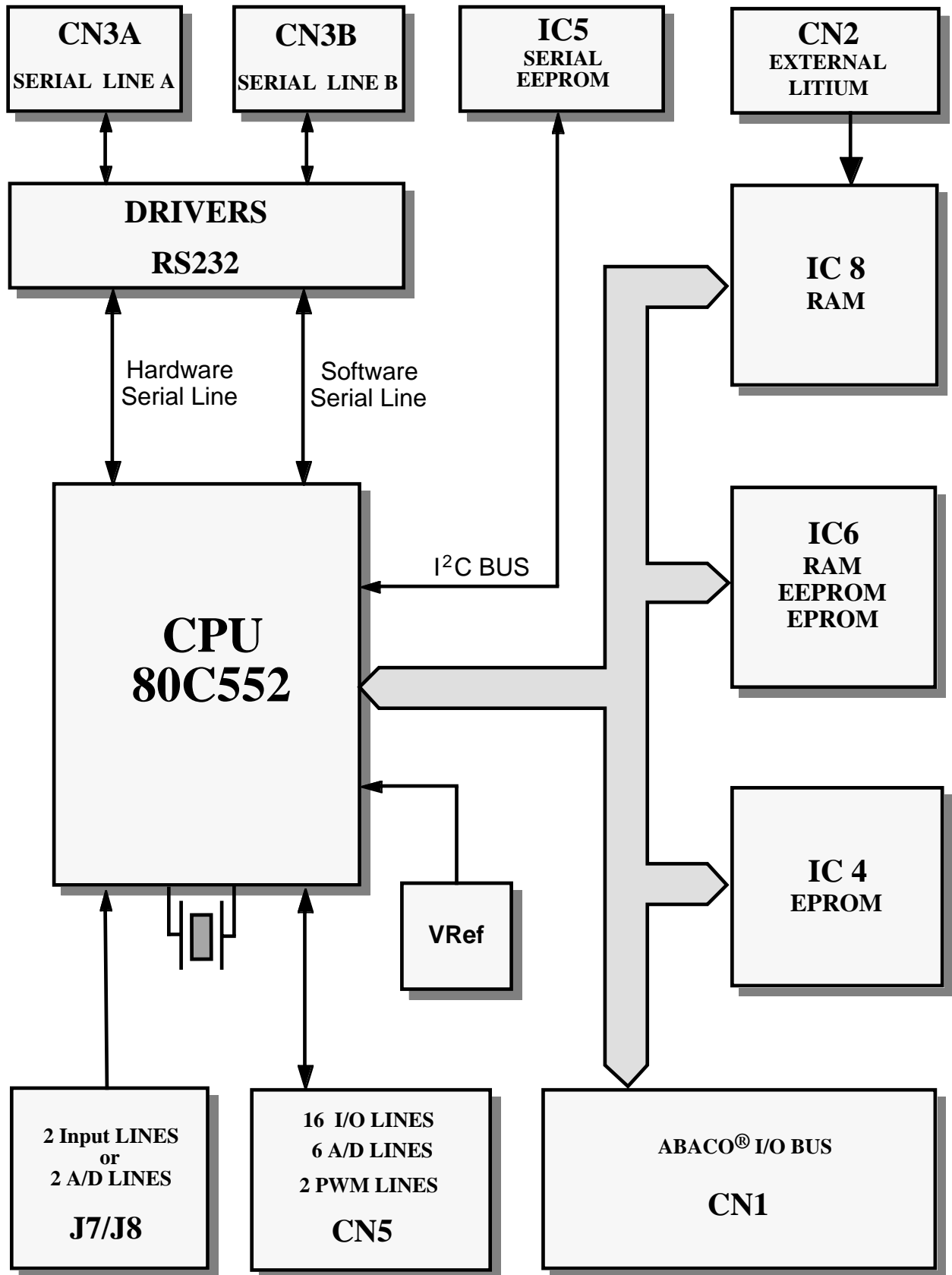


FIGURE 1: BLOCK DIAGRAM

## PERIPHERAL DEVICES

**GPC® 554** is the right card to solve many control problems in automation fields, in fact it is equipped with some peripheral components that facilitate the connection and the management to external system like probes, switches, relays, motor controllers, etc. These peripherals are:

- **SIO 0:** it is a microprocessor peripheral device that manages serial communication with any other system provided of RS 232 serial line. By software the User can set baud rate, length of character, stop bit number, parity and handshake through a simple programming of internal microprocessor registers.
- **A/D converter:** it is a CPU internal peripheral device that converts 6/8 different analog signals with 10 bits of resolution. By software the User selects the channel to convert, starts the conversion and controls the end of conversion, through programming of microprocessor internal registers. The analog inputs must be voltage inputs in the range: 0÷2,49Vdc. Some software tools (BASIC 554, etc.) have high level procedures that manage directly the A/D.
- **PWM:** it is a CPU internal peripheral device that generates two separate PWM signals. By software the User can sets frequency and duty cycle of each signal, programming three 8 bits internal registers.
- **WATCH DOG:** it is a CPU internal peripheral device that can reset the card at programmable time intervals, if not retriggered. By software the User can set the watch dog time (from 1,111 ms to 283,305 ms), enable or disable the watch dog device and retrigger the circuit to prevent card reset.
- **EEPROM seriale:** With the IC5 EEPROM module (range 128÷2048 bytes), there is the possibility to keep data also when power supply failed; in this way the card is always able to maintain parameters, logged data, system status and configuration, etc. without using expensive external UPS. This component has a default size of 512 bytes.

For further information about peripheral device please refer to the technical documentation of the manufacturing company.

## LOCAL USER INTERFACES

With CN5 (standard I/O Abaco® connector) the **GPC® 554** can be connected to some of the numerous **Grifo®** boards modules that have the same pin\_out. It is really important the capability of directly connect a series of boards such as **QTP 24P**, **KDL x24**, **KDF 224**, ecc. that are useful to solve local user interfaces prblems. These boards already have all the resources (alphanumeric displays, matrix keyboards, LEDs etc) necessary to solve the common man-machine communication problems at a short distance from **GPC® 554**. For hardware installation these locals user-interfaces requires only a 20 ways flat cable (with power supply too) while for software the programmer can use the relative procedure contained in all the **GPC® 554** software tools. These procedures normally are drivers software added to the language and they use directly its console instructions (for example INPUT and PRINT for BASIC, PRINTF and SCANF for C etc. ), so for the user is very simple to write on displays and to get data from keyboards.

## TECHNICAL FEATURES

### GENERAL FEATURES

<b>Devices:</b>	16 programmable TTL Input/Output lines. 3 Timer Counters (16 bits). 2 bidirectional RS 232 serial line (1 software). 1 Watch Dog 6/8 A/D converter line. 1 Local contact for reset. 3 software readable user inputs. 2 PWM lines (8 bits). 1 Abaco® I/O BUS expansion connector.
<b>Memory:</b>	IC 4: 32K x 8 EPROM. IC 8: 32K x 8 RAM. IC 6: from 8K x 8 to 32K x 8 RAM/EEPROM//EPROM IC 5: serial EEPROM from 128 bytes to 2048 bytes.
<b>CPU:</b>	PHILIPS 80C552
<b>Clock Frequency:</b>	22.1184 MHz
<b>A/D resolution:</b>	10 bits
<b>A/D conversion time:</b>	27 µs

### PHYSICAL FEATURES

<b>Size:</b>	100 x 50 mm
<b>Weight:</b>	75 g. (Complete configuration)
<b>Connectors:</b>	CN1: 26 pins, male, vertical, low profile connector. CN2: 2 pins, male, vertical connector. CN3A: 6 pins PLUG connector. CN3B: 6 pins PLUG connector. CN5: 26 pins, male, vertical, low profile connector. J7, J8: 4 pins, male, strips connector.
<b>Temperature range:</b>	0÷50 C°.
<b>Relative humidity:</b>	20%÷90% (without condense).
<b>Watch_dog reset Time:</b>	1,111÷283,305 ms

**ELECTRIC FEATURES**

- Power supply voltage:** +5 Vdc
- Consumption on 5 Vdc:** 130 mA
- Back-up external battery:** 3,6÷5 Vdc
- Back-up current:** 1 μA
- Voltage analog inputs:** 0÷2,49 Vdc

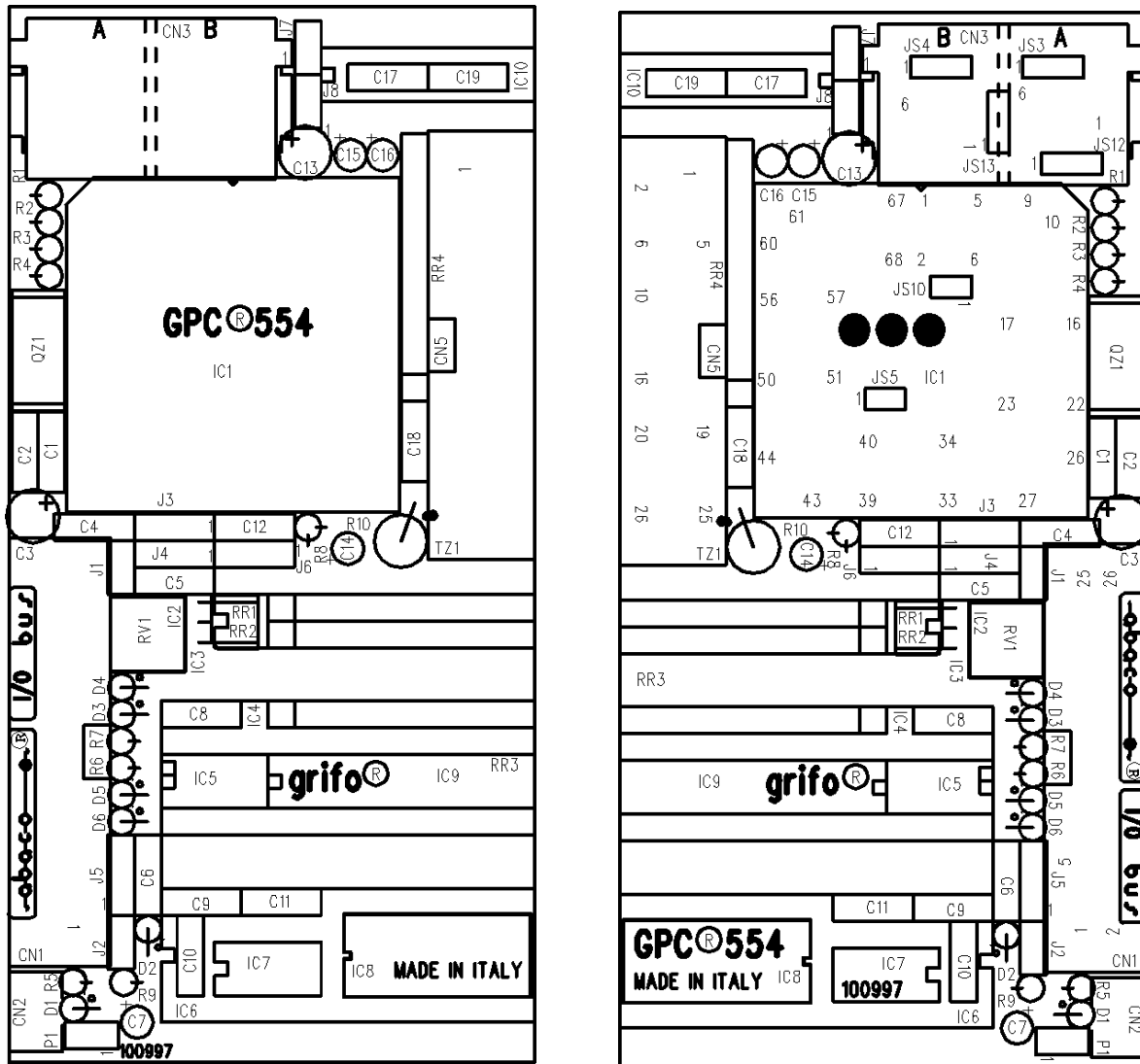


FIGURE 2: COMPONENTS MAPS (SOLDERING SIDE AND COMPONENTS SIDE)

## INSTALLATION

In this chapter there are the information for a right installation and correct use of the card. The User can find the location and functions of each connectors, jumpers and some explanatory diagrams.

### CONNECTIONS

The GPC®554 module has 6 connectors that can be linkeded to other devices or directly to the field, according to system requirements. In this paragraph there are connectors pin out, a short signals description (including the signals direction) and connectors location (see figure 11).

#### J7, J8 - CONNECTOR FOR P5.6 AND P5.7 A/D LINES ACQUISITION

J7, J8 is a 4 pins, male, strips connector with 2,54mm pitch. The pins of this connector have a double function in fact, the P5.6 and P5.7 line can be used as a generic digital input line or as A/D analog input line.

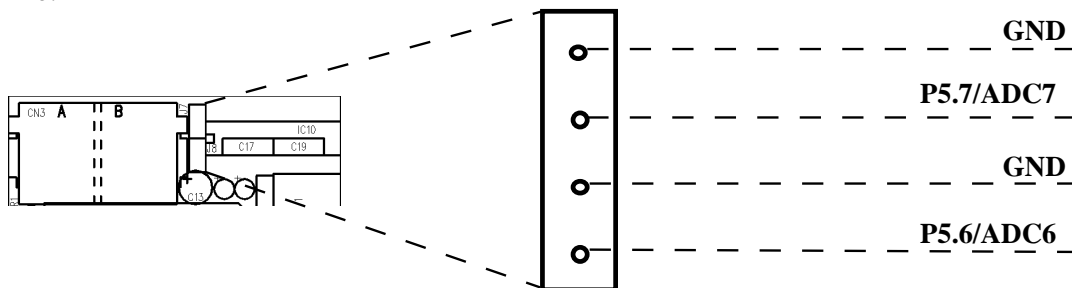


FIGURE 3: J7, J8 - CONNECTOR FOR P5.6 AND P5.7A/D LINES ACQUISITION

Signals description:

**P5.n/ADCn** = I - Digital line "n" or analog channel "n" of A/D.  
**GND** = - Digital and analog ground signal.

#### CN2 - BACK UP EXTERNAL BATTERY CONNECTOR

CN2 is a 2 pins, male, vertical connector with 2,54mm pitch.

Through CN2 the user must connect an external battery for RAM (IC8) back up when the power is switched off (for further information please refer to chapter "BACK UP").

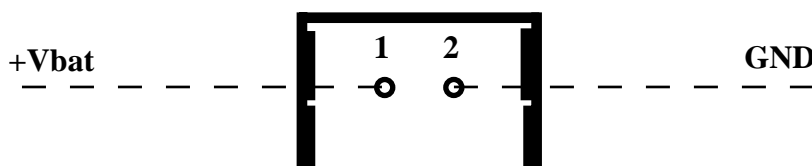


FIGURE 4: CN2 - BACK UP EXTERNAL BATTERY CONNECTOR

Signals description:

**+Vbat** = I - Back up external battery positive pin  
**GND** = - Back up external battery negative pin



## CN1 - ABACO® I/O BUS CONNECTOR

CN1 is a 26 pins, male, vertical, low profile connector with 2,54mm pitch. Through CN1 the card can be connected to some of the numerous **Grifo®** boards, both intelligent and not. For example the user can directly use cards for analog signals acquisition (A/D), cards for analog signals generation (D/A), cards for digital I/O signals management, cards with timers and counters, cards for temperature controls, etc. All this connector signals are at TTL level.

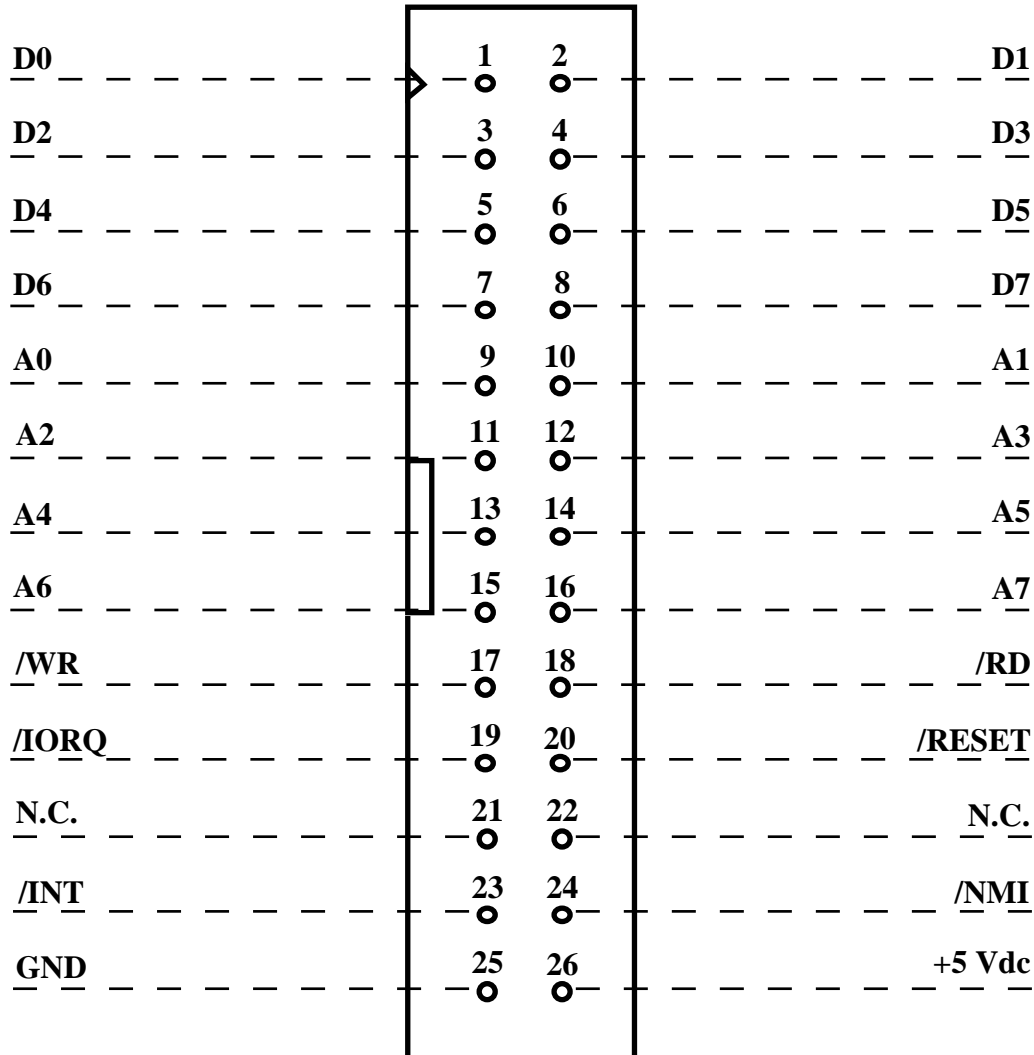


FIGURE 5: CN1 - ABACO® I/O BUS CONNECTOR

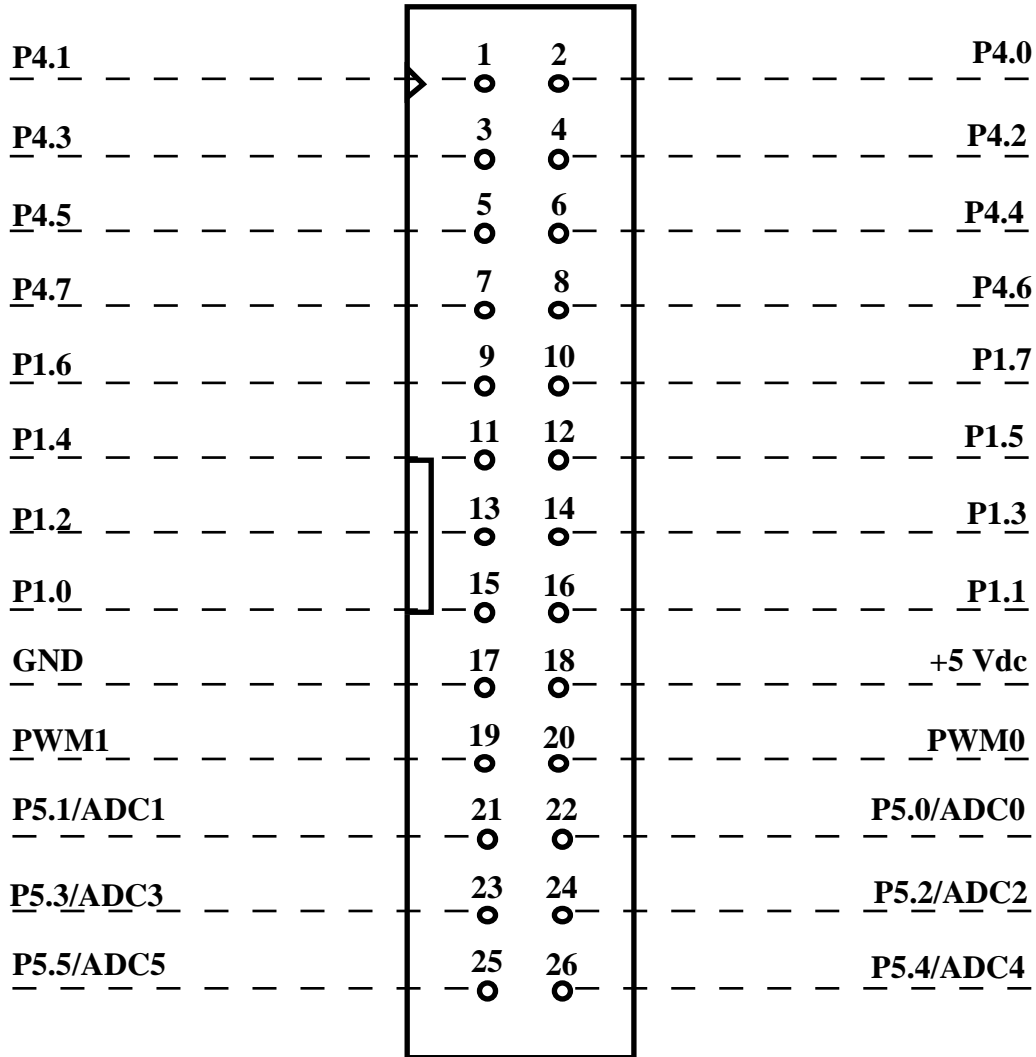
Signals description:

<b>A0-A7</b>	=	O	-	Address BUS.
<b>D0-D7</b>	=	I/O	-	Data BUS.
<b>/INT</b>	=	I	-	Interrupt request (open collector type).
<b>/NMI</b>	=	I	-	Non Mascable Interrupt.
<b>/IORQ</b>	=	O	-	Input Output Request.
<b>/RD</b>	=	O	-	Read cycle status.
<b>/WR</b>	=	O	-	Write cycle status.
<b>/RESET</b>	=	O	-	Reset.
<b>+5 Vdc</b>	=	I/O	-	+5 Vdc power supply.
<b>GND</b>	=	-	-	Digital ground signal.
<b>N.C.</b>	=	-	-	Not Connected.

**CN5 - CONNECTOR FOR CPU I/O, A/D CONVERTER INPUTS, PWM LINES.**

CN5 is a 26 pins, male, vertical, low profile connector with 2,54 mm pitch.

On CN5 are available microprocessor port 1, port 4 and 6 lines of port 5. This last port can be connected either to digital TTL inputs or to analog signals for A/D converter section, thanks to its double functionality. The analog inputs must be voltage inputs in the range 0÷2,49 Vdc. On CN5 connector are also available microprocessor PWM lines useful for motor control and D/A simulation.



**FIGURE 6: CN5- CONNECTOR FOR CPU I/O, A/D CONVERTER INPUTS AND PWM LINES**

Signals description:

- P1.n** = I/O - Digital line n of the CPU port 1.
- P4.n** = I/O - Digital line n of the CPU port 4.
- PWM0** = O - CPU PWM 0 line.
- PWM1** = O - CPU PWM 1 line.
- P5.n/ADCn** = I - Digital line n or A/D channel n of CPU port 5.
- GND** = - - Digital and analog ground signal.
- +5 Vdc** = - - +5 Vdc power supply.

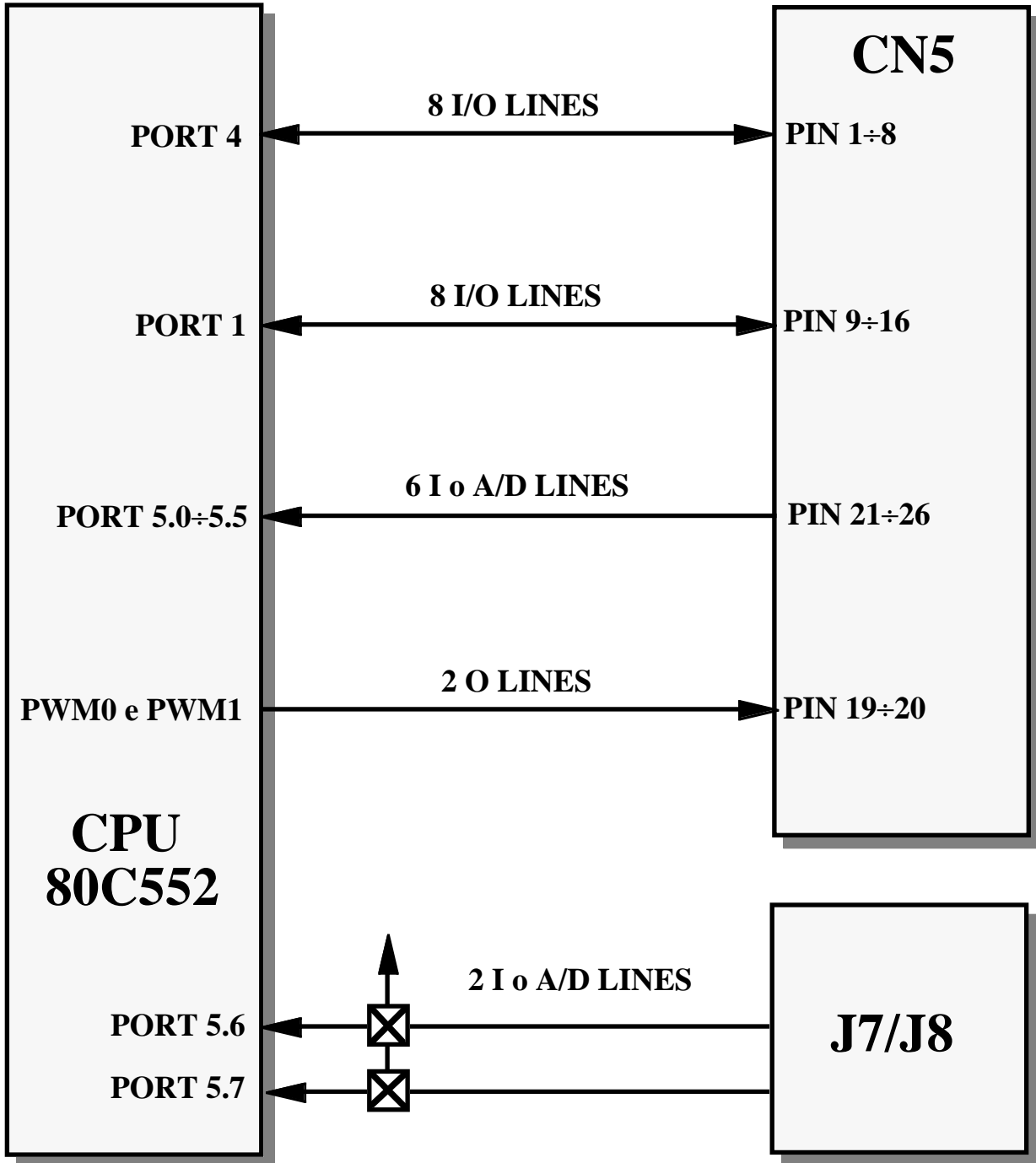


FIGURE 7: I/O LINES CONNECTION DIAGRAM

## CN3A - SERIAL COMMUNICATION LINE "A" CONNECTOR

CN3A is a 6 pins PLUG connector.

On CN3A connector are available the buffered signals for RS 232 serial line "A" communication. The RS 232 electric protocol follows the CCITT normative. All the signals are placed in order to reduce interference and electrical noise.

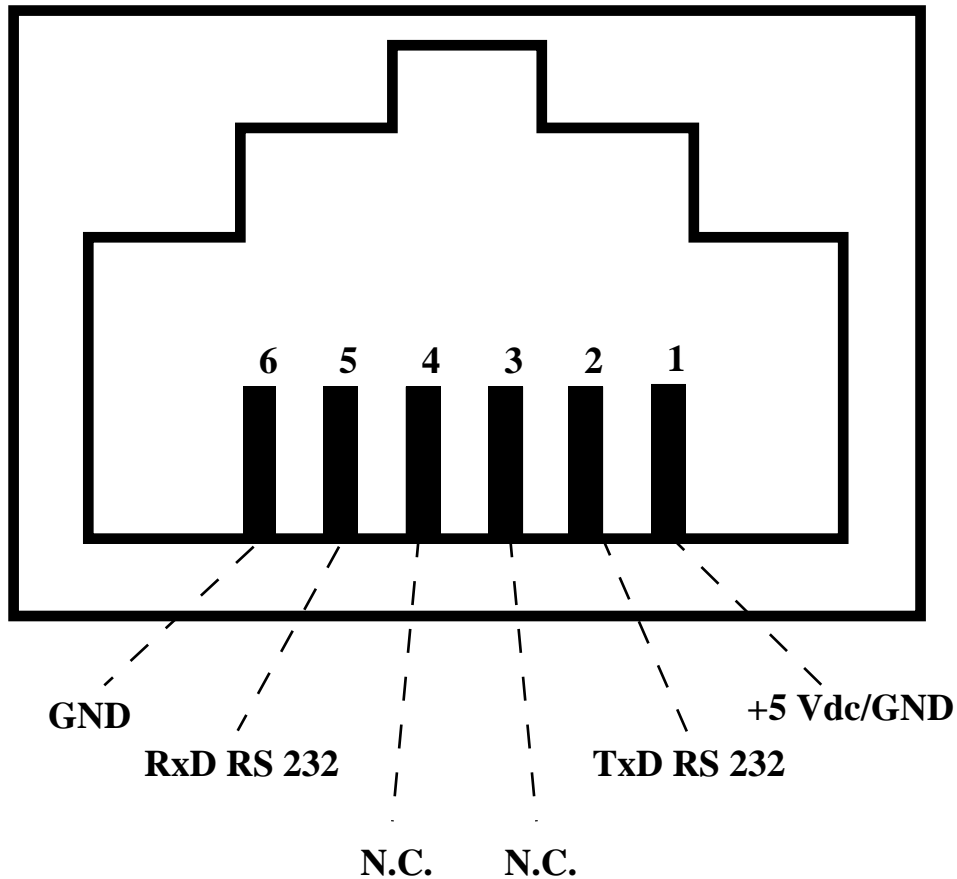


FIGURE 8: CN3A-SERIAL COMMUNICATION LINE "A" CONNECTOR

Signals description:

<b>RxD RS 232</b>	=	I	-	Receive Data for RS 232.
<b>TxD RS 232</b>	=	O	-	Transmit Data for RS 232.
<b>+5 Vdc/GND</b>	=	-	-	+5 Vdc power supply or Digital ground signal.
<b>GND</b>	=	-	-	Digital ground signal.
<b>N.C.</b>	=	-	-	Not Connected.

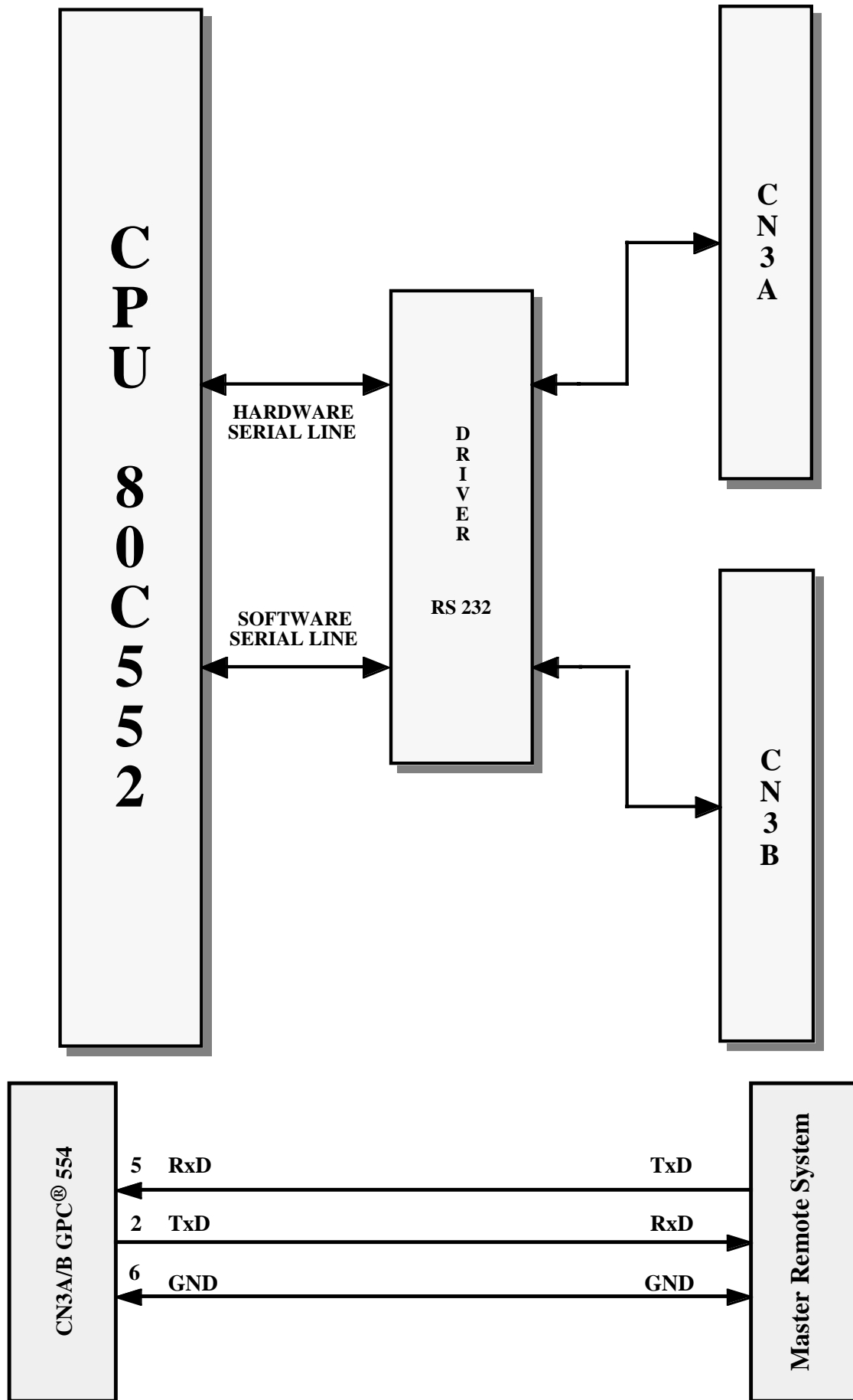


FIGURE 9: SERIAL COMMUNICATION DIAGRAM

## CN3B - SERIAL COMMUNICATION LINE "B" CONNECTOR (SOFTWARE SERIAL LINE)

CN3B is a 6 pins, female, PLUG connector.

On CN3B are available the buffered signals for only RS 232 serial line "B" communication.

All the signals are placed in order to reduce interference and electrical noise; the signals follow the standard CCITT normative. Remember that the serial line "B" is a software serial line so only some software package for example BASIC 554 manage it at high level.

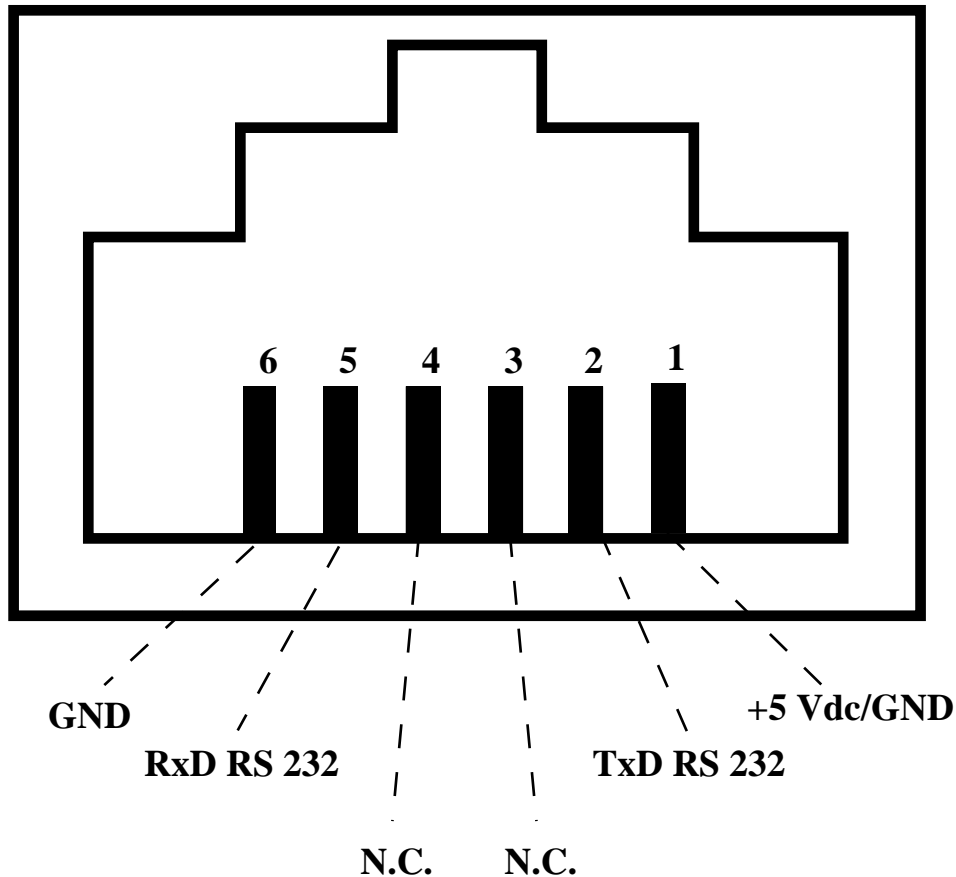


FIGURE 10: CN3B-SERIAL COMMUNICATION LINE "B" CONNECTOR.

Signals description:

<b>RxD RS 232</b>	=	I	-	Receive Data for RS 232.
<b>TxD RS 232</b>	=	O	-	Transmit Data for RS 232.
<b>+5 Vdc/GND</b>	=	-	-	+5 Vdc power supply or Digital ground signal.
<b>GND</b>	=	-	-	Digital ground signal.
<b>N.C.</b>	=	-	-	Not Connected.

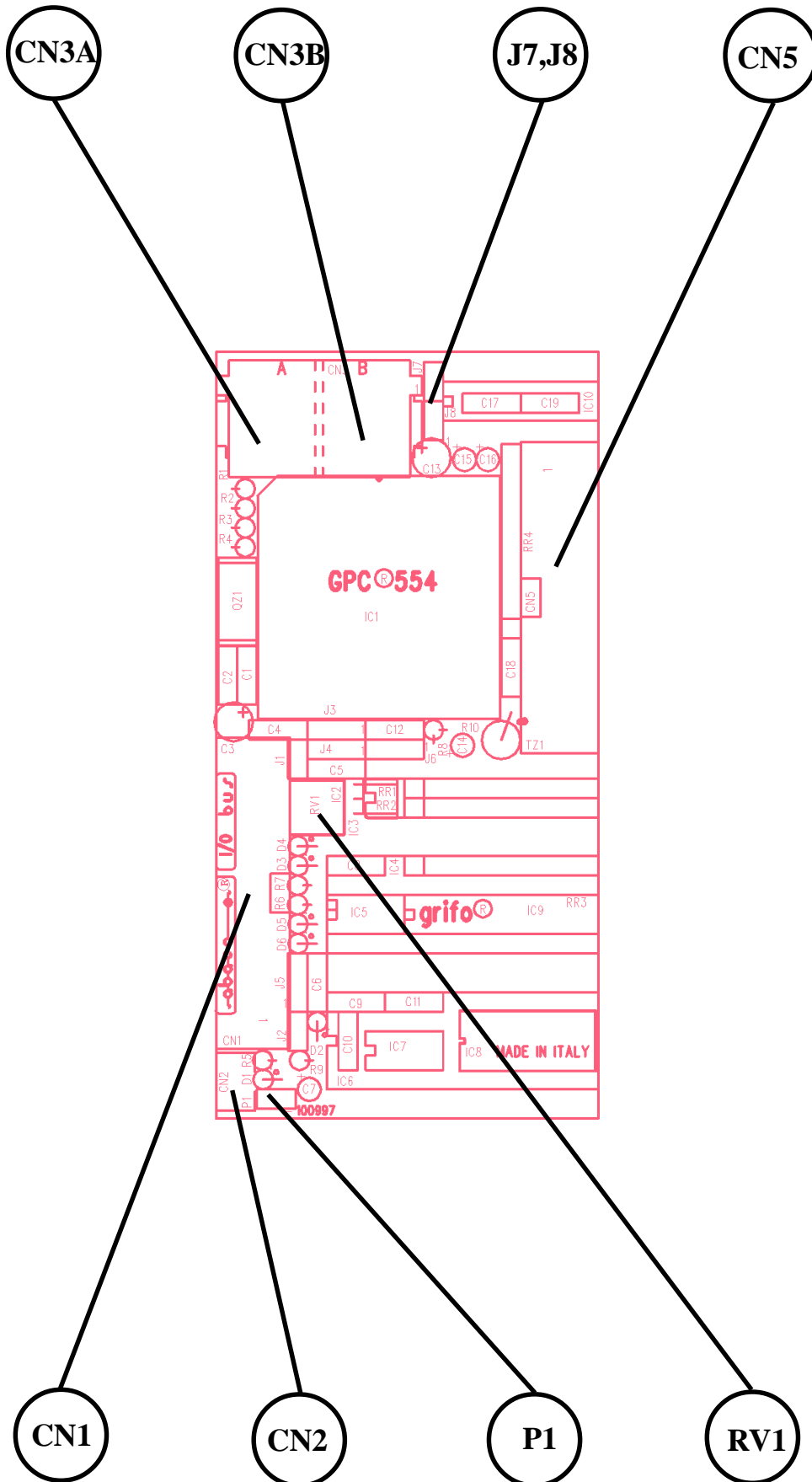


FIGURE 11: P1, RV1 AND CONNECTORS LOCATION

## I/O CONNECTION

To prevent possible connecting problems between **GPC® 554** and the external systems, the User has to read carefully the previous paragraph information and he must follow these instructions:

- For RS 232 signals the User must follow the standard rules of this protocol.
- For all TTL signals the User must follow the rules of this electric standard. The connected digital signal must be always referred to card digital ground and if an electric insulation is necessary, then an opto coupled interface must be connected. For TTL signals, the 0Vdc level corresponds to logic state "0", while 5Vdc level corresponds to logic state "1".
- The analog inputs (A/D section) must be connected to low impedance signals and with the ranges: 0÷+2,49 Vdc.

## ON BOARD INPUT

**GPC® 554** card is equipped with 3 jumpers (J2, J7, J8) that can be read by software. They are normally used for system configuration (operating mode selection, card number programming inside a network system, firmware configuration, etc.). The J2 status ("0" = CONNECTED; "1" = NOT CONNECTED) can be acquired by reading the RUN/DEBUG register that is allocated in the microprocessor addressing space by the control logic, as described in the paragraph "I/O ADDRESSES". The J7 and J8 status ("0" = CONNECTED; "1" = NOT CONNECTED) can be acquired by reading respectively the pin P5.7 and pin P5.6 of the CPU. For recognizing J2, J7 and J8 location on **GPC® 554**, please refer to figure 15.

## INTERRUPTS MANAGEMENT

One of the most important **GPC® 554** features is the powerful interrupts management. Following there is a brief description on interrupt hardware signals management of the card:

- /INT **ABACO®** I/O BUS   ->   generates an interrupt signal on pin 26 (/INT0) of CPU  
(JS12 in 1-2 position)
- /NMI **ABACO®** I/O BUS   ->   generates an interrupt signal on pin 28 (T0) of CPU  
(JS13 in 1-2 position)

For software information about all internal interrupts and the interrupt management by the CPU, please refer to specific documentation of the manufacturing company.

## TRIMMERS AND CALIBRATION

On **GPC® 554** is available a RV1 trimmer that calibrates the Vref voltage of the A/D converter section. Please refer to figure 11 for RV1 location.

The **GPC® 554** is subjected to a careful test that verifies and calibrates all the card sections. The calibration is done in laboratory at +20 C° following this steps:



- The A/D voltage reference (Vref) is calibrated through RV1 trimmer by using a 5 digits tester to a value of +2,4900 Vdc.
- The correspondance between the analog input signal and the A/D combination is verified. The verification is done with a reference signal on the A/D input and testing that the A/D combination and the teoric combination differ at maximum of the A/D section errors sum.
- The trimmer is blocked with paint.

The analog interfaces use high precision components that are selected during mounting phase to avoid complicate and long calibration procedures. After the calibration, all the on board trimmer are blocked with paint to warrant calibration also in presence of mechanics stresses (vibrations, movings, etc.). The user must not modify the card calibration, but if thermic drifts,time drifts, etc require it, he must follow the previous described procedure.

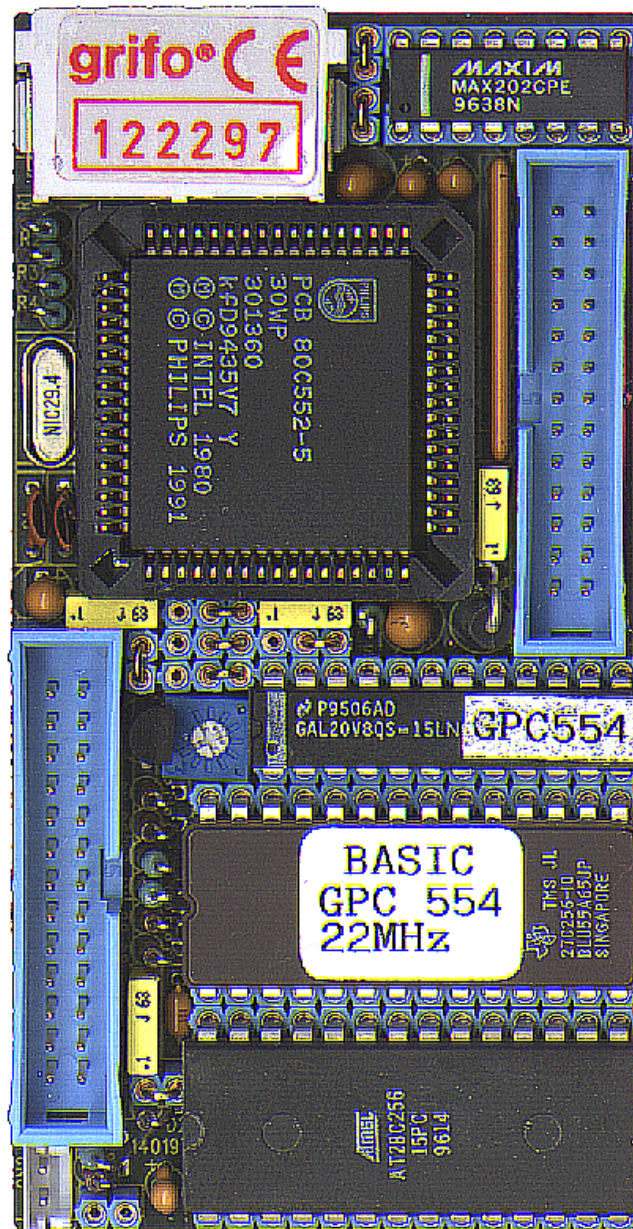


FIGURE 12: CARD PHOTO

## JUMPERS

On **GPC® 554** there are 14 jumpers for card configuration. Connecting these jumpers, the User can define for example the memory type and size, the peripheral devices functionality and so on. Here below is the jumpers list, location and function:

JUMPERS	PIN N°	FUNCTION
J1	2	It selects the memory map.
J2	2	It selects the connection for RUN/DEBUG user input.
J3	3	It selects IC6 memory type.
J4	3	It selects IC6 size and memory type.
J5	3	It selects IC6 size and memory type.
J6	3	It selects the memory map.
J7	2	It selects the connection for pin 62 (P5.7) of the CPU (USER INPUT).
J8	2	It selects the connection for pin 63 (P5.6) of the CPU (USER INPUT).
JS3	3	It selects the connection for pin 1 of CN3A.
JS4	3	It selects the connection for pin 1 of CN3B.
JS5	2	It enables/disables optional microprocessor internal ROM.
JS10	2	It enables/disables the WATCH-DOG by hardware.
JS12	3	It selects the connection for pin 26 (P3.2-/INT0) of the CPU.
JS13	3	It selects the connection for pin 28 (P3.4-T0) of the CPU.

**FIGURE 13: JUMPERS SUMMARIZING TABLE**

The following tables describe all the right connections of **GPC® 554** jumpers with their relative functions. To recognize these valid connections, please refer to the board printed diagram (serigraph) or to figure 2 of this manual, where the pins numeration is listed; for recognizing jumpers location, please refer to figure 15 and appendix A.

**2 PINS JUMPERS**

<b>JUMPERS</b>	<b>CONNECTION</b>	<b>FUNCTION</b>	<b>DEF.</b>
J1	not connected connected	This jumper is used with J6 for the memory map selection so for further information please refer to chapter "MEMORY CONFIGURATIONS".	*
J2	not connected  connected	It sets RUN/DEBUG user input at logic level "1".  It sets RUN/DEBUG user input at logic level "0".	*
J7	not connected  connected	It sets P5.7 user input at logic level "1".  It sets P5.7 user input at logic level "0".	*
J8	not connected  connected	It sets P5.6 user input at logic level "1".  It sets P5.6 user input at logic level "0".	*
JS5	not connected  connected	It enables microprocessor internal ROM.  It disables microprocessor internal ROM.	*
JS10	not connected  connected	It disables the WATCH-DOG by hardware.  It enables the WATCH-DOG by hardware.	*

**FIGURE 14: 2 PINS JUMPERS TABLE**

The "\*" denotes the default connection, or on the other hand the connection set up at the end of testing phase, that is the configuration the User receives.

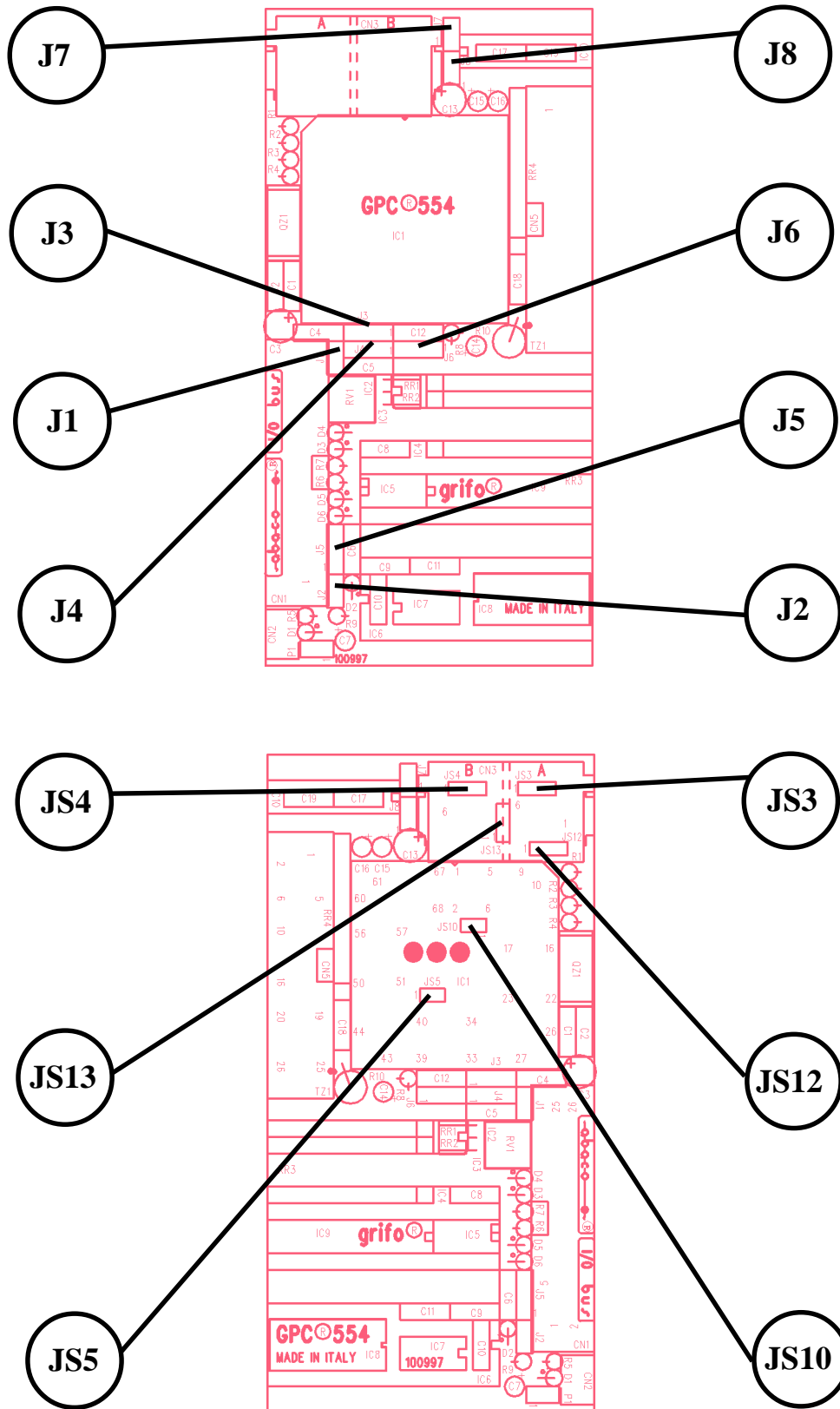


FIGURE 15: JUMPERS LOCATION (COMPONENTS SIDE AND SOLDERING SIDE)

**3 PINS JUMPERS**

JUMPERS	CONNECTION	FUNCTION	DEF.
J3	position 1-2	It configures IC6 for EPROM.	
	position 2-3	It configures IC6 for RAM / EEPROM.	*
J4	position 1-2	It configures IC6 for EPROM	
	position 2-3	It configures IC6 for 32K RAM / EEPROM.	*
	Not connected	It configures IC6 for 8K RAM / EEPROM.	
J5	position 1-2	It configures IC6 for 32K RAM / EEPROM / EPROM.	*
	position 2-3	It configures IC6 for 8K RAM / EEPROM.	
	Not connected	It configures IC6 for 8K EPROM.	
J6	position 1-2	This jumper is used with J1 for the memory map selection so for further information please refer to chapter "MEMORY CONFIGURATIONS".	
	position 2-3		*
	Not connected		
JS3	position 1-2	It connects pin 1 of CN3A to GND.	*
	position 2-3	It connects pin 1 of CN3A to +5 Vdc.	
JS4	position 1-2	It connects pin 1 of CN3B to GND.	*
	position 2-3	It connects pin 1 of CN3B to +5 Vdc.	
JS12	position 1-2	It connects pin 26 of the CPU (P3.2-/INT0) to pin 23 of CN1 (/INT).	
	position 2-3	It connects the receiveing serial line "B" to pin 26 of the CPU (P3.2-/INT0).	*
JS13	position 1-2	It connects pin 28 of the CPU (P3.4-T0) to pin 24 of CN1 (/NMI).	
	position 2-3	It connects the transmission serial line "B" to pin 28 of the CPU (P3.4-T0).	*

**FIGURE 16: 3 PINS JUMPERS TABLE**

The "\*" denotes the default connection, or on the other hand the connection set up at the end of testing phase, that is the configuration the User receives.

**NOTE****SERIAL COMMUNICATION SELECTION**

The serial line "A" is available on connector CN3A and can be buffered only in RS 232.

By software the serial line "A" can be programmed to operate with 7, 8, 9 bits per character, with software parity, with 1 or 2 stop bits at standard or no standard baud rates.

A second software serial line is available on connector CN3B and it can be buffered only in RS 232. By connecting jumpers JS12 and JS13 in 2-3 position the second serial line is hardware enabled and as far as the software, the serial line must be managed through two I/O pins of the processor. The communication parameters are software defined and so the user must refer to the software tool manual.

**MEMORY SELECTION**

On GPC® 554 can be mounted 98K and 2048 bytes of memory divided in several configurations, as described in the following table:

IC	DEVICE	SIZE	JUMPERS CONFIGURATION
6	RAM/EEPROM	8K Bytes	J3 in position 2-3; J4 not connected; J5 in position 2-3
	RAM/EEPROM	32K Bytes	J3 in position 2-3; J4 in position 2-3; J5 in position 1-2
	EPROM	8K Bytes	J3 in position 1-2; J4 in position 1-2; J5 not connected
	EPROM	32K Bytes	J3 in position 1-2; J4 in position 1-2; J5 in position 1-2
8	RAM	32K Bytes	
4	EPROM	32K Bytes	
5	EEPROM	128÷2048 Bytes	

**FIGURE 17: MEMORY SELECTION TABLE**

The sockets IC 4 and IC 6 follow the JEDEC standard, so the mounted memory devices must have JEDEC pin outs. IC 5 is a serial memory device that must be specified at the moment of the order and can be mounted only by Grifo® technicians. Remember that at the moment of the order, on IC 6 can be mounted a BACKED memory.

## SOFTWARE

A wide selection of software development tools can be obtained, allowing use of the module as a system for its own development, both in assembler and in other high level languages; in this way the User can easily develop all the requested application programs in a very short time. Generally all software packages available for the mounted microprocessor, or for the 51 family, can be used. **MCS BASIC 554**: complete development tools for MCS BASIC (interpreted BASIC language for industrial application). It needs a P.C. for console and program saving operations, while the debug, test and program operations are performed on the card. Special instructions which manage the on board peripheral devices have been added.

**BXC51**: cross compiler for source files written in MCS BASIC 554. It allows a considerable speed increment of the starting MCS BASIC program and it is completely executed on external P.C.

**XPAS51**: cross compiler for PASCAL source program, executable on P.C. with MS-DOS.

**FORTH**: complete software development tools to program the card with FORTH high level language. It needs a P.C. for User interface and it is really interesting for its fast execution and small size, of the generated code.

**MICRO/C-51**: integer cross compiler for source files in standard ANSI C. It produces a source assembly file compatible with MICRO/ASM 51 or with Intel macro relocatable assembler MCS 51.

**MICRO/ASM-51**: macro cross assembler available for MS-DOS operating system in absolute and relocatable version. In this relocatable version is supplied with a linker and a library manager.

**MICRO/SLD-51**: source level debugger and simulator. It is executed on P.C. without any additional hardware and it allows loading of HEX and SYMBOLIC files, breakpoint setting, instruction execution in trace mode, registers and memory dump, etc.

**HI-TECH C**: cross compiler for C source program. It is a powerful software tool that includes editor, C compiler, assembler, optimizer, linker, library, and remote symbolic debugger, in one easy to use integrated development environment.

**KSC**: cross compiler for C source program. It is a powerful software tool that includes editor, C compiler, assembler, optimizer, linker, library, simulator and remote symbolic debugger, in one easy to use integrated development environment for Windows.

**DDS C**: low cost cross compiler for C source program. It is a powerful software tool that includes editor, C compiler (integer), assembler, optimizer, linker, library, and remote symbolic debugger, in one easy to use integrated development environment. There are also included the library sources and many utilities.

**MDP**: monitor debugger program able to load and debug each HEX Intel files for 51 microprocessor family. It is provided of the standard commands available on in circuit emulator and requires only an external P.C. connected through a serial line.

**RSD 553**: It is a Remote Symbolic Debugger with cross assembler. It is provided of the standard commands available on in circuit emulator and requires only an external P.C. connected through a serial line. There is at high level user interface that can visualize all the processor status.

**NOICE**: It is a PC-hosted debugger consists of a target-specific DOS program, NOICExxx.EXE, and a target-resident monitor program. The two programs communicate via RS-232. NOICE includes: source level debug; a disassembler; a file viewer; memory display and editing; a virtually unlimited number of breakpoints; hardware-free single step; definition of symbols; the ability to record and play back files of commands; on-line help.

**OPEN 51/UNI**: in circuit emulator for the 51 family. It is a powerful hardware and software tool that includes: source level debugging and symbolic debugging; project management; built-in multi-file editor; execution of external compilers; debugging of several modules at the same time; built-in disassembler; source level step and trace functions; animate functions; inserting and deleting of breakpoints on the source level; watching and modifying variables on symbol and absolute level.

## HARDWARE

### INTRODUCTION

In this chapter are reported all information about card use, related to hardware features of **GPC® 554**. For example, the registers addresses, the memory allocation and peripheral devices software management are described below.

### ADDRESSES

The card devices addresses are managed from a control logic, realized with CMOS gates. This control logic allocates memory and peripheral devices with very low power consumption, in two separate manners. The 80C552 microprocessor addresses 64K bytes of code memory and 64K bytes of data memory and the control logic provides on board memory and peripheral devices allocation inside these addresses spaces. Control logic sets size, type and addresses of memory device through jumpers J3, J4, J5, J1 and J6, while it sets I/O addresses always in the upper 256 bytes of microprocessor data memory. Summarizing the control logic allocates:

- 32K bytes of EPROM on IC 4
- 32K bytes of RAM on IC 8 (without last 256 bytes used for I/O)
- Up to 32K bytes of RAM/EEPROM/EPROM on IC 6 (without last 256 bytes used for I/O)
- **Abaco® I/O BUS**
- RUN/DEBUG (J2 status)

The addresses of all these devices are described in the following paragraphs and can't be set with different value. Other devices as for example EEPROM of IC 5 is managed always by control logic but it is not allocated in memory space in fact this device is driven through CPU I/O lines with a synchronous communication.

### I/O ADDRESSES

I/O addresses are located in the last 256 bytes (192 for **Abaco® I/O BUS** and 64 bytes for RUN/DEBUG reading and future system expansions) of the 64K bytes microprocessor addressing space, to avoid conflict problems. Next table shows addresses, meanings and direction of peripheral devices registers (only the external ones to microprocessor):

DEVICES	REG.	ADDRESS	R/W	FUNCTION
<b>Abaco® I/O BUS</b>	I/O BUS	FF00H÷FFBFH	R/W	Abaco® I/O BUS addresses.
<b>RUN/DEBUG</b>	RUN/DEBUG	FFC0H÷FFFFH	R	J2 status reading register (RUN/DEBUG in BASIC).

**FIGURE 18: I/O ADDRESSES TABLE**

For further information about register meanings, please refer to next paragraph called "PERIPHERAL DEVICES SOFTWARE DESCRIPTION".



## MEMORY CONFIGURATIONS

On the GPC<sup>®</sup> 554 three different memory configurations can be selected. The configuration must be selected (with J1 and J6) both according to used software tools and User requests and/or application features. The following figures describe available memory configurations, with proper J1 and J6 setting.

### MEMORY CONFIGURATION "0"

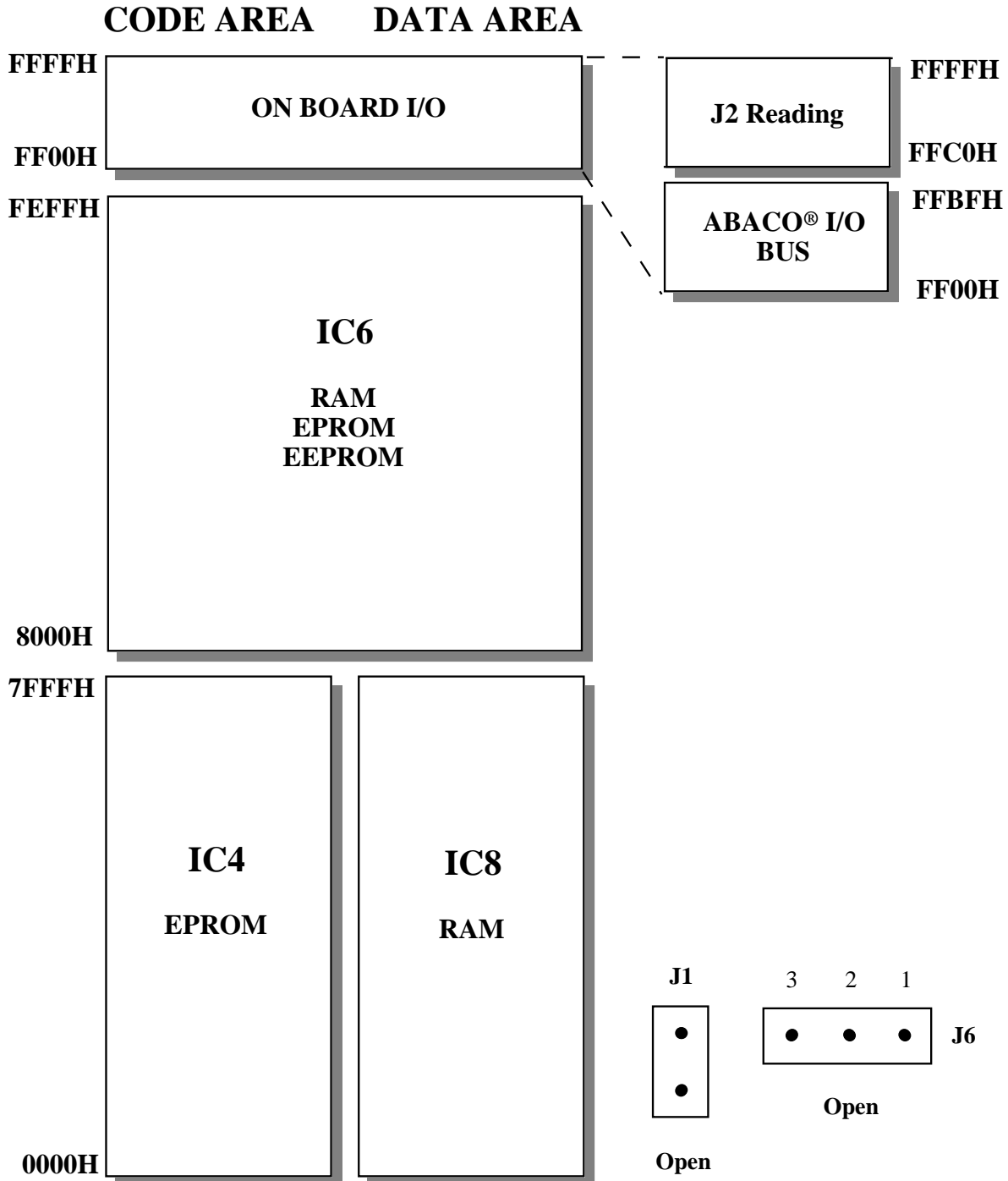


FIGURE 19: MODE 0 MEMORY CONFIGURATION (BASIC+DEBUG)

**Jumpers configuration: J1 NOT CONNECTED; J6 NOT CONNECTED**

Used by software tools as: BASIC 554; BXC51; HI TECH C; DDS C; RSD 554 (J6 in 1-2); etc.

MEMORY CONFIGURATION "1"

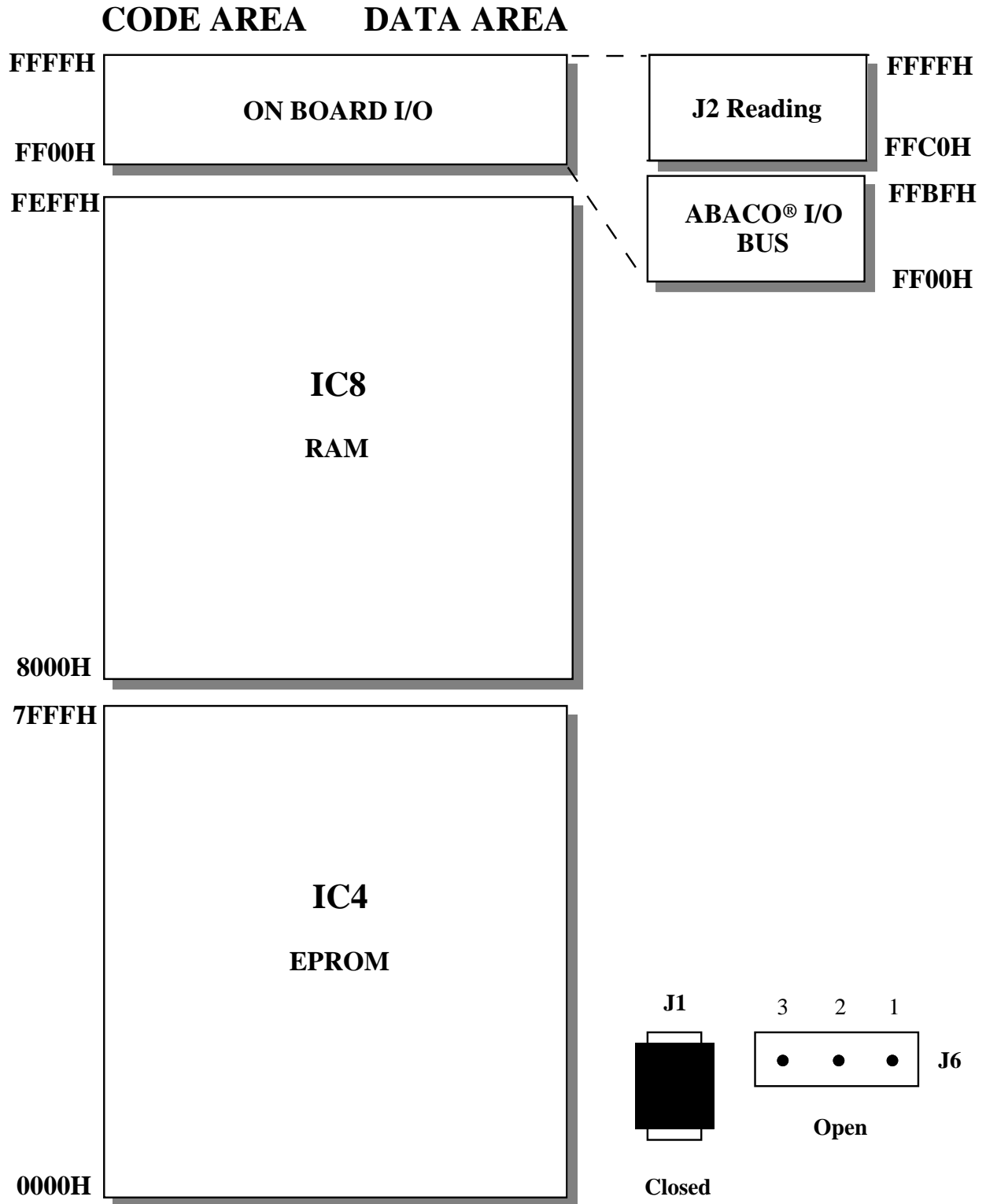


FIGURE 20: MODE 1 MEMORY CONFIGURATION (ASM)

**Jumpers configuration: J1 CONNECTED; J6 NOT CONNECTED**

Used by software tools as: HI TECH C; DDS C; etc.

## MEMORY CONFIGURATION "3"

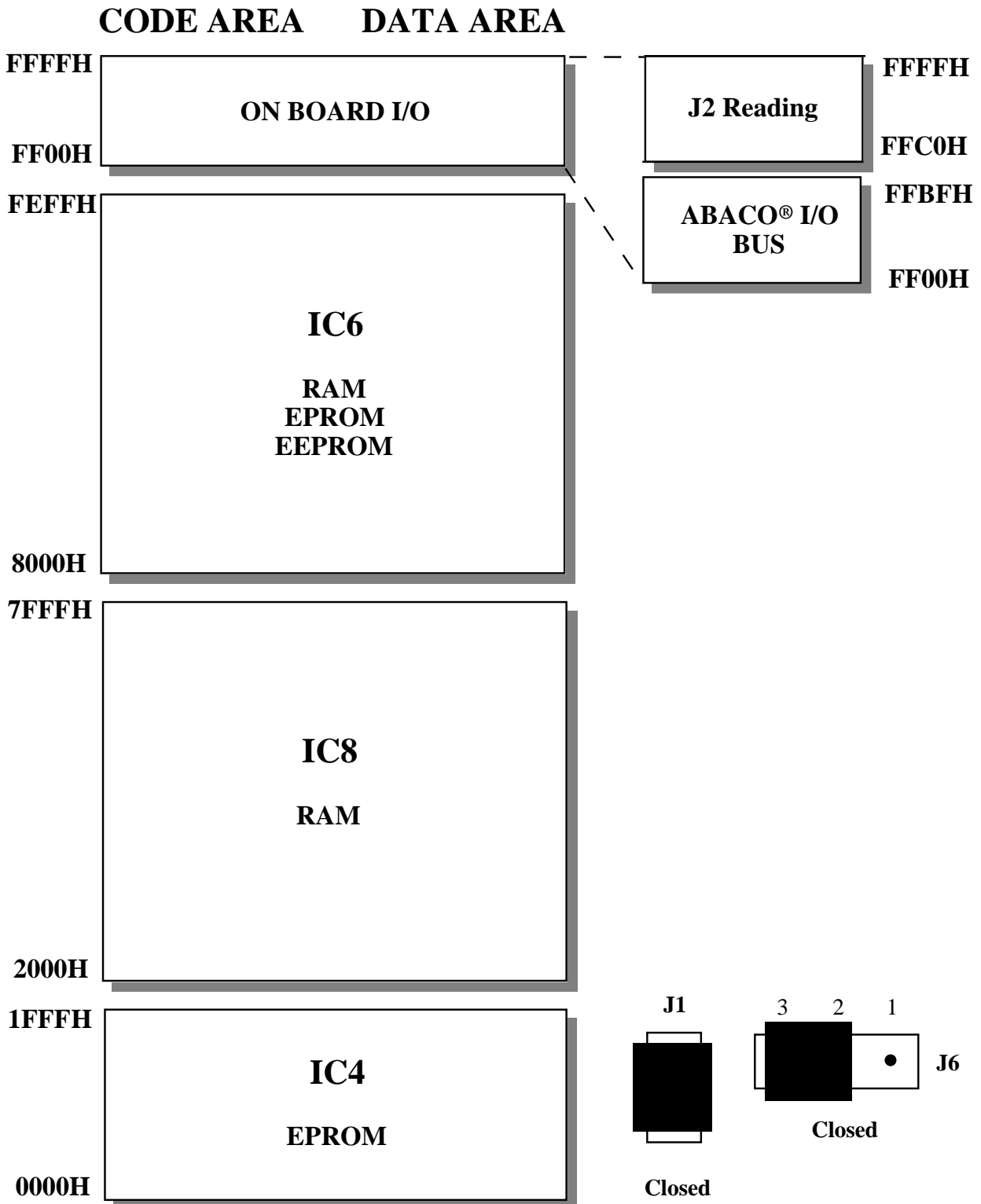


FIGURE 21: MODE 3 MEMORY CONFIGURATION (ASM)

**Jumpers configuration: J1 CONNECTED; J6 CONNECTED in 2-3 position**  
 Used by software tools as: MD/P; LUCIFER HI TECH C; DDS C; etc.

## PERIPHERAL DEVICES SOFTWARE DESCRIPTION

In the previous paragraphs are described the external registers addresses, while in this one there is a specific description of registers meaning and function (please refer to figure 18, for the registers name). For microprocessor internal peripheral devices, not described in this paragraph, or for further information, please refer to manufacturing company documentation.

### **ON BOARD INPUTS: J2 (RUN/DEBUG), J7, J8**

The on board J2 status can be obtained by software, through a simple "read operation" at the RUN/DEBUG register address. The correspondence between register bits and J2 status is as follows:

D7	->	J2 STATUS (RUN/DEBUG in BASIC)
D6÷D0	->	RESERVED

For reading the J7 and J8 status the user must read directly two pins of the CPU:

P5.6	->	J8 STATUS
P5.7	->	J7 STATUS

Remember that if the jumper is **connected** the logic status is "0" and if the jumper is **not connected** the logic status is "1".

### **SERIAL EEPROM**

For software management of serial EEPROM module of IC 5, please refer to specific documentation or to demo programs supplied with the card. The User must realize a serial communication with I<sup>2</sup>C bus standard protocol, through two I/O microprocessor pins. The only necessary information is the electric connection:

DATA line (SDA)	->	pin 27 (P3.3) of the CPU
CLOCK line (SCL)	->	pin 29 (P3.5) of the CPU
A2 address line	->	GND ("0" logic state)
A1 address line	->	GND ("0" logic state)
A0 address line	->	GND ("0" logic state)

The first 30 bytes of serial EEPROM are reserved for software tools use, so they can't be neither read nor written by User program.

### **PWM; UART; A/D CONVERTER; TIMER/COUNTER; WATCH-DOG**

For further information, please refer to specific documentation of the manufacturing company (remember to connect JS10 jumper for the watch-dog hardware enable ).

## EXTERNAL DEVICES FOR GPC® 554

**GPC® 554** can be connected to a wide range of **Grifo®** cards and to many system of other companies. Hereunder these cards are listed, for further information please call **Grifo®**.

### **OBI 01 - OBI 02**

Opto BLOCK Input NPN-PNP

Interface between 16 NPN, PNP optocoupled and displayed input lines, with screw terminal and **Abaco®** standard I/O 20 pins connector; power supply section; connection for DIN  $\Omega$  rails.

### **OBI N8 - OBI P8**

Opto BLOCK Input NPN-PNP

Interface between 8 NPN, PNP optocoupled and displayed input lines, with screw terminal and **Abaco®** standard I/O 20 pins connector; power supply section; connection for DIN  $\Omega$  rails.

### **TBO 01 - TBO 08**

Transistor BLOCK Output

Interface for **ABACO®** standard I/O 20 pins connector; 16 or 8 transistor output lines 45 Vdc 3 A open collector; screw terminal; optocoupled and displayed lines; connection for DIN 247277-1 and 3 rails.

### **RBO 01**

Relé BLOCK Output

Interface for **ABACO®** standard I/O 20 pins connector; 8 displayed 5A or 10A relays; screw terminal; connection for DIN  $\Omega$  rails.

### **RBO 08 - RBO 16**

Relé BLOCK Output

Interface for **ABACO®** standard I/O 20 pins connector; 8 or 16 displayed Relays 3A with MOV; screw terminal; connection for DIN Ctype and  $\Omega$  rails.

### **XBI 01**

miXed BLOCK Input-Output

Interface for **ABACO®** standard I/O 20 pins connector; 8 transistor output lines 45 Vdc 3A; 8 input lines; screw terminal; optocoupled and displayed I/O lines; connection for DIN 247277-1 and 3 rails.

### **XBI R4 - XBI T4**

miXed BLOCK Input-Output

Interface for **ABACO®** standard I/O 20 pins connector; 4 Relays 3A with MOV or 4 optocoupled Transistors 3A open collectors; 4 input lines optocoupled; screw terminal; connection for DIN Ctype and  $\Omega$  rails.

### **FBC - WIRE TO CARD**

Flat Block Contact

This interconnection system "wire to board" allows the connection to many type of flat cable connectors to terminal for external connections. Connection for DIN  $\Omega$  rails.

**IBC 01**

## Interface Block Comunication

Conversion card for serial communication, 2 RS 232 lines; 1 RS 422-485 line; 1 optical fibre line; selectable DTE/DCE interface; quick connection for DIN 46277-1 and 3 rails.

**DEB 01**

## Didactis Experimental Board

Supporting card for 16 TTL I/O lines use. It includes: 16 keys, 16 LEDs, 4 digits, 16 keys matrix keyboard, Centronics printer interface, LCD display and fluorescent display interface, **GPC® 68** I/O connector, field connection with screw terminal.

**MCI 64**

## Memory Cards Interfaces 64 MBytes

Interfacing card for managing 68 pins PCMCIA memory cards, it is directly driven from any **ABACO®** I/O standard connector; High level languages GDOS supported.

**KDL xxx - KDF xxx**

## Keyboard Display interface - LCD or Fluorescent

Interface with Fluorescent or LCD display, LEDs backlit, 20x2 or 20x4 characters; up to 24 keys matrix keyboard connector. It is directly driven by 16 TTL I/O lines; High level languages supported.

**QTP 24 - QTP 24P**

## Quick Terminal Panel 24 keys with Parallel interface

Intelligent user panel equipped with Fluorescent or LCD display, LEDs backlit, 20x2 or 20x4 characters; RS 232, RS 422, RS 485 or Current Loop serial line; serial E2 for set-up and message. Possibility of re-naming keys, LEDs and panel name by inserting label with new name into the proper slot; 24 Keys and 16 LEDs with blinking attribute and Buzzer manageable by software; built-in power supply; RTC option, reader of magnetic badge and relay. The QTP-24P is low cost no intelligent (passive) version. It is directly driven from 16 TTL I/O lines; High level languages supported.

**QTP 16 - QTP 16P**

## Quick Terminal Panel 16 keys with Parallel interface

Intelligent user panel equipped with Fluorescent or LCD display, LEDs backlit, 20x2 or 20x4 characters; RS 232, RS 422, RS 485 or Current Loop serial line; serial E2 for set-up and messages; Buzzer manageable by software; 4 readable auxiliary opto-in lines; power supply 5 Vdc. The QTP-16P is low cost no intelligent (passive) version. It is directly driven from 16 TTL I/O lines.

**QTP G26**

## Quick Terminal Panel - LCD Graphic, 26 keys

Intelligent user panel equipped with graphic LCD display 240x128 pixel, CFC backlit; Optocoupled RS 232 line and additional RS 232, RS 422, RS 485 or Current Loop serial line. Independent optional CAN line controller; serial E2 for set-up; RTC and RAM Lithium backed; primary graphic objects; Possibility of re-naming keys, LEDs and panel name by inserting label with new name into the proper slot; 26 Keys and 16 LEDs with blinking attribute and Buzzer manageable by software; built-in power supply; Reader of magnetic badge, smart-card and relay option.

### ZBR xxx

Zipped BLOCK Relays xx Input + xx Output

Peripheral cards family, Relays outputs, equipped with housing for  $\Omega$  rails mounting. Double power supply built-in; 5Vdc section for powering the on-board logic and an external CPU cards; second section, galvanically coupled, for the optocoupled input lines. All I/O lines are displayed by LEDs. Relays contacts are 3A and are MOV protected. All I/O connections are available on quick terminal connectors. 1 connector interface to **ABACO**<sup>®</sup> I/O BUS. The ZBR serie represent the ideal complement for cards 3 and 4 type. The ZBR cards can be directly driven, through the PC parallel port, by using the PCC-A26 low cost interface card. ZBR 324 -> 32 Opto-In, 24 Relays; ZBR 246 -> 24 Opto-In, 16 Relays; ZBR 168 -> 16 Opto-In, 8 Relays; ZBR 84 -> 8 Opto-In, 4 Relays.

### ZBT xxx

Zipped BLOCK Transistors xx Input + xx Output

Peripheral cards family having optocoupled outputs and 3A Transistor in Open collector. Cards are equipped with housing for  $\Omega$  rails mounting. Double power supply built-in; 5Vdc section for powering the on-board logic and an external CPU cards; second section, galvanically coupled, for the optocoupled input lines. All I/O lines are displayed by LEDs. All output transistors are equipped with protection against inductive loads. All I/O connections are available on easy quick terminal connectors. Connector interface to **ABACO**<sup>®</sup> I/O BUS. The ZBT serie represent the ideal complement for cards 3 and 4 type. The ZBT cards can be directly driven, through the PC parallel port, by using the PCC-A26 low cost interface card. ZBT 324 -> 32 Opto-In, 24 Transistors; ZBT 246 -> 24 Opto-In, 16 Transistors; ZBT 168 -> 16 Opto-In, 8 Transistors; ZBT 84 -> 8 Opto-In, 4 Transistors.

### ABB 03

**ABACO**<sup>®</sup> Block BUS 3 slots

3 slots **ABACO**<sup>®</sup> mother board; 4 TE pitch connectors; **ABACO**<sup>®</sup> I/O BUS connector; screw terminal for power supply; connection for DIN C type and  $\Omega$  rails.

### ABB 05

**ABACO**<sup>®</sup> Block BUS 5 slots

5 slots **ABACO**<sup>®</sup> mother board with Power Supply. Double power supply built-in; 5Vdc 2,5A section for powering the on-board logic; second section at 24Vdc 400mA galvanically coupled, for the optocoupled input lines. Auxiliary connector for **ABACO**<sup>®</sup> I/O BUS. Connection for DIN  $\Omega$  rails.

### IPC 52

Intelligent Peripheral Controller, 24 analogic input

This intelligent peripheral card acquires 24 independent analogic input lines: 8 PT-100 or PT-1000 sensors, 8 J,K,S,T termocouples, 8 analog input  $\pm 2$ Vdc or  $4 \div 20$ mA; 16 bits + sign A/D section; 0.1 °C resolution; 32K RAM for local data-logging; Buzzer; 16 TTL I/O lines; 5 or 8 conversion per second; Facility of networking up 127 IPC 52 cards using serial line. BUS interfacing or through RS 232, RS 422, RS 485 o Current Loop line. Only 5Vdc power supply.

### UAR 24

Universal Analog Regulator, 2 D/A, 4 Relays

This intelligent peripheral card for temperature PID controls, acquires 2 PT-100 sensors and 2 J,K,S,T termocouples; 16 bits + sign A/D section; 0.1 °C resolution; 32K RAM for local data-logging; 4 conversion per second; Buzzer; 4 3A relays; 2 12 bits D/A lines,  $0 \div 10$ Vdc; Facility of networking up 127 IPC 52 cards using serial line. BUS interfacing or through RS 232, RS 422, RS 485 o Current Loop line. Only 5Vdc power supply.

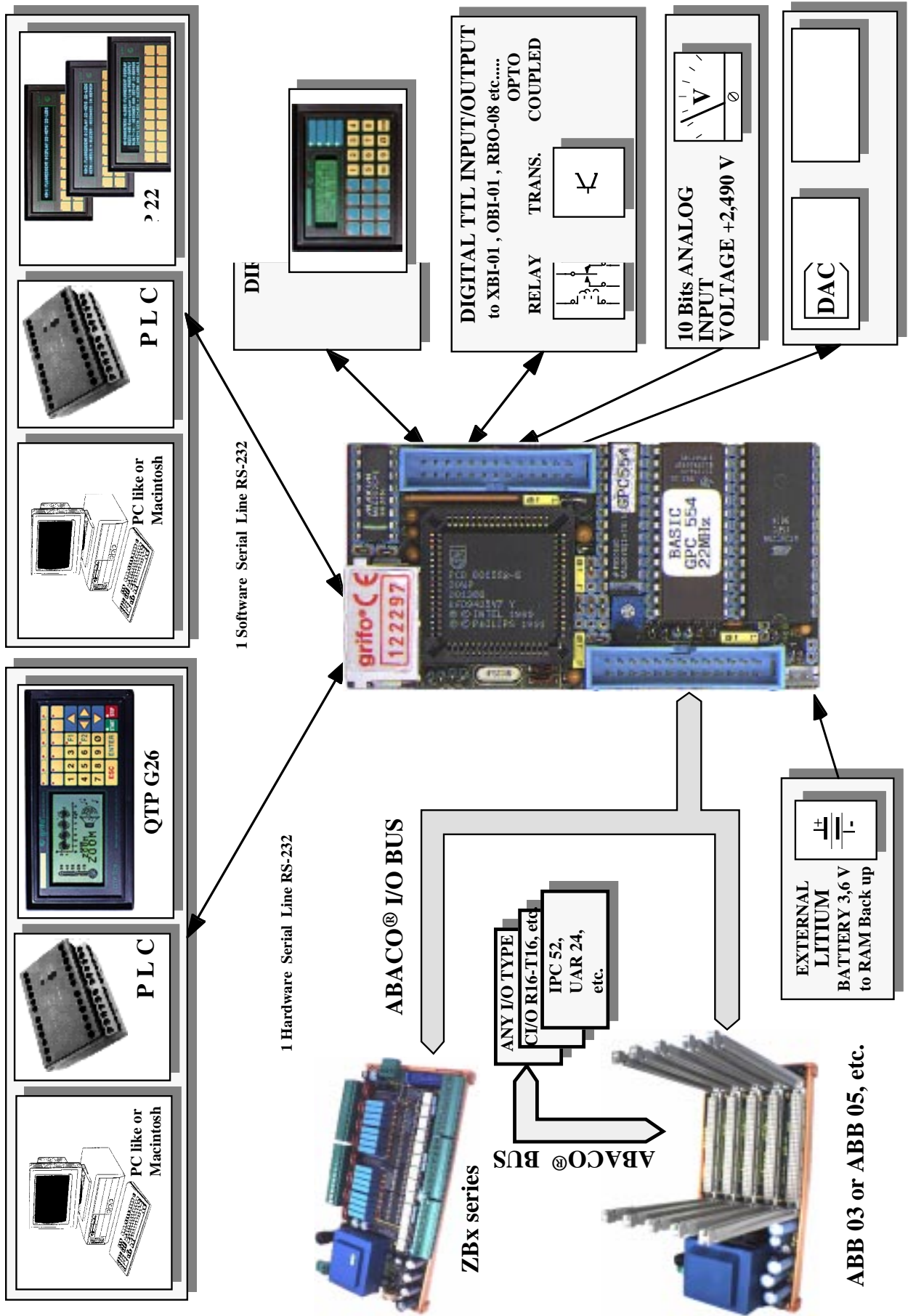


FIGURE 22: GPC<sup>®</sup> 554 AVAILABLE CONNECTIONS DIAGRAM



## BIBLIOGRAPHY

In this chapter there is a complete list of technical books, where the User can find all the necessary documentations on the components mounted on **GPC® 554**.

Data book Manuale TEXAS INSTRUMENTS:	<i>The TTL Data Book - SN54/74 Families</i>
Data book Manuale TEXAS INSTRUMENTS:	<i>Linear Circuits Data Book - Volumi 1 e 3</i>
Data book NEC:	<i>Memory Products</i>
Data book MAXIM:	<i>New Releases Data Book - Volume 4</i>
Data book MAXIM:	<i>Integrated Circuits Data Book</i>
Data book XICOR:	<i>Data Book</i>
Data book PHILIPS:	<i>80C51 - Based 8-Bit Microcontrollers</i>
Data book TOSHIBA:	<i>Mos Memory Products</i>

For further information and upgrades please refer to specific "INTERNET WEB PAGES" of the manufacturing companies.

APPENDIX A: JUMPERS LOCATION

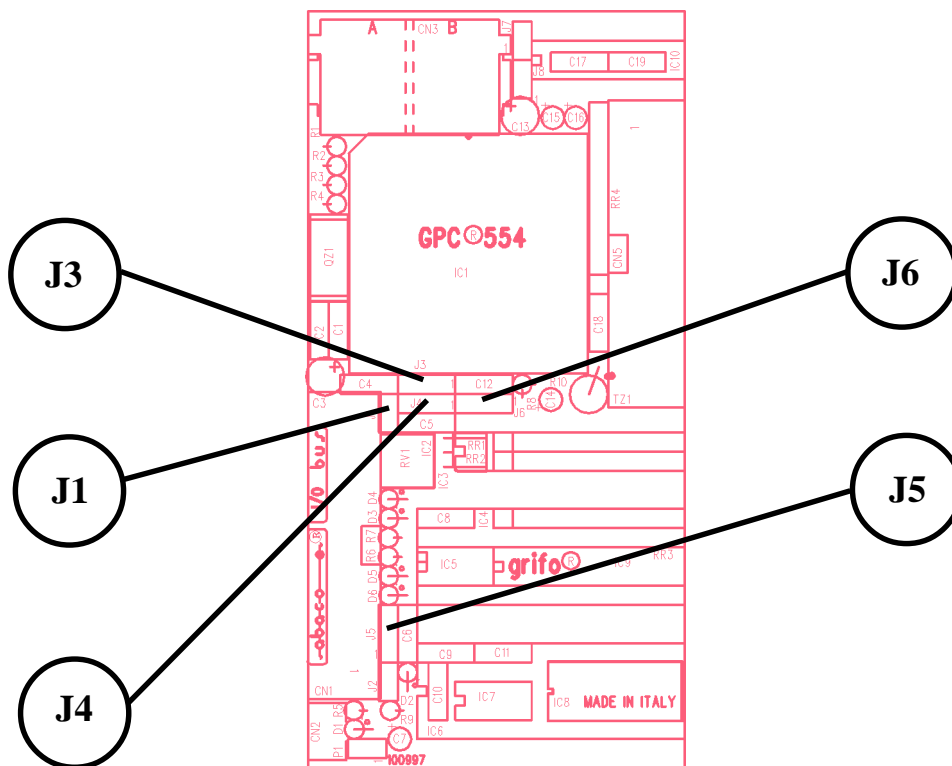


FIGURE 23: MEMORY JUMPERS LOCATION

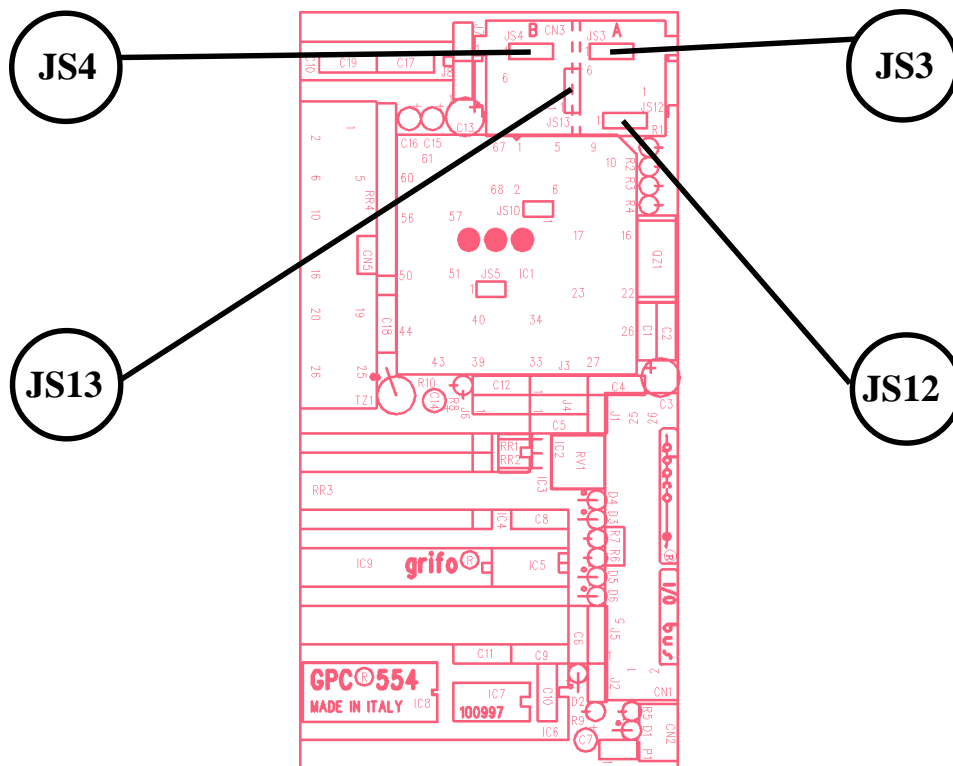


FIGURE 24: SERIAL COMMUNICATION JUMPERS LOCATION



APPENDIX B: MODULE DIMENSION FOR PIGGY-BACK MOUNTING

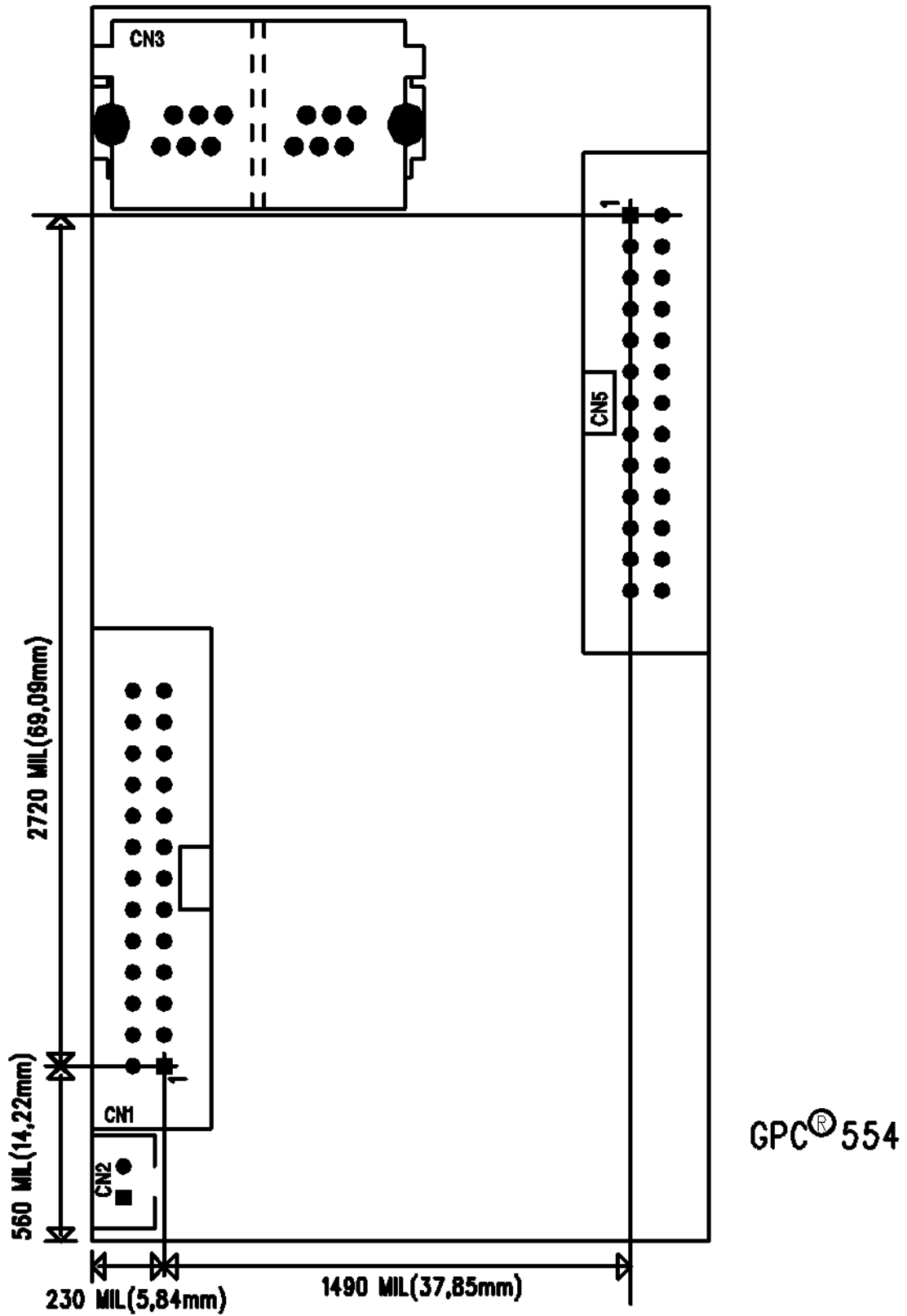


FIGURE 25: MODULE DIMENSION FOR PIGGY-BACK MOUNTING



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