

GPC[®] 550

General Purpose Controller 80C552

TECHNICAL MANUAL



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GPC[®] 550

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Single **Euro** size 100x160mm with interface to **Abaco[®] industrial BUS**; microcontroller **Philips 80C552**, at **22M Hz** or compatible ones; different memory devices: **32K EPROM**; **32K SRAM**; **32K EPROM, FLASH, EEPROM** or **SRAM**; up to **1K** serial **EEPROM**; **256 bytes** serial **SRAM**; **Real Time Clock** able to up date day, month, year, week day, seconds, minutes and hours. It can be programmed to generate an **INT** at periodic intervals defined by software; **back up** circuit for **SRAM** and **RTC** provided of **lithium battery** and connector for external battery; 8 lines **10 bits A/D** converter, with range **+2.49V, 0÷20** or **4÷20 mA**, conversion time **27µs**, provided of pass band filters; **1** status **LED** plus **3** activity **LEDs** and **BUZZER** for signals, driven through software; 8 way **dip switch**: 7 dips are readable by software and it can be used as **RUN/DEBUG** mode selector; **1** hardware serial lines configurable in **RS 232, RS 422, RS 485**, passive **Current Loop** with programmable baud rate up to **115K Baud**. and one software serial line in **RS 232**; **40 I/O TTL** lines, driven by software: 24 managed by **PPI 82C55** and 16 managed by **CPU** ports (some of these lines have double functions); **2** independent **PWM** outputs with 8 bits resolution; **three** 16 bits **timer counter**. One has capture and compare functionalities, joined with inputs and outputs signals available on connectors; two **I2C BUS** lines, one hardware and one software, available on connectors; optional **CAN** line based on **PHILIPS SJA 1000** controller that supports **Basic CAN, CAN 2.0B** and **PeliCan** protocols, with a maximum **1 MBit/sec** bit rate; **PHILIPS 82C250** **CAN** line driver, galvanically optocoupled; **9** standard **connectors**, placed on the front side of the card, to facilitate the connection with the other systems and with the field; single power supply **+5Vdc, 330 mA** maximum consumption; possibility to reduce power consumption with **idle** or **power down** mode; wide range of base software and **development tools** that allow card use with only a standard PC, connected through serial line. Among these: **GET 51; Monitor Debugger** (FMO 52, MD/P, NOICE 51); **Assembler** (ASM51, A51, SXA51); **BASIC** compilers (BASCOM 8051, BXC51); **FORTH**; **C** compilers (HI TECH C 51, DDS MICRO C 51, µC 51, SYS51CW); **PLM 51; PASCAL** compilers (SYS51PW); etc.

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For specific informations on the components mounted on the card, please refer to the Data Book of the builder or second sources.

SYMBOLS DESCRIPTION

In the manual could appear the following symbols:

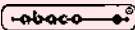


Attention: Generic danger



Attention: High voltage

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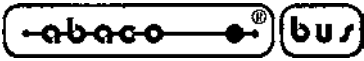
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INTRODUCTION

The use of these devices has turned - IN EXCLUSIVE WAY - to specialized personnel.

The purpose of this handbook is to give the necessary information to the cognizant and sure use of the products. They are the result of a continual and systematic elaboration of data and technical tests saved and validated from the manufacturer, related to the inside modes of certainty and quality of the information.

The reported data are destined- IN EXCLUSIVE WAY- to specialized users, that can interact with the devices in safety conditions for the persons, for the machine and for the environment, impersonating an elementary diagnostic of breakdowns and of malfunction conditions by performing simple functional verify operations , in the height respect of the actual safety and health norms.

The informations for the installation, the assemblage, the dismantlement, the handling, the adjustment, the reparation and the contingent accessories, devices etc. installation are destined - and then executable - always and in exclusive way from specialized warned and educated personnel, or directly from the TECHNICAL AUTHORIZED ASSISTANCE, in the height respect of the manufacturer recommendations and the actual safety and health norms.

The devices can't be used outside a box. The user must always insert the cards in a container that respect the actual safety normative. The protection of this container is not threshold to the only atmospheric agents, but specially to mechanic, electric, magnetic, etc. ones.

To be on good terms with the products, is necessary guarantee legibility and conservation of the manual, also for future references. In case of deterioration or more easily for technical updates, consult the AUTHORIZED TECHNICAL ASSISTANCE directly.

To prevent problems during card utilization, it is a good practice to read carefully all the informations of this manual. After this reading, the user can use the general index and the alphabetical index, respectly at the begining and at the end of the manual, to find information in a faster and more easy way.

CARD VERSION

The present handbook is reported to the GPC® 550 card release **200702** and later. The validity of the bring informations is subordinate to the number of the card release. The user must always verify the correct correspondence among the two denotations. On the card the release number is present in more points both board printed diagram (serigraph) and printed circuit (for example near ABACO® connector on the component side and near battery BT1 on the solder side).

GENERAL INFORMATION

The **GPC® 550** card is a powerful control and managing card in the 100x160mm standard single Europa size. It can operate in stand alone mode as an intelligent peripheral or remoted in a wider telecontrol and acquisition network but it can be easily expanded by the numerous intelligent and non intelligent peripherals, available on **Industrial Abaco® BUS**.

His typical installation is on a mother board mounted inside a rack or on a mother board for **Omega** rails (i.e. **ABB 05** and **ABB 03**) that furthermore allow the management of cards with **BLOCK** format, with **Abaco® I/O BUS**.

The card supports some different versions of microcontrollers as **80C552**, **87C552**, etc. all of them code compatible with the wide diffused **8051 INTEL** and it includes considerable hardware resources. The most interesting ones are the 8 lines of 10 bits **A/D converter**, the numerous TTL digital I/O lines, the **CAN** interface and the **I2C BUS** lines.

Its modularity and the remarkable hardware resources allow **GPC® 550** to be easily used even in complex applications.

The card use is simplified by a wide range of software development tools based either on low or high level languages which allow to work at the best conditions using only a standard PC.

Noteworthy among these tools there are the **C compilers**, the **FORTH** and the handy basic compiler **BASCOM 8051**.

Special care has been devoted to the application developing, by generating programs which allow **remote debug** directly on the card and on board **FLASH** burning with user application program. The **GPC®550** is equipped with a series of normalized, standard **Abaco®** connectors allowing immediate use of all the available **BLOCK I/O** modules, a direct management of local operator interfaces (**KDx x24**, **QTP xxP**) or connections to equipment made by the user, or by third parties companies, obtaining a notable cost reduction.

- Single **Euro** size 100x160mm with interface to **Abaco® industrial BUS**.
- Microcontroller **Philips 80C552**, at **22M Hz** or compatible ones.
- Different memory devices: **32K EPROM**; **32K SRAM**; **32K EPROM**, **FLASH**, **EEPROM** or **SRAM**; up to **1K** serial **EEPROM**; **256 bytes** serial **SRAM**.
- **Real Time Clock** able to up date day, month, year, week day, seconds, minutes and hours. It can be programmed to generate an **INT** at periodic intervals defined by software.
- **Back up** circuit for **SRAM** and **RTC** provided of **lithium battery** and connector for external battery.
- 8 lines **10 bits A/D** converter, with range **+2,49V**, **0÷20** or **4÷20 mA**, conversion time **27µs**, provided of pass band filters.
- **1** status **LED** plus **3** activity **LEDs** and **BUZZER** for signals, driven through software.
- 8 way **dip switch**: 7 dips are readable by software and it can be used as **RUN/DEBUG** mode selector.
- **1** hardware serial lines configurable in **RS 232**, **RS 422**, **RS 485**, passive **Current Loop** with programmable baud rate up to **115K Baud**. and one software serial line in **RS 232**.
- **40 I/O TTL** lines, driven by software: 24 managed by **PPI 82C55** and 16 managed by **CPU** ports (some of these lines have double functions).
- **2** independent **PWM** outputs with 8 bits resolution.
- **Three** 16 bits **timer counter**. One has capture and compare functionalities, joined with inputs and outputs signals available on connectors.
- Two **I2C BUS** lines, one hardware and one software, available on connectors.
- Optional **CAN** line based on **PHILIPS SJA 1000** controller that supports **Basic CAN**, **CAN 2.0B** and **PeliCan** protocols, with a maximum **1 MBit/sec** bit rate.
- **PHILIPS 82C250** **CAN** line driver, galvanically optocoupled.
- **9** standard **connectors**, placed on the front side of the card, to facilitate the connection with the other systems and with the field.
- Single power supply **+5Vdc**, **330 mA** maximum consumption.
- Possibility to reduce power consumption with **idle** or **power down** mode.

- Wide range of base software and **development tools** that allow card use with only a standard PC, connected through serial line. Among these: **GET 51**; **Monitor Debugger** (FMO 52, MD/P, NO ICE 51); **Assembler** (ASM51, A51, SXA51); **BASIC** compilers (BASCOM 8051, BXC51); **FORTH**; **C** compilers (HI TECH C 51, DDS MICRO C 51, μ C 51, SYS51CW); **PLM 51**; **PASCAL** compilers (SYS51PW); etc.

Here follows a description of the board's sections and the operations they perform. To easily locate such section on verify their connections please refer to figure 1.

MEMORY DEVICES

On the card can be mounted 97K and 256 bytes of memory divided with a maximum of 32K EPROM, 32K SRAM/EEPROM, 32K EEPROM/SRAM/FLASH EPROM/EPROM, 256 bytes of serial SRAM+RTC and up to 1K of serial EEPROM.

The **GPC® 550** memory configuration must be chosen considering the application to realize or the specific requirements of the user.

Normally the card is equipped with 32K byte of SRAM, 512 bytes of serial EEPROM and 256 bytes of serial SRAM+RTC, all different configuration must be specified by the user, at the moment of the order.

By the on board Lithium battery, there is the possibility to keep data in the 32K byte SRAM on U2 and 256 bytes serial SRAM on U14 also when power supply is failed; in this way the card is always able to maintain parameters, logged data, system status and configuration, etc. without using an expensive external UPS.

Should the amount of backed memory be insufficient, it is always possible to use backed-RAM modules or order an EEPROM.

In addition to that, the U14 module is provided with a Real Time Clock which manages time (hours, minutes, seconds) and date (day, month, year, day of the week).

The addressing of memory devices is controlled by a specific on board circuit, that provides to allocate the devices in the microprocessor address space.

For further information about memory configuration, sockets description and jumpers connection, please refer to chapter "HARDWARE DESCRIPTION", "PERIPHERAL SOFTWARE DESCRIPTION" and to the paragraph "MEMORY SELECTION".

CPU

The **GPC® 550** can use the microprocessor **PHILIPS 80C552** and all the pin out compatible similar microprocessor. This 8 bit microprocessor is code compatible with the 8051 INTEL and so it has an extended instruction set, fast execution time, easy use of all kind of memory and an efficient interrupt management. The most important features of the described 80C552 microprocessor, are:

- 8k bytes EPROM, 256 bytes RAM;
- 5 independent 8 bits I/O ports (PORT);
- 2 standard 16 bits Timer/Counters (TMR CNT);
- One 16 bits Timer/Counter with Capture and Compare function (TMR CNT);
- 2 priority level for interrupts (ICU);
- 15 internal interrupt sources (ICU);
- 8 lines 10 bits A/D converter (ADC);
- 2 independent 8 bits PWM outputs (PWM);
- 1 synchronus/asynchronous serial line (UART);
- 1 I²C bus line (HW I2C);
- Watch Dog Timer;
- Idle mode or Power down mode;

For further information, please refer to specific documentation of the manufacturing company.

CONTROL LOGIC

The addresses of all peripheral device's registers and of memory devices on **GPC® 550** are assigned from a specific control logic that allocates all these devices in the microprocessor addressing space. For further information please refer to paragraph "I/O ADDRESSES" of this manual.

BUS ABACO®

One of the most important features of **GPC® 550** is its possibility to be interfaced to industrial BUS **ABACO®**. Thanks to its standard BUS **ABACO®** connector, the card can be connected to some of the numerous **grifo®** boards, both intelligent and not. For example the User can directly use cards for analog signals acquisition (A/D), cards for analog signals generation (D/A), cards for digital I/O signals management, cards with timers and counters, cards for temperature controls, etc. Through mother boards like **ABB 03** and **ABB 05** it is also possible to manage serie 3 and 4 boards, which are provided with **ABACO® I/O BUS**. So, **GPC® 550** becomes the right component for each industrial automation systems, in fact BUS **ABACO®** makes the card easily expandable with the best price/performance ratio.

Please remark that all BUS **ABACO®** signals are buffered to warrant a greater immunity against noise and the possibility to drive a higher number of peripheral cards without fan-out problems. Chapter "EXTERNAL CARDS" shows a short description of **grifo®** peripheral cards for BUS **ABACO®** and **ABACO® I/O BUS**.

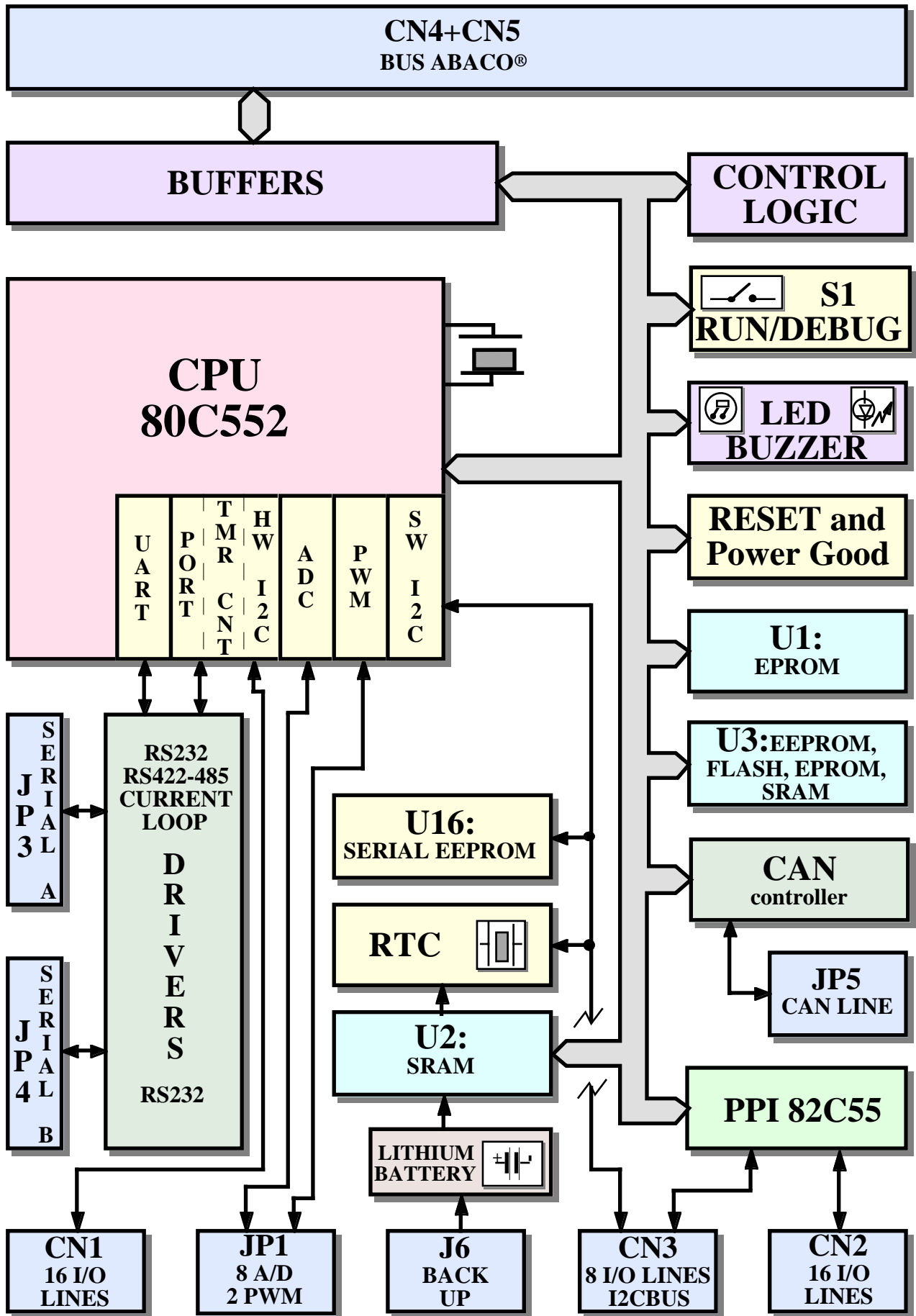


FIGURE 1: BLOCK DIAGRAM

CLOCK DEVICE

On **GPC® 550** there are three separate circuits with crystal to generate the clock signals:

- The first is based on a quartz that generates the clock frequency for the CPU and used also as a base to generate the frequency for microprocessor internal peripherals (like Timer, UART, PWM, etc.) and on-board peripherals (like BUS, etc.). Standard value of this quartz is **22.1184 MHz**, the power management registers of microcontroller can be set by software to change clock and so consumption of the several peripherals. For particolare needs, a specific clock configuration can be agreed directly with **grifo®**.
- The second is based on a quartz that generates the clock frequency for the CAN on-board circuitry. Standard value of this quartz is **24 MHz**. This circuitry is optional and is installed only when the option **.CAN** is requested. Its value is the result of a careful desing and long experimantation.
- The third circuitry generates the correct timing for the on-board Real Time Clock. Its value is **32.768 kHz**.

The choice of using three circuits and threeseparated crystals, has the advantage to change the microprocessor working speed (when best performances are required) without additional changes in software, firmware, etc.

BOARD CONFIGURATION

To make the board and the application program configurable, an 8 pins dip switch has been installed. The software can acquire 7 of the 8 switches without having to access the I/O signals and manage different conditions with an unique program (like different languages, program parameter, operating modalities, etc.).

Some software packages developed for **GPC® 550** use these switches to select the RUN or DEBUG operating condition, as described in their manuals.

In addition, the board is also provided with three signalation LEDs and one buzzer, all software manageable, that can be used to signal in visual and acoustic ways the board status and configuration, as described in the specific paragraphs.

All the configuration resources described are completely software manageable simply programming specific registers allocated in the I/O space by the control logic.

A/D CONVERTER

It is a CPU internal peripheral device that converts 8 different analog signals with 10 bits of resolution. By software the User selects the channel to convert, starts the conversion and controls the end of conversion, through programming of microprocessor internal registers; conversion time is 27 µsec; sample rate is 20 Ksps each channel; easy software management; end of conversion interrupt. The analog inputs can be voltage inputs (0÷2.49V) or current inputs (0÷20 mA or 4÷20 mA) through a specific current-to-voltage converter. Default is voltage input with 2.49V full range.

DIGITAL I/O LINES

The card is provided with two digital I/O controllers used to drive some on-board resources (serial EEPROM, serial SRAM+RTC, software serial line, etc.) and 40 digital TTL I/O lines available to the user:

- 16 lines have user settable directionality each line, connected to CPU PORT section;
- 24 lines have user settable directionality per groups of 8, connected to PPI 82C55.

These lines are connected directly to two 20 pins connectors with standard I/O ABACO® pin out connectors, allowing to be connected directly to several interface cards.

It is possible to define by software the function of these lines, and also to match them to peripherals (like Timer Counter, Interrupt, I²C BUS, etc.), simply programming some CPU internal registers. Please remark that can be available 8 more TTL lines input only alternatively to digital inputs and 2 more TTL lines output only alternatively to PWM outputs; if the application requires more than 40 I/O signals but not A/D nor PWM, the above mentioned are available through a proper software management.

For further information please refer to paragraph "CONNECTIONS", "DIGITAL I/O INTERFACES", "CPU I/O LINES" and "PERIPHERAL DEVICES SOFTWARE DESCRIPTION".

SERIAL COMMUNICATION

GPC® 550 features several interfaces for serial communication: for example I²C BUS lines, a CAN line and two asynchronous lines. The first two lines are described in the following paragraphs, while the remaining are completely software settable by the programmer.

By convention, asynchronous lines are called **A** (hardware serial line managed by CPU internal UART whose baud rate can be set up to 115200 and bits per character can be 8 or 9 programming opportune registers) and **B** (software serial line made by two I/O signals whose baud rate, number of stop bits and parity are defined by the management software).

It is also possible, using some software trick, to set parity and stop bit number for serial line A, this allows to communicate to most of existing devices.

By hardware it is possible to select the electric protocol, through a comfortable set of jumpers and drivers to install. In detail line B is always buffered in **RS 232**, while line A can be buffered in **current loop, RS 232, RS 422 or RS 485**; in these last two cases also abilitation and direction of line can be defined.

If an RS 232 with two handshakes is needed, it is possible to use two communication lines of serial B that will act as RTS, CTS, DTR, RI, etc. by software management.

Please remark that by default the board is provided with both serial lines in RS 232, so any different configuration must be specified in the order.

For further information about serial communication please refer to paragraph: "CONNECTIONS", "SERIAL COMMUNICATION SELECTION" and "SOFTWARE SERIAL B".

CAN INTERFACE

This section is based on the powerful controller PHILIPS **SJA 1000** and is charged to manage all aspects and modalities of CAN protocol.

Overall features are:

- support for protocol BasicCAN;
- support for protocol PeliCAN 2.0B;
- support for 11 and 29 bits identifiers;
- transmission buffer 13 bytes;
- reception buffer 64 bytes;
- baud rate programmable up to 1M Bit/sec;
- no reception comparator;
- programmable message acceptance filters;
- programmable output driver;
- work frequency 24 MHz.

Electrically, the board is provided with line driver PHILIPS **82C250**, galvanically isolated.

This component is compliant to CAN protocol and manages the connection to the field in autonomy without need for software intervention.

On board CAN line is galvanically isolated from other circuitry of the card to warrant immunity against noise from the field; this feature is essential for connections to remote systems supplied from different sources or in case connection cables must run across noisy environments.

A specific DC/DC converter generates the galvanically isolated voltages required from the line driver while the interface to CAN controller lines are performed through high frequency optocouplers. CAN lines connection to the field is made through a 3 pins quick release screw terminal connector and warrants a good signal transmission.

Please remark that CAN section is **optional**, it is installed **only if specified** in the order by the code **.CAN**.

By software, CAN controller is completely configurable programming 64 registers that control logic allocates in I/O space and is capable to generate interrupts when several conditions occur.

For more information the user can refer to specific documentation of manufacturer.

I2C BUS LINES

GPC® 550 is provided with two synchronous I²C BUS serial lines that allow to be connected to the several devices that feature the same kind of serial line.

One line is hardware, that is controlled by an UART internal to the microcontroller:

- bidirectional data transfer between master and slave units;
- multimaster mode;
- line arbitration in case of collision with no data loss;
- synchronization amongst devices at different speeds;
- programmable bit rate up to 1.8M Bit/sec;
- high level management of master transmission, transmission as slave;
- high level management of master reception, reception as slave;
- interrupt generation when several conditions occur.

Second serial line is managed by software and is made using two CPU I/O TTL lines, as described in chapter “PERIPHERAL DEVICES SOFTWARE DESCRIPTION”. It is already connected to I²C BUS on board devices: serial EEPROM and serial SRAM+RTC.

Both I²C lines are available on comfortable low profile connectors, where also power supply is present, to allow a quick connection to other units of the system.

By software, the I²C BUS lines are completely configurable simply programming some CPU internal registers.

PWM LINES

Two independent PWM lines are available. They allow to generate signals with frequency and duty cycle software defineable by the user and resolution 8 bits.

Typical applications of these signals are motor speed control (in fact several motor drivers feature compatible inputs) or analog signals generation (easy to obtain, just add an integrator circuit).

Both lines are available on a low profile connector easy to connect and are managed through three CPU internal registers.

For further information the user can refer to specific documentation of manufacturer.

TECHNICAL FEATURES

GENERAL FEATURES

| | |
|--------------------------------------|--|
| On board resources: | 16 input/output digital TTL 24 input/output digital TTL 3 timer counter resolution 16 bit 1 RS 232 serial line (B) 1 RS 232, RS 422, RS 485 or current loop serial line (A) 2 I ² C BUS lines 1 CAN line 8 A/D converter lines 2 PWM lines 3 software manageable LEDs 1 real time clock 1 buzzer 1 dip switch featuring 8 pins 1 reset and power good circuitry 1 back up circuitry 1 interface BUS ABACO® |
| Addressable memory: | U1: EPROM 32K x 8 U2: SRAM 32K x 8 U3: FLASH, EEPROM, SRAM, EPROM 32K x 8 U14: serial SRAM 256 byte U16: serial EEPROM from 256 byte to 1K byte |
| Access time of memories: | 120 nsec |
| On board CPU: | PHILIPS P80C552 |
| CPU clock frequency: | 22.1184 MHz |
| Highest counters frequency: | CPU clock frequency / 12 |
| CAN clock frequency: | 24 MHz |
| CAN highest bitrate: | 1 Mbit |
| A/D inputs cut-off frequency: | 1 MHz |
| A/D resolution: | 10 bit |
| A/D conversion time: | 27 µsec |
| A/D total error: | ±1 point |
| RTC frequency: | 32.768 KHz |
| Reset time: | 200 msec |

PHYSICAL FEATURES

| | |
|--------------------------|---|
| Size (W x H x D): | EUROCARD format 100 x 160 x 20 100 x 172 x 20 outline |
| Weight: | 150 g (basic version) |
| Connectors: | CN1: 20 pins low profile vertical male CN2: 20 pins low profile vertical male CN3: 20 pins low profile vertical male CN4+CN5: 64 pins DIN 41612 type C 90 degrees male |

JP1: 20 pins low profile vertical male
 JP3: Plug 6 pins 90 degrees female
 JP4: Plug 6 pins 90 degrees female
 JP5: 3pins quick release screw terminal connector
 J6: 2 pins low profile vertical male

Temperature range:

from 0 to 70 centigrad degrees

Relative humidty:

20% up to 90% (without condense)

ELECTRIC FEATURES

Power supply: 5 Vdc $\pm 5\%$

Current consumption on +5 Vdc: 150 mA * (basic configuration)
 100 mA * (power down)
 330 mA * (highest)

On board back up battery: 3.0 Vdc; 1/2 AA

External back up battery: 3.6 \div 5 Vdc

Back up current: 2.7 μ A (on board battery)
 3.4 μ A (external battery 3.6 Vdc)

Analog inputs: 0 \div 2.490 V

Current analog inputs: 0 \div 20; 4 \div 20 mA (with conversion module)

Analog inputs impedance: High (not declared by manufacturer)

Termination network RS 422-485: Line termination resistor =120 Ω
 Positive pull up resistor =3.3 K Ω
 Negative pull down resistor =3.3 K Ω

CAN line impedance: 60 Ω

CAN termination network: 120 Ω resistor, disconnectable

Power good intervent threshold: 4.62 V

* The data are referred to 20 C° work temperature (for further information please refer to chapter "POWER SUPPLY VOLTAGE").

INSTALLATION

In this chapter there are the information for a right installation and correct use of the card. The user can find the location and functions of each connectors, LEDs, jumpers, trimmers, etc. and some explanatory diagrams.

CONNECTIONS

The GPC[®]550 module has 9 connectors that can be linkeded to other devices or directly to the field, according to system requirements. In this paragraph there are connectors pin out, a short signals description (including the signals direction) and connectors location (see figure 25).

J6 - BACK UP EXTERNAL BATTERY CONNECTOR

J6 is a 2 pins, male, vertical connector with 2.54mm pitch.

Through J6 the user must connect an external battery for SRAM and real time clock back up when the power supply is switched off (for further information please refer to chapter "BACK UP").

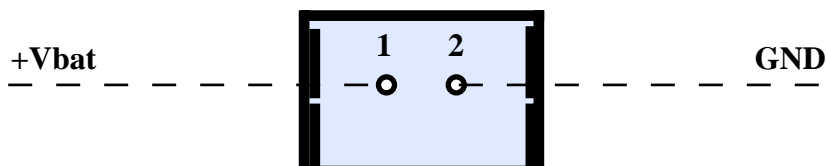


FIGURE 2: J6 - BACK UP EXTERNAL BATTERY CONNECTOR

Signals description:

| | | | | |
|--------------|---|---|---|---------------------------------------|
| +Vbat | = | I | - | Back up external battery positive pin |
| GND | = | | - | Back up external battery negative pin |

CN3 - PPI AND SOFTWARE I2C BUS I/O CONNECTOR

CN3 is a 20 pins, male, 90 degrees, low profile connector with 2.54mm pitch.
 On CN3 are available 8 PPI I/O digital lines, I²C BUS software line and RTC interrupt signal.
 All these signals follow TTL standard and I/O ABACO® standard pin out.

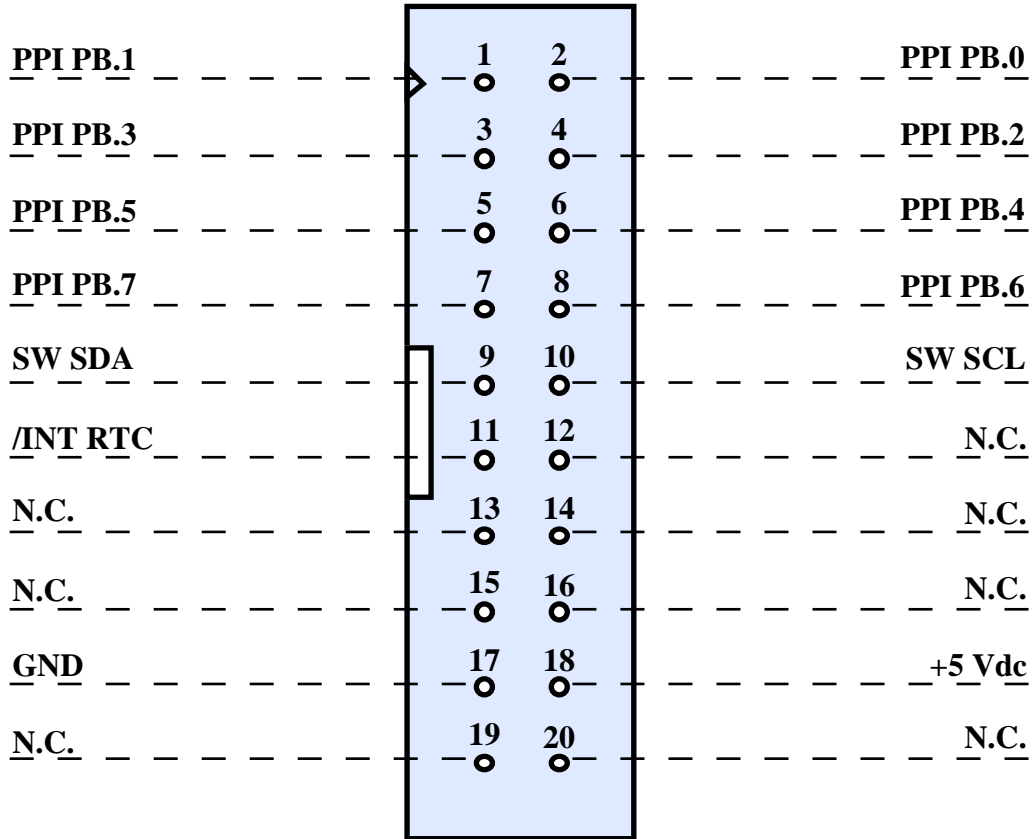


FIGURE 3: CN3 - PPI AND I2C BUS SOFTWARE LINE I/O CONNECTOR

Signals description:

- PPI PB.n** = I/O - n-th digital line of PPI 82C55 port B.
- SW SDA** = I/O - Data signal of I²C BUS software serial line.
- SW SCL** = I/O - Clock signal of I²C BUS software serial line.
- /INT RTC** = O - Real time clock generated interrupt.
- +5 Vdc** = O - Unique +5 Vdc power supply.
- GND** = - Ground.
- N.C.** = - Not connected.

CN2 - PPI I/O CONNECTOR

CN2 is a 20 pins, male, vertical, low profile connector with 2.54mm pitch.

On CN2 are available 16 PPI I/O digital lines.

All these signals follow TTL standard and I/O ABACO® standard pin out.

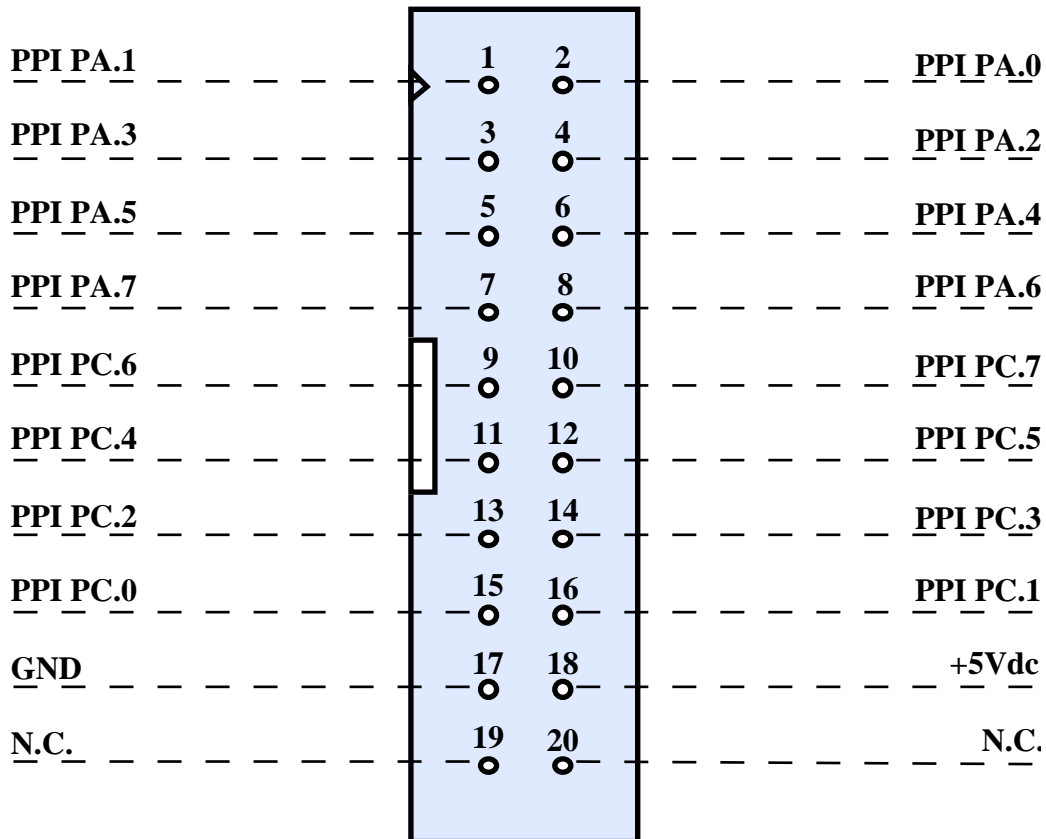


FIGURE 4: CN2 - PPI I/O CONNECTOR

Signals description:

| | |
|-----------------|--|
| PPI PA.n | = I/O - n-th digital line of PPI 82C55 port A. |
| PPI PC.n | = I/O - n-th digital line of PPI 82C55 port C. |
| +5 Vdc | = O - Unique +5 Vdc power supply. |
| GND | = - Ground. |
| N.C. | = - Not connected. |

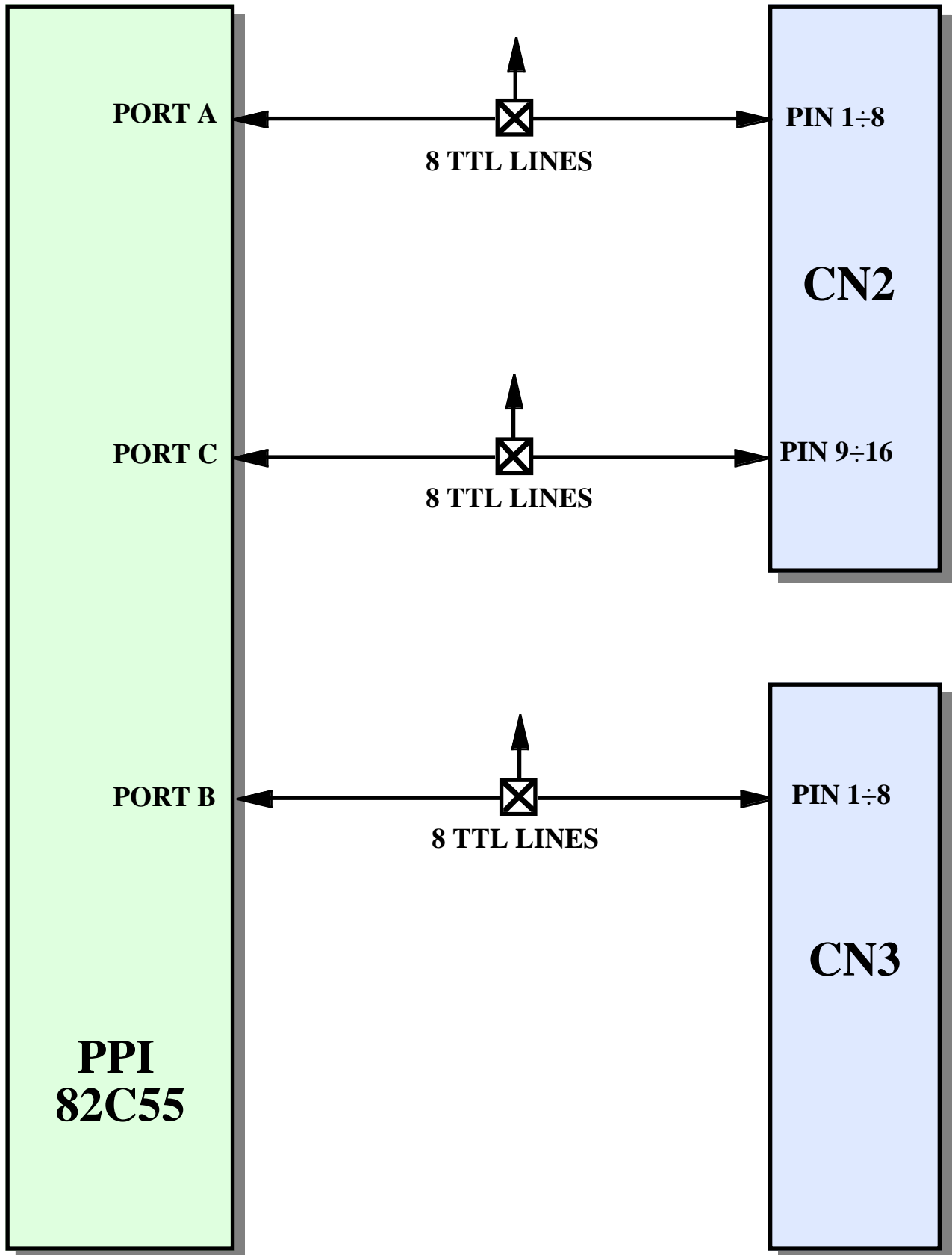


FIGURE 5: PPI BLOCK DIAGRAM

CN1 - CPU I/O CONNECTOR

CN1 is a 20 pins, male, vertical, low profile connector with 2.54mm pitch.

On CN1 are available microprocessor port 1 and 4 I/O digital lines.

Some pins of this connector have multiple purposes, in fact they can be multiplexed by programming some software registers with several CPU internal devices.

All these signals follow TTL standard and I/O **ABACO**[®] standard pin out.

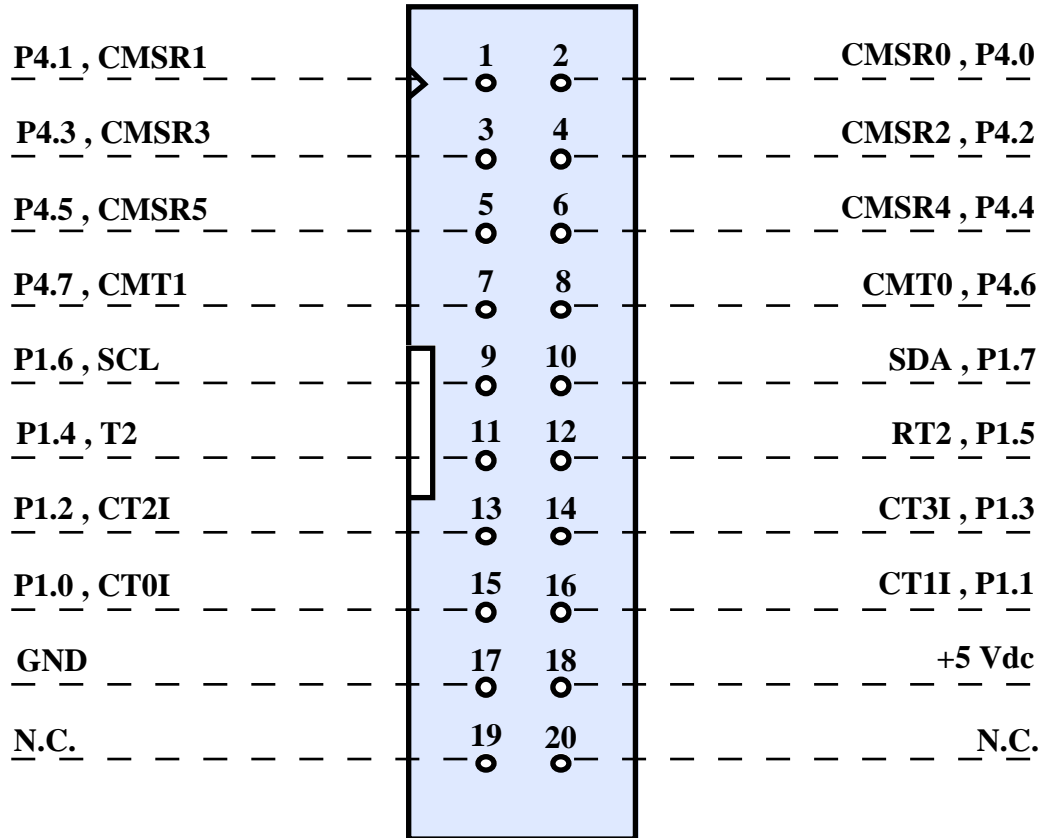


FIGURE 6: CN1 - CPU I/O CONNECTOR

Signals description:

| | |
|---------------|--|
| P1.n | = I/O - n-th digital line of CPU internal port 1. |
| P4.n | = I/O - n-th digital line of CPU internal port 4. |
| CMSRn | = O - n-th compare and set/reset on a match with CPU internal timer 2. |
| CMTn | = O - n-th compare and toggle on a match with CPU internal timer 2. |
| CTnI | = I - n-th capture of CPU internal timer 2. |
| SDA | = I/O - Data signal of I ² C BUS hardware serial line. |
| SCL | = I/O - Clock signal of I ² C BUS hardware serial line. |
| T2 | = I - Counter signal of CPU internal timer 2. |
| RT2 | = I - Reset counter signal of CPU internal timer 2. |
| +5 Vdc | = O - Unique +5 Vdc power supply. |
| GND | = - Ground. |
| N.C. | = - Not connected. |

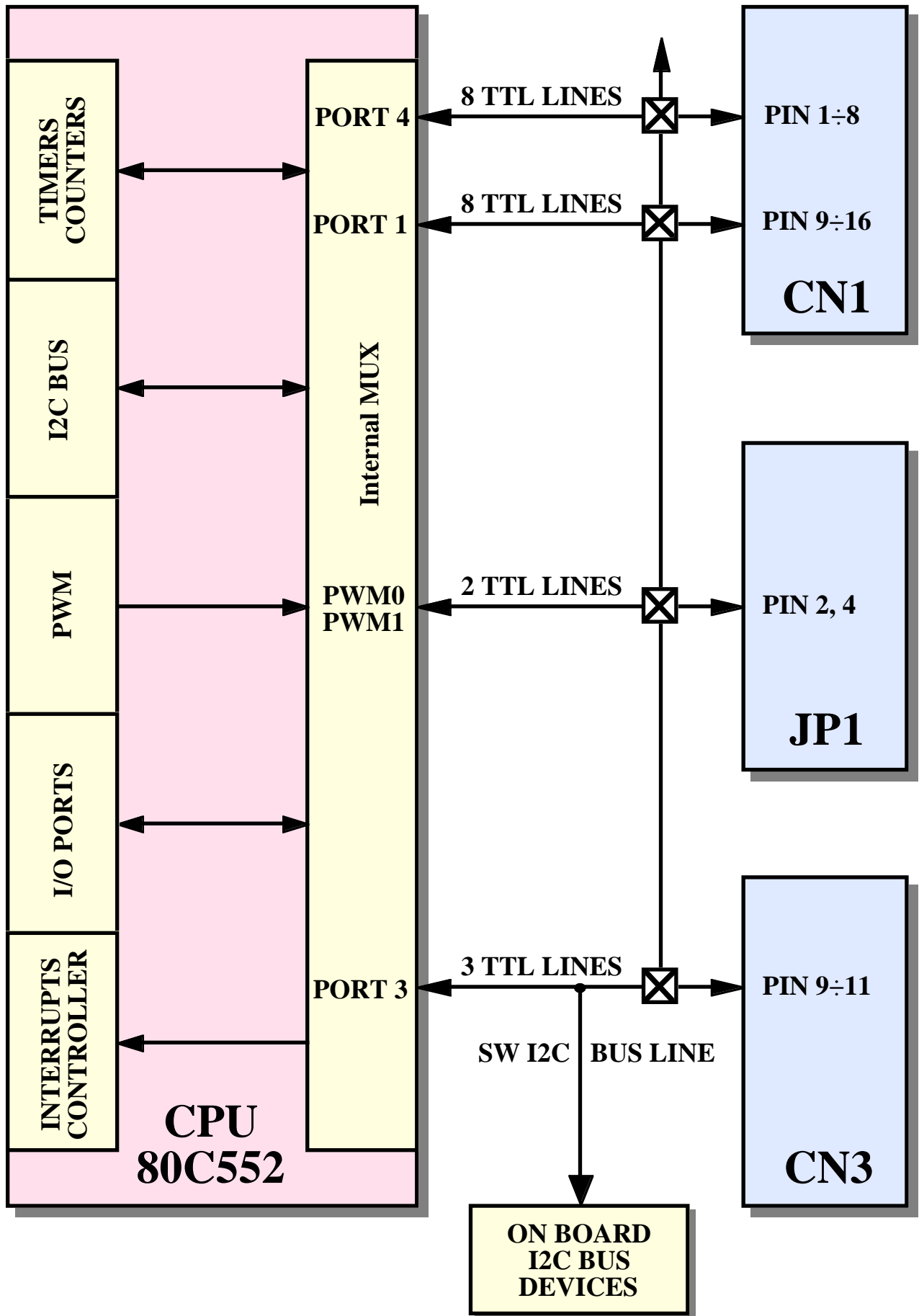


FIGURE 7: CPU I/O SIGNALS BLOCK DIAGRAM

JP3 - SERIAL LINE A CONNECTOR

JP3 is a 6 pins PLUG, 90 degrees, female connector.

On JP3 connector are available the buffered signals for RS 232, RS 422, RS 485 or Current Loop serial communication, managed by CPU internal UART.

No more than one of the described standards, is connected to JP3, but the same connector can be used for each of the listed electric protocols (CCITT normatives compliant).

All the signals are placed in order to reduce interference and electrical noise.

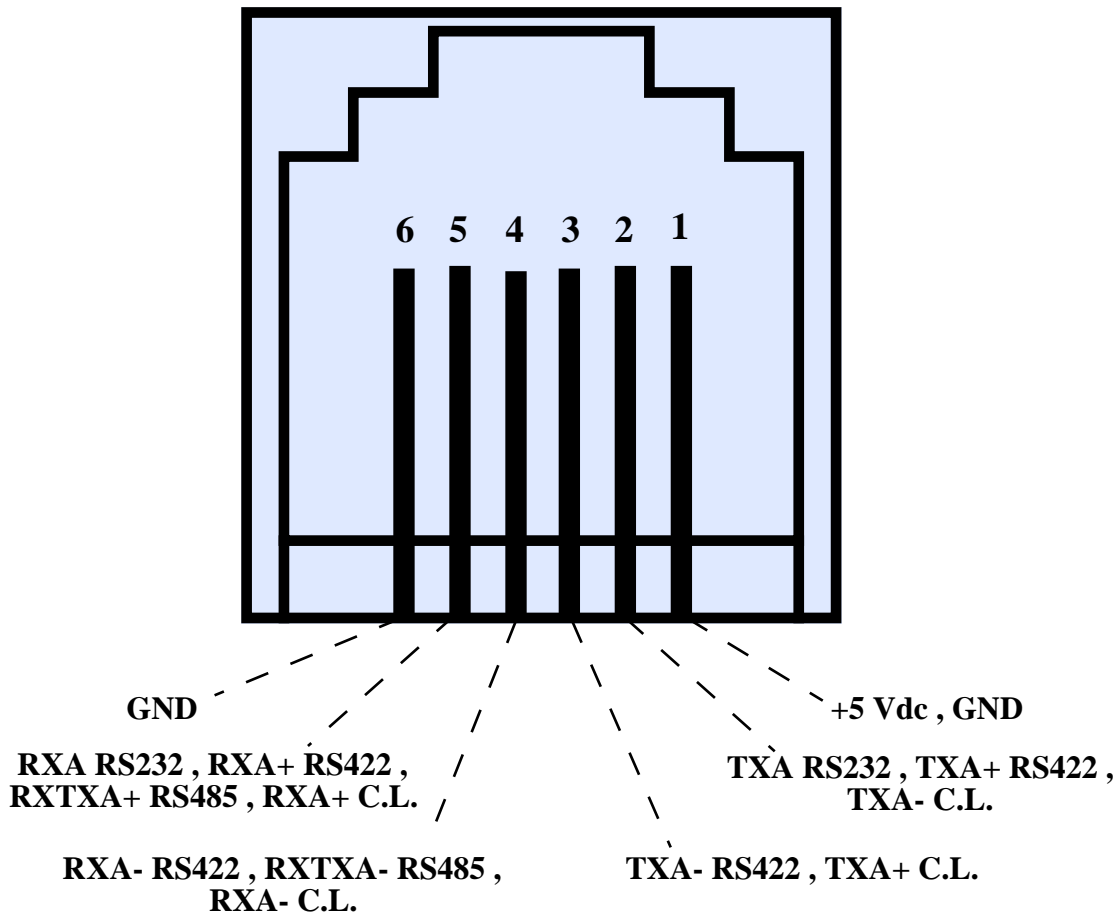


FIGURE 8: JP3 -SERIAL LINE A CONNECTOR

Signals description:

| | | | |
|-------------------|-----|---|--|
| RXA RS232 | = I | - | Receive Data for RS 232. |
| TXA RS232 | = O | - | Transmit Data for RS 232. |
| RXA- RS422 | = I | - | Receive Data Negative for RS 422. |
| RXA+ RS422 | = I | - | Receive Data Positive for RS 422. |
| TXA- RS422 | = O | - | Transmit Data Negative for RS 422. |
| TXA+ RS422 | = O | - | Transmit Data Positive for RS 422. |
| RXA- C.L. | = I | - | Receive Data Negative for Current Loop. |
| RXA+ C.L. | = I | - | Receive Data Positive for Current Loop. |
| TXA- C.L. | = O | - | Transmit Data Negative for Current Loop. |
| TXA+ C.L. | = O | - | Transmit Data Positive for Current Loop. |

- RXTXA+ RS485** = I/O- Receive/Trasmit Data Positive for RS 485.
- RXTXA- RS485** = I/O- Receive/Trasmit Data Negative for RS 485.
- +5 Vdc/GND** = I - +5 Vdc power supply or Digital ground signal.
- GND** = Digital ground signal.

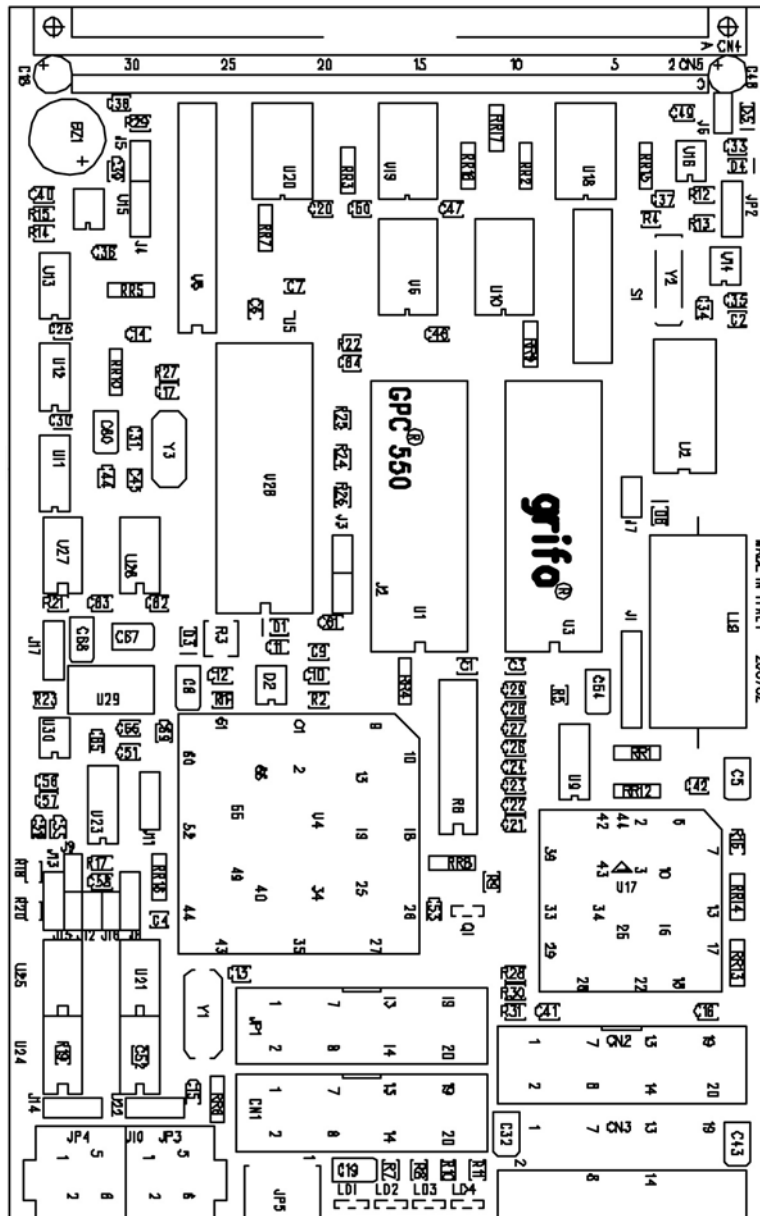


FIGURE 9: COMPONENTS MAP ON SOLDER SIDE

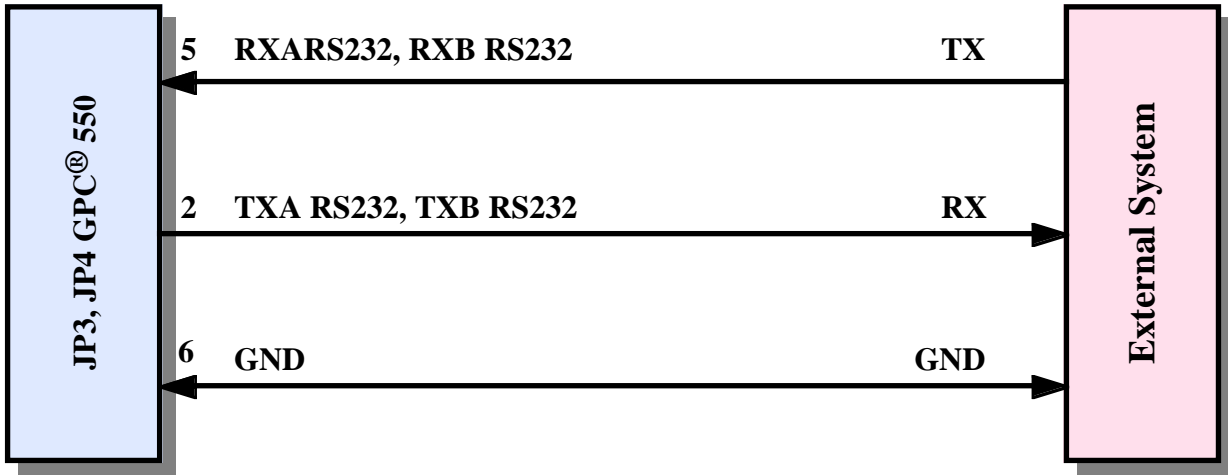


FIGURE 10: RS 232 POINT TO POINT CONNECTION EXAMPLE

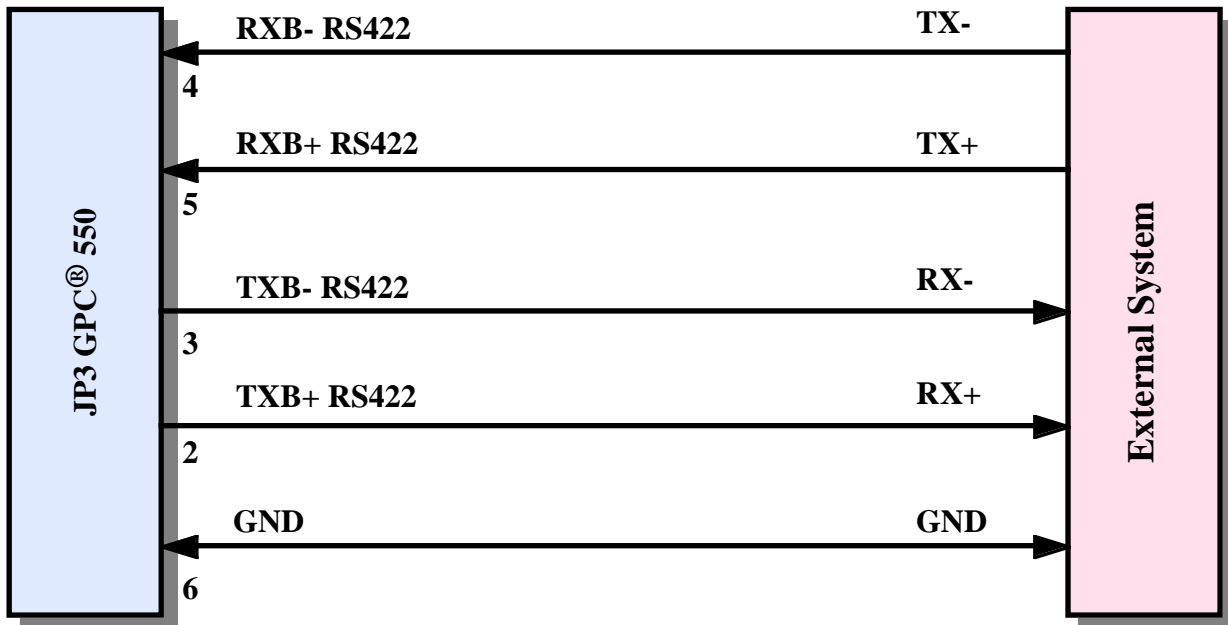


FIGURE 11: RS 422 POINT TO POINT CONNECTION EXAMPLE

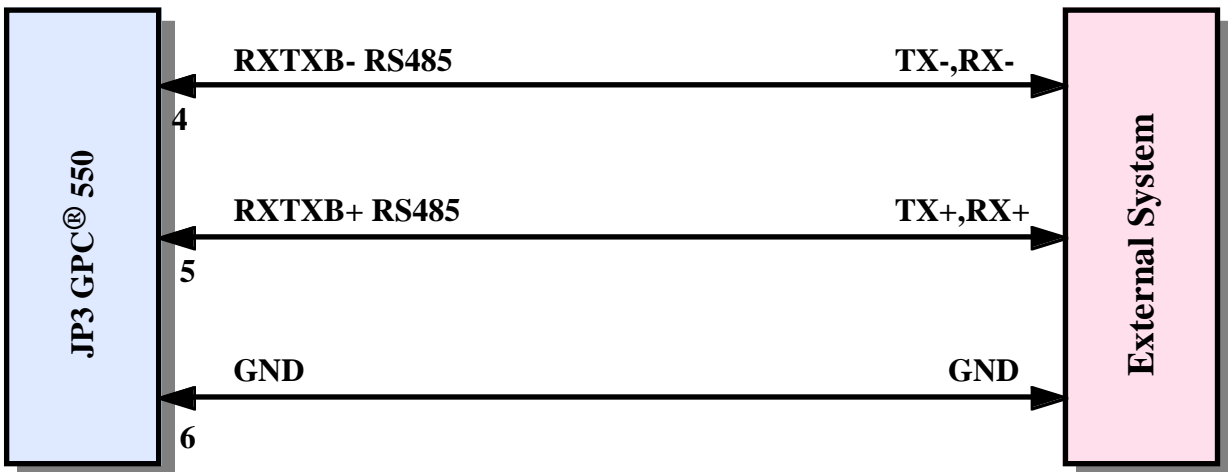


FIGURE 12: RS 485 POINT TO POINT CONNECTION EXAMPLE

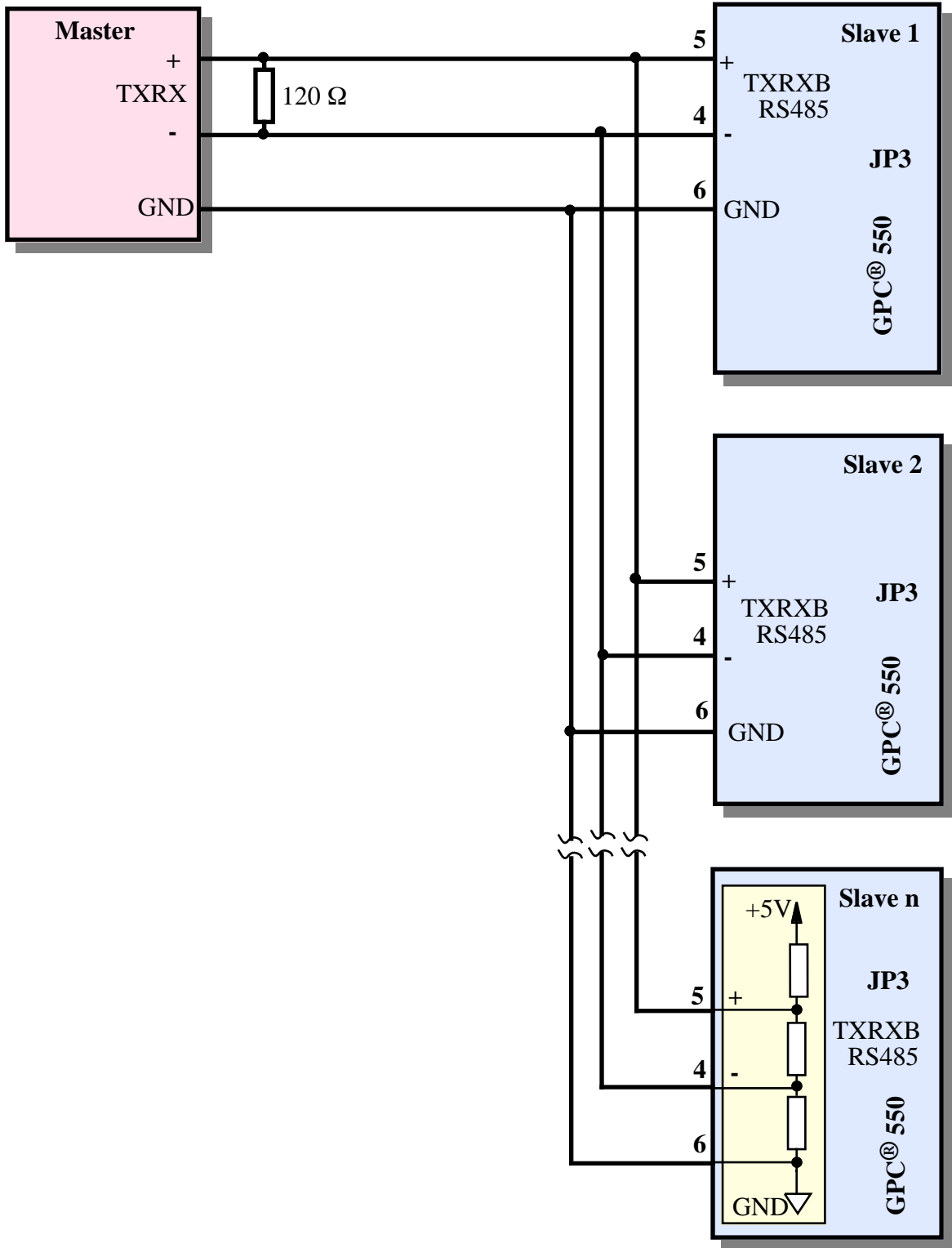


FIGURE 13: RS 485 NETWORK CONNECTION EXAMPLE

Please remark that in a RS 485 network two forcing resistors must be connected across the net and two termination resistors (120 Ω) must be placed at its extremities, respectively near the Master unit and the Slave unit at the greatest distance from the Master.

Forcing and terminating circuitry is installed on GPC® 550 board. It can be enabled or disabled through specific jumpers, as explained later.

For further information please refer to TEXAS INSTRUMENTS Data-Book, "RS 422 and RS 485 Interface Circuits", the introduction about RS 422-485.

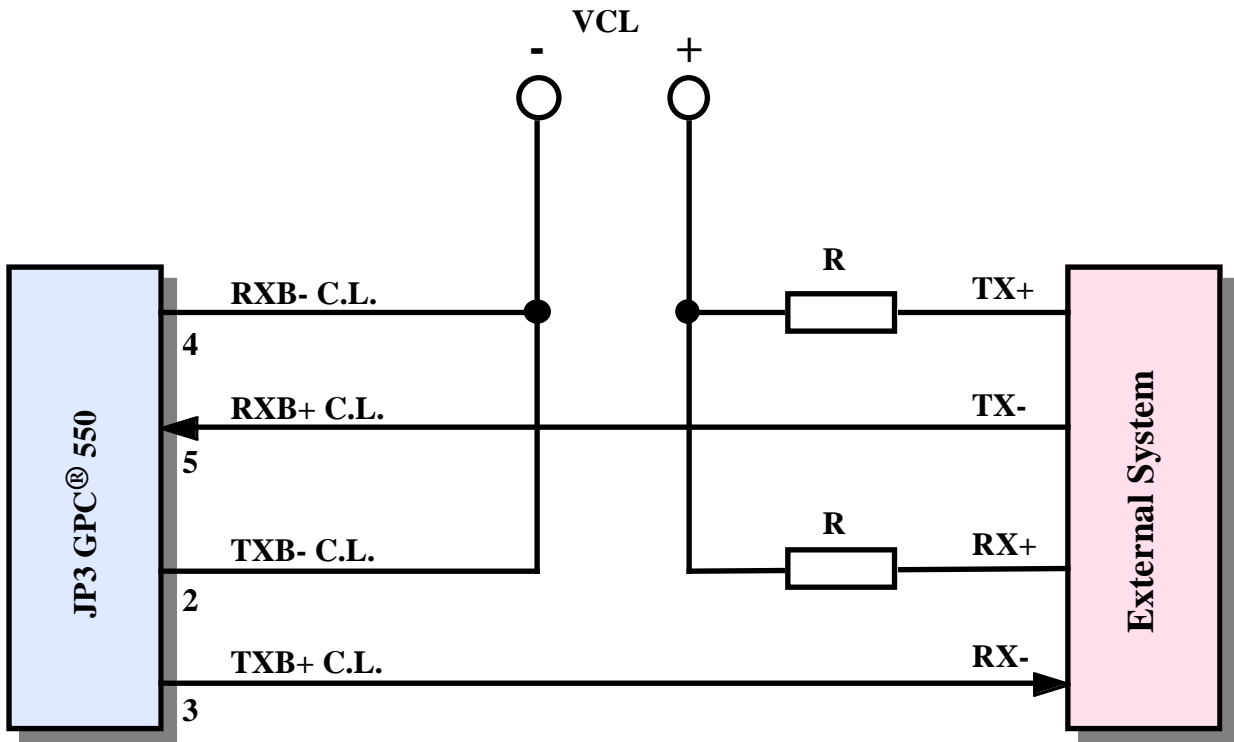


FIGURE 14: CURRENT LOOP 4 WIRES POINT-TO-POINT CONNECTION EXAMPLE

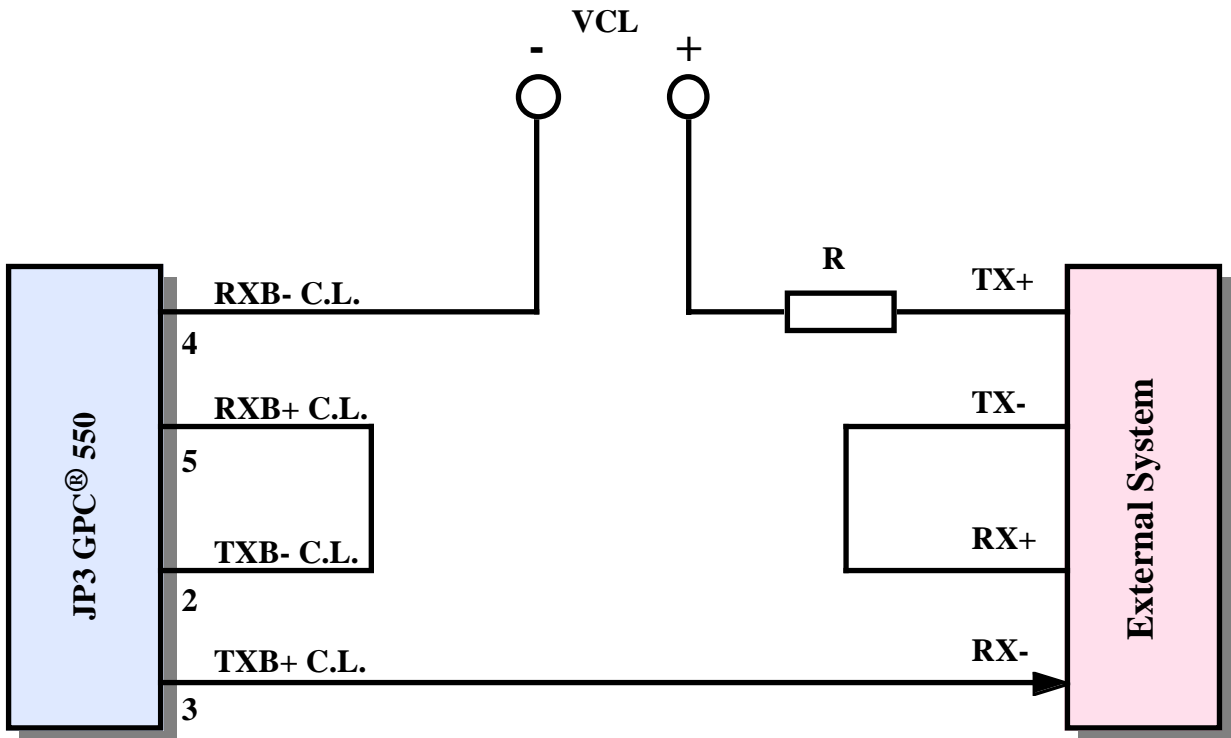


FIGURE 15: CURRENT LOOP 2 WIRES POINT-TO-POINT CONNECTION EXAMPLE

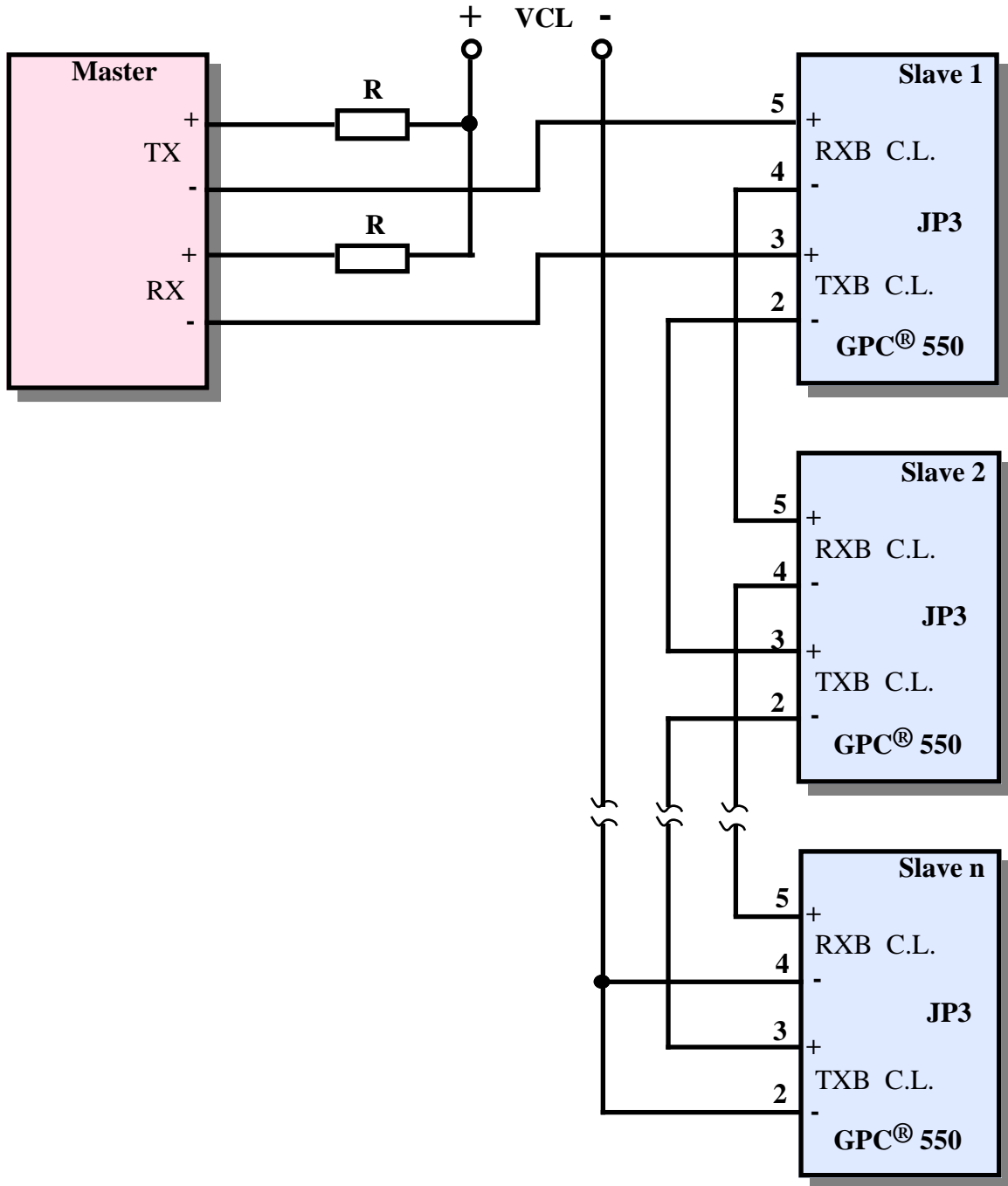


FIGURE 16: CURRENT LOOP NETWORK CONNECTION EXAMPLE

Possible Current Loop connections are two: 2 wires and 4 wires. These connections are shown in figures 14÷16 where it is possible to see the voltage for **VCL** and the resistances for current limitation (**R**). The supply voltage varies in compliance with the number of connected devices and voltage drop on the connection cable.

The choice of the values for these components must be done considering that:

- circulation of a **20 mA** current must be guaranteed;
- potential drop on each transmitter is about **2.35 V** with a 20 mA current;
- potential drop on each receiver is about **2.52 V** with a 20 mA current;
- in case of shortcircuit each transmitter must dissipate at most **125 mW**;
- in case of shortcircuit each receiver must dissipate at most **90 mW**.

For further info please refer to HEWLETT-PACKARD Data Book, (**HCPL 4100** and **4200** devices).

JP4 - SERIAL LINE B CONNECTOR

JP4 is a 6 pins, female, 90 degrees, PLUG connector.

On JP4 are available the buffered signals for only RS 232 serial line B communication.

All the signals are placed in order to reduce interference and electrical noise; the signals follow the standard CCITT normative.

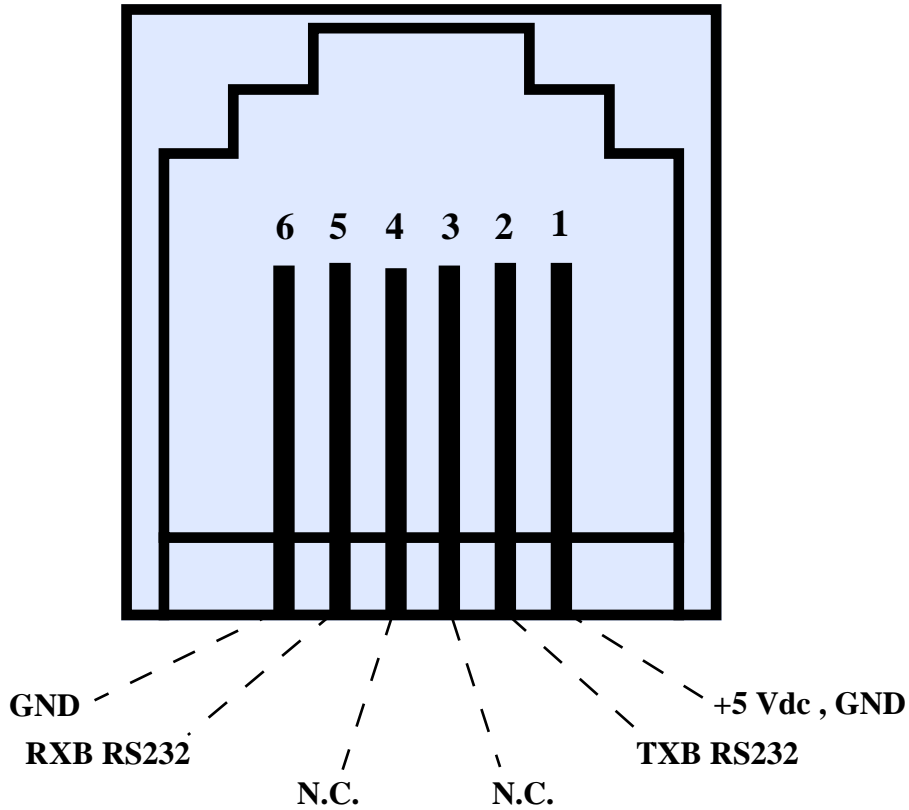


FIGURE 17: JP4 - SERIAL LINE B CONNECTOR.

Signals description:

| | | | | |
|--------------------|---|---|---|---|
| RxDB RS 232 | = | I | - | Receive Data for RS 232. |
| TxDB RS 232 | = | O | - | Transmit Data for RS 232. |
| +5 Vdc/GND | = | I | - | +5 Vdc power supply or Digital ground signal. |
| GND | = | | - | Digital ground signal. |
| N.C. | = | | - | Not Connected. |

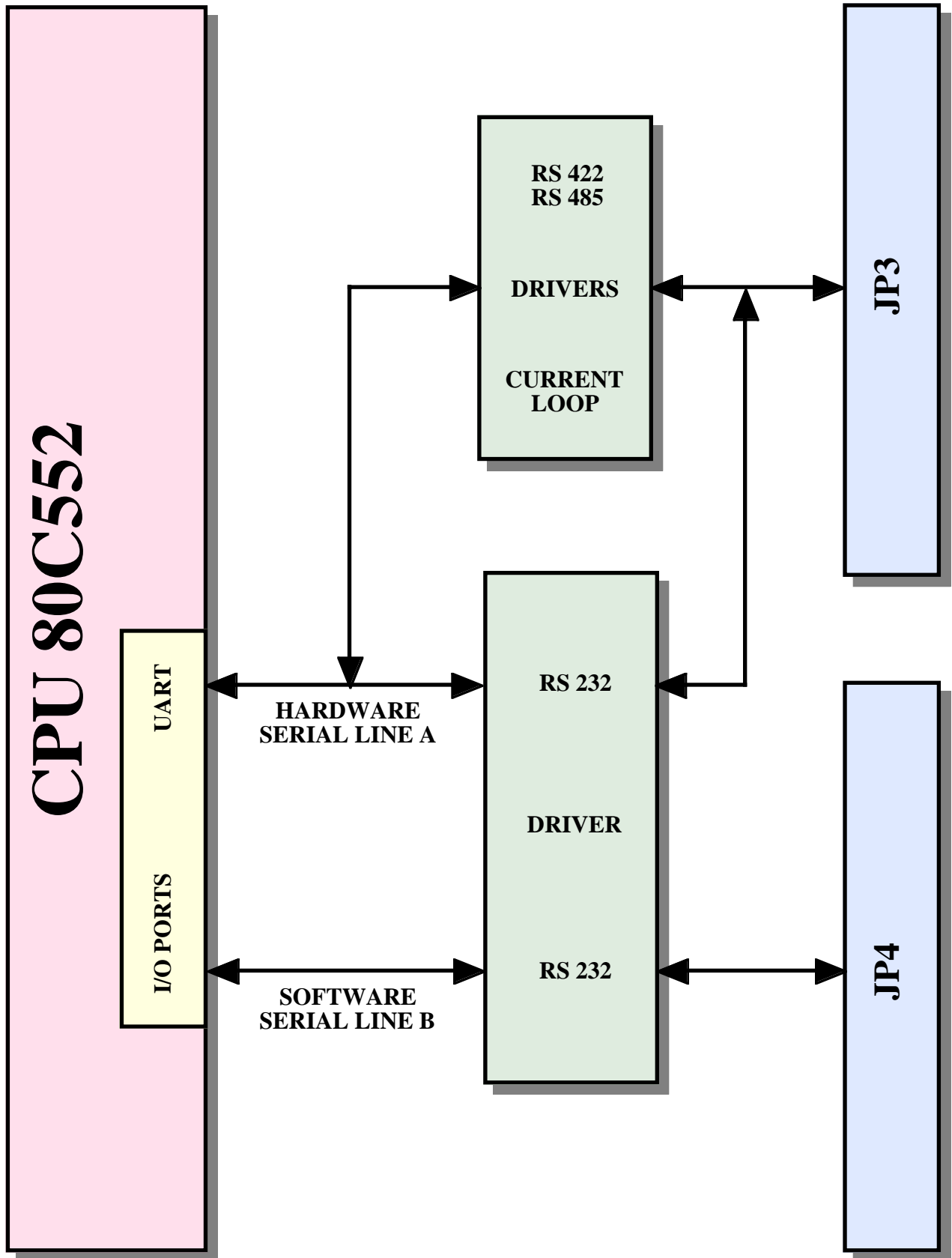


FIGURE 18: SERIAL DEVICES BLOCK DIAGRAM

CN4 + CN5 - CONNECTOR FOR BUS ABACO®

The connector for **ABACO® industrial BUS**, called CN4 and CN5 on board, is a DIN 41612, male, a 90°, type C, A+C.

Here follows the pin-out of the connector installed on **GPC® 550**, in addition there is the standard 8 bits and 16 bits **ABACO® BUS** pin-out.

Please remark that all the signals here described are TTL, except for the power supplies.

| A 16 bit BUS | A 8 bit BUS | A = CN4 GPC 550 | PIN | C = CN5 GPC 550 | C 8 bit BUS | C 16 bit BUS |
|-----------------|----------------|--------------------|-----|--------------------|----------------|-----------------|
| GND | GND | GND | 1 | GND | GND | GND |
| +5 Vdc | +5 Vdc | +5 Vdc | 2 | +5 Vdc | +5 Vdc | +5 Vdc |
| D0 | D0 | D0 | 3 | N.C. | - | D8 |
| D1 | D1 | D1 | 4 | N.C. | - | D9 |
| D2 | D2 | D2 | 5 | N.C. | - | D10 |
| D3 | D3 | D3 | 6 | N.C. | /INT | /INT |
| D4 | D4 | D4 | 7 | N.C. | /NMI | /NMI |
| D5 | D5 | D5 | 8 | N.C. | /HALT | D11 |
| D6 | D6 | D6 | 9 | N.C. | /MREQ | /MREQ |
| D7 | D7 | D7 | 10 | /IORQ | /IORQ | /IORQ |
| A0 | A0 | A0 | 11 | /RD | /RD | /RDLDS |
| A1 | A1 | A1 | 12 | /WR | /WR | /WRLDS |
| A2 | A2 | A2 | 13 | N.C. | /BUSAK | D12 |
| A3 | A3 | A3 | 14 | N.C. | /WAIT | /WAIT |
| A4 | A4 | A4 | 15 | N.C. | /BUSRQ | D13 |
| A5 | A5 | A5 | 16 | /RESET | /RESET | /RESET |
| A6 | A6 | A6 | 17 | N.C. | /M1 | /IACK |
| A7 | A7 | A7 | 18 | N.C. | /RFSH | D14 |
| A8 | A8 | N.C. | 19 | N.C. | /MEMDIS | /MEMDIS |
| A9 | A9 | N.C. | 20 | N.C. | VDUSEL | A22 |
| A10 | A10 | N.C. | 21 | N.C. | /IEI | D15 |
| A11 | A11 | N.C. | 22 | N.C. | - | - |
| A12 | A12 | N.C. | 23 | N.C. | CLK | CLK |
| A13 | A13 | N.C. | 24 | N.C. | - | /RDUDS |
| A14 | A14 | N.C. | 25 | N.C. | - | /WRUDS |
| A15 | A15 | N.C. | 26 | N.C. | - | A21 |
| A16 | - | N.C. | 27 | N.C. | - | A20 |
| A17 | - | N.C. | 28 | N.C. | - | A19 |
| A18 | - | N.C. | 29 | /R.T. | /R.T. | /R.T. |
| +12 Vdc | +12 Vdc | N.C. | 30 | N.C. | -12 Vdc | -12 Vdc |
| +5 Vdc | +5 Vdc | +5 Vdc | 31 | +5 Vdc | +5 Vdc | +5 Vdc |
| GND | GND | GND | 32 | GND | GND | GND |

FIGURE 19: CN4 + CN5 - BUS ABACO® CONNECTOR

Signals description:

8 bits CPU

| | | | |
|----------------|---|-----|---------------------------|
| A0-A15 | = | O | - Address BUS |
| D0-D7 | = | I/O | - Data BUS |
| /INT | = | I | - Interrupt request |
| /NMI | = | I | - Non Maskable Interrupt |
| /HALT | = | O | - Halt state |
| /MREQ | = | O | - Memory Request |
| /IORQ | = | O | - Input Output Request |
| /RD | = | O | - Read cycle status |
| /WR | = | O | - Write cycle status |
| /BUSAK | = | O | - BUS Acknowledge |
| /WAIT | = | I | - Wait |
| /BUSRQ | = | I | - BUS Request |
| /RESET | = | O | - Reset |
| /M1 | = | O | - Machine cycle one |
| /RFSH | = | O | - Refresh for dynamic RAM |
| /MEMDIS | = | I | - Memory Display |
| VDUSEL | = | O | - VDU Selection |
| /IEI | = | I | - Interrupt Enable Input |
| CLK | = | O | - System clock |
| R.B. | = | I | - Reset button |
| +5 Vdc | = | I | - Power supply at +5 Vdc |
| +12 Vdc | = | I | - Power supply at +12 Vdc |
| -12 Vdc | = | I | - Power supply at -12 Vdc |
| GND | = | | - Ground signal |

16 bits CPU

| | | | |
|----------------|---|-----|---------------------------|
| A16-A22 | = | O | - Address BUS |
| D8-D15 | = | I/O | - Data BUS |
| /RD UDS | = | O | - Read Upper Data Strobe |
| /WR UDS | = | O | - Write Upper Data Strobe |
| /IACK | = | O | - Interrupt Acknowledge |
| /RD LDS | = | O | - Read Lower Data Strobe |
| /WR LDS | = | O | - Write Lower Data Strobe |

NOTE

Directionality indications as above stated are referred to a master (GPC®) board and have been kept untouched to avoid ambiguity in case of multi-boards systems.

JP1 - CONNECTOR FOR A/D CONVERTER INPUTS AND PWM

JP1 is a 20 pins, male, vertical, low profile connector with 2.54 mm pitch.

On JP1 is available microprocessor analog signals high impedance inputs for A/D Converter section.

They feature a filtering capacitor and input signal may vary in the range 0÷2.49 Vdc.

Installing a specific conversione module (that can be ordered with code .8420), it is possible to connect current signals in the range 0÷20 mA or 4÷20 mA.

Signals placement is compliant with A/D **ABACO**[®] standard pin out, it has been designed to reduce noise and interference problems, and to warrant a good signals transmission.

On JP1 connector are also available microprocessor PWM lines (8 bits) useful for motor control and D/A simulation.

Several signals are multipurpose, in fact ADC inputs can be multiplexed with I/O TTL port 5.

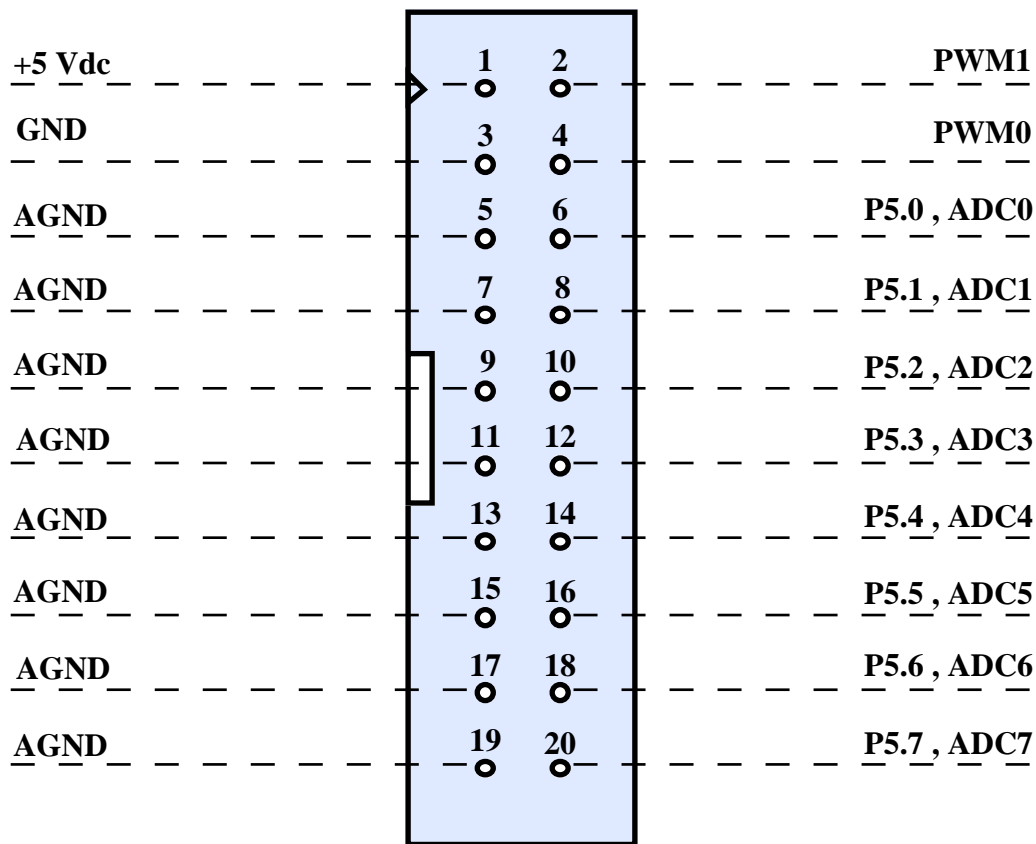


FIGURE 20: JP1 - CONNECTOR FOR A/D CONVERTER INPUTS AND PWM LINES

Signals description:

| | | | | |
|------------------|---|---|---|--|
| PWM0 | = | O | - | CPU PWM n. 0 line. |
| PWM1 | = | O | - | CPU PWM n. 1 line. |
| P5.n/ADCn | = | I | - | Digital line n or A/D channel n of CPU port 5. |
| GND | = | - | - | Digital ground signal. |
| AGND | = | - | - | Analog ground signal. |
| +5 Vdc | = | - | - | +5 Vdc power supply. |

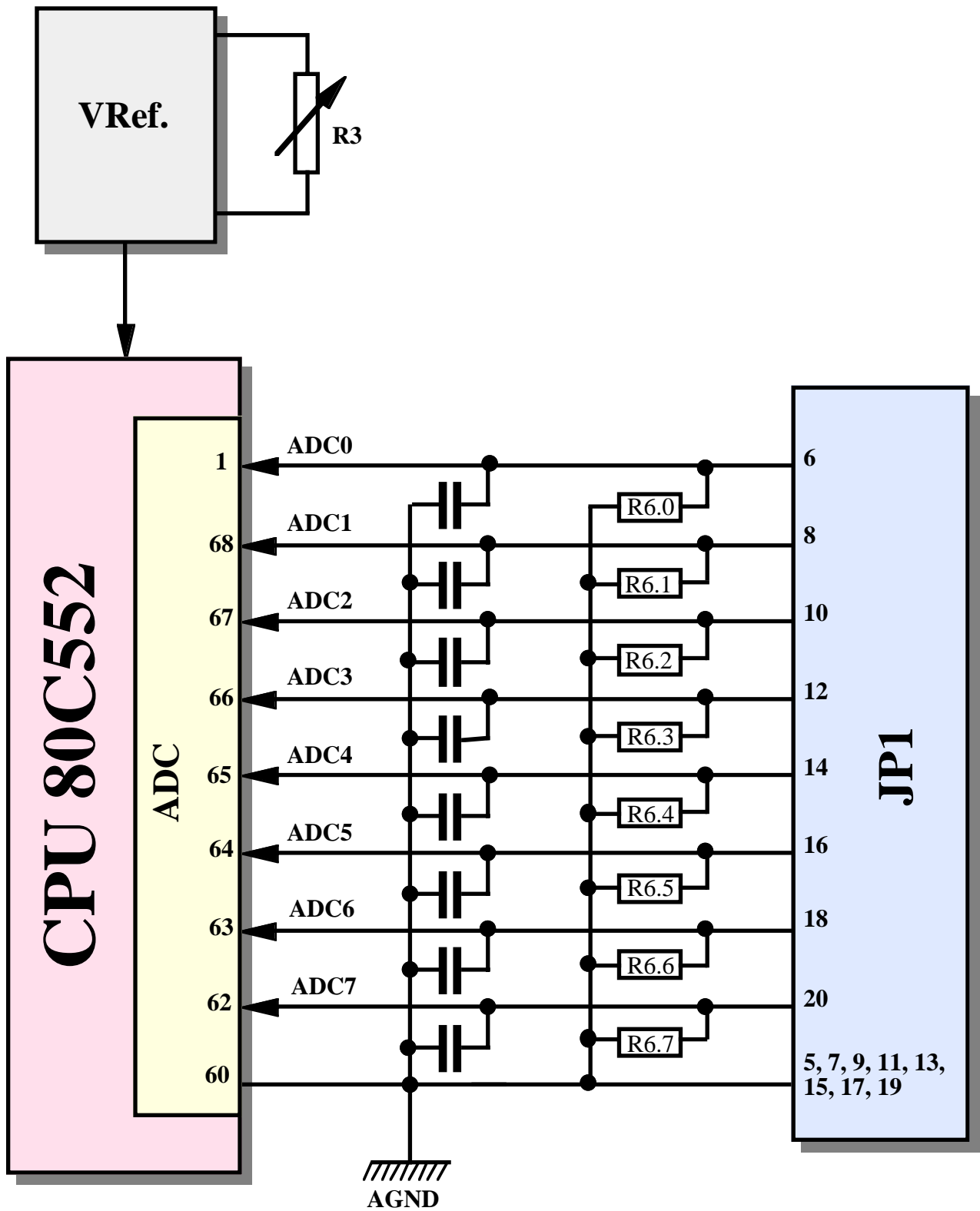


FIGURE 21: A/D CONVERTER INPUTS AND PWM LINES BLOCK DIAGRAM

JP5 - CAN INTERFACE CONNECTOR

JP5 is a 3 pins, male, 90 degrees, quick release screw terminal connector with 3.54 mm pitch. Through JP5 must be connected the CAN serial communication line by following the standard rules defined by the same protocol.

Signal placement has been designed to reduce interference and to easy the connection to the field, according to the standard.

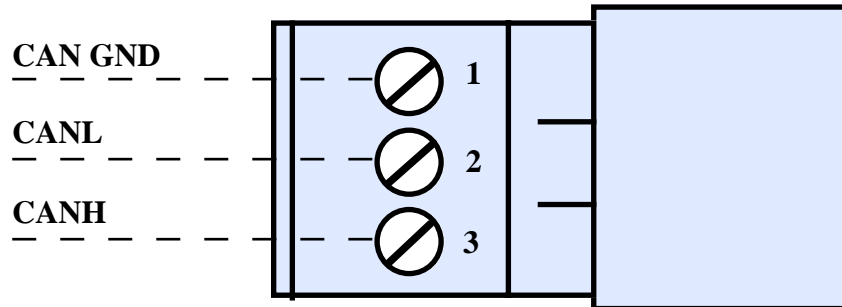


FIGURE 22: JP5 - CAN INTERFACE CONNECTOR

Signals description:

CANH = I/O - Differential line high for CAN interface.
CANL = I/O - Differential line low for CAN interface.
CAN GND = - CAN ground.

NOTE

Power supply of CAN section is galvanically isolated from **GPC® 550** power supply, so **CAN GND must NOT be connected** to signals GND and AGND.

For further information please refer to paragraph "POWER SUPPLY".

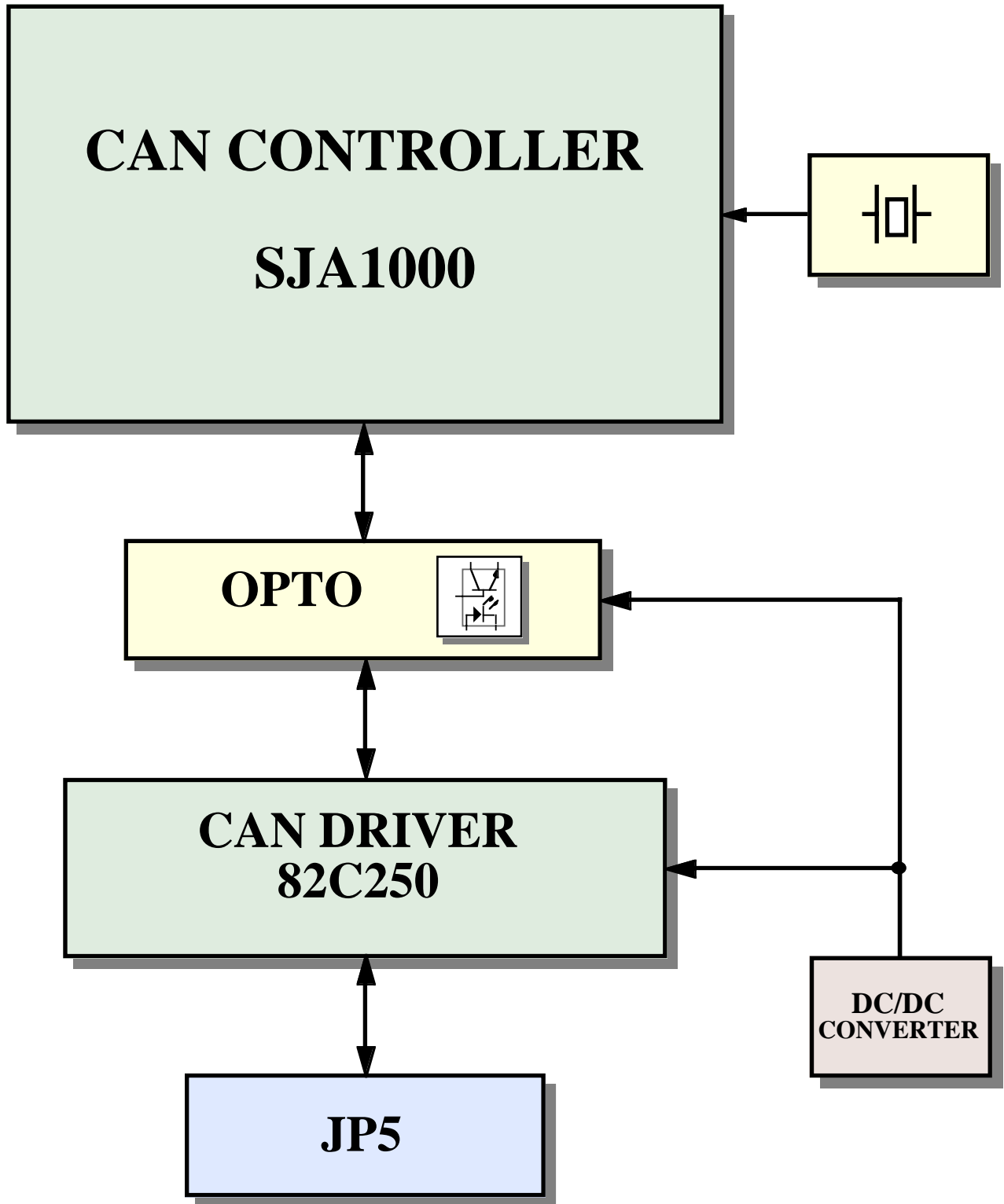


FIGURE 23: CAN LINE BLOCK DIAGRAM

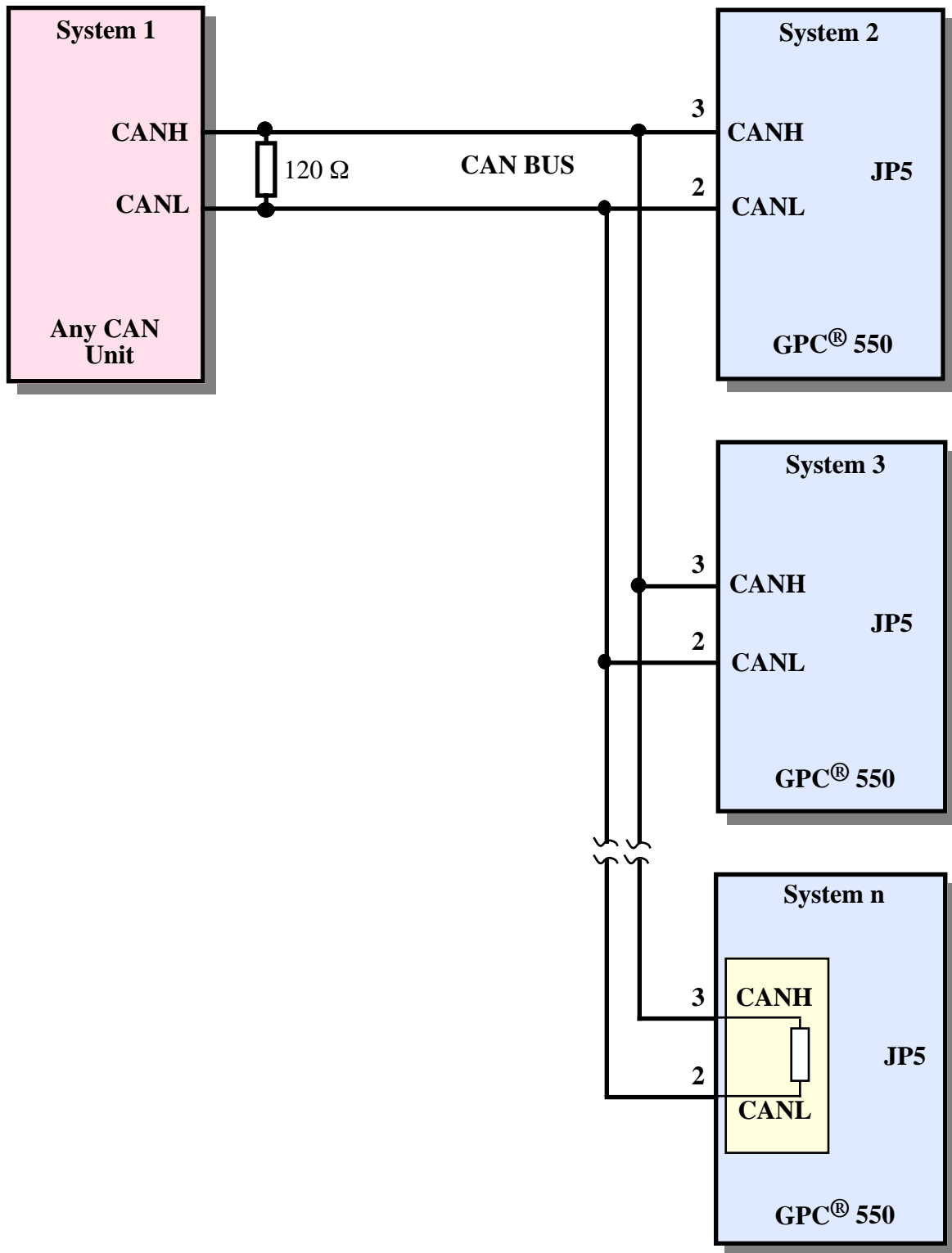


FIGURE 24: CAN INTERFACE CONNECTION EXAMPLE

Please remind that a CAN network must have two termination resistors (120 Ω) placed at its extremities, respectively near the master unit and the slave unit at the greatest distance from the master.

On GPC® 550 board the terminating circuitry is already installed: it can be connected or not through specific jumper, as explained later, in paragraph "JUMPERS".

Should the system to connect be at very different potentials, it is possible to connect also the grounds of the systems, that is pin 1 of JP5, to solve eventual problems of communication and/or correct working.

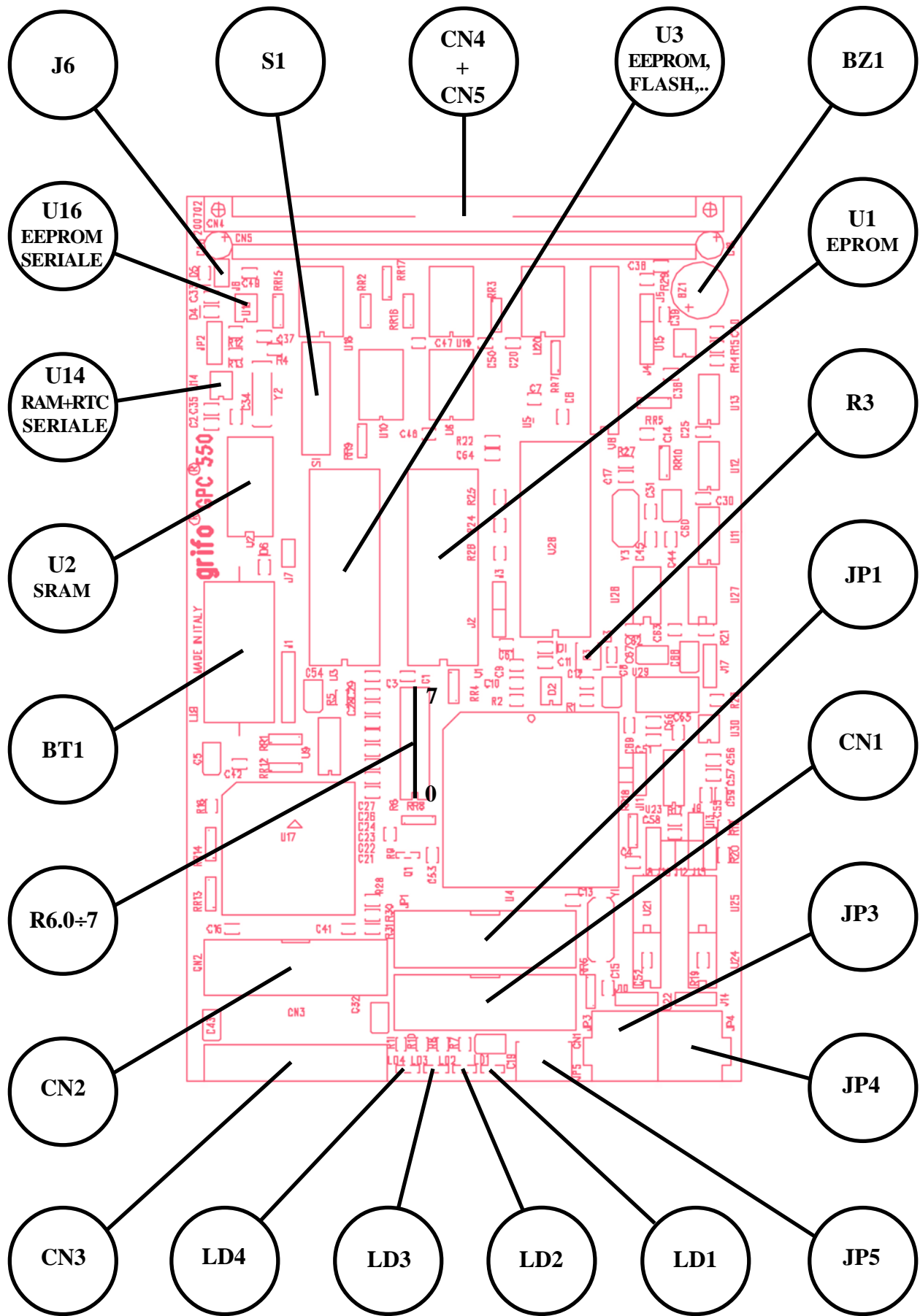


FIGURE 25: CONNECTORS, TRIMMER, BATTERY, MEMORIES, ETC. LOCATION

I/O CONNECTION

To prevent possible connecting problems between **GPC® 550** and the external systems, the user has to read carefully the previous paragraph information and he must follow these instructions:

- For RS 232, RS 422, RS 485, Current Loop and CAN signals the user must follow the standard rules of each one of these protocols;
- For all TTL signals the user must follow the rules of this electric standard. The connected digital signal must be always referred to card digital ground and if an electric insulation is necessary, then an opto coupled interface must be connected. For TTL signals, the 0V level corresponds to logic state 0, while 5V level corresponds to logic state 1.
- The analog inputs (A/D Converter section) must be connected to signals in the ranges: $0 \div +2.49$ Vdc or $0 \div 20$ mA according to card configuration. Inputs feature high impedance, anyway an eventual interfacing circuitry should provide low impedance to assure greater stability and precision. Please remark that the eight analog inputs on JP1 are provided with filtering capacitors that warrant more stability on the signal to acquire and lower the cut-off frequency to 1 MHz, very greater than maximum frequency for A/D acquisition: 20 KHz.
- PWM signals are TTL so they must be buffered to interface the power circuitry. Typical interfaces can be current driver (if PWM signal is still required) or an integrator circuit if analog voltage required.
- Also I²C BUS signals are TTL, as defined by the standard; for completeness it is remarked that in a network with several devices and rather long it is better to use hardware I²C BUS. Output stage, many operational modes and programmable bit rate allow to communicate in any condition.

TRIMMERS AND CALIBRATION

On **GPC® 550** is available a trimmer, named **R3**, that calibrates the Vref voltage of the A/D Converter section.

The **GPC® 550** is subjected to a careful test that verifies and calibrates all the card sections. To easily locate the trimmer, please refer to figure 25. The calibration is executed in laboratory, with a controlled +20 C° room temperature, following these steps:

- The A/D voltage reference (Vref) is calibrated through R3 trimmer, by using a 5 digits precision galvanically isolated multimeter, to a value of 2.490 V dc between pin 59 (+) and pin 58 (-) of CPU on U4.
- The correspondance between the analog input signal and the combination read from A/D is verified. This check is performed with a reference signal connected to A/D inputs and testing that the A/D combination and the theoretic combination differ at maximum of the A/D section errors sum.
- The trimmer is blocked with paint.

The analog interfaces use high precision components that are selected during mounting phase to avoid complicate and long calibration procedures.

After the calibration, the on board trimmer is blocked with paint to mantain calibration also in presence of mechanic stresses (vibrations, movings, delivery, etc.).

The user must not modify the card calibration, but if thermic drifts,time drifts and so on, make necessary a new calibration, the user must strictly follow the previous described procedure.

ANALOG INPUTS SELECTION

One of the GPC® 550 particular features is the possibility to acquire tension and/or current signals for all the 8 A/D inputs. The CURRENT signals selection is obtained throuhg proper resistors mounted on the conversion module (option .8420) with the following correspondence:

| | | |
|------|----|-----------|
| R6.0 | -> | channel 0 |
| R6.0 | -> | channel 1 |
| R6.2 | -> | channel 2 |
| R6.3 | -> | channel 3 |
| R6.4 | -> | channel 4 |
| R6.5 | -> | channel 5 |
| R6.6 | -> | channel 6 |
| R6.7 | -> | channel 7 |

If the resistor is not mounted (default) the channel can acquire a TENSION signal in the range 0÷+2.49 Vdc, instead if the resistor is mounted the channel can acquire a CURRENT signal.

The resistors value for the CURRENT/VOLTAGE converter section is calculated with the following formula:

$$R = +2.49 \text{ V} / I_{\text{max}}$$

Normaly the precision CURRENT/VOLTAGE resistor value is 124Ω suitable for 0÷20 mA or 0÷20 mA analog inputs.

For eventuel requirements outdise these standard ranges please contact grifo®.

Please refer to figure 25 for the resistors location.

DIGITAL I/O INTERFACES

Through CN1, CN2 and CN3 (**I/O ABACO**[®] standard connector) the **GPC**[®] **550** card can be connected to all of the numerous **grifo**[®] boards featuring the same standard pin out. Installation of these interface is very easy; in fact only a 20 pins flat cable (code FLT.20+20) is required, while the software management of these interfaces is as easy; in fact most of the software packages available for **GPC**[®] **550** card are provided with the necessary procedures.

These latter are “software drivers” or libraries added to the language that allow to use directly the high level instructions of the language and so their full power.

Remarkable modules are:

- **QTP 16P, QTP 24P, KDL x24, KDF 224, DEB 01**, etc. that solve all the local operator interfacing problems. These modules are provided with all the resources needed to obtain a high-level human-machine interface (they feature alphanumeric displays, matrix keyboard and visualization LEDs) at a short distance from **GPC**[®] **550** card. The available software drivers allow to manage the operator interface resources directly through the high-level instructions for console management.
- **IAC 01, DEB 01**: it is an interface for CENTRONICS parallel printer that can be connected with a standard printer cable. The printer is managed by software through the high level instructions of the selected programming language (LPRINT for BASIC, PRINTF for C, etc.).
- **MCI 64**: it a large mass memory support that can directly manage the PCMCIA memory cards (RAM, FLASH, ROM, etc.) in their available sizes. About software the developed drivers provide a complete file system interfacing allowing to access the informations stored in the memory card directly through the high-level file management instructions.
- **RBO xx, TBO xx, XBI xx, OBI xx**: these are buffer interfaces for I/O TTL signals. With these modules the the TTL input signals are converted in NPN or PNP optoisolated inputs and the TTL output signals are converted in relays or transistor optoisolated outputs.

For more information please refer to "EXTERNAL CARDS" chapter and the software tools documentation.

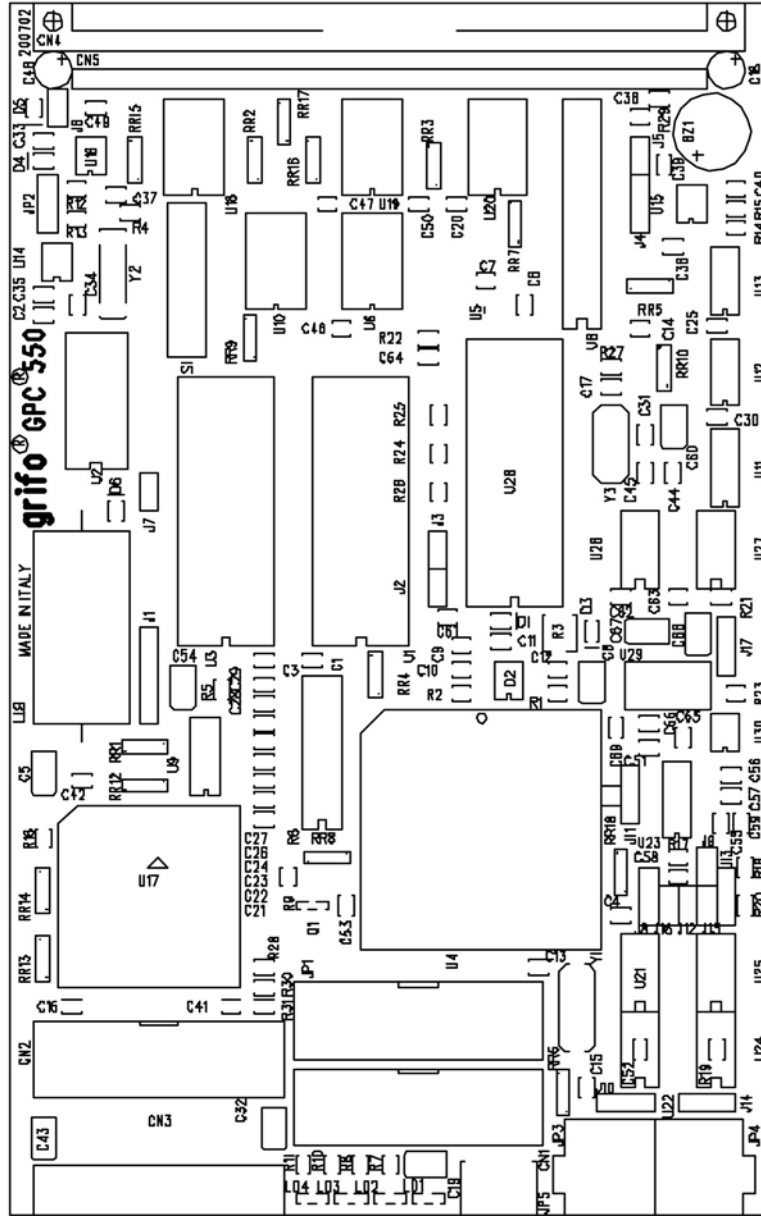


FIGURE 26: COMPONENTS MAP OF COMPONENT SIDE

JUMPERS

On GPC® 550 there are 16 jumpers and one dip switch for card configuration. Connecting these jumpers, the user can define for example the memory type and size, the peripheral devices functionality, the serial communication interface and so on. Here below is the jumpers list, location and function:

| JUMPER | N. PINS | PURPOSE |
|-----------|---------|--|
| J1 | 5 | Select memory device installed on U3. |
| J2 | 2 | Reserved. |
| J3 | 2 | Select ROM code area internal or external. |
| J4 | 3 | Matched with J5, selects memory mapping. |
| J5 | 2 | Matched with J4, selects memory mapping. |
| J7 | 2 | Connects on-board battery BT1 to back up circuitry. |
| J8 | 3 | Selects electric protocol for serial line A. |
| J9 , J15 | 2 | Connect termination and forcing circuitry for serial line A in RS 422, RS 485. |
| J10 | 3 | Selects the connection type for pin 1 of JP3. |
| J11 | 4 | Selects interrupt source for /INT0. |
| J12 , J16 | 2 | Connect serial line A, buffered in RS 232, to connector JP3. |
| J13 | 3 | Selects direction and operating mode for serial line A in RS 422, RS 485. |
| J14 | 3 | Selects the connection type for pin 1 of JP4. |
| J17 | 3 | Connects termination circuitry to CAN serial line. |
| S1.7 | 2 | Connects signal PWM1 to RS 422, RS 485 abilitation line. |

FIGURE 27: JUMPERS SUMMARIZING TABLE

The following tables describe all the right connections of GPC® 550 jumpers with their relative functions.

To recognize these valid connections, please refer to the board printed diagram (serigraph) or to figure 32 of this manual, where the pins numeration is listed; for recognizing jumpers location, please refer to figure 32 again.

The "*" denotes the default connection, or on the other hand the connection set up at the end of testing phase, that is the configuration the user receives.

2 PINS JUMPERS

| JUMPER | CONNECTION | PURPOSE | DEF. |
|-----------|---------------|---|------|
| J2 | not connected | Reserved for internal use. | * |
| | connected | Reserved for internal use. | |
| J3 | not connected | Enable acces to microcontrolloer internal code ROM. | * |
| | connected | Enable acces to on board memory devices for microcontrolloer external code ROM. | |
| J5 | not connected | Matched to J4, this jumper is used to select the memory mapping. For further information please see the paragraph “MEMORY ADDRESSES”. | * |
| | connected | | |
| J7 | not connected | Does not connect on board battery BT1 to back up circuitery. | * |
| | connected | Connects on board battery BT1 to back up circuitery. | |
| J9 , J15 | not connected | Do not connect forcing and termination circuitery to RS 485 receiver/transmitter or to RS 422 receiver of serial line A. | * |
| | connected | Connect forcing and termination circuitery to RS 485 receiver/transmitter or to RS 422 receiver of serial line A. | |
| J12 , J16 | not connected | Do not connect serial line A, buffered in RS 232, to its specific pins on JP3. | * |
| | connected | Connect serial line A, buffered in RS 232, to its specific pins on JP3. | |
| S1.7 | OFF | Does not connect signal PWM1 to RS 422, RS 485 transmitter abilitation pin. | * |
| | ON | Connecst signal PWM1 to RS 422, RS 485 transmitter abilitation pin. | |

FIGURE 28: 2 PINS JUMPERS TABLE

4 PINS JUMPERS

| JUMPER | CONNECTION | PURPOSE | DEF. |
|--------|---------------|--|------|
| J11 | not connected | Does not connect /INT0 to any interrupt source. | * |
| | position 1-2 | Connects /INT0 to CAN controller interrupt. | |
| | position 2-3 | Connects /INT0 to serial line B reception interrupt. | |
| | position 2-4 | Connects /INT0 to Real time Clock generated interrupt. | |

FIGURE 29: 4 PINS JUMPERS TABLE

3 PINS JUMPERS

| JUMPER | CONNECTION | PURPOSE | DEF. |
|--------|---|---|------|
| J4 | not connected position 1-2 position 2-3 | Matched to J5, this jumper is used to select the memory mapping. For further information please see the paragraph "MEMORY ADDRESSES". | * |
| J8 | position 1-2 position 2-3 | Configures serial line A for RS 422, RS 485 and current loop electric protocols. Configures serial line A for RS 232 electric protocol. | * |
| J10 | position 1-2 position 2-3 | Connects pin 1 of JP3 to +5 Vdc. Connects pin 1 of JP3 to GND. | * |
| J13 | position 1-2 position 2-3 | Configures serial line A for RS 485 (half duplex) electric protocol. Configures serial line A for RS 422 (full duplex or 4-wires half duplex) electric protocol. | * |
| J14 | position 1-2 position 2-3 | Connects pin 1 of JP4 to +5 Vdc. Connects pin 1 of JP4 to GND. | * |
| J17 | position 1-2 position 2-3 | Connects 120 Ω termination resistor to CAN serial line. Does not connect 120 Ω termination resistor to CAN serial line. | * |

FIGURE 30: 3 PINS JUMPERS TABLE

5 PINS JUMPERS

| JUMPER | CONNECTION | PURPOSE | DEF. |
|--------|--|---|------|
| J1 | position 1-2 and 3-4 position 2-3 and 4-5 position 3-4 | Configures U3 as 32Kbytes FLASH EPROM. Configures U3 as 32Kbytes SRAM or EEPROM. Configures U3 as 32Kbytes EPROM. | * |

FIGURE 31: 5 PINS JUMPERS TABLE

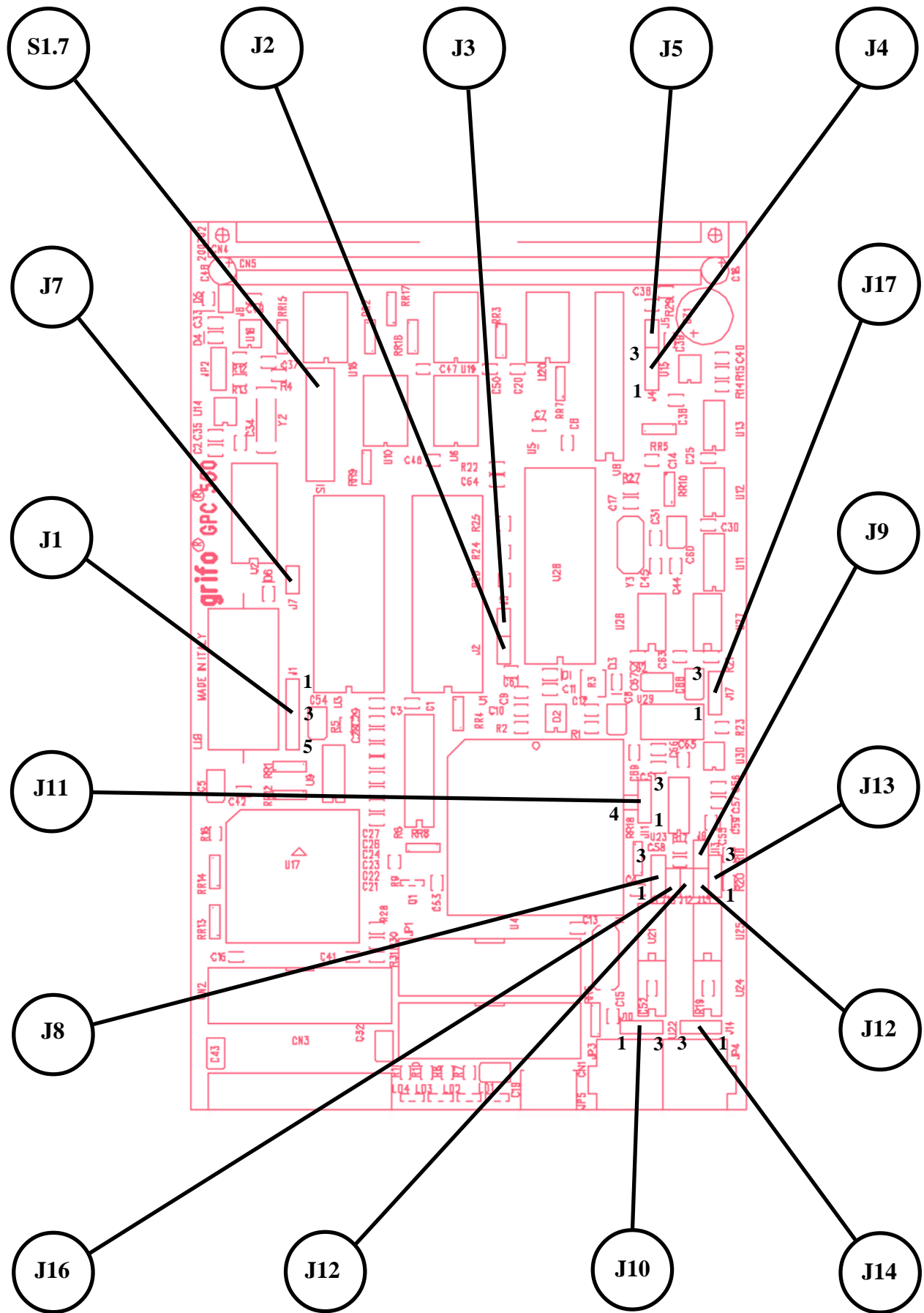


FIGURE 32: JUMPERS PLACEMENT AND NUMERATION

RESET AND POWER GOOD

GPC® 550 features two different reset sources:

- power good circuitry; it activates reset when power supply voltage goes under the threshold of 4.62 Vdc;
- external reset key, that must be connected to pin 29 C of CN4+CN5 (signal R.T. of BUS ABACO®); it can be a normally open key that connects signal R.T. to GND when pressed. Its main purpose is to exit from infinite loop conditions during debuggin or to restart the application program without interrupting power supply.

Each of the above described conditions activates the reset circuitry with correct timings (200 msec), so it restarts the execution of the program stored on EPOM U1 at address 0000H from a general reset condition.

Please remark that /RESET signal generated by the board is connected to pin 16 C or connector CN4+CN5 to reset also eventual peripheral boards connected to BUS ABACO®.

This reset circuitry assures correct working for the card and eventual electronic devices connected to it in any operating condition, especially during the critical power on and off phases.

VISUAL SIGNALATIONS

GPC® 550 features the LEDs described in the following table:

| LED | COLOUR | PURPOSE |
|-----|--------|---|
| LD1 | Green | Software managed activity LED |
| LD2 | Red | Software managed activity LED |
| LD3 | Green | Software managed activity LED |
| LD4 | Red | Displays Real Time Clock interrupt activation |

FIGURE 33: LEDs TABLE

The main function of LEDs is to inform the user about card status, with a simple visual indication and in addition to this, LEDs make easier the debug and test operations of the complete system. To recognize the LED location on the card, please refer to figure 24.

For further information please refer to paragraphs “ACTIVITY LEDS” and “REAL TIME CLOCK”.

INTERRUPTS

A remarkable feature of **GPC® 550** card is the powerful interrupt management.

Here follows a short description of which devices can generate interrupts and their modalities; for further information about interrupts management please refer to the microprocessor data sheet.

- Real Time Clock -> Generates an interrupt on CPU pin /INT0 if jumper J11 is connected in position 2-4.
- CAN controller -> Generates an interrupt on CPU pin /INT0 if jumper J11 is connected in position 2-1.
- Software serial line -> Generates an interrupt on CPU pin /INT0 if jumper J11 is connected in position 2-3.
- CPU peripherals -> Generate an internal interrupt. CPU section capable to generate such interrupt are: Timer/Counter, A/D converter, serial line and I²C line.

An interrupt manager (ICU) allows to enable, disable, mask and prioritize the interrupt sources, so the user has the possibility to respond promptly and efficiently to any external event.

POWER SUPPLY

GPC® 550 must be supplied by a +5 Vdc±5% that must be provided through specific pins of CN4+CN5.

Board layout has been designed to distribute the unique supply across the whole card; this explains directionality reported in connectors description.

Should the user decide to provide power supply through another connector, a correct working verify must be done.

For example, to supply the card through JP3 or JP4 (for examples, in networks where an unique cable carries signals and supply for all the terminals), jumpers J10 and J14 must be configured properly. An efficient filtering distributed circuitry protects the card against interference and noise from the field, improving the overall system efficiency.

Please remark that logic supply (+5 Vdc and GND) is galvanically isolated from CAN interface supply. So, signal GND must NOT be connected to CAN GND on JP5.

A/D converter section uses logic power supply refiltered and redistributed.

For shielding and tracks location reasons, ground of this section is called AGND to distinguish it from supply GND, even if they are electrically connected.

To reduce power consumption, CPU power down and idle modes can be employed.

These modalities allow to reduce the CPU working frequency and can be enabled programming the CPU internal register PCON.

The user program can reduce supply consumption up to as low as 100 mA and eventually restore the normal working mode when a specific event occurs, like an interrupt, a variation on an analog or digital input, a timeout, etc.

For further information please refer to paragraph "ELECTRIC FEATURES".

SERIAL COMMUNICATION SELECTION

Serial line B can be buffered only as RS 232 while serial line A can be buffered in RS 232, RS 422, RS 485 or Current Loop. By hardware can be selected which one of these electric standards is used, through jumpers connection (as described in the previous tables) and drivers installation. By software the serial line can be programmed to operate with all the standard physical protocols, in fact the bits per character, parity, stop bits and baud rates can be decided by setting oportunes CPU internal registers. In the following paragraphs there are all the informations on serial communication configurations.

Some devices needed for RS 422, RS 485 and Current Loop configurations are not mounted on the board in standard configuration; this is why each fist non-standard (non-RS 232) serial configuration for line A must be always performed by **grifo**® technicians. This far the User can change in autonomy the configuration following the informations below:

- HW SERIAL LINE A IN RS 232 (default configuration)

| | | | | |
|----------|---|---------------|-----|-------------|
| S 1.7 | = | indifferent | | |
| J8 | = | position 2-3 | U21 | = no device |
| J12, J16 | = | connected | U22 | = no device |
| J13 | = | indifferent | U24 | = no device |
| J9, J15 | = | not connected | U25 | = no device |

- HW SERIAL LINE A IN CURRENT LOOP (option .CLOOP)

| | | | | |
|----------|---|---------------|-----|------------------|
| S 1.7 | = | indifferent | | |
| J8 | = | position 1-2 | U21 | = no device |
| J12, J16 | = | not connected | U22 | = no device |
| J13 | = | indifferent | U24 | = driver HP 4200 |
| J9, J15 | = | not connected | U25 | = driver HP 4100 |

Please remark that Current Loop serial interface is passive, so it must be connected an active Current Loop serial line, that is a line provided with its own power supply, like described in figures 14÷16. Current Loop interface can be employed to make both point-to-point and multi-point connections through a 2-wires or a 4-wires connection.

- HW SERIAL LINE A IN RS 422 (option .RS 422)

| | | | | |
|----------|---|---------------|-----|------------------------------|
| S 1.7 | = | OFF or ON | | |
| J8 | = | position 1-2 | U21 | = driver SN 75176 or MAX 483 |
| J12, J16 | = | not connected | U22 | = driver SN 75176 or MAX 483 |
| J13 | = | position 2-3 | U24 | = no device |
| J9, J15 | = | (*) | U25 | = no device |

Status of signal PWM1 (software managed), allows to enable or disable the transmitter:

PWM1 =DIR= low level = logic state 0 -> transmitter enabled

PWM1 = DIR=high level = logic state 1 -> transmitter disabled

In point-to-point connections, signal PWM1 can be always kept low (trasmitter always enabled), while in multi-point connections transmitter must be enabled only when a transmission is requested.

- HW SERIAL LINE A IN RS 485 (option .RS 485)

| | | | | |
|----------|---|---------------|-----|------------------------------|
| S 1.7 | = | ON | | |
| J8 | = | position 1-2 | U21 | = driver SN 75176 or MAX 483 |
| J12, J16 | = | not connected | U22 | = no device |
| J13 | = | position 1-2 | U24 | = no device |
| J9, J15 | = | (*) | U25 | = no device |

In this modality the signals to use are pins 4 and 5 of connector JP3, that become transmission or reception lines according to the status of signal PWM1, managed by software, as follows:

PWM1 = DIR=low level = logic state 0 -> transmitter enabled
 PWM1 = DIR=high level = logic state 1 -> transmitter disabled

This kind of serial communication can be used for multi-point connections, in addition it is possible to listen to own transmission, so the user is allowed to verify the succes of transmission. In fact, any conflict on the line can be recognized by testing the received character after each transmission.

- (*) If using the RS 422 or RS 485 serial line, it is possible to connect the terminating and forcing circuit on the line by using J9 and J15. This circuit must be always connected in case of point-to-point connections, while in case of multi-point connections it must be connected only in the farrest boards, that is on the edges of the communication line.

During a reset or a power on, signal PWM1=DIR is at logic level high, so during these phases driver RS 485 is in reception or transmission driver RS 422 is disabled, to avoid conflicts on line.

Please remark that RS 232 communication signals available on JP4 can be used as hardware handshakes (RTS, CTS, DTR, RI, DSR, etc.) matched to communication signals of serial line A on JP3.

This allows the user to use GPC® 550 also to communicate with systems that require these signals, like for example modem, radio bridges, etc.

For further informations about serial communication please refer to the examples of figures 10÷16 and to paragraph "SOFTWARE SERIAL LINE B" of this manual.

BACK UP

On GPC® 550 is provided with a Lithium battery, called BT1, that keeps data on SRAM components and keeps the Real Time Clock counting, also when power supply fails.

Jumper J7 connects or disconnects the battery to save its duration whenever back up is not required. A second external battery, with voltage greater than the one on board, can be connected to back up circuitry through J6.

This latter is not influenced by jumper J7 and replaces completely BT1.

For the selection of the external battery features please refer to "ELECTRIC FEATURES" paragraph.

To locate the battery please refer to figure 25.

MEMORY SELECTION

On GPC® 550 can be mounted up to 97K bytes and 256 bytes of memory divided in several configurations, as described in the following table:

| NAME | DEVICE | SIZE | JUMPER CONFIGURATION |
|------|-----------------|----------------|----------------------------|
| U1 | EPROM | 32K Bytes | - |
| U2 | SRAM | 32K Bytes | - |
| U3 | EPROM | 32K Bytes | J1 in position 3-4 |
| | EEPROM | 32K Bytes | J1 in position 2-3 and 4-5 |
| | FLASH EPROM | 32K Bytes | J1 in position 1-2 and 3-4 |
| | SRAM | 32K Bytes | J1 in position 2-3 and 4-5 |
| U14 | serial SRAM+RTC | 256 Bytes | - |
| U16 | serial EEPROM | 256÷1024 Bytes | - |

FIGURE 35: MEMORY SELECTION TABLE

All the above described devices must feature a JEDEC compliant pin out except for the serial devices installed on U14 and U16 that must be requested to grifo® in the ordering phase. To determine the name of the memory devices that can be mounted, please refer to the manufacturer documentation.

GPC® 550 is delivered in its default configuration, this means 32K SRAM on U2, 512 bytes serial EEPROM on U16 and 256 bytes of SRAM+RTC on U14; any different memory configuration can be mounted by the user in autonomy or requested to grifo® in the order. Below are reported the order codes for the several optional memory configurations:

| | | |
|----------------|----|--|
| .32K | -> | 32K SRAM expansion on U3 |
| .32KMOD | -> | 32K Bytes backed SRAM on U3 |
| .32KF | -> | 32K Bytes parallel FLASH EPROM on U3 |
| .32EE | -> | 32K parallel EEPROM on U3 |
| .EE02 | -> | 2K bit (=256 Bytes) serial EEPROM on U16 |
| .EE08 | -> | 8K bit (=1K Bytes) serial EEPROM on U16 |

For further informations about memory options and their cost please contact grifo®, while to easily locate the memory devices on the board please refer to figure 25.

CAN INTERFACE

Jumper J17 connects or does not connect CAN termination resistor, as described in figure 30.

CAN bus must be a differential line with 60Ω of impedance so termination resistors must be connected to obtain this value.

This connection, in specific, must be always made in case of point-to-point communication, while in multi-point communication it must be connected only in the cards at the greatest distance, that is at the ends of the lines (please see example of figure 24).

Correct CAN termination contributes remarkably to correct communication; in fact on board interface can suppress transients and is immune against radio frequency and electromagnetic disturbs only if connection to the field is made correctly.

CAN line is galvanically isolated (as described in paragraph "POWER SUPPLY") from board supply voltage. Ground of CAN line (called CAN GND) is available on a pin of connector JP5.

This latter can be used to equilibrate difference of potentials amongst several CAN systems, but also to shield physical connection, using CAN shielded cable, to obtain the greatest protection against external noise.

SOFTWARE

A wide selection of software development tools can be obtained, allowing use of the module as a system for its own development, both in assembler and in other high level languages; in this way the User can easily develop all the requested application programs in a very short time. Generally all software packages available for the mounted microprocessor, or for the 51 family, can be used.

GET 51: it is a complete program with editor, communication driver and mass memory management for all '51 family cards. This program developed by grifo® allows to operate in the best conditions when MCS BASIC, BXC51, MDP, FMO52, etc. software tools are used. The program is menu driven and mouse driven. It is designed to run under MS-DOS but can run also in MACINTOSH environment with VIRTUAL-PC. It is delivered in MS-DOS 3 1/2 floppy disks.

µC/51: It is a comfortable, low cost, software package with a complete IDE that allows to use an editor, and ANSI C compiler, and assembler, a linker and a remote source level debugger user configurable. Sources of main libraries and remote debugger are included, and so several utility and demo programs.

MCS BASIC 553: complete development tools for MCS BASIC (interpreted BASIC language for industrial application). It needs a P.C. for console and program saving operations, while the debug, test and program operations are performed on the card. Special instructions which manage the on board peripheral devices have been added.

BXC51: cross compiler for source files written in MCS BASIC 553. It allows a considerable speed increment of the starting MCS BASIC program and it is completely executed on external P.C.

XPAS51: cross compiler for PASCAL source program, executable on P.C. with MS-DOS.

FORTH: complete software development tools to program the card with FORTH high level language. It needs a P.C. for User interface and it is really interesting for its fast execution and small size, of the generated code.

MICRO/C-51: integer cross compiler for source files in standard ANSI C. It produces a source assembly file compatible with MICRO/ASM 51 or with Intel macro relocatable assembler MCS 51.

MICRO/ASM-51: macro cross assembler available for MS-DOS operating system in absolute and relocatable version. In this relocatable version is supplied with a linker and a library manager.

MICRO/SLD-51: source level debugger and simulator. It is executed on P.C. without any additional hardware and it allows loading of HEX and SYMBOLIC files, breakpoint setting, instruction execution in trace mode, registers and memory dump, etc.

HI-TECH C: cross compiler for C source program. It is a powerful software tool that includes editor, C compiler, assembler, optimizer, linker, library, and remote symbolic debugger, in one easy to use integrated development environment.

KSC: cross compiler for C source program. It is a powerful software tool that includes editor, C compiler, assembler, optimizer, linker, library, simulator and remote symbolic debugger, in one easy to use integrated development environment for Windows.

MDP: monitor debugger program able to load and debug each HEX Intel files for 51 microprocessor family. It is provided of the standard commands available on in circuit emulator and requires only an external P.C. connected through a serial line.

RSD 553: It is a Remote Symbolic Debugger with cross assembler. It is provided of the standard commands available on in circuit emulator and requires only an external P.C. connected through a serial line. There is at high level user interface that can visualize all the processor status.

NOICE: It is a PC-hosted debugger consists of a target-specific DOS program, NOICExxx.EXE, and a target-resident monitor program. The two programs communicate via RS-232. NOICE includes: source level debug; a disassembler; a file viewer; memory display and editing; a virtually unlimited number of breakpoints; hardware-free single step; definition of symbols; the ability to record and play back files of commands; on-line help.

OPEN 51/UNI: in circuit emulator for the 51 family. It is a powerfull hardware and software tool that includes: source level debugging and symbolic debugging; project management; built-in multi-file editor; execution of external compilers; debugging of several modules at the same time; built-in disassembler; source level step and trace functions; animate functions; inserting and deleting of breakpoints on the source level; watching and modifying variables on symbol and absolute level.

BASCOM 8051: cross compiler for BASIC source program. It is a powerful software tool that includes editor, BASIC compiler and simulator included in an easy to use integrated development environment for Windows. Many memory models, data types and direct use of hardware resource instructions are available.

FM052: monitor debugger program able to load and debug each HEX Intel files for 51 microprocessor family. It is provided of the standard commands available on in circuit emulator and requires only an external P.C. connected through a serial line. It is preconfigured to work directly with BASCOM 8051 and GET51 software tools.

It is also capable to program on FLAH EPROM the user application for debugging and execute it in autorun mode.

DDS C: low cost ross compiler for C source program. It is a powerful software tool that includes editor, C compiler (integer), assembler, optimizer, linker, library, and remote symbolic debugger, in one easy to use integrated development environment. There are also included the library sources and many utilities.

LADDERWORK: It is a easy to use system to generate automation application using the very famouts contact logic. It features a graphic editor to place and connect components that refer to hardware resources (like digital I.O, counters, A/D, etc.) like on an electric diagram and define their properties, and efficent compiler to create the executable code and an utility to download it. Integrated IDE makes comfortable use of these tools. Delivered in a CD for Windows with user manual and hardware key.

ADDRESSES AND MAPS

INTRODUCTION

In this chapter are reported all information about card use, related to hardware features of **GPC® 553**. For example, the registers addresses, the memory allocation and peripheral devices software management are described below.

ADDRESSES

The card devices addresses are managed from a control logic, realized with programable logic. This control logic allocates memory and peripheral devices with very low power consumption, in two separate manners.

The 80C552 microprocessor addresses 64K bytes of code memory and 64K bytes of data memory and the control logic provides on board memory and peripheral devices allocation inside these addresses spaces.

Control logic sets size, type and addresses of memory device through jumpers J4 and J5.

It sets I/O addresses of external devices always in locations that avoid conflicts with microprocessor internal devices.

Summarizing the control logic allocates:

- Up to 32K bytes of EPROM on U1
- Up to 32K bytes of SRAM/EEPROM on U2
- Up to 32K bytes of SRAM/EEPROM/EPROM on U3
- **BUS ABACO®**
- S1 configuration Dip Switch
- Activity LEDs
- Buzzer
- Digital I/O controller PPI 82c55
- CAN controller

The addresses listed here and in the following paragraphs cannot be reallocated.

Other devices are managed always by control logic but they are not allocated in memory space in fact these devices are driven through CPU I/O lines with a synchronous communication.

MEMORY CONFIGURATIONS

On the **GPC® 550** three different memory configurations can be selected. The configuration must be selected (with jumpers J4 and J5) both according to used software tools and user requests and/or application features.

Please remark that position 1-2 of jumper J4 is not described because reserved for future expansions. The following figures describe available memory configurations, distinguishing between code area and data area, accessible respectively with CPU instructions MOV_C and MOV_X.

MEMORY CONFIGURATION 0

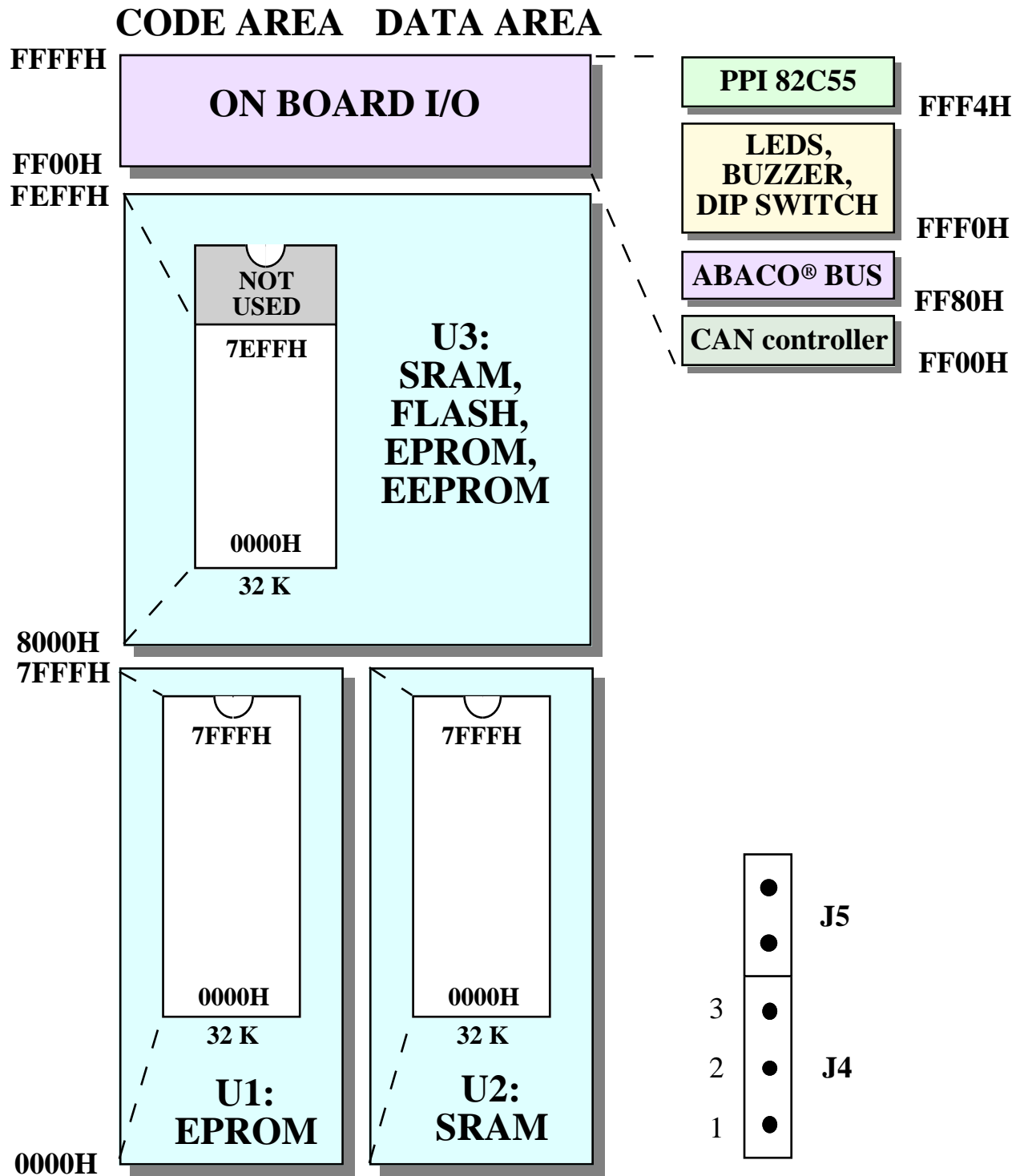


FIGURE 37: MODE 0 MEMORY CONFIGURATION (BASIC+DEBUG)

Used by software tools as: BASIC 550; BXC51; HI TECH C 51; DDS MICRO C 51; SYS51PW; SYS51CW; BASCOM 8051; µC/51; etc.

MEMORY CONFIGURATION 1

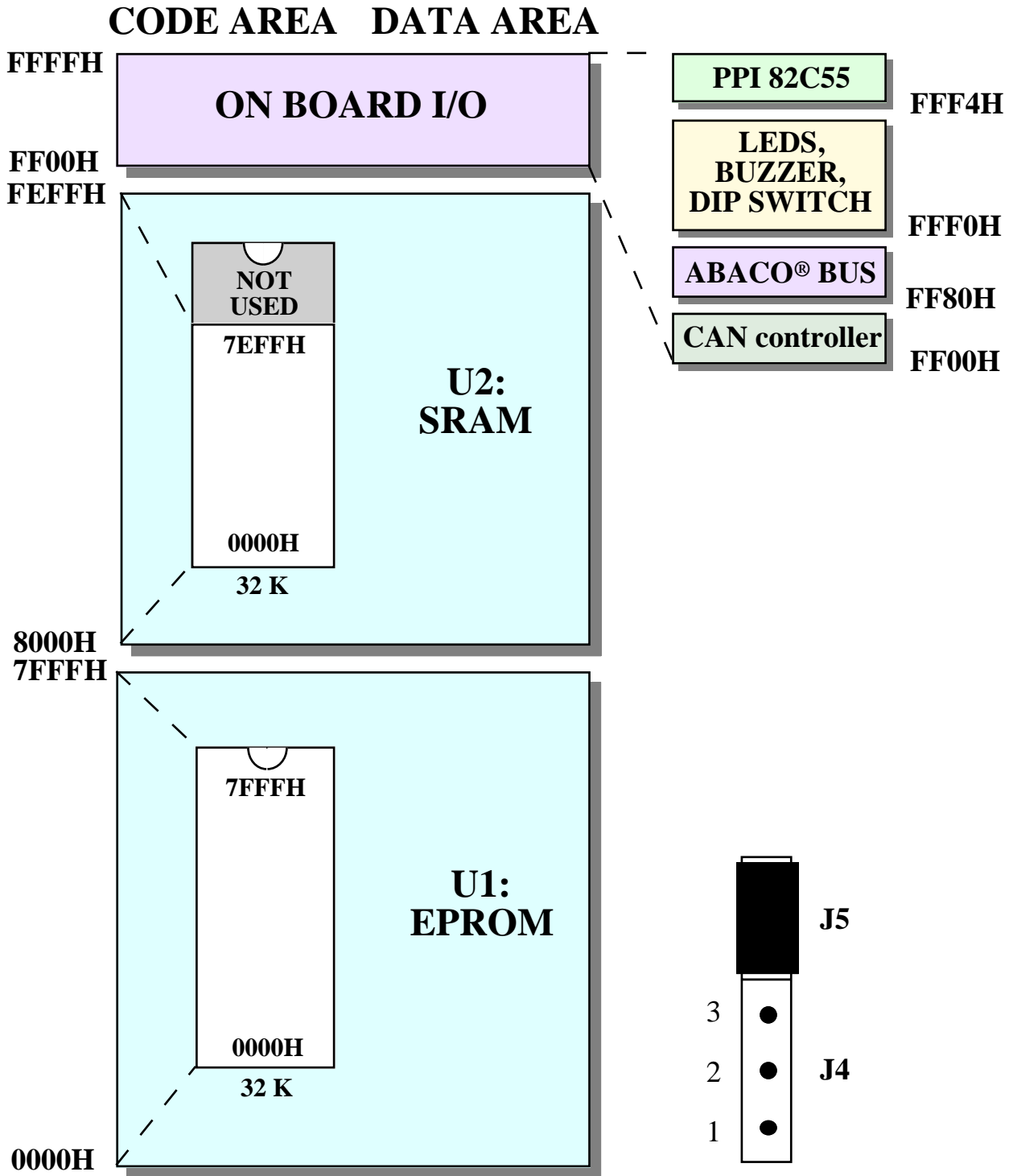


FIGURE 38: MODE 1 MEMORY CONFIGURATION

Used by software tools as: HI TECH C 51; DDS MICRO C 51; SYS51PW; SYS51CW; BASCOM 8051; µC/51; etc.

MEMORY CONFIGURATION 3

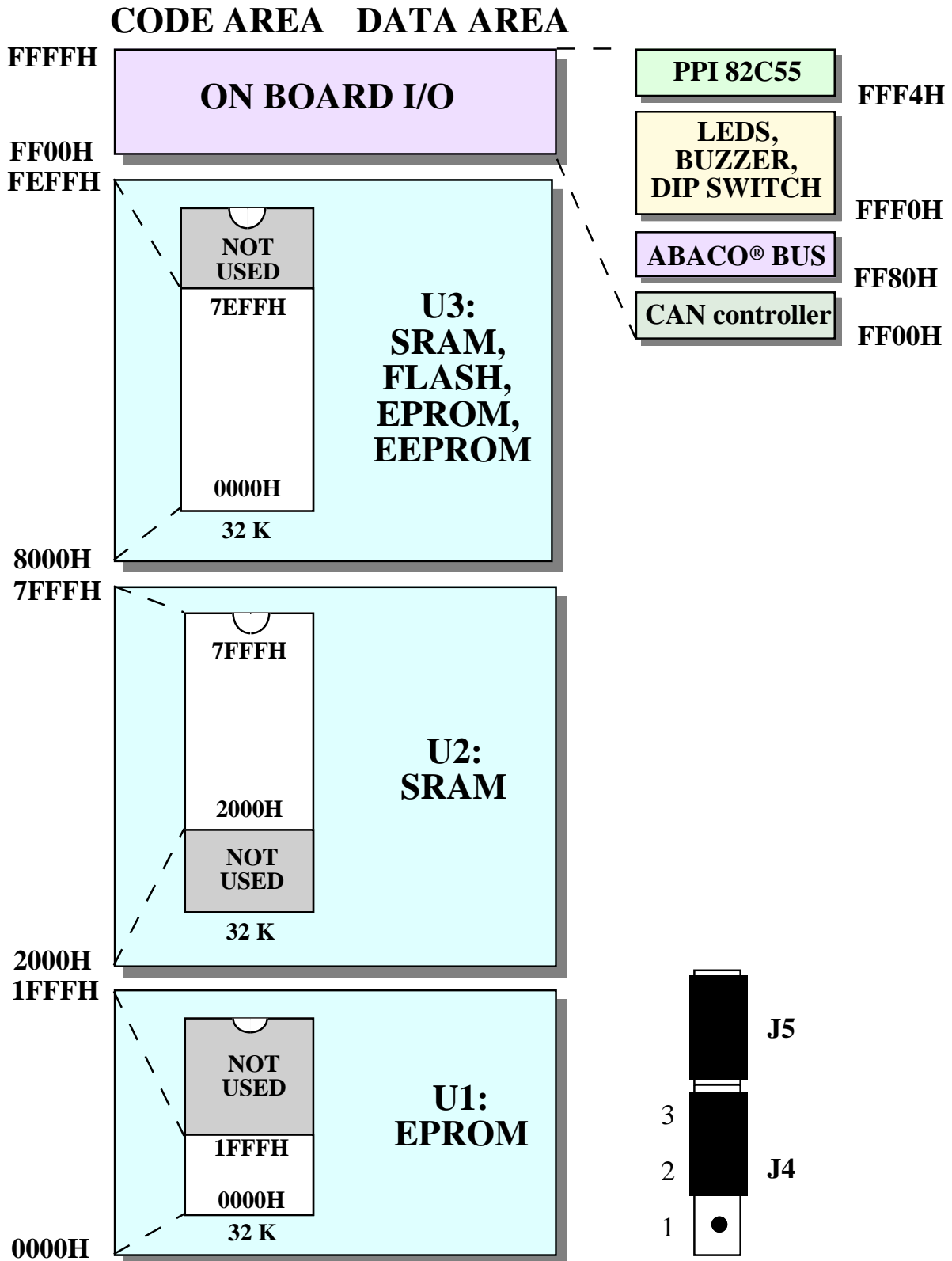


FIGURE 39: MODE 3 MEMORY CONFIGURATION

Used by software tools as: MD/P; FMO52; LUCIFER per HI TECH C 51; DDS MICRO C 51; SYS51PW; SYS51CW; BASCOM 8051; µC/51; etc.

BUS ABACO® MAPPING

GPC® 550 control logic manages also **BUS ABACO®** addressing; as shown in figure 40, it is available starting from BUS addresses for 112 bytes of extension.

Accessing any address in this range enables signal /IORQ and all the other control signals of CN4+CN5.

On ly least significant byte of I/O address is used when addressing peripherals cards, because **BUS ABACO®** employs only 8 bits for addressing and 8 bits for data.

I/O ADDRESSES

I/O addresses are located in the last 256 bytes of the 64K bytes microprocessor addressing space, to avoid conflict problems.

Next table shows addresses, meanings and direction of peripheral devices registers (only the external ones to microprocessor):

| DEVICE | REGISTER | ADDRESS | R/W | MEANING |
|--------------------------------|----------|-------------|-----|--|
| CAN controller SJA 1000 | CAN | FF00H÷FF7FH | R/W | Register for management of UART CAN SJA 1000 in BasicCAN or PelloCAN modality (registers are the same as reported in the component data sheet, plus an <u>offset of FF00H</u>). |
| ABACO® BUS | BUS | FF80H÷FFEFH | R/W | ABACO® BUS management addresses. |
| Activity LED | LED | FFF1H | W | Activity LEDs LD1, LD2 and LD3 management register. |
| BUZZER | BUZ | FFF1H | W | Buzzer BZ1 management register. |
| DIP SWITCH | DIP | FFF3H | R | Dip switch S1 acquisition register. |
| PPI 82C55 | PA | FFF4H | R/W | Port A data register |
| | PB | FFF5H | R/W | Port B data register |
| | PC | FFF6H | R/W | Port C data register |
| | RC | FFF7H | R/W | Command and control register |

FIGURE 40: I/O ADDRESSES TABLE

For further information about register meanings, please refer to next paragraph called "PERIPHERAL DEVICES SOFTWARE DESCRIPTION".

Please remark that the above table reports the description of external devices registers only, for a description of microcontroller internal registers please refer to manufacturer documentation.

PERIPHERAL DEVICES SOFTWARE DESCRIPTION

In the previous paragraphs are described the external registers addresses, while in this one there is a specific description of registers meaning and function (please refer to I/O addresses table, for the registers names and addresses values). For a more detailed description of the devices, please refer to manufacturing company documentation; for microprocessor internal peripheral devices, not described in this paragraph, refer to appendix B. In the following paragraphs the **D7÷D0** and **.0÷7** indications denote the eight bits of the combination used in I/O operations.

SOFTWARE I2C BUS

Software I²C BUS line installed on **GPC® 550** is made using two bidirectional I/O lines of CPU:

| | | | |
|-------------|----|-------------------|-----------------|
| P3.3 | -> | line DATA | = SW SDA |
| P3.5 | -> | line CLOCK | = SW SCL |

they can be easily managed by the user to obtain sequences and timings defined by this standard. More easily, the user can use the high level procedures provided with programmin package that perform complete management of protocol just passing them few parameters.

On software I²C BUS line devices at slave addresses A0H and A8H are already installed, like described in paragraphs “SERIAL SRAM+RTC” and “SERIAL EEPROM”.

ACTIVITY LEDS

Control logic allows to manage three activity LEDs, using as many bits of LED register:

| | | |
|------------------|----|----------------|
| LED.7 = 0 | -> | LD1 OFF |
| LED.7 = 1 | -> | LD1 ON |
| LED.6 = 0 | -> | LD3 OFF |
| LED.6 = 1 | -> | LD3 ON |
| LED.5 = 0 | -> | LD2 OFF |
| LED.5 = 1 | -> | LD2 ON |

LED register shares its address with other on board peripherals, so each read/write operation to this register affects the programming of these other devices.

LED register is set to 0 after reset or power on, so during these phases LEDs are all OFF.

BUZZER

Buzzer BZ1 is software managed through bit D0 of register BUS:

BUZ.0 = 0 -> **BZ1 OFF**
BUZ.0 = 1 -> **BZ1 ON**

Main purpose of buzzer is acoustic signalation of application program status conditions to obtain attention from the user (for example to send an alert, etc).

BUZ register shares its address with other on board peripherals, so each read/write operation to this register affects the programming of these other devices.

BUZ register is set to 0 after reset or power on, so during these phases buzzer is OFF.

SERIAL EEPROM

For software management of serial EEPROM module of U16, please refer to specific documentation or to demo programs supplied with the card. The User must realize a serial communication with I²C bus standard protocol, through two I/O microprocessor pins. The first 32 bytes of serial EEPROM are reserved for software tools use, so they can't be neither read nor written by User program.

The only necessary information is the electric connection:

DATA signal (SW SDA) -> **P3.3** of CPU
CLOCK signal (SW SCL) -> **P3.5** of CPU

Signals **A0,A1,A2** of slave address are connected to the following logic levels: **0, 0, 1**.

Logic status 0 means logic status low (=0 V), while logic status 1 means logic status high (=5 V). For further information about port management modalities, please refer to CPU technical documentation.

EEPROM management lines are set to 1 after reset or power on.

DIP SWITCH S1

The on board S1 Dip Switch status can be obtained by software, through a simple "read operation" at the DIP register address.

The correspondence between register bits and Dip Switch is as follows:

DIP.7 -> **dip switch S1.8**
DIP.6 -> **0**
DIP.5 -> **dip switch S1.6**
DIP.4 -> **dip switch S1.5**
DIP.3 -> **dip switch S1.4**
DIP.2 -> **dip switch S1.3**
DIP.1 -> **dip switch S1.2**
DIP.0 -> **dip switch S1.1**

Reading DIP register by software, the user obtains a complemented combination, in fact "ON" position corresponds to **0** logic status and "OFF" position corresponds to **1** logic status. Dip switch 8 of S1 features the RUN (ON) and DEBUG (OFF) function, specific for some software packaged of **grifo®**.

To easily locate dip switch S1 please refer to figures 25 and 26.

BACKED SRAM + SERIAL RTC

The U14 SRAM module, can be provided with on board Lithium battery and with Real Time Clock which manages time (hours, minutes, seconds) and date (day, month, year, day of the week).

RTC section can also generate periodic interrupts whose period can be programmed by the user, so it can be used to awaken CPU from low consumption working modes.

For software management of serial SRAM+RTC module of U14, please refer to specific documentation or to demo programs supplied with the card. The User must realize a serial communication with I²C bus standard protocol, through two I/O microprocessor pins. The only necessary information is the electric connection:

DATA signal (SW SDA) -> **P3.3** of CPU
CLOCK signal (SW SCL) -> **P3.5** of CPU

Signal **A0** is connected to logic level **0**, so its slave address is **A0H**.

As the communication signals are used both for RAM+RTC and EEPROM, if U14 is mounted then a serial EEPROM with a maximum size of 1024 bytes (24C08) can be installed on U16.

CPU INTERNAL PERIPHERALS

Registers description and purpose for all internal peripherals (ADC, TMR CNT, ICU, UART, I2C BUS HW, etc.) is available in the manufacturer data sheet.

Please refer to chapter "BIBLIOGRAPHY" and to appendix B of this manual to easily locate such documentation.

RS 422-485 COMMUNICATION DIRECTION

As described in paragraph “SERIAL COMMUNICATION SELECTION”, the RS 422 or RS 485 communication direction is enabled by software, driven by a signal called DIR which is connected to signal PWM1 of CPU.

Internal register PWM1 can set the signal, to control the communication as follows:

Point-to-point RS 422 communication: both transmitter and receiver are enabled

- by hardware it is enough to set dip switch S1.7 OFF, to disconnect PWM1 signal from DIR signal and so to keep transmission enabled;
- by software no management is required;

Network RS 422 communication: transmitter is enabled in transmission, receiver is always enabled

- by hardware it is enough to set dip switch S1.7 ON, to connect PWM1 signal from DIR signal;
- by software transmitter management is made as follows:

| | | | |
|------------------------|----------------------|----|----------------------|
| register PWM1 = 00H -> | DIR = logic status 0 | -> | transmitter enabled |
| register PWM1 = FFH -> | DIR = logic status 1 | -> | transmitter disabled |

Network RS 485 communication: transmitter is enabled in transmission, receiver is always enabled, communication is half duplex

- by hardware it is enough to set dip switch S1.7 ON, to connect PWM1 signal from DIR signal;
- by software transmitter management is made as follows:

| | | | |
|------------------------|----------------------|----|--------------|
| register PWM1 = 00H -> | DIR = logic status 0 | -> | reception |
| register PWM1 = FFH -> | DIR = logic status 1 | -> | transmission |

Please remark that when S1.7 is ON, DIR signal is connected to PWM1 signal so this latter cannot be used for other purposes.

After a reset or a power on, PWM1 = DIR is at logic level high, so transmission is disabled, to avoid interference in the line.

Please refer to specific technical documentatio for setting register PWM1.

SOFTWARE SERIAL LINE B

Serial line B of GPC® 550 is a software serial line, in fact it is made using two CPU I/O signals electrically buffered in RS 232. The I/O signals are:

| | | | |
|----------------------|----|-----------------------|-----------------------------|
| P3.4 (output) | -> | line TXB RS232 | |
| P3.2 (input) | -> | line RXB RS232 | (if J11 is in position 2-4) |

In conformance to standard RS 232, logic status 0 of pins is the positive status (+9 V) of signal, while logic status 1 is negative status (-9 V).

Serial B management must be done completely by the application program, that must create the correct time sequence on pin P3.4 for transmission and examine pin P3.2 for reception.

By means to simplify such management it is better to use an internal timer for time base and use interrupt /INT0 to signal automatically the beginning of a character in reception.

The user can also take advantage of some software packages (like for example **BASCOM 8051** or **BASIC 550**) that support serial software management with high level instructions; this allows to send and receive characters, using preset physical protocol, without any direct interaction with I/O lines and timing problems.

For further information about PORT signals management, please refer to CPU technical documentation. After a reset or a power on, both signals of software serial B are set to logic level high.

PPI 82C55

This external peripheral device is managed through 4 registers: one status register (CNT) and three data registers (PDA, PDB, PDC). The data registers are available both for read operation (to obtain signal status) and for write operation (to set signal status) with the correspondence described in figure 23. The PPI 82C55 can work in three different modes:

MODE 0 = it provides two 8 bits bidirectional ports (A,B) and two 4 bits bidirectional ports (C LOW, C HIGH); output signals are latched and input signals are not latched; no handshake signals are provided.

MODE 1 = it provides two 12 bits ports (A+C LOW and B+C HIGH) where ports A and B are used as 8 I/O lines and port C are used as 4 handshake lines. Both inputs and outputs are latched.

MODE 2 = it provides a 13 bits port (A+C_{3÷7}) where port A is used as 8 I/O lines and the 5 bits of port C are used as handshake, and a 11 bits port (B+C_{0÷2}) where port B is used as 8 I/O lines and the 3 bits of port C are used as handshakes. Both inputs and outputs are latched.

The device is programmed writing an 8 bits word in the status register CNT, with the following bit meaning:

CNT = SF M1 M2 A CH M3 B CL

where

SF = mode Set Flag: if activated (1) the device is enabled for standard I/O operation

M1 M2 = mode selection:

0 0 = mode 0

0 1 = mode 1

1 X = mode 2

A = port A direction: 1=input; 0=output

CH = port C HIGH direction: 1=input; 0=output

M3 = mode selection: 1=mode 1; 0=mode 0

B = port B direction: 1=input; 0=output

CL = port C LOW direction: 1=input; 0=output

After Reset or power on PPI 82C55 is programmed in mode 0 with all three ports in input; in this way any connection of PPI 82C55 signals can be used without conflict problems.

I/O SIGNALS OF CPU

Microcontroller P80C552, installed on **GPC® 550**, features three 8 bit ports (Port 1, 4 and 5) totalizing 24 digital I/O signals.

Many of these signals are physically multiplexed inside the microprocessor and so can perform different tasks according to their software programming.

The user can decide without limitations the function of signals connected to CN1 and JP1, while must not absolutely program Port 0 and 2.

Remaining Port 3 is dedicated to software I²C BUS and serial line, so it must be programmed carefully.

Wrong programming or initialization of Port 0, 2 or 3 can cause incorrect working or hang of application program.

For further information about PORT signals management, please refer to CPU technical documentation. After a reset or a power on, all Port signals set to logic level high as inputs.

CAN CONTROLLER

As shown in table of figure 41, CAN controller **SJA 1000** is managed through a set of status and/or command registers described in detail in appendix B of this manual and used in the examples delivered with the board.

This paragraph reports only additional information to use correctly these registers.

- 1) Communication Bit Rate, as can be seen from information in appendix B, is calculated with following formula:

$$\text{BAUD RATE} = \text{Freq} / 2 * (\text{BRP} + 1) * (3 + \text{TSEG1} + \text{TSEG2})$$

where:

- Freq = CAN controller clock frequency in Hz (24000000 for **GPC® 550**).
- BRP = Value of bit **BRP.x** or **Bus Timing Register 0** (BTR0, address **FF06H**).
- TSEG1 = Value of bit **TSEG1.x** or **Bus Timing Register 1** (BTR1, address **FF07H**).
- TSEG2 = Value of bit **TSEG2.x** or **Bus Timing Register 1** (BTR1, address **FF07H**).

- 2) To interface correctly CAN controller **SJA 1000** and line driver **82C250**, it is essential to program **Output Control Register** (OCR, address **INDPCS6 + 8**) with value **FA Hex**; this configures the device for "Normal output mode", with outputs TX0 and TX1 in "Push Pull".

- 3) The following figure shows the flow chart of suggested initialization for CAN controller **SJA 1000**: it is easy to see that there is no initialization for interrupt. To eventually manage them, it is essential to program opportunely the bits of control register (CR, address **INDPSC6 + 0**).

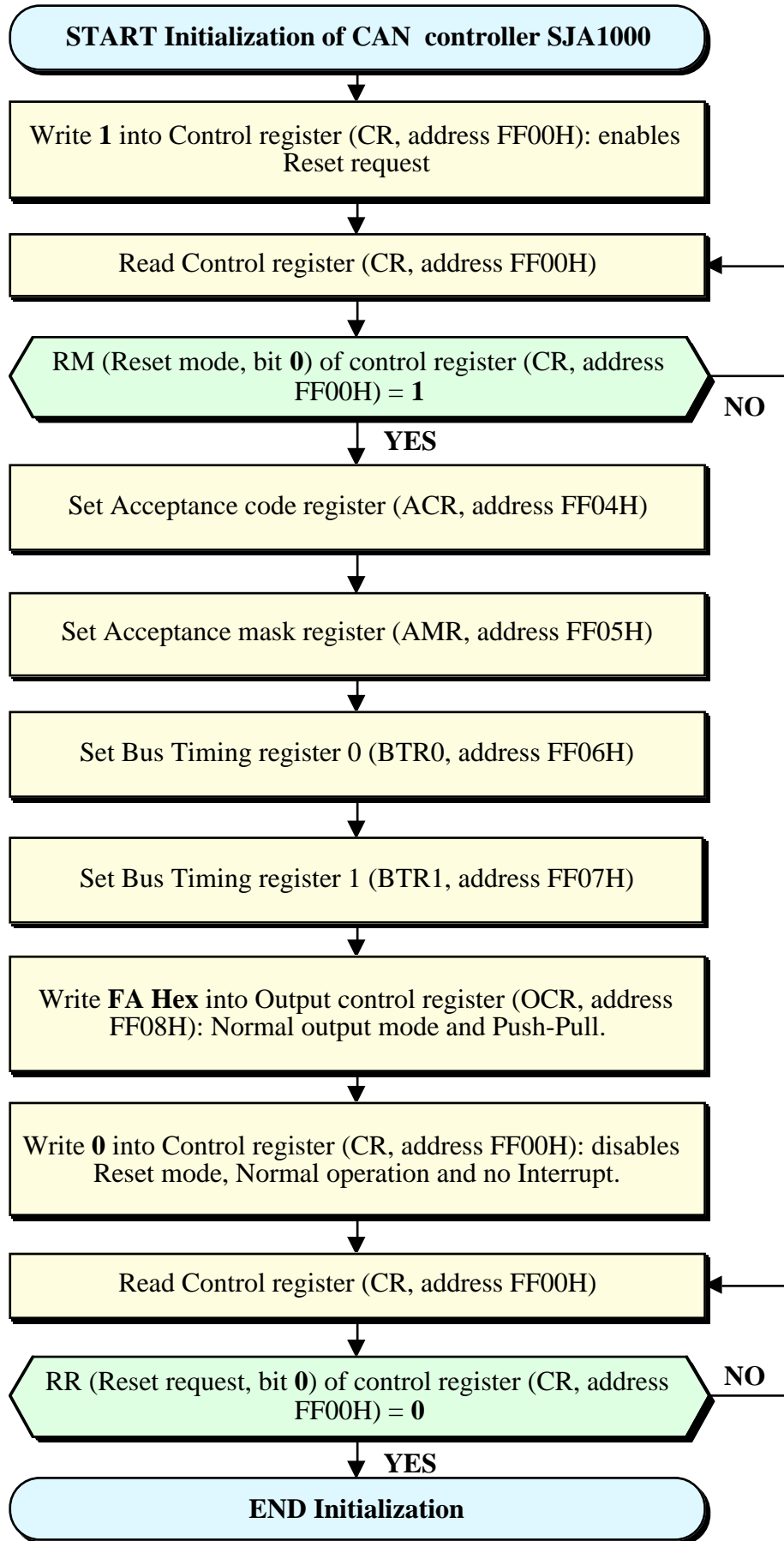


FIGURE 41: CAN CONTROLLER INITIALIZATION FLOW CHART

EXTERNAL CARDS

GPC® 550 can be connected to a wide range of block modules and operator interface system produced by **grifo®**, or to many system of other companies. The on board resources can be expanded with a simple connection to the numerous peripheral **grifo®** boards, both intelligent and not, thanks to its standard **ABACO®** BUS connector. Even cards with **ABACO®** I/O BUS can be connected, by using the proper mother boards. Hereunder some of these cards are briefly described; ask the detailed information directly to **grifo®**, if required.

OBI 01 - OBI 02

Opto BLOCK Input NPN-PNP

Interface between 16 NPN, PNP optocoupled and displayed input lines, with screw terminal and **Abaco®** standard I/O 20 pins connector; power supply section; connection for DIN Ω rails.

OBI N8 - OBI P8

Opto BLOCK Input NPN-PNP

Interface between 8 NPN, PNP optocoupled and displayed input lines, with screw terminal and **Abaco®** standard I/O 20 pins connector; power supply section; connection for DIN Ω rails.

TBO 01 - TBO 08

Transistor BLOCK Output

Interface for **ABACO®** standard I/O 20 pins connector; 16 or 8 transistor output lines 45 Vdc 3 A open collector; screw terminal; optocoupled and displayed lines; connection for DIN 247277-1 and 3 rails.

RBO 01

Relé BLOCK Output

Interface for **ABACO®** standard I/O 20 pins connector; 8 displayed 5A or 10A relays; screw terminal; connection for DIN Ω rails.

RBO 08 - RBO 16

Relé BLOCK Output

Interface for **ABACO®** standard I/O 20 pins connector; 8 or 16 displayed Relays 3A with MOV; screw terminal; connection for DIN Ctype and Ω rails.

KDL X24 - KDF 224

Keyboard Display LCD 2,4 rows 24 keys

Interface with Fluorescent or LCD display, LEDs backlit, 20x2 or 20x4 characters; up to 24 keys matrix keyboard connector. It is directly driven by a 20 pins **ABACO®** I/O standard connector; High level languages supported; standard pinout for telephone keyboard.

XBI R4 - XBI T4

miXed BLOCK Input-Output

Interface for **ABACO®** standard I/O 20 pins connector; 4 Relays 3A with MOV or 4 optocoupled Transistors 3A open collectors; 4 input lines optocoupled; screw terminal; connection for DIN Ctype and Ω rails.

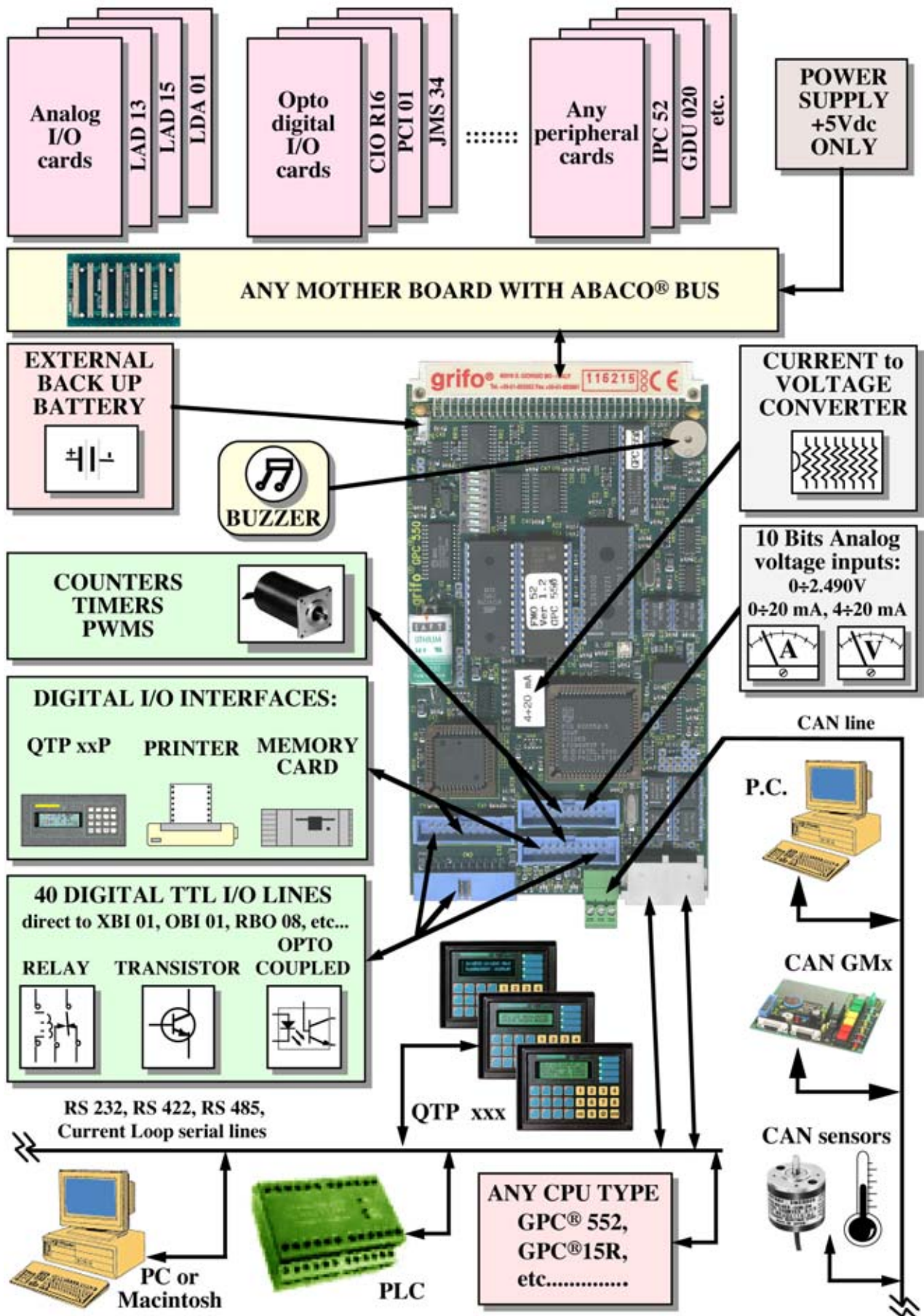


FIGURE 42: POSSIBLE CONNECTIONS DIAGRAM

FBC - WIRE TO CARD

Flat Block Contact

This interconnection system "wire to board" allows the connection to many type of flat cable connectors to terminal for external connections. Connection for DIN Ω rails.

XBI 01

miXed BLOCK Input-Output

Interface for **ABACO**[®] standard I/O 20 pins connector; 8 transistor output lines 45 Vdc 3A; 8 input lines; screw terminal; optocoupled and displayed I/O lines; connection for DIN 247277-1 and 3 rails.

QTP 24 - QTP 24P

Quick Terminal Panel 24 keys with Parallel interface

Intelligent user panel equipped with Fluorescent or LCD display, LEDs backlit, 20x2 or 20x4 characters; RS 232, RS 422, RS 485 or current loop serial line; serial E2 for set up and message. Possibility of re-naming keys, LEDs and panel name by inserting label with new name into the proper slot; 24 Keys and 16 LEDs with blinking attribute and buzzer manageable by software; built in power supply; RTC option, reader of magnetic badge and relay. The QTP 24P is low cost no intelligent (passive) version. It is directly driven from 16 TTL I/O lines; high level languages supported.

QTP G28

Quick Terminal Panel - LCD Graphic, 28 keys

LCD display 240x128 pixels, CFC backlit; Optocoupled RS 232 line and additional RS 232/422/485/ C. L. line; CAN line controller; E² for set up; RTC and RAM lithium backed; primary graphic object; possibility of re-naming keys, LEDs and panel name; 28 keys and 16 LEDs with blinking attribute and buzzer manageable by software; Buzzer; built-in power supply; reader of magnetic badge and relay option.

DEB 01

Didactic Experimental Board

Supporting card for 16 TTL I/O lines use. It includes: 16 keys, 16 LEDs, 4 digits, 16 keys matrix keyboard, Centronics printer interface, LCD display and fluorescent display interface, **GPC**[®] 68 I/O connector, field connection with screw terminal.

ABB 03

ABACO[®] Block BUS 3 slots

3 slots **ABACO**[®] mother board; 4 TE pitch connectors; **ABACO**[®] I/O BUS connector; screw terminal for power supply; connection for DIN C type and Ω rails.

ABB 05

ABACO[®] Block BUS 5 slots

5 slots **ABACO**[®] mother board with power supply. Double power supply built in; 5Vdc 2,5A section for powering the on board logic; second section at 24Vdc 400mA galvanically coupled, for the optocoupled input lines. Auxiliary connector for **ABACO**[®] I/O BUS. Connection for DIN Ω rails.

MCI 64

Memory Cards Interfaces 64 MBytes

Interfacing card for managing 68 pins PCMCIA memory cards, it is directly driven from any **ABACO**[®] I/O standard connector; High level languages GDOS supported.

IAC 01

Interface Adapter Centronics

Interface between **ABACO**® standard I/O 20 pins connector and D 25 pins connector with Centronics standard pin out.

IBC 01

Interface Block Communication

Conversion card for serial communication, 2 RS 232 lines; 1 RS 422-485 line; 1 optical fibre line; selectable DTE/DCE interface; quick connection for DIN 46277-1 and 3 rails.

OBI N8 - OBI P8

Opto BLOCK Input NPN-PNP

Interface between 8 NPN, PNP optocoupled and displayed input lines, with screw terminal and **ABACO**® standard I/O 20 pins connector; power supply section; connection for DIN Ω rails.

TBO 01 - TBO 08

Transistor BLOCK Output

Interface for **ABACO**® standard I/O 20 pins connector; 16 or 8 transistor output lines 45 Vdc 3 A open collector; screw terminal; optocoupled and displayed lines; connection for DIN 247277-1 and 3 rails.

RBO 08 - RBO 16

Relé BLOCK Output

Interface for **ABACO**® standard I/O 20 pins connector; 8 or 16 displayed Relays 3A with MOV; screw terminal; connection for DIN Ctype and Ω rails.

FBC 20 - FBC 120

Flat Block Contact 20 vie

Interfaccia tra 2 o 1 connettori a perforazione di isolante (scatolino da 20 vie maschi) e la filatura da campo (morsettiere a rapida estrazione). Attacco rapido per guide tipo DIN 46277-1 e 3.

IPC 52

Intelligent Peripheral Controller, 24 analogic input

This intelligent peripheral card acquires 24 independent analogic input lines: 8 PT 100 or PT 1000 sensors, 8 J,K,S,T termocouples, 8 analog input ± 2 Vdc or $4 \div 20$ mA; 16 bits + sign A/D section; 0.1 °C resolution; 32K RAM for local data logging; buzzer; 16 TTL I/O lines; 5 or 8 conversion per second; facility of networking up to 127 IPC 52 cards using serial line. BUS interfacing or through RS 232, RS 422, RS 485 or current loop line. Only 5Vdc power supply.

ADC 812

Analog to Digital Converter, 12 bits, multi range

DAS (Data Acquisition System) multi range 8 channels 12 bit A/D conversion lines; track and hold; 6 μ s conversion time; range ± 10 , ± 5 , +10, +5Vdc or $0 \div 20$, $4 \div 20$ mA; analog inputs connections through quick terminal screw connectors; **ABACO**® I/O BUS interface; direct mounting for DIN 247277-1 and 3 rails; 4 type dimension.

DAC 212

Digital to Analog Converter 12 bits, multi range

Digital to Analog converter; multi range 2 channels 12 bits ± 10 , +10 Vdc output; analog outputs connections through quick terminal screw connectors; **ABACO**® I/O BUS interface; direct mounting for DIN 247277-1 and 3 rails; 4 type dimension.

BIBLIOGRAPHY

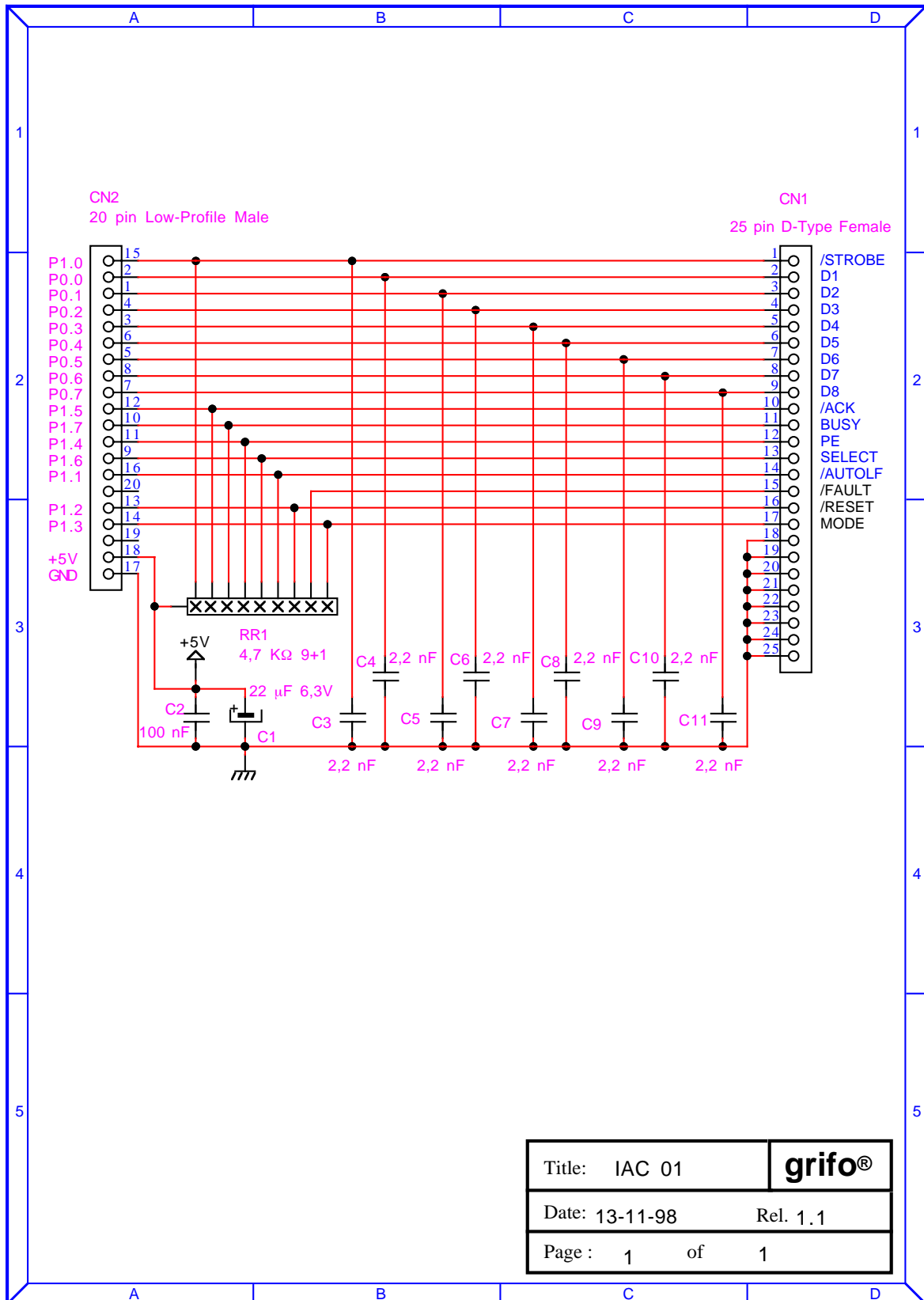
In this chapter there is a complete list of technical books, where the user can find all the necessary documentations on the components mounted on **GPC® 550**.

| | |
|--------------------------------|---|
| Manual ATMEL: | <i>Non volatile memory</i> |
| Manual HEWLETT PACKARD: | <i>Optoelectronics Designer's Catalog</i> |
| Manual NATIONAL SEMICONDUCTOR: | <i>Linear Databook - Volume 1</i> |
| Manual NEC: | <i>Microprocessors and Peripherals - Volume 3</i> |
| Manual NEC: | <i>Memory Products</i> |
| Manual NEWPORT: | <i>DC-DC Converters</i> |
| Manual MAXIM: | <i>New Releases Data Book - Volume IV</i> |
| Manual MAXIM: | <i>New Releases Data Book - Volume V</i> |
| Manual PHILIPS: | <i>80C51 - Based 8-Bit Microcontrollers</i> |
| Manual PHILIPS: | <i>IC12 - I²C bus</i> |
| Manual PHILIPS: | <i>Application notes and development tools for 80C51 microcontrollers</i> |
| Manual SGS-THOMSON: | <i>Programmable Logic Manual GAL Products</i> |
| Manual TEXAS INSTRUMENTS: | <i>The TTL Data Book - SN54/74 Families</i> |
| Manual TEXAS INSTRUMENTS: | <i>RS-422 and RS-485 Interface Circuits</i> |
| Manual TOSHIBA: | <i>Photo couplers Data Book</i> |
| Manual XICOR: | <i>Data Book</i> |

Please connect to the manufactures Web sites to get the latest version of all manuals and data sheets.

APPENDIX A: ELECTRIC DIAGRAMS

This chapter shows the electric diagram of the most frequently used interfaces for **GPC® 550**. Every one of these interfaces can be made by the User in autonomy, while only few of them are **grifo®** standard boards and can be ordered.



| | |
|----------------|----------|
| Title: IAC 01 | grifo® |
| Date: 13-11-98 | Rel. 1.1 |
| Page : 1 | of 1 |

FIGURE A1: IAC 01 ELECTRIC DIAGRAM

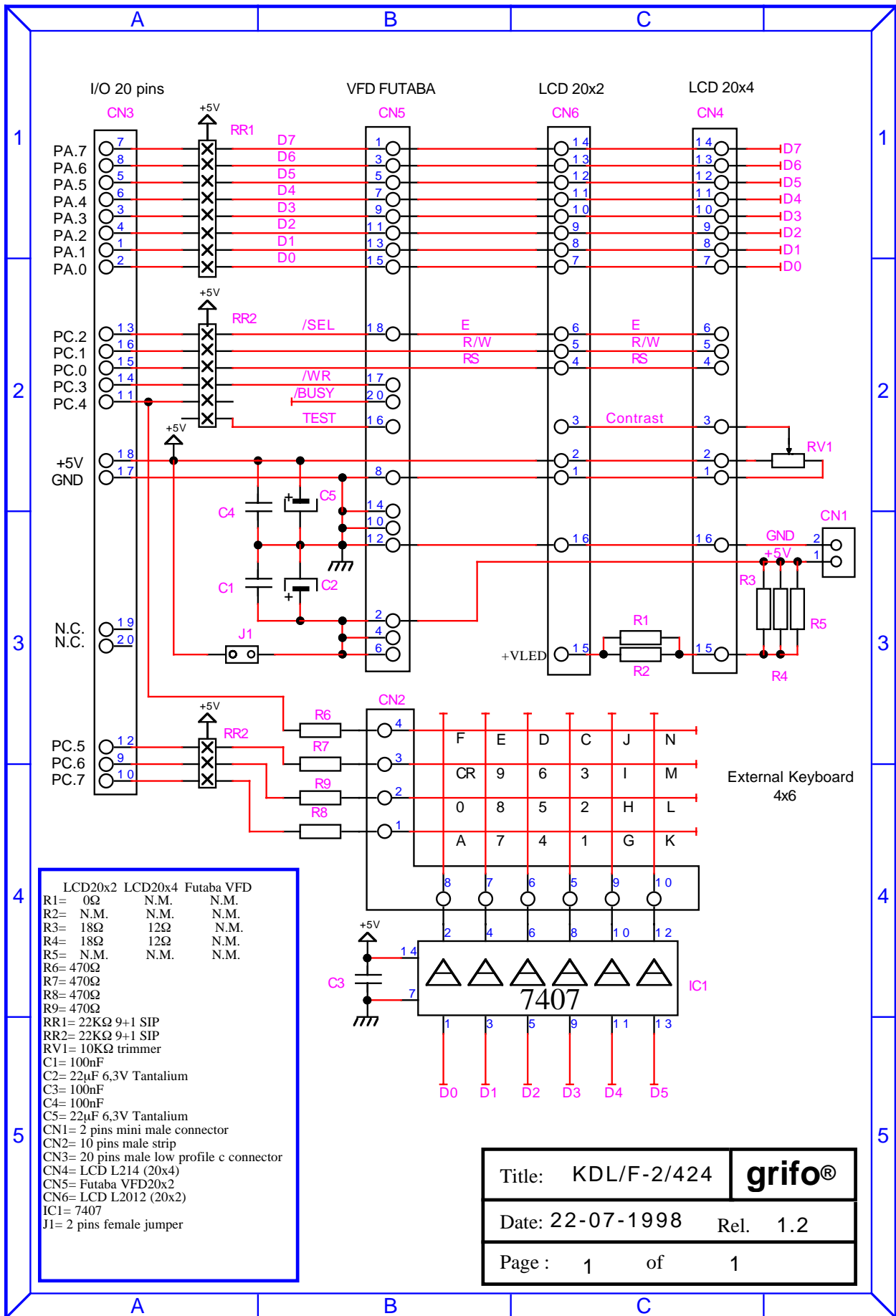
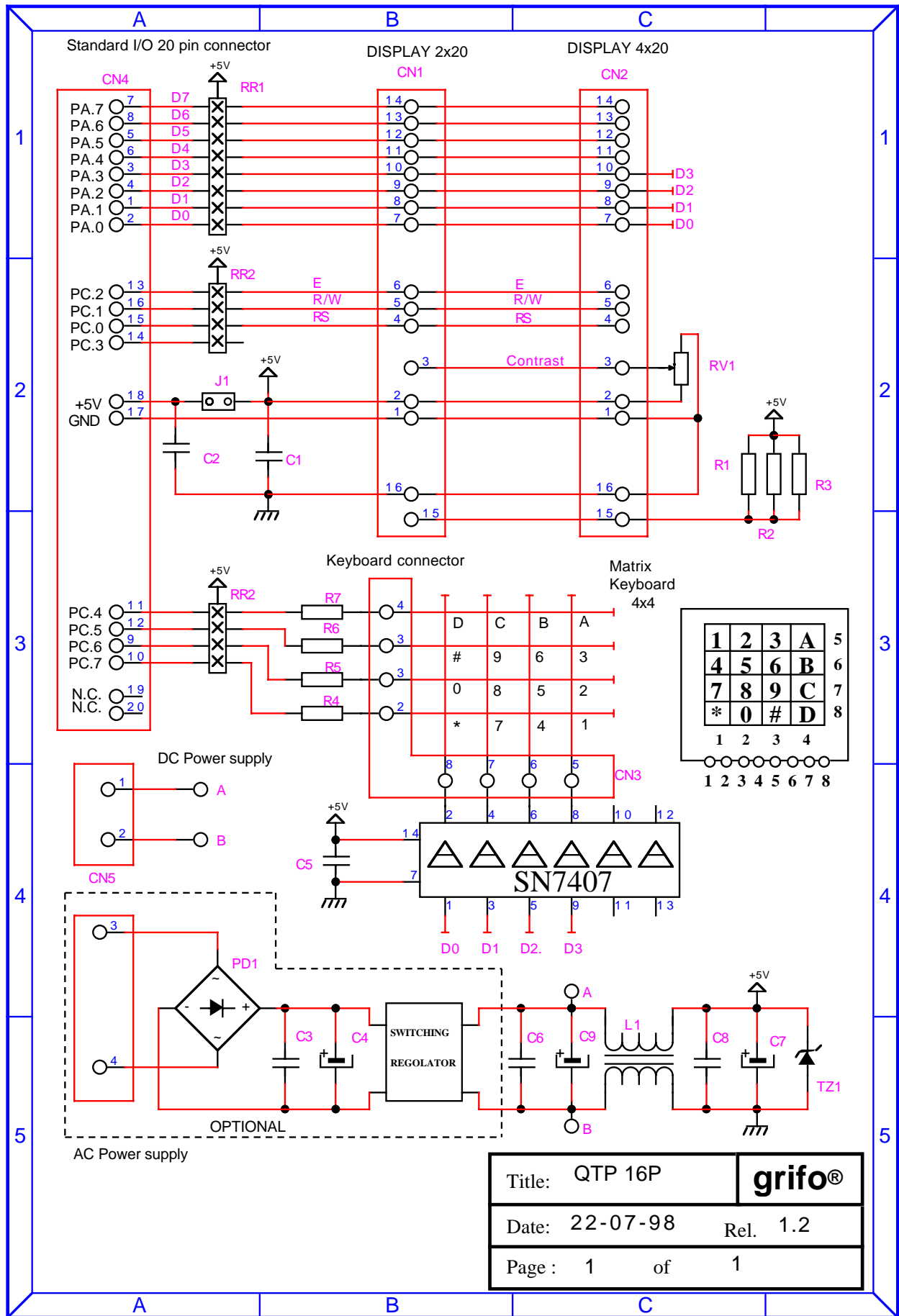


FIGURE A2: KDX x24 ELECTRIC DIAGRAM





| | |
|----------------|---------------|
| Title: QTP 16P | grifo® |
| Date: 22-07-98 | Rel. 1.2 |
| Page : 1 | of 1 |

FIGURE A3: QTP 16P ELECTRIC DIAGRAM



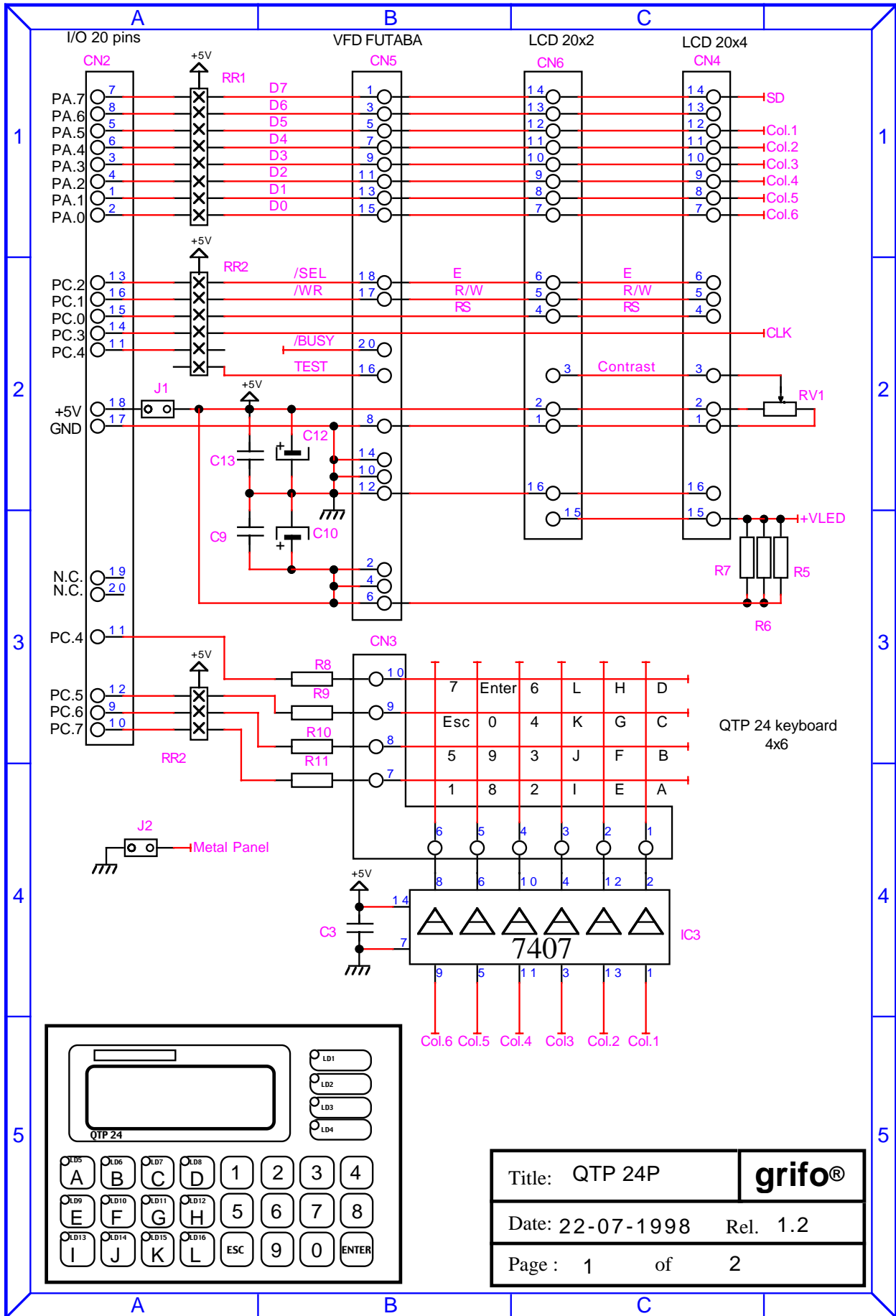
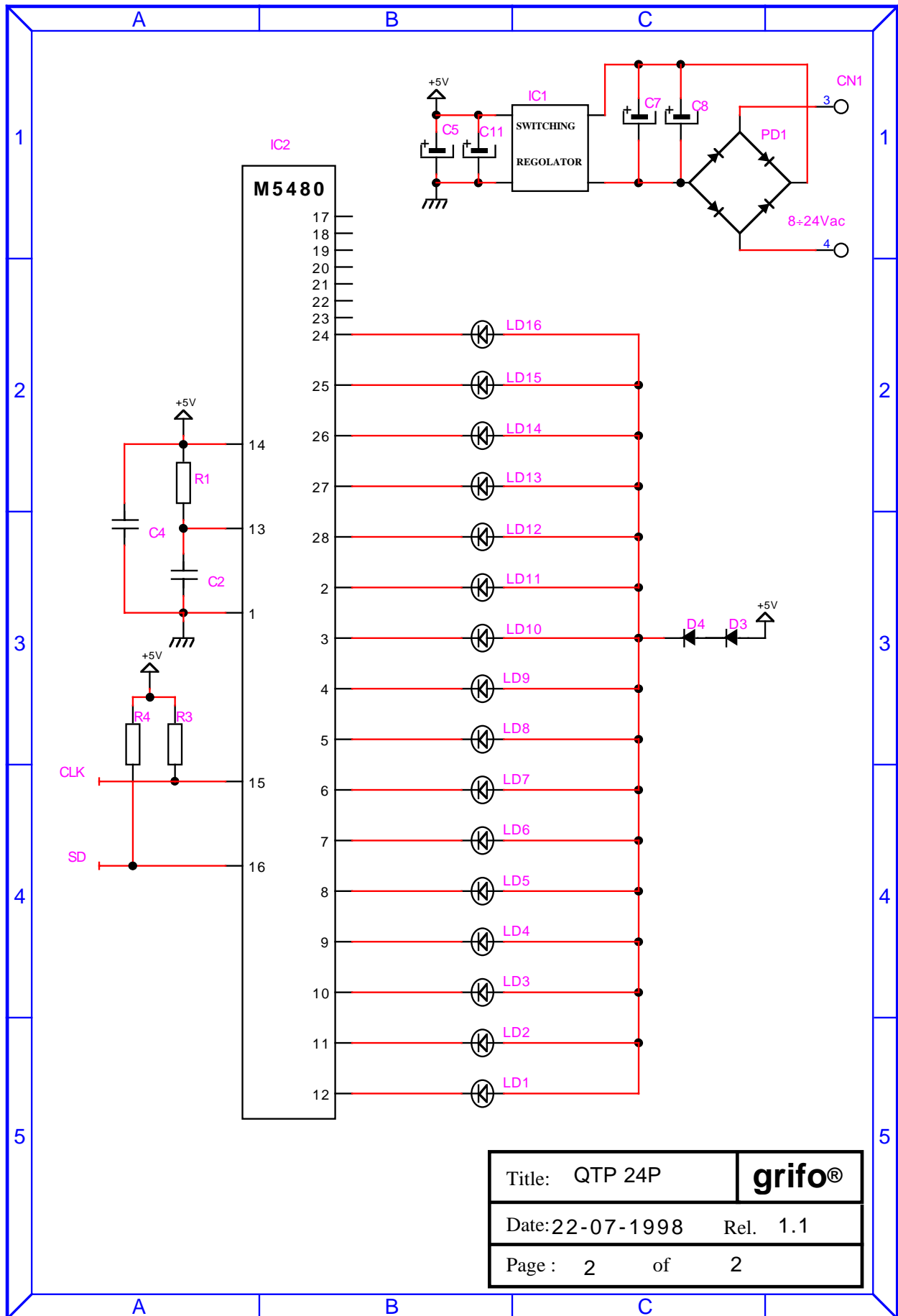


FIGURE A4: QTP 24P ELECTRIC DIAGRAM - PART 1



| | |
|------------------|---------------|
| Title: QTP 24P | grifo® |
| Date: 22-07-1998 | Rel. 1.2 |
| Page : 1 | of 2 |



| | |
|------------------|---------------|
| Title: QTP 24P | grifo® |
| Date: 22-07-1998 | Rel. 1.1 |
| Page : 2 | of 2 |

FIGURE A5: QTP 24P ELECTRIC DIAGRAM - PART 2

APPENDIX B: ON BOARD COMPONENTS DESCRIPTION

grifo® provides a completely free technical documentation service to make available data sheets of on board components. Please refer to downloadable documents; their location in the site and complete URL are reported below.

CPU 80C552

- Link: Home | Technical Documentation Service | Philips | Data-Sheet 80C552
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Philips Semiconductors

Product specification

Single-chip 8-bit microcontroller

80C552/83C552

Single-chip 8-bit microcontroller with 10-bit A/D, capture/compare timer, high-speed outputs, PWM



DESCRIPTION

The 80C552/83C552 (hereafter generically referred to as 8XC552) Single-Chip 8-Bit Microcontroller is manufactured in an advanced CMOS process and is a derivative of the 80C51 microcontroller family. The 8XC552 has the same instruction set as the 80C51. Three versions of the derivative exist:

- 83C552—8k bytes mask programmable ROM
- 80C552—ROMless version of the 83C552
- 87C552—8k bytes EPROM (described in a separate chapter)

The 8XC552 contains a non-volatile 8k × 8 read-only program memory (83C552), a volatile 256 × 8 read/write data memory, five 8-bit I/O ports, one 8-bit input port, two 16-bit timer/event counters (identical to the timers of the 80C51), an additional 16-bit timer coupled to capture and compare latches, a 15-source, two-priority-level, nested interrupt structure, an 8-input ADC, a dual DAC pulse width modulated interface, two serial interfaces (UART and I²C-bus), a "watchdog" timer and on-chip oscillator and timing circuits. For systems that require extra capability, the 8XC552 can be expanded using standard TTL compatible memories and logic.

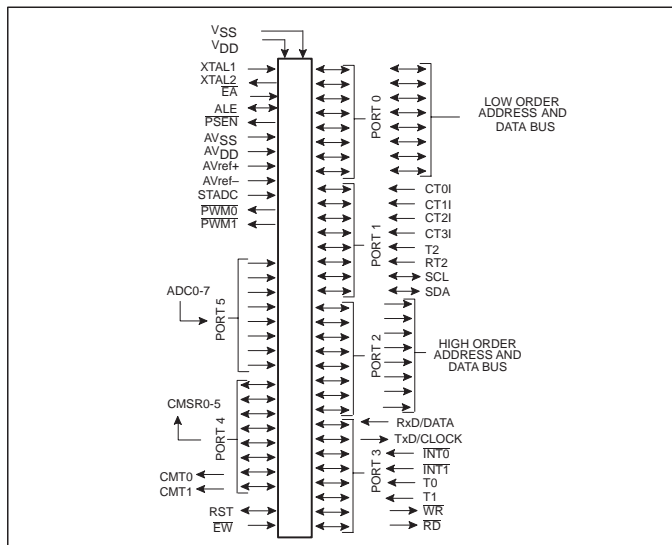
In addition, the 8XC552 has two software selectable modes of power reduction—idle mode and power-down mode. The idle mode freezes the CPU while allowing the RAM, timers, serial ports, and interrupt system to continue functioning. The power-down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative.

The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 45 two-byte, and 17 three-byte. With a 16MHz (24MHz) crystal, 58% of the instructions are executed in 0.75µs (0.5µs) and 40% in 1.5µs (1µs). Multiply and divide instructions require 3µs (2µs).

FEATURES

- 80C51 central processing unit
- 8k × 8 ROM expandable externally to 64k bytes
- ROM code protection
- An additional 16-bit timer/counter coupled to four capture registers and three compare registers
- Two standard 16-bit timer/counters
- 256 × 8 RAM, expandable externally to 64k bytes
- Capable of producing eight synchronized, timed outputs
- A 10-bit ADC with eight multiplexed analog inputs
- Two 8-bit resolution, pulse width modulation outputs
- Five 8-bit I/O ports plus one 8-bit input port shared with analog inputs
- I²C-bus serial I/O port with byte oriented master and slave functions
- Full-duplex UART compatible with the standard 80C51
- On-chip watchdog timer
- Three speed ranges:
 - 3.5 to 16MHz
 - 3.5 to 24MHz (ROM, ROMless only)
 - 3.5 to 30MHz (ROM, ROMless only)
- Three operating ambient temperature ranges:
 - P83C552xBx: 0°C to +70°C
 - P83C552xFx: -40°C to +85°C (XTAL frequency max. 24 MHz)
 - P83C552xHx: -40°C to +125°C (XTAL frequency max. 16 MHz)

LOGIC SYMBOL



Single-chip 8-bit microcontroller

80C552/83C552

PIN DESCRIPTION

| MNEMONIC | PIN NO. | | TYPE | NAME AND FUNCTION |
|-----------------|----------|--------------|------|--|
| | PLCC | QFP | | |
| V _{DD} | 2 | 72 | I | Digital Power Supply: +5V power supply pin during normal operation, idle and power-down mode. |
| STADC | 3 | 74 | I | Start ADC Operation: Input starting analog to digital conversion (ADC operation can also be started by software). This pin must not float. |
| PWM0 | 4 | 75 | O | Pulse Width Modulation: Output 0. |
| PWM1 | 5 | 76 | O | Pulse Width Modulation: Output 1. |
| EW | 6 | 77 | I | Enable Watchdog Timer: Enable for T3 watchdog timer and disable power-down mode. This pin must not float. |
| P0.0-P0.7 | 57-50 | 58-51 | I/O | Port 0: Port 0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed address and data bus during accesses to external program and data memory. In this application it uses strong internal pull-ups when emitting 1s. |
| P1.0-P1.7 | 16-23 | 10-17 | I/O | Port 1: 8-bit I/O port. Alternate functions include: |
| | 16-21 | 10-15 | I/O | (P1.0-P1.5): Quasi-bidirectional port pins. |
| | 22-23 | 16-17 | I/O | (P1.6, P1.7): Open drain port pins. |
| | 16-19 | 10-13 | I | CT0-CT3: (P1.0-P1.3): Capture timer input signals for timer T2. |
| | 20 | 14 | I | (P1.4): T2 event input. |
| | 21 | 15 | I/O | RT2 (P1.5): T2 timer reset signal. Rising edge triggered. |
| | 22 | 16 | I/O | SCL (P1.6): Serial port clock line I ² C-bus. |
| | 23 | 17 | I/O | SDA (P1.7): Serial port data line I ² C-bus. |
| | | | | Port 1 is also used to input the lower order address byte during EPROM programming and verification. A0 is on P1.0, etc. |
| P2.0-P2.7 | 39-46 | 38-42, 45-47 | I/O | Port 2: 8-bit quasi-bidirectional I/O port. Alternate functions include: |
| | | | | Alternate function: High-order address byte for external memory (A08-A15). |
| P3.0-P3.7 | 24-31 | 18-20, 23-27 | I/O | Port 3: 8-bit quasi-bidirectional I/O port. Alternate functions include: |
| | 24 | 18 | | RD(P3.0): Serial input port. |
| | 25 | 19 | | TXD (P3.1): Serial output port. |
| | 26 | 20 | | INT0 (P3.2): External interrupt. |
| | 27 | 23 | | INT1 (P3.3): External interrupt. |
| | 28 | 24 | | T0 (P3.4): Timer 0 external input. |
| | 29 | 25 | | T1 (P3.5): Timer 1 external input. |
| | 30 | 26 | | WR (P3.6): External data memory write strobe. |
| | 31 | 27 | | RD (P3.7): External data memory read strobe. |
| P4.0-P4.7 | 7-14 | 80, 1-2, 4-8 | I/O | Port 4: 8-bit quasi-bidirectional I/O port. Alternate functions include: |
| | 7-12 | 80, 1-2, 4-6 | O | CMSR0-CMSR5 (P4.0-P4.5): Timer T2 compare and self/reset outputs on a match with timer T2. |
| | 13, 14 | 7, 8 | O | CMT0, CM1 (P4.6, P4.7): Timer T2 compare and toggle outputs on a match with timer T2. |
| P5.0-P5.7 | 68-62, 1 | 71-64, | I | Port 5: 8-bit input port. |
| | | | | ADC0-ADC7 (P5.0-P5.7): Alternate function: Eight input channels to ADC. |
| RST | 15 | 9 | I/O | Reset: Input to reset the 8XC552. It also provides a reset pulse as output when timer T3 overflows. |
| XTAL1 | 35 | 32 | I | Crystal Input 1: Input to the inverting amplifier that forms the oscillator, and input to the internal clock generator. Receives the external clock signal when an external oscillator is used. |
| XTAL2 | 34 | 31 | O | Crystal Input 2: Output of the inverting amplifier that forms the oscillator. Left open-circuit when an external clock is used. |

Single-chip 8-bit microcontroller

80C552/83C552

PIN DESCRIPTION (Continued)

| MNEMONIC | PIN NO. | | TYPE | NAME AND FUNCTION |
|-----------------|---------|-------|------|---|
| | PLCC | QFP | | |
| V _{SS} | 36, 37 | 34-36 | I | Two Digital ground pins. |
| PSEN | 47 | 48 | O | Program Store Enable: Active-low read strobe to external program memory. |
| ALE | 48 | 49 | O | Address Latch Enable: Latches the low byte of the address during accesses to external memory. It is active every six clock periods. During an external data memory access, the ALE pulse expands to eight clock periods. ALE can drive up to eight LS TTL inputs and handles CMOS inputs without an external pull-up. |
| EA | 49 | 50 | I | External Access: When EA is held at TTL level high, the CPU executes out of the internal program ROM provided the program counter is less than 8192. When EA is held at TTL low level, the CPU executes out of external program memory. EA is not allowed to float. |
| AVREF- | 58 | 59 | I | Analog to Digital Conversion Reference Resistor: Low-end. |
| AVREF+ | 59 | 60 | I | Analog to Digital Conversion Reference Resistor: High-end. |
| AVSS | 60 | 61 | I | Analog Ground |
| AVDD | 61 | 63 | I | Analog Power Supply |

NOTE:

- To avoid "latch-up" effect at power-on, the voltage on any pin at any time must not be higher or lower than V_{DD} + 0.5V or V_{SS} - 0.5V, respectively.

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier. The pins can be configured for use as an on-chip oscillator, as shown in the logic symbol, page 2.

To drive the device from an external clock source, XTAL1 should be driven while XTAL2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, because the input to the internal clock circuitry is through a divide-by-two flip-flop. However, minimum and maximum high and low times specified in the data sheet must be observed.

RESET

A reset is accomplished by holding the RST pin high for at least two machine cycles (24 oscillator periods), while the oscillator is running. To insure a good power-on reset, the RST pin must be high long enough to allow the oscillator time to start up (normally a few milliseconds) plus two machine cycles. At power-on, the voltage on V_{DD} and RST must come up at the same time for a proper start-up.

IDLE MODE

In the idle mode, the CPU puts itself to sleep while some of the on-chip peripherals stay active. The instruction to invoke the idle mode is the last instruction executed in the normal operating mode before the idle mode is activated. The CPU contents, the on-chip RAM, and all of the special function registers remain intact during this mode. The idle mode can be terminated either by any enabled interrupt (at which time the process is picked up at the interrupt service routine and continued), or by a hardware reset which starts the processor in the same manner as a power-on reset.

POWER-DOWN MODE

In the power-down mode, the oscillator is stopped and the instruction to invoke power-down is the last instruction executed. Only the contents of the on-chip RAM are preserved. A hardware reset is the only way to terminate the power-down mode. The control bits for the reduced power modes are in the special function register PCON. Table 1 shows the state of the I/O ports during low current operating modes.

ROM CODE PROTECTION (83C552)

The 83C552 has an additional security feature. ROM code protection may be selected by setting a mask-programmable security bit (i.e., user dependent). This feature may be requested during ROM code submission. When selected, the ROM code is protected and cannot be read out at any time by any test mode or by any instruction in the external program memory space.

The MOVX instructions are the only instructions that have access to program code in the internal or external program memory. The EA input is latched during RESET and is "don't care" after RESET (also if the security bit is not set). This implementation prevents reading internal program code by switching from external program memory to internal program memory during a MOVX instruction or any other instruction that uses immediate data.

Table 1. External Pin Status During Idle and Power-Down Modes

| MODE | PROGRAM MEMORY | ALE | PSEN | PORT 0 | PORT 1 | PORT 2 | PORT 3 | PORT 4 | PWM0/ PWM1 |
|------------|----------------|-----|------|--------|--------|---------|--------|--------|------------|
| Idle | Internal | 1 | 1 | Data | Data | Data | Data | Data | 1 |
| Idle | External | 1 | 1 | Float | Data | Address | Data | Data | 1 |
| Power-down | Internal | 0 | 0 | Data | Data | Data | Data | Data | 1 |
| Power-down | External | 0 | 0 | Float | Data | Data | Data | Data | 1 |



FAMIGLIA I51

Link: Home | Technical Documentation Service | Philips | Fam.8051 Programmers Guide
 URL: <http://www.grifo.com/PRESS/DOC/Philips/PROGGUI.PDF>

Philips Semiconductors

80C51 Family 80C51 family programmer's guide and instruction set

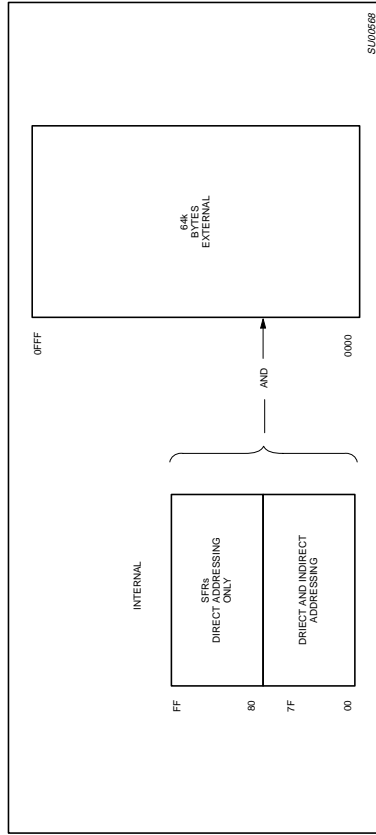


Figure 2. 80C51 Data Memory

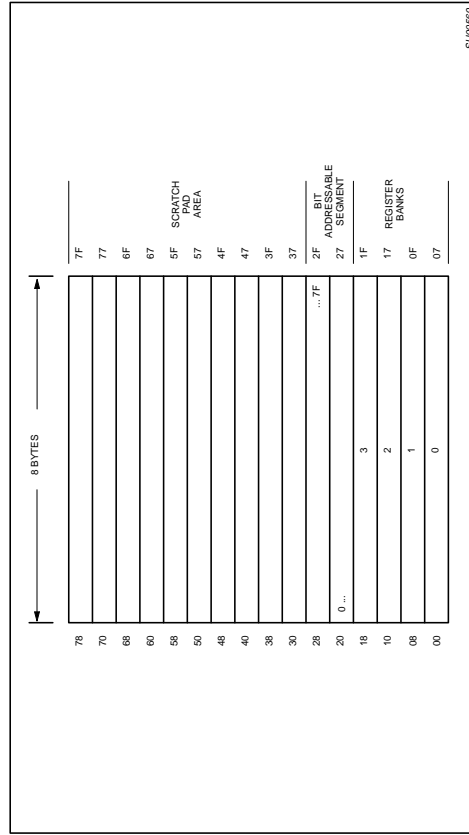


Figure 3. 128 Bytes of RAM Direct and Indirect Addressable

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80C51 Family 80C51 family programmer's guide and instruction set

PROGRAMMER'S GUIDE AND INSTRUCTION SET

Memory Organization

Program Memory

The 80C51 has separate address spaces for program and data memory. The Program memory can be up to 64k bytes long. The lower 4k can reside on-chip. Figure 1 shows a map of the 80C51 program memory.

The 80C51 can address up to 64k bytes of data memory to the chip. The MOVX instruction is used to access the external data memory.

The 80C51 has 128 bytes of on-chip RAM, plus a number of Special Function Registers (SFRs). The lower 128 bytes of RAM can be accessed either by direct addressing (MOV data addr) or by indirect addressing (MOV @R). Figure 2 shows the Data Memory organization.

Direct and Indirect Address Area

The 128 bytes of RAM which can be accessed by both direct and indirect addressing can be divided into three segments as listed below and shown in Figure 3.

1. Register Banks 0-3: Locations 0 through 1FH (32 bytes). The device after reset defaults to register bank 0. To use the other register banks, the user must select them in software. Each

2. Bit Addressable Area: 16 bytes have been assigned for this segment, 20H-2FH. Each one of the 128 bits of this segment can be directly addressed (0-7FH). The bits can be referred to in two ways, both of which are acceptable by most assemblers. One way is to refer to their address (i.e., 0-7FH). The other way is with reference to bytes 20H to 2FH. Thus, bits 0-7 can also be referred to as bits 20.0-20.7, and bits 6FH are the same as 21.0-21.7, and so on. Each of the 16 bytes in this segment can also be addressed as a byte.
3. Scratch Pad Area: 30H through 7FH are available to the user as data RAM. However, if the stack pointer has been initialized to this area, enough bytes should be left aside to prevent SP data destruction.

Figure 2 shows the different segments of the on-chip RAM.

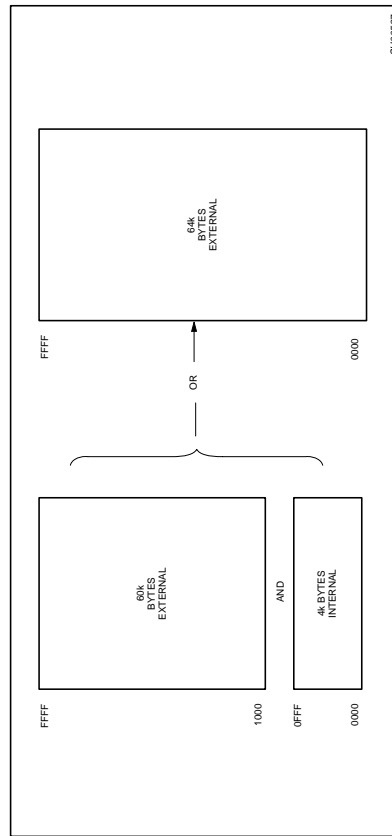


Figure 1. 80C51 Program Memory



CONTROLORE CAN SJA 1000

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Philips Semiconductors Preliminary specification
Stand-alone CAN controller SJA1000

BLOCK DIAGRAM

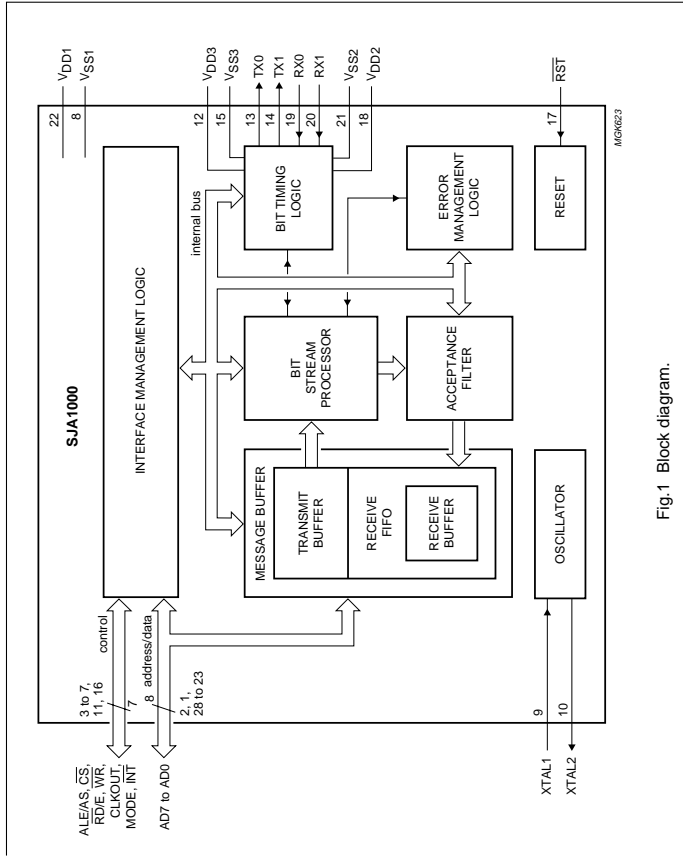


Fig.1 Block diagram.

Philips Semiconductors Preliminary specification
Stand-alone CAN controller SJA1000

FEATURES

- In compatibility to the PCA82C200 stand-alone CAN controller
- Identical compatibility to the PCA82C200 stand-alone CAN controller
- Software-compatibility mode to the PCA82C200 BasicCAN mode is default
- Extended receive buffer (64-byte FIFO)
- CAN 2.0B protocol compatibility (extended frame access in PCA82C200 compatibility mode)
- Supports 11-bit identifier as well as 29-bit identifier bit rates up to 1 Mbits/s
- Pelican mode extensions:
 - Error counters with read/write access
 - Programmable error warning limit
 - Last error code register
- Error interrupt for each CAN-bus error
- Arbitration lost interrupt with detailed bit position
- Single-shot transmission (no re-transmission)
- Listen only mode (no acknowledge, no active error flags)
- Hot plugging support (software driven bit rate detection)
- Acceptance filter extension (4-byte code, 4-byte mask)
- Reception of 'own' messages (self reception request)
- 4 MHz clock frequency
- Interfaces to a variety of microprocessors
- Programmable CAN output driver configuration
- Extended ambient temperature range (-40 to +125 °C).

2 GENERAL DESCRIPTION

The SJA1000 is a stand-alone controller for the Controller Area Network (CAN) used within automotive and general industrial environments. It is designed to be hardware and software compatible to the PCA82C200 CAN controller (BasicCAN) from Philips Semiconductors. Additionally, a new mode of operation is implemented (Pelican) which supports the CAN 2.0B protocol specification with several new features.

ORDERING INFORMATION

| PART NUMBER | PACKAGE | | |
|-------------|---------|--|-----------|
| | NAME | DESCRIPTION | VERSION |
| A1000 | DIP28 | plastic dual in-line package; 28 leads (600 mil) | SOT-117-1 |
| A1000T | SO28 | plastic small outline package; 28 leads; body width 7.5 mm | SOT-136-1 |



SRAM+RTC PCF8583

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PCF8583

Clock/calendar with 240 x 8-bit RAM

PCF8583

Clock/calendar with 240 x 8-bit RAM

FEATURES

- I²C-bus interface operating supply voltage: 2.5 V to 6 V
- I²C-bus interface operating supply voltage (0 to +70 °C): 0 V to 6.0 V
- 40 x 8-bit low-voltage RAM
- Data retention voltage: 1.0 V to 6 V
- Operating current (at f_{SCL} = 0 Hz): max. 50 µA
- I²C-bus function with four year calendar
- Universal timer with alarm and overflow indication 4 or 12 hour format
- 2.768 kHz or 50 Hz time base
- Serial input/output bus (I²C)
- Automatic word address incrementing
- Programmable alarm, timer and interrupt function
- Slave address:
 - READ: A1 or A3
 - WRITE: A0 or A2.

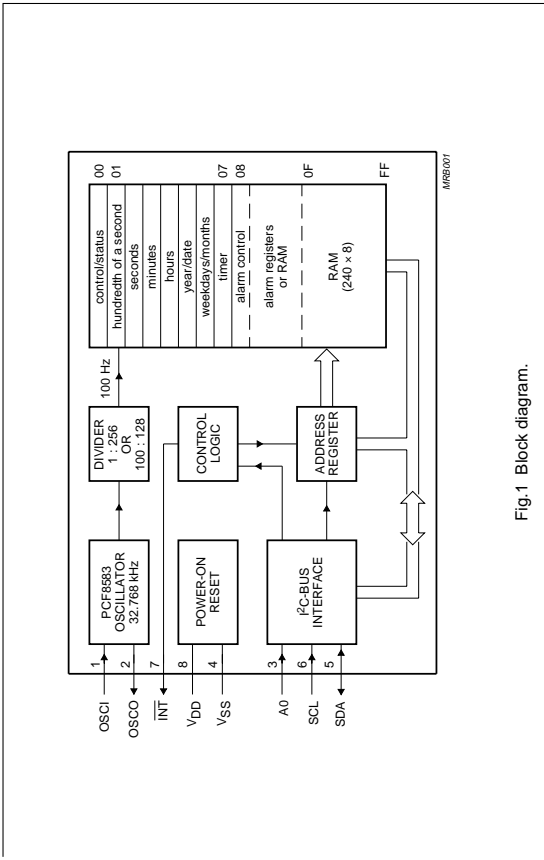
BLOCK DIAGRAM


Fig.1 Block diagram.

PINNING

| MBOL | PIN | DESCRIPTION |
|------|-----|--|
| 1 | 1 | oscillator input, 50 Hz or event-pulse input |
| 2 | 2 | oscillator output |
| 3 | 3 | address input |
| 4 | 4 | negative supply |
| 5 | 5 | serial data line |
| 6 | 6 | serial clock line |
| 7 | 7 | open drain interrupt output (active LOW) |
| 8 | 8 | positive supply |

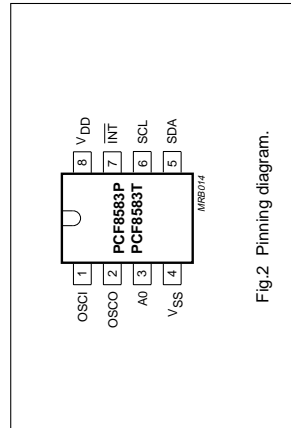


Fig.2 Pinning diagram.

2 GENERAL DESCRIPTION

The PCF8583 is a clock/calendar circuit based on a 2048-bit static CMOS RAM organized as 256 words by 8 bits. Addresses and data are transferred serially via the two-line bidirectional I²C-bus. The built-in word address register is incremented automatically after each written or read data byte. Address pin A0 is used for programming the hardware address, allowing the connection of two devices to the bus without additional hardware.

The built-in 32.768 kHz oscillator circuit and the first 8 bytes of the RAM are used for the clock/calendar and counter functions. The next 8 bytes may be programmed as alarm registers or used as free RAM space. The remaining 240 bytes are free RAM locations.

QUICK REFERENCE DATA

| SYMBOL | PARAMETER | CONDITION | MIN. | TYP. | MAX. | UNIT |
|--------|-------------------------------------|--|------|------|------|------|
| D | supply voltage operating mode | I ² C-bus active | 2.5 | - | 6.0 | V |
| D | supply voltage operating mode | I ² C-bus inactive | 1.0 | - | 6.0 | V |
| D | supply current operating mode | f _{SCL} = 100 kHz | - | - | 200 | µA |
| D | supply current clock mode | f _{SCL} = 0 Hz; V _{DD} = 5 V | - | 10 | 50 | µA |
| D | operating ambient temperature range | f _{SCL} = 0 Hz; V _{DD} = 1 V | -40 | - | +85 | °C |
| D | storage temperature range | | -65 | - | +150 | °C |

ORDERING INFORMATION

| TYPE | PACKAGE | DESCRIPTION | VERSION |
|----------|---------|---|----------|
| PCF8583P | DIP8 | plastic dual in-line package; 8 leads (300 mil) | SOT97-1 |
| PCF8583T | S08 | plastic small outline package; 8 leads; body width 7.5 mm | SOT176-1 |



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