Single Euro size 100x160mm with interface to Abaco® Industrial BUS; microcontroller Philips 80C552, at 22M Hz or compatible ones; different memory devices: 128K EPROM; 128K SRAM; 512K EPROM, FLASH, EEPROM or SRAM; up to 1K serial EEPROM; 240 Bytes serial SRAM; 256 Bytes microcontroller internal RAM; MMU circuit for memory management; Real Time Clock able to generate Interrupts; Back Up circuit for SRAM and RTC provided of Lithium Battery either on board and external. Hardware Watch Dog: 8 lines A/D converter with: 10 bits resolution, input range +2.49V, 0+20 or 4+20 mA, conversion time 27µs; 4 status and activity LEDs plus BUZZER; one dip switch with 8 ways, readable by software; 1 hardware serial lines configurable in RS232, RS422, RS485, passive Current Loop, 1 software serial line in RS232; 40 TTL I/O lines, driven by software: 24 managed by PPI 82C55 and 16 managed by CPU (some of these lines have double functions); 2 independent PWM outputs with 8 bits resolution; three 16 bits Timers Counters. Two I2C BUS lines, one hardware and one software; optional CAN line based on Philips SJA 1000 controller that supports all standard protocols, up to 1 MBit/sec maximum bit rate; CAN line driver, galvanically optocoupled. 9 standard connettors, mainly placed on the front side of the card, to facilitate the connection; single power supply +5 Vdc, 340 mA maximum consumption; possibility to reduce power consumption with Idle or Power Down mode; Wide range of base software and Development Tools that allow card use with only a standard PC. Among these we remind: GET 51; Monitor Debugger; Assembler; BASIC compilers; C compilers; PASCAL compilers; LADDER contact logic; real time Operating Systems; etc.
IMPORTANT

Although all the information contained herein have been carefully verified, grifo® assumes no responsibility for errors that might appear in this document, or for damage to things or persons resulting from technical errors, omission and improper use of this manual and of the related software and hardware.

grifo® reserves the right to change the contents and form of this document, as well as the features and specification of its products at any time, without prior notice, to obtain always the best product.

For specific informations on the components mounted on the card, please refer to the Data Book of the builder or second sources.

SYMBOLS DESCRIPTION

In the manual could appear the following symbols:

- Attention: Generic danger
- Attention: High voltage
- Attention: ESD sensitive device

Trade Marks

GPC®, grifo®: are trade marks of grifo®.

Other Product and Company names listed, are trade marks of their respective companies.
GENERAL INDEX

INTRODUCTION ................................................................................................................... 1

VERSION ............................................................................................................................... 3

GENERAL INFORMATION ...................................................................................................... 4
- ON BOARD MICROCONTROLLER .................................................................................... 5
- MEMORY DEVICES ............................................................................................................. 6
- A/D CONVERTER ................................................................................................................ 6
- CONTROL LOGIC ............................................................................................................... 8
- ABACO® BUS .................................................................................................................. 8
- DIGITAL I/O LINES ........................................................................................................... 8
- CLOCK ....................................................................................................................... 9
- BOARD CONFIGURATION ............................................................................................... 9
- PWM LINES ........................................................................................................................ 9
- SERIAL COMMUNICATION ............................................................................................... 10
- I2C BUS LINES ................................................................................................................ 10
- CAN LINE ....................................................................................................................... 11

TECHNICAL FEATURES ........................................................................................................ 12
- GENERAL FEATURES .......................................................................................................... 12
- PHYSICAL FEATURES ......................................................................................................... 12
- ELECTRIC FEATURES ........................................................................................................ 13

INSTALLATION ................................................................................................................... 14
- CONNECTIONS .................................................................................................................. 14
  - CN9 - BACK UP EXTERNAL BATTERY CONNECTOR .............................................. 14
  - CN3 - PPI I/O AND SW I2C BUS CONNECTOR ............................................................ 15
  - CN7 - PPI I/O CONNECTOR ........................................................................................... 16
  - CN1 - CPU I/O CONNECTOR ......................................................................................... 18
  - CN4A - SERIAL LINE A CONNECTOR ......................................................................... 20
  - CN4B - SERIAL LINE B CONNECTOR .......................................................................... 26
  - CN5 - CONNECTOR FOR ABACO® BUS ....................................................................... 28
  - CN2 - A/D CONVERTER INPUTS AND PWM SIGNALS CONNECTOR .................. 30
  - CN8 - CAN LINE CONNECTOR ....................................................................................... 32
- I/O CONNECTIONS ............................................................................................................... 36
  - I2C BUS LINES CONNECTION ...................................................................................... 37
- TRIMMERS AND CALIBRATION ....................................................................................... 39
- TEST POINT ........................................................................................................................... 39
- ANALOG INPUTS SELECTION .......................................................................................... 40
- DIGITAL I/O INTERFACES ................................................................................................. 40
- VISUAL SIGNALATIONS ..................................................................................................... 41
- JUMPERS ................................................................................................................................ 42
  - 2 PINS JUMPERS ........................................................................................................... 43
  - 4 PINS JUMPERS ........................................................................................................... 43
  - 3 PINS JUMPERS ........................................................................................................... 44
4 PINS JUMPERS ................................................................. 44
9 PINS JUMPERS ................................................................. 46
SOLDER JUMPERS ................................................................. 46
BACK UP ........................................................................ 46
INTERRUPTS ..................................................................... 48
POWER SUPPLY ................................................................. 48
RESET, POWER GOOD, WATCH DOG .................................. 49
SERIAL COMMUNICATION SELECTION ......................... 50
MEMORY SELECTION .......................................................... 52
CAN INTERFACE ................................................................. 54
SOFTWARE ......................................................................... 56

ADDRESSES AND MAPS .................................................. 58
ON BOAR RESOURCES MAPPING ........................................ 58
BUS ABACO® MAPPING ...................................................... 58
PERIPHERALS MAPPING ..................................................... 59
MEMORY MAPPING ............................................................. 59
  MAPPING 0 ................................................................. 60
  MAPPING 1 ................................................................. 61
  MAPPING 2 ................................................................. 62
  MAPPING 3 ................................................................. 63
SOFTWARE DESCRIPTION ................................................ 64
SOFTWARE I2C BUS .......................................................... 64
ACTIVITY LEDS ................................................................. 64
BUZZER ........................................................................ 65
SERIAL EEPROM .............................................................. 65
DIP SWITCH DSW1 ............................................................ 65
BACKED SRAM + SERIAL RTC ........................................... 66
CPU INTERNAL PERIPHERALS .......................................... 66
RS 422-485 COMMUNICATION .......................................... 68
SOFTWARE SERIAL LINE B ................................................. 68
PPI 82C55 ........................................................................ 69
I/O SIGNALS OF CPU ........................................................ 70
CAN CONTROLLER ............................................................ 70
MEMORY MANAGEMENT UNIT ......................................... 72

BIBLIOGRAPHY ............................................................... 77

APPENDIX A: ELECTRIC DIAGRAMS .................................. A-1

APPENDIX B: ON BOARD COMPONENTS DESCRIPTION ........................ B-1
  CPU 80C552 ................................................................. B-1
  FAMIGLIA I51 ............................................................... B-2
  CONTROLLORE CAN SJA 1000 ..................................... B-3
  SRAM+RTC PCF8583 .................................................... B-4

APPENDIX C: ALPHABETICAL INDEX .................................... C-1
FIGURES INDEX

FIGURE 1: LOCATION OF PRINTED CIRCUIT VERSION ................................................................. 3
FIGURE 2: BLOCK DIAGRAM .................................................................................................... 7
FIGURE 3: CN9 - BACK UP EXTERNAL BATTERY CONNECTOR .................................................. 14
FIGURE 4: CN3 - PPI I/O AND SW I2C BUS CONNECTOR .......................................................... 15
FIGURE 5: CN7 - PPI I/O CONNECTOR ....................................................................................... 16
FIGURE 6: PPI BLOCK DIAGRAM ............................................................................................ 17
FIGURE 7: CN1 - CPU I/O CONNECTOR ...................................................................................... 18
FIGURE 8: CPU I/O SIGNALS BLOCK DIAGRAM ......................................................................... 19
FIGURE 9: CN4A - SERIAL LINE A CONNECTOR ......................................................................... 20
FIGURE 10: COMPONENTS MAP ON SOLDER SIDE ................................................................. 21
FIGURE 11: RS 232 POINT TO POINT CONNECTION EXAMPLE ............................................... 22
FIGURE 12: RS 422 POINT TO POINT CONNECTION EXAMPLE ............................................... 22
FIGURE 13: RS 485 POINT TO POINT CONNECTION EXAMPLE ............................................... 22
FIGURE 14: RS 485 NETWORK CONNECTION EXAMPLE ........................................................ 23
FIGURE 15: CURRENT LOOP 4 WIRES POINT-TO-POINT CONNECTION EXAMPLE .................. 24
FIGURE 16: CURRENT LOOP 2 WIRES POINT-TO-POINT CONNECTION EXAMPLE ............... 24
FIGURE 17: CURRENT LOOP NETWORK CONNECTION EXAMPLE ........................................ 25
FIGURE 18: CN4B - SERIAL LINE B CONNECTOR ....................................................................... 26
FIGURE 19: SERIAL COMMUNICATION BLOCK DIAGRAM ..................................................... 27
FIGURE 20: CN5 - ABACO® BUS CONNECTOR ......................................................................... 28
FIGURE 21: CN2 - A/D CONVERTER INPUTS AND PWM SIGNALS CONNECTOR .................. 30
FIGURE 22: A/D CONVERTER BLOCK DIAGRAM ..................................................................... 31
FIGURE 23: CN8 - CAN LINE CONNECTOR ................................................................................ 32
FIGURE 24: CAN LINE BLOCK DIAGRAM ................................................................................ 33
FIGURE 25: CAN NETWORK CONNECTION EXAMPLE .......................................................... 34
FIGURE 26: CONNECTORS, TRIMMER, BATTERY, MEMORIES, ETC. LOCATION ..................... 35
FIGURE 27: I2C BUS DEVICES CONNECTION ......................................................................... 37
FIGURE 28: I2C BUS NETWORK CONNECTION EXAMPLE ..................................................... 38
FIGURE 29: LEDs TABLE .......................................................................................................... 41
FIGURE 30: JUMPERS SUMMARIZING TABLE ............................................................................ 42
FIGURE 31: 2 PINS JUMPERS TABLE ......................................................................................... 43
FIGURE 32: 3 PINS JUMPERS TABLE ......................................................................................... 44
FIGURE 33: 4 PINS JUMPERS TABLE ......................................................................................... 44
FIGURE 34: JUMPERS PLACEMENT AND NUMERATION ......................................................... 45
FIGURE 35: 9 PINS JUMPERS TABLE ......................................................................................... 46
FIGURE 36: COMPONENTS MAP OF COMPONENT SIDE .......................................................... 47
FIGURE 37: SERIAL LINE A (HARDWARE) COMMUNICATION DRIVERS .................................. 51
FIGURE 38: MEMORY SELECTION TABLE ................................................................................ 53
FIGURE 39: CARD PHOTO ...................................................................................................... 55
FIGURE 40: PERIPHERALS ADDRESSES TABLE ....................................................................... 59
FIGURE 41: MODE 0 MEMORY CONFIGURATION .................................................................... 60
FIGURE 42: MODE 1 MEMORY CONFIGURATION .................................................................... 61
FIGURE 43: MODE 2 MEMORY CONFIGURATION .................................................................... 62
FIGURE 44: MODE3 MEMORY CONFIGURATION ................................................................. 63
FIGURE 45: POTENTIAL CONNECTION DIAGRAM ............................................................... 67
FIGURE 46: CAN CONTROLLER INITIALIZATION FLOW CHART ................................................................. 71
FIGURE 47: MMU SECTION PAGE NUMERATION .............................................................................. 73
FIGURE 48: MMU MAPPING PROGRAMMING TABLE 1 ..................................................................... 74
FIGURE 49: MMU MAPPING PROGRAMMING TABLE 2 ..................................................................... 75
FIGURE 50: MMU MAPPING PROGRAMMING TABLE 3 ..................................................................... 76
FIGURE A1: IAC 01 ELECTRIC DIAGRAM ...................................................................................... A-1
FIGURE A2: KD X 24 ELECTRIC DIAGRAM ..................................................................................... A-2
FIGURE A3: QTP 16P ELECTRIC DIAGRAM .................................................................................. A-3
FIGURE A4: QTP 24P ELECTRIC DIAGRAM - PART 1 ................................................................. A-4
FIGURE A5: QTP 24P ELECTRIC DIAGRAM - PART 2 ..................................................................... A-5
FIGURE A6: SPA 01 ELECTRIC DIAGRAM .................................................................................... A-6
INTRODUCTION

The use of these devices has turned - IN EXCLUSIVE WAY - to specialized personnel.

This device is not a safe component as defined in directive 98-37/CE.

Pins of module are not provided with any kind of ESD protection. Many pins of the card are directly connected to their respective pins of on board's components and these last are sensitive to electrostatic noises. So personnel who handles the product/s is invited to take all necessary precautions that avoid possible damages caused by electrostatic discharges.

The purpose of this handbook is to give the necessary information to the cognizant and sure use of the products. They are the result of a continual and systematic elaboration of data and technical tests saved and validated from the manufacturer, related to the inside modes of certainty and quality of the information.

The reported data are destined- IN EXCLUSIVE WAY- to specialized users, that can interact with the devices in safety conditions for the persons, for the machine and for the enviroment, impersonating an elementary diagnostic of breakdowns and of malfunction conditions by performing simple functional verify operations, in the height respect of the actual safety and health norms.

The informations for the installation, the assemblage, the dismantlement, the handling, the adjustment, the reparation and the contingent accessories, devices, installation, etc. are destined - and then executable - always and in exclusive way from specialized warned and educated personnel, or directly from the AUTHORIZED TECHNICAL ASSISTANCE, in the height respect of the manufacturer recommendations and the actual safety and health norms.

The devices can't be used outside a box. The user must always insert the cards in a container that respect the actual safety normative. The protection of this container is not threshold to the only atmospheric agents, but specially to mechanic, electric, magnetic, etc. ones.

To be on good terms with the products, is necessary guarantee legibility and conservation of the manual, also for future references. In case of deterioration or more easily for technical updates, consult the AUTHORIZED TECHNICAL ASSISTANCE directly.
To prevent problems during card utilization, it is a good practice to read carefully all the information of this manual. After this reading, the user can use the general index and the alphabetical index, respectively at the beginning and at the end of the manual, to find information in a faster and more easy way.

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All trademarks listed in this manual are copyright of the relative manufacturers.
This handbook makes reference to printed circuit version 120605 and following ones. The validity of the information contained in this manual is subordinated to the version number on the used card, and so the user must always verify the correct correspondence between the notations. The version number is reported in several places on the electronic part of the product, and following figure shows the most accessible one, that is under the battery BT1 either on component and solder side.

**Figure 1: Location of printed circuit version**
GENERAL INFORMATION

The GPC® 550 card is a powerful control and managing card in the 100x160mm standard single Euro size. It is can operate in stand alone mode as an intelligent peripheral or remoted in a wider telecontrol and aquisition network but it can be easily expanded by the numerous intelligent and non intelligent peripherals, available on Industrial Abaco® BUS.

His typical installation is over a mother board mounted inside a rack or over a mother board for Omega rails (i.e. ABB 05 and ABB 03) that furthermore allow the management of cards with BLOCK format, with Abaco® I/O BUS.

The card supports some different versions of microcontrollers as 80C552, 87C552, etc. all of them are code compatible with the wide diffused 8051 INTEL and they include considerable hardware resources. The most interesting ones are the 8 lines of 10 bits A/D converter, the numerous TTL digital I/O lines, the CAN interface and the I2C BUS lines.

Its modularity and the remarkable hardware resources allow GPC® 550 to be easily used even in complex applications.

The card use is simplified by a wide range of software development tools based either on low or high level languages which allow to work at the best conditions using only a standard PC.

Noteworthy among these tools there are the C compilers, the PASCAL and the handy BASIC compiler BASCOM 8051.

Special care has been devoted to the application developing, by generating programs which allow remote debug directly on the card and on board FLASH burning with user application program. The GPC® 550 is equipped with a series of normalized, standard Abaco® connectors allowing immediate use of all the available BLOCK I/O modules, a direct management of local operator interfaces (KDx24, QTP xxP) or connections to equipment produced by the user, or by third parties companies, obtaining a notable cost reduction.

The overall features of the card, complete of all available options, are listed below:

- Single Euro size 100x160 mm with interface to Abaco® industrial BUS.
- Microcontroller Philips 80C552, at 22M Hz or compatible ones.
- Some different memory devices: 128K EPROM; 128K SRAM; 512K EPROM, FLASH, EEPROM or SRAM; up to 1K serial EEPROM; 240 Bytes serial SRAM; plus 256 Bytes of RAM internal to microcontroller.
- Memory Management Unit that allows to address the physical memories devices into the microcontroller's addressing space, through pages organization.
- Real Time Clock able to up date day, month, year, week day, seconds, minutes and hours. It can be programmed to generate a periodic interrupt at intervals defined by software or when a specified time is reached, as an alarm clock.
- Back up circuit for SRAM and RTC provided of lithium battery and connector for external battery.
- Hardware Watch dog capable to reset and restart the card when the executed program malfunctions.
- 8 lines 10 bits A/D converter, with range +2.49V, 0÷20 or 4÷20 mA, conversion time 27μs, provided of pass band filters.
- 1 status LED plus 3 activity LEDs and BUZZER for signals, driven through software.
- 8 way dip switch: 7 dips are readable by software and it can be used as RUN/DEBUG mode selector.
- 1 hardware serial line configurable in RS 232, RS 422, RS 485, passive Current Loop with programmable baud rate up to 115K Baud.
- 1 software serial line in RS 232.
- 2 independent PWM outputs with 8 bits resolution.
- 40 I/O TTL lines, driven by software: 24 managed by PPI 82C55 and 16 managed by CPU ports (some of these lines have double functions).
- **Three** 16 bits **timer counter**. One has capture and compare functionalities, joined with inputs and outputs signals available on connectors.
- Two **I2C BUS** lines, one hardware and one software, available on connectors.
- Optional **CAN** line based on PHILIPS SJA 1000 controller that supports Basic CAN, CAN 2.0B and Pelican protocols, with a maximum 1 MBit/sec bit rate.
- PHILIPS 82C250 CAN line driver, galvanically optocoupled.
- 9 standard connectors, placed on the front side of the card, to facilitate the connection with the other systems and with the field.
- Single power supply +5Vdc, 340 mA maximum consumption.
- Possibility to reduce power consumption with idle or power down mode.
- Wide range of base software and development tools that allow card use with only a standard PC, connected through serial line. Among these: GET 51; Monitor Debugger (FMO 53, NO ICE 51); Assembler (ASM51, A51, SXA51); BASIC compilers (BASCOM 8051, BX51); C compilers (HI TECH C 51, DDS MICRO C 51, μC 51, SYS51CW); PASCAL compilers (SYS51PW); contact logic languages (Ladder WORK); real time operating systems (CMX-RTX); etc.

Here follows a description of the board's sections and the operations they perform. In order to easily locate such sections and verify their connections, please refer to figure 2.

**ON BOARD MICROCONTROLLER**

The **GPC® 550** can use the microcontrollers PHILIPS 80C552 and all the pin out compatible devices. This 8 bit processor is code compatible with the famous 8051 INTEL and so it has an extended instruction set, fast execution time, easy use of all kinds of memory and an efficient interrupts management. The most important features of the described microcontroller, are the following ones:

- 256 bytes internal RAM;
- 5 independent groups of 8 digital I/O signals (PORT);
- 2 standard 16 bits Timer Counters (TMR CNT);
- One enhanced 16 bits Timer Counter with Capture and Compare functions (TMR CNT);
- 2 priority level for interrupts (ICU);
- 15 internal interrupt sources (ICU);
- 8 lines of 10 bits A/D converter (ADC);
- 2 independent 8 bits PWM outputs (PWM);
- 1 synchronous and asynchronous serial line (UART);
- 1 I2C BUS line (HW I2C);
- Watch Dog Timer;
- Idle mode or Power down mode;

For further information, please refer to specific documentation of the manufacturing company.
MEMORY DEVICES

On the card can be mounted up to 769K and 496 bytes of memory properly divided with a maximum of:

- 256 Bytes RAM (internal to microcontroller)
- 128 KBytes EPROM
- 128 KBytes SRAM
- 512 KBytes SRAM, EEPROM, FLASH EPROM, EPROM
- 240 Bytes of serial SRAM
- 1 KBytes of serial EEPROM

The card memory configuration must be chosen considering the application to realize or the specific requirements of the user. Normally the card is equipped with 128 KBytes of SRAM, 512 Bytes of serial EEPROM, 240 Bytes of serial SRAM and 256 Bytes of internal RAM; all different configurations must be specified by the user, at the moment of the order.

Thanks to the on board Back up circuit, there is the possibility to keep data in the 128K and 240 Bytes of SRAM also when power supply is off. In this way the card is always able to maintain parameters, logged data, system status and configuration, and so on., without using an expensive external UPS. The Back up circuit takes energy from on board Lithium battery and/or from an external battery, connected through a specific connector. Whenever the amount of backed memory is not sufficient (i.e. for data logging systems), it could be used some additional devices of backed SRAM and/or EEPROM.

Furthermore the serial SRAM module mounted on IC23 is provided of an internal Real Time Clock capable to manage by software the time (hours, minutes, seconds) and date (day, month, year, week day).

The addressing of memory devices is controlled by a specific on board circuit, named MMU, that provides to allocate the devices in the microcontroller address space; this control logic manages in a complete automatic mode some different maps required by the software development tools available for GPC® 550.

For further information about memory allocations and access please refer to paragraphs ADDRESSES AND MAPS and MEMORY MANAGEMENT UNIT. While for detailed info on device types, sockets description and jumpers connection, please refer to chapter MEMORY SELECTION paragraph.

A/D CONVERTER

The A/D conversion on GPC® 550 is based on the ADC section that is integrated in the microcontroller. It converts 8 analog signals with the following features: 10 bits of resolution; 27 µsec conversion time on single channel; 20 Ksps sample rate for each channel; SAR technique; end of conversion interrupt; easy software management.

The analog inputs can be voltage inputs (0÷2.49V) or current inputs (0÷20 mA or 4÷20 mA) through an optional current to voltage converter. Default is 8 voltage inputs with 2.49V full range.

By software the User selects the channel to convert, starts the conversion and controls the end of conversion, through programmation of two microcontroller internal registers. In order to simplify and speed up the A/D converter management, some software tools provide utility procedures that cover the typical application requirements.
FIGURE 2: BLOCK DIAGRAM
CONTROL LOGIC

The mapping and the management of all peripheral devices and of some memories on GPC® 550 are assigned to a specific control logic that allocates all these devices in the microcontroller addressing space.
For further information please refer to I/O ADDRESSES paragraph and PERIPHERAL DEVICES SOFTWARE DESCRIPTION chapter of this manual.

ABACO® BUS

One of the most important features of GPC® 550 is the possibility to be interfaced to industrial ABACO® BUS. Through this standard connector, the card can be connected to some of the numerous grifo® boards, both intelligent and not. For example the User can directly use cards for analog signals acquisition (A/D), cards for analog signals generation (D/A), cards with counters and timers, cards for buffered I/O signals management, cards for axis controls, cards for temperature controls, etc.
By using mother boards as the ABB 03 and ABB 05 it is also possible to manage all the peripheral cards in BLOCK format, which are provided with ABACO® I/O BUS interface. So, GPC® 550 becomes the right component for many industrial automation systems, in fact ABACO® BUS makes the card easily expandable with the best price/performance ratio.
Please remark that all ABACO® BUS signals are buffered to warrant a greater immunity against noise and the possibility to drive a higher number of peripheral cards, without typical fan-out problems.
The figure 45 shows some of the grifo® expansion cards and how they can be easily interconnected in a single system.

DIGITAL I/O LINES

The card is provided with two digital I/O controllers used to drive some on board resources (serial EEPROM, serial RTC+SRAM, software serial line, etc.) and 40 digital TTL I/O lines available for the user:
- 16 lines are connected to microcontroller PORT secion and have selectable direction for each line,
- 24 lines are connected to PPI 82C55 and have selectable direction for groups of 8 lines.
These lines are connected directly to two 20 pins connectors with standard I/O ABACO® pin out connectors, in order to be connected directly to several interface cards.
Through software it is possible to define the function of these lines, and also to link them to card’s peripherals (as Timers Counters, Interrupts, hardware I2C BUS, etc.), by simply programming some microcontroller internal registers.
Please remind that on GPC® 550 can be available 8 additional TTL input lines alternative to analog inputs and 2 additional TTL output lines alternative to PWM outputs; if the application requires more than 40 I/O signals but not A/D nor PWM, the above mentioned lines are available through a proper software management.
For further information please refer to paragraphs CONNECTIONS, DIGITAL I/O INTERFACES and PERIPHERAL DEVICES SOFTWARE DESCRIPTION chapter.
CLOCK

On GPC® 550 there are three separate clock circuits:
- The first is based on a crystal that generates the clock frequency for the microcontroller that is used also to generate the frequency for integrated peripherals (as Timer, Serial line, hardware I2C BUS, PWM, etc.). Standard value of this clock frequency is 22.1184 MHz, that is equal to the crystal mounted on board; the power management registers of microcontroller can be set by software to change clock and so consumption of the several peripherals. For specific requirements, a different clock value for microcontroller can be ordered, but it must be first agreed directly with grifo®. 
- The second circuit is based on a 24 MHz crystal that generates all the frequencies used by CAN controller. This circuit is optional and it is installed only when the option .CAN is ordered, while its value is the result of a careful desing and long experimentation.
- The third circuit generates the correct timing for the on board Real Time Clock. Its based on a typical 32.768 kHz crystal.

The choice of using three circuits and three separated crystals, has the advantage to change the microcontroller working speed (when best performances are required) without additional changes in software, firmware, etc.

BOARD CONFIGURATION

An 8 ways dip switch has been introduced expressly to make the board, and in detail the application program, configurable. The possibility to read by software the status of 7 of these selectors give the user the ability to manage many different conditions by an unique program, without loosing other input signals (typical applications are: language choice, program parameters definition, operating mode selection, etc.).

Some software tools developed for GPC® 550 use one of the switches to select the RUN or DEBUG operating modalities, as described in the manuals of the tools themselves.

In addition the board is provided with three activity LEDs and one buzzer, all software driven, that can be used to signal in visual and acoustic ways the current board status and configuration, as described in the specific paragraphs.

All the configuration resources described are completely software manageable by simply programming specific registers allocated in the I/O space.

PWM LINES

On the board there are two indipendent PWM lines that generate signals with software selectable frequency and duty cycle with 8 bits resolution. Typical applications of these signals are motor speed control (in fact several motor drivers have compatible inputs) or analog signals generation (easily obtained, by just adding an integrator circuit). Both lines are available on a low profile connector in order to simplify the connection and they are managed through three microcontroller internal registers.

For further information the user can refer to specific documentation of manufacturer.
SERIAL COMMUNICATION

On GPC® 550 are available several interfaces for serial communication, as the I2C BUS lines, the CAN line and two asynchronous lines. The first two lines are described in the following paragraphs, while the remaining are completely software configurable by the programmer.

By convention, asynchronous communication lines are named A (hardware serial line managed by microcontroller internal UART whose baud rate can be set up to 115200 and bits per character can be 8 or 9, by programming proper registers) and B (software serial line two I/O signals whose baud rate, bits per character, stop bits and parity are all defined by the same management software). When required, it is also possible (through some software trick) to set parity and stop bits number even for serial line A: this allows to communicate with all the devices available on the market.

By hardware it is possible to select the electric protocol, through a comfortable set of jumpers and drivers to install. In detail line B is always buffered in RS 232, while line A can be buffered in Current Loop, RS 232, RS 422 or RS 485; in these last two cases also activation and direction of line can be defined. If an RS 232 line with two handshakes is needed, it is possible to use the two communication lines of serial B that will act as RTS, CTS, DTR, RI, etc. by software management.

Please remind that in default configuration the board is provided with both serial lines in RS 232, so any different configuration must be specified in the order.

For further information about serial communication please refer to paragraphs: CONNECTIONS, SERIAL COMMUNICATION SELECTION and SOFTWARE SERIAL B.

I2C BUS LINES

GPC® 550 is provided with two synchronous I2C BUS serial lines that allow the connection to several devices that feature the same kind of interface.

One line is hardware, or in other word controlled by a specific section integrated in the microcontroller, with the following features:

- bidirectional data transfer between master and slave units;
- multimaster mode;
- line arbitration in case of collision with no data loss;
- synchronization amongst devices at different speeds;
- programmable bit rate up to 1.8M Bit/sec;
- high level management of master transmission and slave transmission;
- high level management of master reception and slave reception;
- interrupt generation when several conditions occur.

Second line is managed by software and it is driven by two TTL I/O lines of the microcontroller, as described in chapter PERIPHERAL DEVICES SOFTWARE DESCRIPTION. This line is already connected to both I2C BUS devices of the board: serial EEPROM and serial RTC+SRAM.

Both I2C lines are available on comfortable low profile connectors, where also power supply is present, in order to allow a quick connection to other units of the system.

The I2C BUS lines are completely software configurable by simply programming some microcontroller's internal registers.
CAN LINE

This section is based on the powerful controller PHILIPS SJA 1000 and is charged to manage all aspects and modalities of CAN protocol. The overall features are:

- support for protocol BasicCAN;
- support for protocol PeliCAN 2.0B;
- support for 11 and 29 bits identifiers;
- 13 bytes transmission buffer;
- 64 bytes reception buffer;
- baud rate programmable up to 1M Bit/sec;
- no reception comparator;
- programmable messages acceptance filters;
- programmable output driver;
- 24 MHz work frequency.

About electric point of view, the board is provided with line driver PHILIPS 82C250, galvanically isolated. This component is compliant to CAN protocol and manages the connection to the field in autonomy without need of software intervene.

On board CAN line is galvanically isolated from other circuits of the card in order to warrant immunity against noise from the field; this feature is essential for connections to remote systems supplied from different sources or when connection cables must run across noisy environments. A specific DC/DC converter generates the galvanically isolated voltages required from the line driver while the interface to CAN controller lines are performed through high frequency optocouplers. CAN lines connection to the field is made through a 3 pins quick release screw terminal connector that warrants a good signal transmission.

Please remind that CAN section is optional and it is installed only when specified in the order, by the proper code .CAN.

By software, CAN controller is completely configurable through 64 registers located in I/O space from control logic and it is able to generate interrupts when several conditions occur. For more information the user can refer to specific documentation of manufacturer.
TECHNICAL FEATURES

GENERAL FEATURES

On board resources:
- 16 digital TTL input/output
- 24 digital TTL input/output
- 3 timer counter with 16 bits resolution
- 1 RS 232 sw serial line (B)
- 1 RS 232, RS 422, RS 485 or Current Loop hw serial line (A)
- 2 I2C BUS lines
- 1 CAN line
- 8 A/D converter lines
- 2 PWM lines
- 3 software manageable LEDs
- 1 Real Time Clock
- 1 buzzer
- 1 dip switch with 8 ways
- 1 reset and power good circuit
- 1 back up circuit

Memories:
- IC25: internal RAM 256 Bytes
- IC19: EPROM from 32K x 8 to 128K x 8
- IC7: SRAM 128K x 8
- IC18: FLASH, EEPROM, SRAM, EPROM from 32K x 8 to 512K x 8
- IC23: serial SRAM 240 Bytes
- U16: serial EEPROM from 256 Bytes to 1K Bytes

Access time of memories: 120 nsec
Microcontroller: PHILIPS P80C552
Microc. clock frequency: 22.1184 MHz
Highest counters frequency: Microcontroller clock frequency / 12
CAN clock frequency: 24 MHz
CAN highest bitrate: 1 Mbit
A/D inputs cut-off frequency: 1 MHz
A/D resolution: 10 bit
A/D conversion time: 27 µsec
A/D total error: ±1 point
RTC frequency: 32.768 KHz
Reset time: 200 msec
Watch dog intervent time: 1.111±283.305 msec

PHYSICAL FEATURES

Size (W x H x D):
- EUROCARD format 100 x 160 x 20
- 100 x 172 x 20 outline (base configuration)

Weight: 150 g
Connectors:

- CN1: 20 pins low profile vertical male
- CN2: 20 pins low profile vertical male
- CN3: 20 pins low profile vertical male
- CN4A: Plug 6 pins 90° female
- CN4B: Plug 6 pins 90° female
- CN5: 64 pins DIN 41612 type C 90° male
- CN7: 20 pins low profile vertical male
- CN8: 3pins quick release screw terminal connector
- CN9: 2 pins low profile vertical male

Temperature range: from 0 to 70 centigrad degreeses
Relative humidity: 20% up to 90% (without condense)

**ELECTRIC FEATURES**

Power supply: 5 Vdc ±5%
Current consumption on +5 Vdc:
- 250 mA * (default configuration)
- 180 mA * (power down)
- 340 mA * (maximum)

Power good intervent threshold: 4.65 V
On board back up battery: 3.0 Vdc; 1/2 AA
External back up battery: 3.6+5 Vdc
Back up current:
- 4.0 µA (on board battery)
- 4.8 µA (external 3.6 Vdc battery)

A/D reference voltage: 0÷2.490 V
Voltage analog inputs: 0÷2.490 V
Current analog inputs: 0÷20; 4÷20 mA (with conversion module)

Analog inputs impedance: High (not declared by manufacturer)

**RS 422-485 termination network:**
- Line termination resistor =120 Ω
- Positive pull up resistor =3.3 KΩ
- Negative pull down resistor =3.3 KΩ

**CAN line impedance:** 60 Ω

**CAN termination network:** 120 Ω resistor, disconnectable

**Pull up resistor on TTL digital I/O:** 100 KΩ
**Pull up resistor on HW I2C BUS:** 100 KΩ
**Pull up resistor on SW I2C BUS:** 4.7 KΩ

* These data coincide with the highest consumption in the described condition and they refer to a 20°C work temperature (for further information please refer to chapter POWER SUPPLY).
INSTALLATION

In this chapter there are the information for a right installation and correct use of the card. The user can find the location and functions of each connectors, LEDs, jumpers, trimmers, etc. available on GPC®550.

CONNECTIONS

The GPC®550 module has 9 connectors that can be linked to other devices or directly to the field, according to system requirements. In this paragraph there are the connectors pin outs, a short signals description (including the signals direction); in order to easily locate the connectors, please see figure 26 while for details about connections types, please refer to following diagrams that explain the links performed on the board.

CN9 - BACK UP EXTERNAL BATTERY CONNECTOR

CN9 is a 2 pins, male, vertical, low profile connector with 2.54 mm pitch. Through CN9 the user can connect an external battery for SRAMs and Real Time Clock back up when the power supply is switched off (for further information please refer to BACK UP paragraph).

![Figure 3: CN9 - Back up external battery connector](image)

Signals description:

<table>
<thead>
<tr>
<th>Signal</th>
<th>Pin</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>+Vbat</td>
<td>1</td>
<td>Back up external battery positive pin</td>
</tr>
<tr>
<td>GND</td>
<td>2</td>
<td>Back up external battery negative pin</td>
</tr>
</tbody>
</table>

Among the board accessories there is the .LITIO that is an external lithium battery, featured by an high capacity and provided with a cable already terminated with a female connector suitable for CN9. It is a ready to use battery that ensures long time data retention on the board.
CN3 - PPI I/O AND SW I2C BUS CONNECTOR

CN3 is a 20 pins, male, 90°, low profile connector with 2.54 mm pitch. On CN3 are available 8 digital I/O lines of the PPI 82C55 interface, the I2C BUS software line and the RTC interrupt signal. All these signals follow the TTL electric standard and the normalized I/O ABACO® pin out.

**Figure 4: CN3 - PPI I/O and SW I2C BUS Connector**

<table>
<thead>
<tr>
<th>Signal</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>PPI PB.n</td>
<td>I/O - Digital line n of PPI 82C55 port B.</td>
</tr>
<tr>
<td>SW SDA</td>
<td>I/O - Data signal of I2C BUS software serial line.</td>
</tr>
<tr>
<td>SW SCL</td>
<td>I/O - Clock signal of I2C BUS software serial line.</td>
</tr>
<tr>
<td>/INT RTC</td>
<td>O - Real time clock generated interrupt.</td>
</tr>
<tr>
<td>+5 Vdc</td>
<td>O - +5 Vdc power supply.</td>
</tr>
<tr>
<td>GND</td>
<td>- Ground signal.</td>
</tr>
<tr>
<td>N.C.</td>
<td>- Not connected.</td>
</tr>
</tbody>
</table>
CN7 - PPI I/O CONNECTOR

CN7 is a 20 pins, male, vertical, low profile connector with 2.54 mm pitch. On CN7 are available 16 digital I/O lines of the PPI 82C55 interface, grouped in two parallel Ports with 8 Bits wide. All these signals follow the TTL electric standard and the normalized I/O ABACO® pin out.

<table>
<thead>
<tr>
<th>PPI PA.1</th>
<th>1</th>
<th>2</th>
<th>PPI PA.0</th>
</tr>
</thead>
<tbody>
<tr>
<td>PPI PA.3</td>
<td>3</td>
<td>4</td>
<td>PPI PA.2</td>
</tr>
<tr>
<td>PPI PA.5</td>
<td>5</td>
<td>6</td>
<td>PPI PA.4</td>
</tr>
<tr>
<td>PPI PA.7</td>
<td>7</td>
<td>8</td>
<td>PPI PA.6</td>
</tr>
<tr>
<td>PPI PC.6</td>
<td>9</td>
<td>10</td>
<td>PPI PC.7</td>
</tr>
<tr>
<td>PPI PC.4</td>
<td>11</td>
<td>12</td>
<td>PPI PC.5</td>
</tr>
<tr>
<td>PPI PC.2</td>
<td>13</td>
<td>14</td>
<td>PPI PC.3</td>
</tr>
<tr>
<td>PPI PC.0</td>
<td>15</td>
<td>16</td>
<td>PPI PC.1</td>
</tr>
<tr>
<td>GND</td>
<td>17</td>
<td>18</td>
<td>+5Vdc</td>
</tr>
<tr>
<td>N.C.</td>
<td>19</td>
<td>20</td>
<td>N.C.</td>
</tr>
</tbody>
</table>

FIGURE 5: CN7 - PPI I/O CONNECTOR

Signals description:

- **PPI PA.n** = I/O - Digital line n of PPI 82C55 port A.
- **PPI PC.n** = I/O - Digital line n of PPI 82C55 port C.
- **+5 Vdc** = O - +5 Vdc power supply.
- **GND** = - Ground signal.
- **N.C.** = - Not connected.
FIGURE 6: PPI BLOCK DIAGRAM
CN1 - CPU I/O CONNECTOR

CN1 is a 20 pins, male, vertical, low profile connector with 2.54 mm pitch. On CN1 are available microcontroller Port 1 and 4, equal to 16 digital I/O lines. Some pins of this connector have multiple purposes, in fact several internal sections can be multiplexed with I/O signals by software programming. All these signals follow the TTL electric standard and the normalized I/O ABACO® pin out.

**FIGURE 7: CN1 - CPU I/O CONNECTOR**

Signals description:

- **P1.n** = I/O - Digital line n of microcontroller Port 1.
- **P4.n** = I/O - Digital line n of microcontroller Port 4.
- **CMSRn** = O - Line n for compare and set/reset on a match from microcontroller Timer 2.
- **CMTn** = O - Line n for compare and toggle on a match from microcontroller Timer 2.
- **CTnI** = I - Line n for capture from microcontroller Timer 2.
- **HW SDA** = I/O - Data signal of I2C BUS hardware serial line.
- **HW SCL** = I/O - Clock signal of I2C BUS hardware serial line.
- **T2** = I - Counter signal of microcontroller Timer 2.
- **RT2** = I - Reset counter signal of microcontroller Timer 2.
- **+5 Vdc** = O - +5 Vdc power supply.
- **GND** = - Ground signal.
- **N.C.** = - Not connected.
FIGURE 8: CPU I/O SIGNALS BLOCK DIAGRAM

- **CN1**
  - PIN 1-8
  - PIN 9-16

- **CN2**
  - PIN 2, 4

- **CN3**
  - PIN 9-11
  - SW I2C BUS LINE
  - ON BOARD I2C BUS DEVICES

**CPU 80C552**

- **PORT 4**
  - 8 TTL LINES

- **PORT 1**
  - 8 TTL LINES

- **PORT 3**
  - 2 TTL LINES

- **PWM0**
- **PWM1**

- **Internal MUX**

- **TIMERS COUNTERS**

- **HW I2C BUS**

- **PWM**

- **I/O PORTS**

- **INTERRUPTS CONTROLLER**

**ITSC TECHNOLOGY**
**CN4A - SERIAL LINE A CONNECTOR**

CN4A is a 6 pins PLUG, 90°, female connector. On this connector there are the signals for communication in RS 232, RS 422, RS 485, Current Loop, performed through hardware serial line A, connected to microcontroller internal UART. Signals placement has been designed in order to reduce interferences and electrical noises and to simplify the connections with other system; the electric protocols follow the CCITT directives of the used standard.

Male connectors for CN4A are directly available between grifo® accessories, and it can be ordered by using the codes **CCR.Plugxxx**, as described in APPENDIX C of the manual. For further information on serial communication please refer to figure 19 and to SERIAL COMMUNICATION SELECTION paragraph.

![Figure 9: CN4A - Serial line A connector](image)

**Signals description:**

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RS 232 serial line A:</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>RXA RS232</td>
<td>I</td>
<td>Receive data for RS 232 hardware serial line A.</td>
</tr>
<tr>
<td>2</td>
<td>TXA RS232</td>
<td>O</td>
<td>Transmit data for RS 232 hardware serial line A.</td>
</tr>
<tr>
<td>6</td>
<td>GND</td>
<td></td>
<td>Ground signal.</td>
</tr>
<tr>
<td>RS 422 serial line A:</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>RXA- RS422</td>
<td>I</td>
<td>Negative receive data for RS 422 hardware serial line A.</td>
</tr>
<tr>
<td>5</td>
<td>RXA+ RS422</td>
<td>I</td>
<td>Positive receive data for RS 422 hardware serial line A.</td>
</tr>
<tr>
<td>3</td>
<td>TXA- RS422</td>
<td>O</td>
<td>Negative transmit data for RS 422 hardware serial line A.</td>
</tr>
<tr>
<td>2</td>
<td>TXA+ RS422</td>
<td>O</td>
<td>Positive transmit data for RS 422 hardware serial line A.</td>
</tr>
<tr>
<td>6</td>
<td>GND</td>
<td></td>
<td>Ground signal.</td>
</tr>
<tr>
<td>RS 485 serial line A:</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>RXTXA+ RS485</td>
<td>I/O</td>
<td>Positive receive and trasmit data for RS 485 hardware serial line A.</td>
</tr>
<tr>
<td>5</td>
<td>RXTXA- RS485</td>
<td>I/O</td>
<td>Negative receive and trasmit data for RS 485 hardware serial line A.</td>
</tr>
<tr>
<td>6</td>
<td>GND</td>
<td></td>
<td>Ground signal.</td>
</tr>
<tr>
<td>Pin</td>
<td>Signal</td>
<td>Direction</td>
<td>Description</td>
</tr>
<tr>
<td>-----</td>
<td>---------</td>
<td>-----------</td>
<td>-------------</td>
</tr>
<tr>
<td>1</td>
<td>+5 Vdc , GND</td>
<td>O</td>
<td>- +5 Vdc power supply signal or ground signal (according with J19).</td>
</tr>
<tr>
<td>4</td>
<td>RXA- C.L.</td>
<td>I</td>
<td>- Negative receive data for Current Loop hardware serial line A.</td>
</tr>
<tr>
<td>5</td>
<td>RXA+ C.L.</td>
<td>I</td>
<td>- Positive receive data for Current Loop hardware serial line A.</td>
</tr>
<tr>
<td>2</td>
<td>TXA- C.L.</td>
<td>O</td>
<td>- Negative transmit data for Current Loop hardware serial line A.</td>
</tr>
<tr>
<td>3</td>
<td>TXA+ C.L.</td>
<td>O</td>
<td>- Positive transmit data for Current Loop hardware serial line A.</td>
</tr>
</tbody>
</table>

**Power supply voltages:**

**Figure 10: Components map on solder side**
Figure 11: RS 232 point to point connection example

Figure 12: RS 422 point to point connection example

Figure 13: RS 485 point to point connection example
Please remark that in a RS 485 network two forcing resistors must be connected across the net and two termination resistors (120 Ω) must be placed at its extremis, respectively near the Master unit and the Slave unit at the greatest distance from the Master. 

Forcing and terminating circuitry is installed on GPC® 550 board. It can be enabled or disabled through specific jumpers, as explained later.

About termination resistor of Master unit, connect it only if not already present (for example many RS 232-RS 485 converters already have it inside).

For further information please refer to TExAS INSTRUMENTS Data-Book, "RS 422 and RS 485 Interface Circuits", the introduction about RS 422-485.
**Figure 15:** Current loop 4 wires point-to-point connection example

**Figure 16:** Current loop 2 wires point-to-point connection example
Possible Current Loop connections are two: 2 wires and 4 wires. These connections are shown in figures 15+17 where it is possible to see the voltage for the loop (VCL) and the resistors for current limitation (R). The values of both these components change in compliance with the number of connected devices and voltage drop on the connection cable. The choice of their values must be done considering that:
- circulation of a 20 mA current must be guaranteed;
- potential drop on each transmitter is about 2.35 V with a 20 mA current;
- potential drop on each receiver is about 2.52 V with a 20 mA current;
- in case of shortcircuit each transmitter must dissipate at most 125 mW;
- in case of shortcircuit each receiver must dissipate at most 90 mW.
For further info please refer to HEWLETT-PACKARD Data Book, (HCPL 4100 and 4200 devices).
CN4B - SERIAL LINE B CONNECTOR

CN4B is a 6 pins, female, 90°, PLUG connector. On this connector there are the signals for communication in RS 232 performed through software serial line B. Signals placement has been designed in order to reduce interferences and electrical noises and to simplify the connections with other system; the electric protocols follow the CCITT directives of RS 232 standard.

Male connectors for CN4B are directly available between grifo® accessories, and it can be ordered by using the codes CCR.Plugxxx, as described in APPENDIX C of the manual. For further information on serial communication please refer to figure 19 and to SERIAL COMMUNICATION SELECTION paragraph.

**Figure 18: CN4B - Serial Line B Connector.**

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RS 232 serial line B:</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>RXB RS232</td>
<td>I</td>
<td>- Receive data for RS 232 software serial line B.</td>
</tr>
<tr>
<td>2</td>
<td>TXB RS232</td>
<td>O</td>
<td>- Transmit data for RS 232 software serial line B.</td>
</tr>
<tr>
<td>6</td>
<td>GND</td>
<td></td>
<td>- Ground signal.</td>
</tr>
</tbody>
</table>

**Power supply voltages:**

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>+5 Vdc , GND</td>
<td>O</td>
<td>- +5 Vdc power supply signal or ground signal (according with J18).</td>
</tr>
<tr>
<td>6</td>
<td>GND</td>
<td></td>
<td>- Ground signal.</td>
</tr>
<tr>
<td>3</td>
<td>N.C.</td>
<td></td>
<td>- Not Connected.</td>
</tr>
<tr>
<td>4</td>
<td>N.C.</td>
<td></td>
<td>- Not Connected.</td>
</tr>
</tbody>
</table>
**Figure 19: Serial Communication Block Diagram**
CN5 - CONNECTOR FOR ABACO® BUS

CN5 is a 64 pins, male, 90°, DIN 41612, type C, A+C rows, with 2.54 mm pitch. On this connector are available all the signals of industrial ABACO® BUS and it can be used for connections to many other peripheral cards. In the table below there are the standard pin outs both for 8 bits and 16 bits CPU and the signals connected on GPC® 550. All signals follow TTL standard, except the power supplies.

<table>
<thead>
<tr>
<th>A row 16 bits BUS</th>
<th>A row 8 bits BUS</th>
<th>A row GPC 550</th>
<th>PIN</th>
<th>C row GPC 550</th>
<th>C row 8 bits BUS</th>
<th>C row 16 bits BUS</th>
</tr>
</thead>
<tbody>
<tr>
<td>GND</td>
<td>GND</td>
<td>GND</td>
<td>1</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
</tr>
<tr>
<td>+5 Vdc</td>
<td>+5 Vdc</td>
<td>+5 Vdc</td>
<td>2</td>
<td>+5 Vdc</td>
<td>+5 Vdc</td>
<td>+5 Vdc</td>
</tr>
<tr>
<td>D0</td>
<td>D0</td>
<td>D0</td>
<td>3</td>
<td>N.C.</td>
<td>-</td>
<td>D8</td>
</tr>
<tr>
<td>D1</td>
<td>D1</td>
<td>D1</td>
<td>4</td>
<td>N.C.</td>
<td>-</td>
<td>D9</td>
</tr>
<tr>
<td>D2</td>
<td>D2</td>
<td>D2</td>
<td>5</td>
<td>N.C.</td>
<td>/INT</td>
<td>D10</td>
</tr>
<tr>
<td>D3</td>
<td>D3</td>
<td>D3</td>
<td>6</td>
<td>N.C.</td>
<td>/INT</td>
<td></td>
</tr>
<tr>
<td>D4</td>
<td>D4</td>
<td>D4</td>
<td>7</td>
<td>N.C.</td>
<td>/NMI</td>
<td>/NMI</td>
</tr>
<tr>
<td>D5</td>
<td>D5</td>
<td>D5</td>
<td>8</td>
<td>N.C.</td>
<td>/HALT</td>
<td>D11</td>
</tr>
<tr>
<td>D6</td>
<td>D6</td>
<td>D6</td>
<td>9</td>
<td>N.C.</td>
<td>/MREQ</td>
<td>/MREQ</td>
</tr>
<tr>
<td>D7</td>
<td>D7</td>
<td>D7</td>
<td>10</td>
<td>/IORQ</td>
<td>/IORQ</td>
<td>/IORQ</td>
</tr>
<tr>
<td>A0</td>
<td>A0</td>
<td>A0</td>
<td>11</td>
<td>/RD</td>
<td>/RD</td>
<td>/RDLDS</td>
</tr>
<tr>
<td>A1</td>
<td>A1</td>
<td>A1</td>
<td>12</td>
<td>WR</td>
<td>/WR</td>
<td>/WRLDS</td>
</tr>
<tr>
<td>A2</td>
<td>A2</td>
<td>A2</td>
<td>13</td>
<td>N.C.</td>
<td>/BUSAK</td>
<td>D12</td>
</tr>
<tr>
<td>A3</td>
<td>A3</td>
<td>A3</td>
<td>14</td>
<td>N.C.</td>
<td>/WAIT</td>
<td>/WAIT</td>
</tr>
<tr>
<td>A4</td>
<td>A4</td>
<td>A4</td>
<td>15</td>
<td>N.C.</td>
<td>/BUSRQ</td>
<td>D13</td>
</tr>
<tr>
<td>A5</td>
<td>A5</td>
<td>A5</td>
<td>16</td>
<td>/RESET</td>
<td>/RESET</td>
<td>/RESET</td>
</tr>
<tr>
<td>A6</td>
<td>A6</td>
<td>A6</td>
<td>17</td>
<td>N.C.</td>
<td>/M1</td>
<td>/IACK</td>
</tr>
<tr>
<td>A7</td>
<td>A7</td>
<td>A7</td>
<td>18</td>
<td>N.C.</td>
<td>/RFSH</td>
<td>D14</td>
</tr>
<tr>
<td>A8</td>
<td>A8</td>
<td>N.C.</td>
<td>19</td>
<td>N.C.</td>
<td>/MEMDIS</td>
<td>/MEMDIS</td>
</tr>
<tr>
<td>A9</td>
<td>A9</td>
<td>N.C.</td>
<td>20</td>
<td>N.C.</td>
<td>VDUSEL</td>
<td>A22</td>
</tr>
<tr>
<td>A10</td>
<td>A10</td>
<td>N.C.</td>
<td>21</td>
<td>N.C.</td>
<td>/EI</td>
<td>D15</td>
</tr>
<tr>
<td>A11</td>
<td>A11</td>
<td>N.C.</td>
<td>22</td>
<td>N.C.</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>A12</td>
<td>A12</td>
<td>N.C.</td>
<td>23</td>
<td>N.C.</td>
<td>CLK</td>
<td>CLK</td>
</tr>
<tr>
<td>A13</td>
<td>A13</td>
<td>N.C.</td>
<td>24</td>
<td>N.C.</td>
<td>-</td>
<td>/RDUDS</td>
</tr>
<tr>
<td>A14</td>
<td>A14</td>
<td>N.C.</td>
<td>25</td>
<td>N.C.</td>
<td>-</td>
<td>/WRUDS</td>
</tr>
<tr>
<td>A15</td>
<td>A15</td>
<td>N.C.</td>
<td>26</td>
<td>N.C.</td>
<td>-</td>
<td>A21</td>
</tr>
<tr>
<td>A16</td>
<td>-</td>
<td>N.C.</td>
<td>27</td>
<td>N.C.</td>
<td>-</td>
<td>A20</td>
</tr>
<tr>
<td>A17</td>
<td>-</td>
<td>N.C.</td>
<td>28</td>
<td>N.C.</td>
<td>-</td>
<td>A19</td>
</tr>
<tr>
<td>+12 Vdc</td>
<td>+12 Vdc</td>
<td>N.C.</td>
<td>30</td>
<td>N.C.</td>
<td>-12 Vdc</td>
<td>-12 Vdc</td>
</tr>
<tr>
<td>+5 Vdc</td>
<td>+5 Vdc</td>
<td>+5 Vdc</td>
<td>31</td>
<td>+5 Vdc</td>
<td>+5 Vdc</td>
<td>+5 Vdc</td>
</tr>
<tr>
<td>GND</td>
<td>GND</td>
<td>GND</td>
<td>32</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
</tr>
</tbody>
</table>

**FIGURE 20: CN5 - ABACO® BUS CONNECTOR**
Signals description:

8 bits CPU

A0-A15 = O - Address BUS
D0-D7 = I/O - Data BUS
/INT = I - Interrupt request
/NMI = I - Non Maskable Interrupt
/HALT = O - Halt state
/MREQ = O - Memory Request
/ORQ = O - Input Output Request
/RD = O - Read cycle status
/WR = O - Write cycle status
/BUSAK = O - BUS Acknowledge
/WAIT = I - Wait
/BUSRQ = I - BUS Request
/RESET = O - Reset
/M1 = O - Machine cycle one
/RFSH = O - Refresh for dynamic RAM
/MEMDIS = I - Memory Display
/VDUSEL = O - VDU Selection
/IEI = I - Interrupt Enable Input
/CLK = O - System clock
/R.B. = I - Reset button
/+5 Vdc = I - +5 Vdc power supply
/+12 Vdc = I - +12 Vdc power supply
/-12 Vdc = I - -12 Vdc power supply
/GND = - Ground signal.
/N.C. = - Not connected.

16 bits CPU

A16-A22 = O - Address BUS
D8-D15 = I/O - Data BUS
/RD UDS = O - Read Upper Data Strobe
/WR UDS = O - Write Upper Data Strobe
/IACK = O - Interrupt Acknowledge
/RD LDS = O - Read Lower Data Strobe
/WR LDS = O - Write Lower Data Strobe

NOTE
The direction indications reported in the previous description are referred to a master (GPC® or CPU) board and have been kept untouched in order to avoid ambiguity when multi boards systems must be developed.
CN2 - A/D CONVERTER INPUTS AND PWM SIGNALS CONNECTOR

CN2 is a 20 pins, male, vertical, low profile connector with 2.54 mm pitch. On CN2 are available the two PWM output signals and the 8 analog inputs lines. The last are directly connected to A/D converter section of the microcontroller, they have an high impedance, they are connected to filter capacitor and they accept input signal in the range 0\(\text{÷}2.49\) V. By installing a specific conversione module (that can be ordered with 8420 code), the same connector accepts up to 8 current signals in the range 0\(\text{÷}20\) mA or 4\(\text{÷}20\) mA.

Signals placement is compliant with normalized A/D ABACO® pin out and it has been designed in order to reduce noises and interferences problems, and to warrant a good signals transmission. In addition on CN2 are also available the two PWM lines (8 bits) useful for motor control and generic D/A signals generation.

Several signals of this connector are multipurpose, in fact ADC inputs can be multiplexed with digital I/O TTL signals of Port 5.

![Figure 21: CN2 - A/D CONVERTER INPUTS AND PWM SIGNALS CONNECTOR](image)

Signals description:

- **PWM0** = O - PWM line 0 of microcontroller.
- **PWM1** = O - PWM line 1 of microcontroller.
- **ADCn** = I - Analog input connected to A/D channel n of microcontroller.
- **P5.n** = I - Digital line n of microcontroller Port 5.
- **AGND** = - Analog ground signal.
- **+5 Vdc** = - +5 Vdc power supply.
- **GND** = - Ground signal.
FIGURE 22: A/D CONVERTER BLOCK DIAGRAM
CN8 - CAN LINE CONNECTOR

CN8 is a 3 pins, male, 90°, quick release screw terminal connector, with 3.5 mm pitch. Through CN8 can be connected the card to a CAN serial communication line by obtaining a fast and comfortable node on the field BUS defined by the same protocol. Signal placement has been designed in order to reduce interference and to simplify the connection to the field, by following the normative of the CAN standard.

**Figure 23: CN8 - CAN line connector**

Signals description:

- **CANH** = I/O - Differential line high for CAN interface.
- **CANL** = I/O - Differential line low for CAN interface.
- **CAN GND** = - CAN ground.

**NOTE**

Power supply of CAN section is galvanically isolated from GPC® 550 power supply, so CAN GND must NOT be connected to GND and AGND signals available on the other connectors. For further information please refer to paragraph POWER SUPPLY.
Figure 24: CAN Line Block Diagram

CAN CONTROLLER
SJA1000

OPTO

CAN DRIVER
82C250

CN8

DC/DC CONVERTER
Please remind that a CAN network must have two termination resistors (120 Ω) placed at its extremes, respectively near the master unit and the slave unit at the greatest distance from the master. On GPC® 550 board the terminating circuitry is already installed: it can be connected or not through specific jumper, as explained later, in paragraph JUMPERS.

When the system connected on the CAN line have very different potentials, it is possible to connect also the grounds of the systems, that is pin 1 of CN8, in order to solve possible problems of communication and/or correct working.

**Figure 25: CAN network connection example**
FIGURE 26: CONNECTORS, TRIMMER, BATTERY, MEMORIES, ETC. LOCATION
I/O CONNECTIONS

In order to prevent possible connecting problems between GPC® 550 and the external systems, the user has to read carefully the previous paragraphs information and the joined figures, that show the internal connection diagrams. In addition he must follow all the following instructions:

- For RS 232, RS 422, RS 485, Current Loop and CAN signals the user must follow the standard rules of each one of these protocols.

- For all TTL signals the user must follow the rules of this electric standard and ensure that the connected digital signals are always referred to card digital ground GND. The 0V level corresponds to logic state 0, while 5V level corresponds to logic state 1. Please read ELECTRIC FEATURES paragraph to obtain the values of pull up resistors connected to TTL digital I/O lines of the card.

- The analog inputs of A/D converter section must be connected to signals in the ranges 0 to 2.49 V or 0 to 20 mA. These inputs have high impedance, anyway when an interfacing circuit must be developed and interposed, it is preferable to provide low impedance signals in order to assure greater stability and precision. Please remark that the eight analog inputs on CN2 are provided with filter capacitors that warrant more stability on the acquired signals, but decrease the cutoff frequency to 1 MHz; anyway this is not a real limit, in fact the maximum frequency for A/D acquisition is lower (20 KHz).

- PWM signals are at TTL level, so they must be properly buffered and then connected to power circuits. Typical interfaces can be current drivers (when a PWM signal is still required) or an integrator circuit if analog voltage is required.

- The industrial ABACO® BUS signals are TTL type and they are buffered in order to obtain an higher protection against external noises and to increase the number of peripheral cards that can be connected as expansion. The maximum number of these expansion cards must be properly defined in order to avoid fan out problems. If you require the signals waveforms and timings of the signals available on CN5, please contact directly grifo® technicians; the figure A-6 shows an interesting electric diagram that shows how this connector can be interfaced.

- Also I2C BUS signals are TTL level, as defined by the same standard; for completeness it is remarked that in a network with several devices and rather long, it is better to use the hardware I2C BUS. In fact its output stage, the numerous operational modes and programmable bit rate, allow to communicate in every condition. When an I2C BUS network is realized, it must be noted that both interfaces of GPC® 550 have pull up resistors on the communication signals, as described on figure 28.
I2C BUS LINES CONNECTION

The two I2C BUS synchronous communication lines are available on as many connectors of the card and they can be used for a link to the numerous other devices provided of the same type of interface. In the following figure are listed some of these devices either manufactured by grifo® or by other companies.

Next figure shows in details how different devices can be physically connected on a local I2C BUS network. Please remind that this communication standard must be used only on short distances and inside an electric clean environment. Furthermore we underline that the hardware I2C BUS interface is certainly preferable to software one, in fact it is based on a real controller capable to: recognize and manage possible errors and collisions, support all communication modalities either as master or slave, obtain higher transfer rates, don’t keep busy the CPU, etc.
Please remind that in a I2C BUS network must be connected two pull up resistors at the net extrems, respectively near the master unit and the slave unit at the greatest distance from the master. On GPC® 550 these resistors are always present (*1) in default configuration and they but their values change as described in ELECTRIC FEATURES paragraph. The user must select or configure the I2C BUS devices to connect, by taking care of this feature.

For further information please refer to document "THE I2C-BUS SPECIFICATIONS", from PHILIPS semiconductors.
TRIMMERS AND CALIBRATION

On GPC® 550 is available a trimmer, named RV1 or RV2, that calibrates the reference voltage that is a fundamental part of of the A/D converter section. The card is subjected to a careful post production test that verifies and calibrates all the card sections. This calibration is executed in laboratory, with a controllable +20°C room temperature, by following these steps:

- The A/D voltage reference Vref is calibrated to a value of 2.490 V, through RV1 or RV2 trimmer, by using a 5 digits precision galvanically isolated multimeter, connected on two pins of test point TP1.

- The correspondence between the analog input signal and the combination read from A/D is verified. This check is performed with a certified signal (generated by a proper calibrator) connected to analog inputs and testing that the A/D combination and the theoretical combination differ at maximum, of the A/D section errors sum.

- The trimmer is blocked with paint.

The analog interfaces use high precision components that are selected during mounting phase to avoid complicated and long calibration procedures. For this reason, after the calibration, the on board trimmer is blocked with paint, in order to maintain calibration also in presence of mechanical stresses (vibrations, movements, delivery, etc.). In normal conditions the user must not modify the card calibration, but if thermic drifts, time drifts and so on, make necessary a new calibration, then the user must strictly follow the previous described procedure. The trimmer RV1, RV2 and the test point TP1 can be easily located on board by using figure 26.

TEST POINT

As described in previous paragraph, the board is provided with a test point named TP1, that allows to read, through a galvanically isolated multimeter, the reference voltage calibrated in laboratory at 2.490 V. TP1 is composed by two contacts:

- pin + (external) -> Vref
- pin - (internal) -> AGND

The test point can be easily located on the board through figure 26; the two contacts can be recognized through the component map of the card (or through the indications external and internal, above used, that refer to perimeter of the card). Finally for further information about Vref signal, please refer to TRIMMERS AND CALIBRATION paragraph.
ANALOG INPUTS SELECTION

**GPC® 550** board can accept analog voltage and/or current inputs, as described in previous paragraphs and chapters. The analog input type selection must be defined during the order phase and it is performed by mounting a specific current-voltage conversion module (option code .8420). This module is realized with precision resistors, connected with the following correspondence:

- RR15.0 -> channel 0
- RR15.1 -> channel 1
- RR15.2 -> channel 2
- RR15.3 -> channel 3
- RR15.4 -> channel 4
- RR15.5 -> channel 5
- RR15.6 -> channel 6
- RR15.7 -> channel 7

When the conversion module is not mounted (default configuration) the corresponding channel accepts a voltage input signal in the range 0÷2.49 V; otherwise a current input signal is accepted. The resistors value for the current to voltage converter is calculated with the following formula:

\[ R = \frac{2.49 \text{ V}}{I_{\text{max}}} \]

Usually the value of the precision resistors used in .8420 module is 124Ω suitable for 0÷20 mA or 4÷20 mA analog inputs. Any other possible configuration for \(I_{\text{max}}\) and \(R\), out of this standard, should be directly asked to grifo®.

Please refer to figure 26 for easily locate the current-voltage conversion module and the relative resistors.

DIGITAL I/O INTERFACES

Through CN1, CN3 and CN7 (I/O ABACO® standard connector) the **GPC® 550** card can be connected to the numerous grifo® boards provided of the same standard pin out. Installation of these interfaces is very easy, in fact only a 20 pins flat cable (code FLT.20+20) is required and it carry even the power supply. The software management of the same interfaces is as easy, in fact most of the software packages available for **GPC® 550** are provided with the necessary procedures. These latter ones are “software drivers” or libraries added to programming languages that allow to use directly the high level instructions with their full power.

Remarkable modules directly connectable are:

- QTP 16P, QTP 24P, KDx x24, DEB 01, etc. that solve all the local operator interfacing problems.

These modules are provided with all the resources needed to obtain a high level human machine interface (they include alphanumeric displays, matrix keyboard and visualization LEDs) at a short distance from **GPC® 550** card. The available software drivers allow to manage the operator interface resources directly through the high level instructions for console management.
- **IAC 01, DEB 01**: it is an interface for CENTRONICS parallel printer that can be connected with a standard printer cable. The printer is managed by software through the high level instructions of the selected programming language (LPRINT for BASIC, PRINTF for C, etc.).

- **MCI 64**: it a large mass memory support that can directly manage the PCMCIA memory cards RAM, FLASH, ROM, etc.) in their available sizes. About software the developed drivers provide a complete file system interfacing that allows to access the informations stored in the memory card directly through the high level file management instructions.

- **RBO xx, TBO xx, XBI xx, OBI xx**: these are buffer interfaces for I/O TTL signals. With these modules the TTL input signals are converted in NPN or PNP optoisolated inputs and the TTL output signals are converted in relays or transistor optoisolated outputs.

For more information about digital I/O interfaces, please refer to homonimous products described in *grifo®* web site and in the used software tools documentation.

**VISUAL SIGNALATIONS**

*GPC® 550* is provided of visual signalation described in the following table:

<table>
<thead>
<tr>
<th>LED</th>
<th>COLOUR</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>LD1</td>
<td>Red</td>
<td>Visualizes Real Time Clock interrupt activation</td>
</tr>
<tr>
<td>LD2</td>
<td>Green</td>
<td>Activity LED managed by software</td>
</tr>
<tr>
<td>LD3</td>
<td>Red</td>
<td>Activity LED managed by software</td>
</tr>
<tr>
<td>LD4</td>
<td>Green</td>
<td>Activity LED managed by software</td>
</tr>
</tbody>
</table>

**FIGURE 29: LEDs table**

The main function of LEDs is to inform the user about card status and, in addition to this, visual signalations make easier the debug and test operations of the complete system.

In order to recognize the LEDs location on the card, please refer to figure 26, while for further information on LEDs activation, please refer to paragraphs ACTIVITY LEDS and REAL TIME CLOCK.
JUMPERS

On GPC® 550 there are 17 jumpers, 1 solder jumper and one dip switch for card configuration. By connecting them, the user performs some selections that regard the working condition of the module. Below there is the jumpers list, location and functions in the possible connection modalities:

<table>
<thead>
<tr>
<th>JUMPER</th>
<th>N. PINS</th>
<th>PURPOSE</th>
</tr>
</thead>
<tbody>
<tr>
<td>J1</td>
<td>2</td>
<td>Selects memory map together with J2 and J12.</td>
</tr>
<tr>
<td>J2</td>
<td>2</td>
<td>Selects memory map together with J1 and J12.</td>
</tr>
<tr>
<td>J3</td>
<td>3</td>
<td>Selects memory device installed on IC18, together with J7.</td>
</tr>
<tr>
<td>J4</td>
<td>3</td>
<td>Connects termination circuitry to CAN line.</td>
</tr>
<tr>
<td>J5</td>
<td>4</td>
<td>Selects interrupt source for /INT0.</td>
</tr>
<tr>
<td>J6</td>
<td>3</td>
<td>Manages hardware enable of Watch dog.</td>
</tr>
<tr>
<td>J7</td>
<td>9</td>
<td>Selects memory device installed on IC18, together with J3.</td>
</tr>
<tr>
<td>J10</td>
<td>2</td>
<td>Connects on board battery BT1 to back up circuitry.</td>
</tr>
<tr>
<td>J11, J13</td>
<td>2</td>
<td>Connects serial line A, buffered in RS 232, to connector CN4A.</td>
</tr>
<tr>
<td>J12</td>
<td>2</td>
<td>Selects memory map by software, together with J1 and J2.</td>
</tr>
<tr>
<td>J14, J16</td>
<td>2</td>
<td>Connects termination and forcing circuitry to serial line A in RS 422, RS 485.</td>
</tr>
<tr>
<td>J15</td>
<td>3</td>
<td>Selects direction and operating mode for serial line A in RS 422, RS 485.</td>
</tr>
<tr>
<td>J17</td>
<td>3</td>
<td>Selects electric interface for serial line A.</td>
</tr>
<tr>
<td>J18</td>
<td>3</td>
<td>Selects the connection type for pin 1 of CN4B.</td>
</tr>
<tr>
<td>J19</td>
<td>3</td>
<td>Selects the connection type for pin 1 of CN4A.</td>
</tr>
<tr>
<td>JS1</td>
<td>2</td>
<td>Select ROM code area internal or external to microcontroller.</td>
</tr>
<tr>
<td>DSW1.7</td>
<td>2</td>
<td>Connects circuitry that enables RS 422, RS 485 drivers to proper signal managed by software.</td>
</tr>
</tbody>
</table>

FIGURE 30: JUMPERS SUMMARIZING TABLE

The valid connections and locations of these jumpers can be recognized through the board printed diagram (serigraph) or to figure 34 of this manual, where the pins numeration is listed.
In all the following tables, the "*" denotes the default connection, or on the other hand the connection set up at the end of testing phase, that is the configuration the user receives. The user can check the default configuration of all the modifiable features, also in APPENDIX C at the end of the manual.
Further information about purpose and effects of the jumpers are reported in the following paragraphs, properly organized in the hardware sections they act on.
## 2 PINS JUMPERS

<table>
<thead>
<tr>
<th>JUMPER</th>
<th>CONNECTION</th>
<th>PURPOSE</th>
<th>DEF.</th>
</tr>
</thead>
<tbody>
<tr>
<td>J1</td>
<td>not connected</td>
<td>This jumper selects memory map together with J2 and J12. For further information refer to MEMORY MAPPING paragraph.</td>
<td>*</td>
</tr>
<tr>
<td>J1</td>
<td>connected</td>
<td></td>
<td></td>
</tr>
<tr>
<td>J2</td>
<td>not connected</td>
<td>This jumper selects memory map together with J1 and J12. For further information refer to MEMORY MAPPING paragraph.</td>
<td>*</td>
</tr>
<tr>
<td>J2</td>
<td>connected</td>
<td></td>
<td></td>
</tr>
<tr>
<td>J10</td>
<td>not connected</td>
<td>Does not connect on board battery BT1 to back up circuitry.</td>
<td>*</td>
</tr>
<tr>
<td>J10</td>
<td>connected</td>
<td>Connects on board battery BT1 to back up circuitry.</td>
<td></td>
</tr>
<tr>
<td>J10</td>
<td>connected</td>
<td></td>
<td></td>
</tr>
<tr>
<td>J11, J13</td>
<td>not connected</td>
<td>Do not connect serial line A, buffered in RS 232, to specific pins on CN4A.</td>
<td>*</td>
</tr>
<tr>
<td>J11, J13</td>
<td>connected</td>
<td>Connect serial line A, buffered in RS 232, to specific pins on CN4A.</td>
<td></td>
</tr>
<tr>
<td>J12</td>
<td>not connected</td>
<td>Memory mapping is selected only by J1 and J2 jumpers.</td>
<td>*</td>
</tr>
<tr>
<td>J12</td>
<td>connected</td>
<td>Connects PWM0 signal to memories mapping circuit in order to allow the memory map selection by software, together with J1 and J2. For further information refer to MEMORY MAPPING paragraph.</td>
<td></td>
</tr>
<tr>
<td>J12</td>
<td>connected</td>
<td></td>
<td></td>
</tr>
<tr>
<td>J14, J16</td>
<td>not connected</td>
<td>Do not connect forcing and termination circuitry to RS 485 receiver/transmitter or to RS 422 receiver of serial line A.</td>
<td>*</td>
</tr>
<tr>
<td>J14, J16</td>
<td>connected</td>
<td>Connect forcing and termination circuitry to RS 485 receiver/transmitter or to RS 422 receiver of serial line A.</td>
<td></td>
</tr>
<tr>
<td>J14, J16</td>
<td>connected</td>
<td></td>
<td></td>
</tr>
<tr>
<td>JS1</td>
<td>not connected</td>
<td>Enables code reading from internal ROM of microcontroller.</td>
<td>*</td>
</tr>
<tr>
<td>JS1</td>
<td>connected</td>
<td>Enables code reading from external ROM of microcontroller = memories of the board.</td>
<td></td>
</tr>
<tr>
<td>JS1</td>
<td>connected</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DSW1.7</td>
<td>OFF</td>
<td>Does not connect signal PWM1 to RS 422, RS 485 abilitation circuit.</td>
<td>*</td>
</tr>
<tr>
<td>DSW1.7</td>
<td>ON</td>
<td>Connects signal PWM1 to RS 422, RS 485 abilitation circuit.</td>
<td></td>
</tr>
<tr>
<td>DSW1.7</td>
<td>ON</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Figure 31: 2 PINS JUMPERS Table**
### 3 PINS JUMPERS

<table>
<thead>
<tr>
<th>JUMPER</th>
<th>CONNECTION</th>
<th>PURPOSE</th>
<th>DEF.</th>
</tr>
</thead>
<tbody>
<tr>
<td>J3</td>
<td>position 1-2</td>
<td>Configures IC18 for memories up to 128K Bytes (see MEMORIES SELECTION paragraph).</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>position 2-3</td>
<td>Configures IC18 for memories larger than 128K Bytes (see MEMORIES SELECTION paragraph).</td>
<td></td>
</tr>
<tr>
<td>J4</td>
<td>position 1-2</td>
<td>Connects 120 Ω termination resistor to CAN line.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>position 2-3</td>
<td>Does not connect 120 Ω termination resistor to CAN line.</td>
<td>*</td>
</tr>
<tr>
<td>J6</td>
<td>position 1-2</td>
<td>Disables by hardware the watch dog circuit.</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>position 2-3</td>
<td>Enables by hardware the watch dog circuit.</td>
<td></td>
</tr>
<tr>
<td>J15</td>
<td>position 1-2</td>
<td>Configures serial line A for RS 485 (half duplex on 2 wires) electric protocol.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>position 2-3</td>
<td>Configures serial line A for RS 422 (full duplex or half duplex on 4 wires) electric protocol.</td>
<td>*</td>
</tr>
<tr>
<td>J17</td>
<td>position 1-2</td>
<td>Configures serial line A for RS 422, RS 485 and Current Loop electric protocols.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>position 2-3</td>
<td>Configures serial line A for RS 232 electric protocol.</td>
<td>*</td>
</tr>
<tr>
<td>J18</td>
<td>position 1-2</td>
<td>Connects pin 1 of CN4B to +5 Vdc.</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>position 2-3</td>
<td>Connects pin 1 of CN4B to GND.</td>
<td></td>
</tr>
<tr>
<td>J19</td>
<td>position 1-2</td>
<td>Connects pin 1 of CN4A to +5 Vdc.</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>position 2-3</td>
<td>Connects pin 1 of CN4A to GND.</td>
<td></td>
</tr>
</tbody>
</table>

### 4 PINS JUMPERS

<table>
<thead>
<tr>
<th>JUMPER</th>
<th>CONNECTION</th>
<th>PURPOSE</th>
<th>DEF.</th>
</tr>
</thead>
<tbody>
<tr>
<td>J5</td>
<td>not connected</td>
<td>Does not connect /INT0 to any interrupt source.</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>position 1-2</td>
<td>Connects /INT0 to interrupt generated by Real Time Clock.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>position 2-3</td>
<td>Connects /INT0 to interrupt generated by CAN controller.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>position 2-4</td>
<td>Connects /INT0 to reception line of software serial line B.</td>
<td></td>
</tr>
</tbody>
</table>

**Figure 32: 3 pins jumpers table**

**Figure 33: 4 pins jumpers table**
FIGURE 34: JUMPERS PLACEMENT AND NUMERATION
9 PINS JUMPERS

<table>
<thead>
<tr>
<th>JUMPER</th>
<th>CONNECTION</th>
<th>PURPOSE</th>
<th>DEF.</th>
</tr>
</thead>
<tbody>
<tr>
<td>J7</td>
<td>position x-x ; 4-5 ; x-x</td>
<td>Configures IC18 for 32K EPROM.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>position 2-3 ; 4-5 ; x-x</td>
<td>Configures IC18 for 64K EPROM.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>position 2-3 ; 4-5 ; NC</td>
<td>Configures IC18 for 128K and 256K EPROM.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>position 2-3 ; 4-5 ; 8-9</td>
<td>Configures IC18 for 512K EPROM.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>position 2-4 ; 5-6 ; x-x</td>
<td>Configures IC18 for 32K SRAM, EEPROM.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>position 2-4 ; 5-6 ; 7-8</td>
<td>Configures IC18 for 128K and 512K SRAM, EEPROM.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>position 1-2 ; 4-5 ; 6-8</td>
<td>Configures IC18 for 32K FLASH EPROM.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>position 2-3 ; 4-5 ; 6-8</td>
<td>Configures IC18 for 128K and 512K FLASH EPROM.</td>
<td></td>
</tr>
</tbody>
</table>

**FIGURE 35: 9 PINS JUMPERS TABLE**

SOLDER JUMPERS

The default configuration of solder jumper JS1 is performed with a thin copper connection on the component side, between the two pods of the same jumper. So if its configuration must be changed, the first time the user must cut this connection by using a sharpened cutter while for the next variation the two pods must be connected or not by using a low power soldering tool, some non corrosive tin and a proper flux.

BACK UP

GPC® 883 is provided with a on board Lithium battery, named BT1, that keeps data on SRAM components and keeps the Real Time Clock counting, also when power supply is switched off. Jumper J10 connects or disconnects the battery to preserve its duration whenever the card is not used or when back up is not required. Through CN9 connector it can be connected a second external battery, that must have an higher voltage than the on board one: configuration of jumper J10 does not affect the working of this battery and it replace BT1 completely.

All the technical features of the back up circuit (useful also for selection of the external battery), are reported in ELECTRIC FEATURES paragraph; while the circuit components locations are described on figure 26.

Among the board accessories there is the .LITIO that is an external lithium battery, featured by an high capacity and provided with a cable ready for CN9 connection. It is a ready to use battery that ensures long time data retention, as described in APPENDIX C.
FIGURE 36: COMPONENTS MAP OF COMPONENT SIDE
INTERRUPTS

A remarkable feature of GPC® 550 card is the powerful interrupt management. Here follows a short description of which devices can generate interrupts with their modalities:

- **Real Time Clock** -> Generates an interrupt on /INT0 of microcontroller when jumper J5 is connected in position 1-2.
- **CAN controller** -> Generates an interrupt on /INT0 of microcontroller when jumper J5 is connected in position 2-3.
- **Software serial line B** -> Generates an interrupt on /INT0 of microcontroller when jumper J5 is connected in position 2-4.
- **Microc. peripherals** -> Generate an internal interrupt. In details these possible interrupt sources are: hardware I2C BUS, A/D converter, Timer 0, Timer 1, Timer 2 and its capture and compare modality, UART for hardware serial line..

An interrupt manager (ICU) allows to enable, disable, mask and prioritize the interrupt sources, so the user has the possibility to respond promptly and efficiently to any external events, even when they are contemporaneous..

For further information about interrupts management please refer to the microcontroller data sheet.

POWER SUPPLY

GPC® 550 must be supplied by a +5 Vdc±5% voltage that must be provided through specific pins of CN5. Board layout has been designed in order to get the single supply by CN5 and to distribute it across the whole card; this explains the directionality reported in connectors descriptions, where the +5 Vdc is an input signal only on CN5 and an output signal on all the other connectors. When the user has specific requirements he can connect the power voltage even through the other connectors, but he must previously verify the correct working of the whole system. For example, to supply the card through CN4A or CN4B (probable condition in networks where an unique cable carries communication signals and supply for all the nodes), jumpers J18 and J19 must be properly configured.

An efficient distributed filtering circuit protects the card against interference and noise from the field, improving the overall system performances.

Please remind that logic supply voltage (+5 Vdc and GND) is galvanically isolated from CAN interface supply voltage. So, signal GND, available on many card connector, must NOT be connected to CAN GND on CN8.

The A/D converter section uses card power supply properly refiltered and redistributed. For shielding and tracks location reasons, the ground of this section is named AGND in order to distinguish it from supply GND, even if they are electrically connected.

In order to reduce the overall card power consumption, it can be enabled the microcontroller power down and idle modes. These modalities allow to reduce the CPU working frequency and can be activated by programming the internal register PCON. Thus the user program can reduce power consumption down to 180 mA and eventually restore the normal working mode when a specific event occurs, like an interrupt, a variation on analog or digital inputs, a timeout elapsed, etc.

For further information please refer to paragraph ELECTRIC FEATURES.
RESET, POWER GOOD, WATCH DOG

On GPC® 550 there are three different reset sources, that can be summarized as below described:

1) Power good circuit that enables reset when power supply voltage goes under the threshold of 4.65 Vdc.
2) External reset button, that must be connected to pin 29 C of CN5 = signal R.B. of ABACO® BUS; it can be a normally open push button that connects signal R.B. to GND when pressed. Its main purpose is the exit from infinite loop conditions during debug phase or to restart the application program without interrupting power supply of the card.
3) Watch Dog circuit, integrated in microcontroller, that is really efficient and easy to use. In detail the most important features of this circuit are:
   - astable functionality;
   - intervent time programmable by software, from 1.111 msec to 283.305 msec;
   - hardware activation through J6 jumper;
   - software retrigger.
   In astable mode, when intervent time is elapsed the circuit become active, it stay active for the reset time and after it is deactivated. The main purpose of this section is to supply a real security to the system controlled by GPC® 550 in order to work correctly in any operating conditions and to avoid dangerous malfunctions not examined during develop phase. In fact if the program is no more executed correctly, it doesn't perform the periodic retrigger of the watch dog circuit and then this become active and it resets the card, as below described. Additional information about Watch dog and retrigger operation, please refer to microcontroller documentation or APPENDIX B of this manual.

According with the source that has enabled the reset circuit, the card acts with specific modality and timings, as described in the following points:

Source = Power good and Reset button (1 and 2):
- the circuit remains active for a reset time = 200 msec;
- all the card's sections are reset to warrant a general start condition;
- the /RESET signal, generated from card and connected to pin 16C of CN5 connector, is activated in order to reset also the possible peripheral cards, connected to ABACO® BUS;
- at the end of reset time the card restart the execution of the program saved on IC19 (EPROM), at the address 0000H of the CPU.

Source = Watch dog (3):
- the circuit remains active for only 2 µsec (sufficient to reset the single microcontroller);
- the card's sections are not reset and they maintain their previous status;
- the /RESET signal, generated from card and connected to pin 16C of CN5 connector, is not activated and the possible peripheral cards, connected to ABACO® BUS are not reset;
- at the end of reset time the card restart the execution of the program saved on IC19 (EPROM), at the address 0000H of the CPU.

A reset circuit provided of the described features ensures correct working of the card and possible connected electronic devices, in any operating conditions, especially during the critical power on and power off phases.
SERIAL COMMUNICATION SELECTION

Serial line B can be buffered only in RS 232 while serial line A can be buffered in RS 232, RS 422, RS 485 or Current Loop. By software on both the serial lines can be defined the physical communication protocol, thanks to management firmware and through the settings of some internal registers of microcontroller. In detail they can be programmed to operate with 8, 9 bits per characters; even, odd, no parity; 1 or 2 stop bits; with standard and not standard baud rate, up to 115200 Baud. The selection of the electric protocol on serial line A is performed by hardware, through jumpers configurations (as described in the previous tables) and communication drivers installations. Some devices needed for RS 422, RS 485 and Current Loop configurations are not mounted on the board in standard base configuration; this is why each fist non standard (non RS 232) serial configuration for line A, must be always performed by grifo® technicians. This far the user can change in autonomy the configuration following the informations below:

- HW SERIAL LINE A IN RS 232 (default configuration)
  
  DSW1.7 = indifferent  
  J17 = position 2-3  IC28 = no device  
  J11, J13 = connected  IC29 = no device  
  J15 = indifferent  IC30 = no device  
  J14, J16 = not connected  IC31 = no device

- HW SERIAL LINE A IN CURRENT LOOP (option .CLOOP)
  
  DSW1.7 = indifferent  
  J17 = position 1-2  IC28 = driver HP 4200  
  J11, J13 = not connected  IC29 = driver HP 4100  
  J15 = indifferent  IC30 = no device  
  J14, J16 = not connected  IC31 = no device

Please remind that Current Loop serial interface is passive, so it must be connected an active Current Loop serial line, that is a line provided with its own power supply, as described in figures 15+17. Current Loop interface can be employed to make both point to point and multi points connections through a 2 wires (half duplex) or a 4 wires (full duplex) connection.

- HW SERIAL LINE A IN RS 422 (option .RS 422)
  
  DSW1.7 = OFF or ON  
  J17 = position 1-2  IC28 = no device  
  J11, J13 = not connected  IC29 = no device  
  J15 = position 2-3  IC30 = driver SN 75176 or MAX 483  
  J14, J16 = (*)  IC31 = driver SN 75176 or MAX 483

Status of signal PWM1 = DIR (software managed), allows to enable or disable the transmitter as follows:

  PWM1 = DIR = low level = logic state 0 -> transmitter enabled
  PWM1 = DIR = high level= logic state 1 -> transmitter disabled

In point to point connections, the PWM1=DIR signal can be always kept low (transmitter always enabled), while in multi points connections transmitter must be enabled only when a transmission is requested. The last condition (DIR settable) needs absolutely DSW1.7 in ON, while the first condition (DIR forced low) can be obtained with DSW1.7 in ON and DIR forced low by software or with DSW1.7 in OFF and DIR status indifferent.
FIGURE 37: SERIAL LINE A (HARDWARE) COMMUNICATION DRIVERS

Serial A in RS 232

Serial A in Current Loop

Serial A in RS 422

Serial A in RS 485
- HW SERIAL LINE A IN RS 485 (option .RS 485)

DSW1.7 = ON
J17 = position 1-2 IC28 = no device
J11, J13 = not connected IC29 = no device
J15 = position 1-2 IC30 = driver SN 75176 or MAX 483
J14, J16 = (*) IC31 = no device

In this modality the signals to use are pins 4 and 5 of connector CN4A, that become transmission or reception lines according to the status of signal PWM1 = DIR, managed by software, as follows:

PWM1 = DIR = low level = logic state 0 -> line in transmission
PWM1 = DIR = high level= logic state 1 -> line in reception

This kind of serial communication can be used for point to point connections or multi points connections, in half duplex mode. All the transmitted characters are at the same time received (echo) when RS485 communication is used. So the user is allowed to verify the success of transmission, in fact, any conflicts on the line can be recognized by testing the echo received character, after each transmission and vice versa.

(*) When using the RS 422 or RS 485 serial line, it is possible to connect the terminating and forcing circuit on the line, by using J14 and J16. This circuit must be always connected in case of point to point connections, while in case of multi points connections it must be connected only in the farthest boards, that is on the edges of the communication line.

During a reset or power on, signal PWM1 = DIR is at logic high level , so during these phases the RS 485 driver is in reception and RS 422 transmission driver is disabled, in order to avoid conflicts on communication line.

Please remind that RS 232 communication signals available on CN4B can be used as hardware handshakes (RTS, CTS, DTR, RI, DSR, etc.) that can be added to communication signals of serial line A, on CN4A. This possibility allows to use the GPC® 550 also in application where the card must communicate with systems that require serial hardware handshakes, as for example modem, radio bridges, printers, etc.

For further informations about serial communication please refer to the connection examples of figures 11÷17 and to paragraph SOFTWARE SERIAL LINE B.

The connection of the serial lines can be simplified by proper communication cables, independently from the selected electric protocol. This cables are generally named CCR.Plugxxx and they are available between grifo® accessories, as described in APPENDIX C. The cables most frequently used (i.e. suitable for PC, modem, serial printers, operator panels QTP xxx connections) are ready to use but for specific requirements they can be realized on user specifications.

MEMORY SELECTION

On GPC® 550 can be mounted up to 769K bytes and 256 bytes of memory divided in various modes. Normally GPC® 550 is provided in its default configuration with 128K SRAM on IC7, 256 bytes of serial SRAM on IC23 and 512 bytes of serial EEPROM on IC21; each different configuration can be reached in the order phase or assembled by user. In this last case the board has to be set as described in the following table:
All the above described devices must feature a JEDEC compliant pin out except for the serial devices installed on U21 and U23 that must be requested to grifo® in the ordering phase. To determine the name of the memory devices that can be mounted, please refer to the manufacturer documentation.

(*). If needed on the IC19 socket can be put a 128K bytes FLASH EPROM too, that is managed in reading only. That configuration can be comfortable during the development phase for long.

<table>
<thead>
<tr>
<th>NAME</th>
<th>DEVICE</th>
<th>SIZE</th>
<th>JUMPERS CONFIGURATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>IC19</td>
<td>EPROM</td>
<td>32K Bytes</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>EPROM</td>
<td>64K Bytes</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>EPROM (*)</td>
<td>128K Bytes</td>
<td>-</td>
</tr>
<tr>
<td>IC7</td>
<td>SRAM</td>
<td>128K Bytes</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>EPROM</td>
<td>32K Bytes</td>
<td>J7 in x-x ; 4-5 ; x-x and J3 in 1-2</td>
</tr>
<tr>
<td></td>
<td>EPROM</td>
<td>64K Bytes</td>
<td>J7 in 2-3 ; 4-5 ; x-x and J3 in 1-2</td>
</tr>
<tr>
<td></td>
<td>EPROM</td>
<td>128K Bytes</td>
<td>J7 in 2-3 ; 4-5 ; NC and J3 in 1-2</td>
</tr>
<tr>
<td></td>
<td>EPROM</td>
<td>256K Bytes</td>
<td>J7 in 2-3 ; 4-5 ; NC and J3 in 2-3</td>
</tr>
<tr>
<td></td>
<td>EPROM</td>
<td>512K Bytes</td>
<td>J7 in 2-3 ; 4-5 ; 8-9 and J3 in 2-3</td>
</tr>
<tr>
<td>IC18</td>
<td>SRAM , EEPROM</td>
<td>32K Bytes</td>
<td>J7 in 2-4 ; 5-6 ; x-x and J3 in 1-2</td>
</tr>
<tr>
<td></td>
<td>SRAM , EEPROM</td>
<td>128K Bytes</td>
<td>J7 in 2-4 ; 5-6 ; 7-8 and J3 in 1-2</td>
</tr>
<tr>
<td></td>
<td>SRAM , EEPROM</td>
<td>512K Bytes</td>
<td>J7 in 2-4 ; 5-6 ; 7-8 and J3 in 2-3</td>
</tr>
<tr>
<td></td>
<td>FLASH EPROM</td>
<td>32K Bytes</td>
<td>J7 in 1-2 ; 4-5 ; 6-8 and J3 in 1-2</td>
</tr>
<tr>
<td></td>
<td>FLASH EPROM</td>
<td>128K Bytes</td>
<td>J7 in 2-3 ; 4-5 ; 6-8 and J3 in 1-2</td>
</tr>
<tr>
<td></td>
<td>FLASH EPROM</td>
<td>512K Bytes</td>
<td>J7 in 2-3 ; 4-5 ; 6-8 and J3 in 2-3</td>
</tr>
<tr>
<td>IC23</td>
<td>serial SRAM+RTC</td>
<td>256 Bytes</td>
<td>-</td>
</tr>
<tr>
<td>IC21</td>
<td>serial EEPROM</td>
<td>256÷1024 Bytes</td>
<td>-</td>
</tr>
</tbody>
</table>

Figure 38: Memory selection table
programs, in fact it avoids to use an EPROM and its long erasing time. For more information and their cost please contact grifo®, while to easily locate the memory devices on the board please refer to figure 26.

CAN INTERFACE

Jumper J4 connects or does not connect CAN termination resistor, as described in figure 32. CAN bus must be a differential line with 60Ω of impedance so termination resistors must be connected to obtain this value. This connection, in specific, must be always made in case of point-to-point communication, while in multi-point communication it must be connected only in the cards at the greatest distance, that is at the ends of the lines (please see example of figure 25). Correct CAN termination contributes remarkably to correct communication; in fact on board interface can suppress transients and is immune against radio frequency and electromagnetic disturbances only if connection to the field is made correctly.

CAN line is galvanically isolated (as described in paragraph “POWER SUPPLY”) from board supply voltage. Ground of CAN line (called CAN GND) is available on a pin of connector CN8. This latter can be used to equilibrate difference of potentials amongst several CAN systems, but also to shield physical connection, using CAN shielded cable, to obtain the greatest protection against external noise.
FIGURE 39: CARD PHOTO
A wide selection of software development tools can be obtained, allowing use of the module as a system for its own development, both in assembler and in other high level languages; in this way the User can easily develop all the requested application programs in a very short time. Generally all software packages available for the mounted microprocessor, or for the 51 family, can be used. All these software packages provided by grifo® are always attached by examples that show how to manage each board section and by a using complete documentation. Among them we remind:

**GET 51:** it is a complete program with editor, communication driver and mass memory management for all '51 family cards. This program developed by grifo® allows to operate in the best conditions when MCS BASIC, BXC51, MDP, FMO52, etc. software tools are used. The program is menu driven and mouse driven. It is designed to run under MS-DOS but can run also in MACINTOSH environment with VIRTUAL-PC. It is delivered in MS-DOS 3”1/2 floppy disks.

**MDP:** monitor debugger program able to load and debug each HEX Intel files for 51 microprocessor family. It is provided of the standard commands available on in circuit emulator and requires only an external P.C. connected through a serial line.

**FORTH:** complete software development tools to program the card with FORTH high level language. It needs a P.C. for User interface and it is really interesting for its fast execution and small size, of the generated code.

**BASIC 550:** complete development tools for MCS BASIC (interpreted BASIC language for industrial application). It needs a P.C. for console and program saving operations, while the debug, test and program operations are performed on the card.

**BXC51:** cross compiler for source files written in BASIC 550. It allows a considerable speed increment of the starting BASIC 550 program and it is completely executed on external P.C.

**HI-TECH C:** cross compiler for C source program. It is a powerful software tool that includes editor, C compiler, assembler, optimizer, linker, library, and remote symbolic debugger, in one easy to use integrated development environment.

**SYS51CW:** cross compiler for C source program, executable on P.C. with WINDOWS and with a confortable IDE You can use: editor, C compiler, assembler, obtimizator, linker, library of a remote symbolic debugger.

**SYS51PW:** cross compiler for C source program, executable on P.C. with WINDOWS and with a confortable IDE You can use: editor, PASCAL compiler, assembler, obtimizator, linker, library of a remote symbolic debugger.

**XPAS51:** cross compiler for PASCAL source program, executable on P.C. with MS-DOS

**DDS MICRO C 51:** low cost cross compiler for C source program. It is a powerful software tool that includes editor, C compiler (integer), assembler, optimizer, linker, library, and remote symbolic debugger, in one easy to use integrated development environment. There are also included the library sources and many utilities.
NOICE51: It is a PC-hosted debugger consists of a target-specific DOS program, NOICExxx.EXE, and a target-resident monitor program. The two programs communicate via RS-232. NOICE includes: source level debug; a disassembler; a file viewer; memory display and editing; a virtually unlimited number of breakpoints; hardware-free single step; definition of symbols; the ability to record and play back files of commands; on-line help.

BASCOM 8051: cross compiler for BASIC source program. It is a powerful software tool that includes editor, BASIC compiler and simulator included in an easy to use integrated development environment for Windows. Many memory models, data types and direct use of hardware resource instructions are available.

FM053: monitor debugger program able to load and debug each HEX Intel files for 51 microprocessor family. It is provided of the standard commands available with an hardware emulator and provides to user the possibility to operate with all the on board resources. This bundle requires only an external P.C. connected through a serial line. FMO53 can be used in according with a lot of the other cross compiler.
It is also capable to program on FLAH EPROM the user application for debugging and execute it in autorun mode.

µC/51: It is a comfortable, low cost, software package with a colplete IDE that allows to use an editor, and ANSI C compiler, and assembler, a linker and a remote source level debugger user configurable. Sources of main libraries and remote debugger are included, and so severl utility and demo programs.

LADDERWORK: It is a easy to use system to generate automation application using the very famouts contact logic. It features a graphic editor to place and connect components that refer to hardware resources (like digital I.O, counters, A/D, etc.) like on an electric diagram and define their properties, and efficent compiler to create the executable code and an utility to download it. Integrated IDE makes comfortable use of these tools. Delivered in a CD for Windows with user manual and hardware key.
ADRESSES AND MAPS

In this chapter are reported all information about card use, related to hardware features of GPC® 553. For example, the registers addresses, the memory allocation and peripheral devices software management are described below.

ON BOARD RESOURCES MAPPING

The card devices addresses are managed from a control logic, realized with programamble logic. This control logic allocates memory and peripheral devices with very low power consumption, in two separate manners.

The 80C552 microprocessor addresses 256 bytes of internal RAM, 64K bytes of code memory and 64K bytes of data memory and the control logic provides on board memory and peripheral devices allocation inside these addresses spaces.

This management is done via hardware through the the positions of some jumpers (J1,J2,J127) and via software through the MMU setting. In this mode we can define the memories to use and the relative addresses range. For I/O mapping we have to reming that the control logic naturally does not use the reserved location for the internal peripherals of CPU, in order to avoid any mechanical problem.

Summarizing the control logic allocates:
- Up to 128K bytes of EPROM on IC19
- 128K bytes of RAM on IC7
- Up to 128K bytes of SRAM/EPPROM/EPROM on IC18
- BUS ABACO®
- DSW1 configuration Dip Switch
- Activity LEDs
- Buzzer
- MMU memories management unit.
- Digital I/O controller PPI 82c55
- CAN controller

The addresses listed here and in the following paragraphs cannot be reallocated. Other devices are managed always by control logic but they are not allocated in memory space in fact these devices are drived through CPU I/O lines with a synchronous communication.

BUS ABACO® MAPPING

GPC® 550 control logic manages also BUS ABACO® addressing; as shown in figure 40, it is available starting from BUS addresses for 112 bytes of extension.

Accessing any address in this range enables signal /IORQ and all the other control signals of CN4+CN5.

On ly least significant byte of I/O address is used when addressing peripherals cards, becauseBUS ABACO® employs ony 8 bits for addressing and 8 bits for data.
PERIPHERALS MAPPING

For some peripherals presents on board are located in the last 256 bytes of the 64K bytes microprocessor data and/or code area, to avoid conflict problems. Next table shows addresses, meanings and direction of peripheral devices registers (only the external ones to microprocessor):

<table>
<thead>
<tr>
<th>DEVICE</th>
<th>REGISTER</th>
<th>ADDRESS</th>
<th>R/W</th>
<th>MEANING</th>
</tr>
</thead>
<tbody>
<tr>
<td>CAN controller SJA 1000</td>
<td>CAN</td>
<td>FF00H÷FF7FH</td>
<td>R/W</td>
<td>Registers for management of CAN controller SJA 1000 in Basic CAN or PeliCAN modality (registers are the same as those reported in component data sheet, plus an FF00H offset).</td>
</tr>
<tr>
<td>ABACO® BUS</td>
<td>BUS</td>
<td>FF80H÷FFEFH</td>
<td>R/W</td>
<td>ABACO® BUS management addresses.</td>
</tr>
<tr>
<td>Memory Management Unit</td>
<td>MEM</td>
<td>FF00H</td>
<td>W</td>
<td>Register for paged memories management.</td>
</tr>
<tr>
<td>Activity LEDs</td>
<td>LED</td>
<td>FFF1H</td>
<td>W</td>
<td>Activity LEDs LD1, LD2 and LD3 management register.</td>
</tr>
<tr>
<td>BUZZER</td>
<td>BUZ</td>
<td>FFF1H</td>
<td>W</td>
<td>Buzzer BZ1 management register.</td>
</tr>
<tr>
<td>DIP SWITCH</td>
<td>DIP</td>
<td>FFF3H</td>
<td>R</td>
<td>Dip switch DSW1 acquisition register.</td>
</tr>
<tr>
<td>PPI 82C55</td>
<td>PA</td>
<td>FFF4H</td>
<td>R/W</td>
<td>Port A data register</td>
</tr>
<tr>
<td></td>
<td>PB</td>
<td>FFF5H</td>
<td>R/W</td>
<td>Port B data register</td>
</tr>
<tr>
<td></td>
<td>PC</td>
<td>FFF6H</td>
<td>R/W</td>
<td>Port C data register</td>
</tr>
<tr>
<td></td>
<td>RC</td>
<td>FFF7H</td>
<td>R/W</td>
<td>Command and control register</td>
</tr>
</tbody>
</table>

**Figure 40: Peripherals addresses table**

For further information about register meanings, please refer to next paragraph called "PERIPHERAL DEVICES SOFTWARE DESCRIPTION".

Please remark that the above table reports the description of external devices registers only, for a description of microcontroller internal registers please refer to manufacturer documentation.

MEMORY MAPPING

For memory mapping, the board can be configured in 4 ways. Following is reported a diagram of these addressing, with the indications to configure jumpers and signals that performe this selection. The mapping selection has to be performed from users based on the used software and/or requirements.

It is important to note that the following figures report the differences between code area and data area that meet the two external memory accesses type of the micro (MOVC and MOVX).
Figure 41: Mode 0 Memory Configuration

Used by software tools as: BASIC 550; BXC51; HI TECH C 51; DDS MICRO C 51; SYS51PW; SYS51CW; BASCOM 8051; μC/51; etc.
FIGURE 42: MODE 1 MEMORY CONFIGURATION

Used by software tools as: HI TECH C 51; DDS MICRO C 51; SYS51PW; SYS51CW; BASCOM 8051; µC/51; etc.
MAPPING 2

**CODE AREA**  **DATA AREA**

- **FF00H** to **FFFFH**: ON BOARD I/O
  - **0000H** to **128 K**: IC7: SRAM
  - **128 K** to **C000H**: NOT USED
  - **C000H** to **BFFFH**: 32÷128 K IC19: EPROM
  - **BFFFH** to **07EFFH**: NOT USED
  - **07EFFH** to **04000H**: NOT USED
  - **04000H** to **07EFFFH**: 32÷512 K

- **0000H** to **8000H**: IC18: SRAM, FLASH, EPROM, EEPROM
  - **8000H** to **7FFFH**: NOT USED
  - **7FFFH** to **00000H**: 32÷512 K
  - **00000H** to **07EFFFH**: NOT USED
  - **07EFFFH** to **04000H**: IC18: SRAM, FLASH, EPROM, EEPROM

- **8000H** to **C000H**: IC18: SRAM, FLASH, EPROM, EEPROM

- **FFF4H** to **FFF0H**: PPI 82C55
  - **FFF4H** to **FFF0H**: DIP SWITCH, BUZZER, LEDS, MMU
  - **FFF0H** to **FFF80H**: ABACO® BUS
  - **FFF80H** to **FFF00H**: CAN controller

**Figure 43: MODE 2 memory configuration**

Used by software tools as NOICE51.
FIGURE 44: MODE 3 MEMORY CONFIGURATION

Used by software tools: MD:P; FMO53; LUCIFER for HI TECH C 51; DDS MICRO C 51; SYS51PW; SYS51CW; BASCOM 8051; μC:51; etc.
SOFTWARE DESCRIPTION

In the previous paragraphs are described the external registers addresses, while in this one there is a specific description of registers meaning and function (please refer to I/O addresses table, for the registers names and addresses values). For a more detailed description of the devices, please refer to manufacturing company documentation; for microprocessor internal peripheral devices, not described in this paragraph, refer to appendix B. In the following paragraphs the D7÷D0 and .0÷.7 indications denote the 8 bits of the combination used in I/O operations.

SOFTWARE I2C BUS

Software I2C BUS line installed on GPC® 550 is made using two bidirectional I/O lines of CPU:

- P3.3 -> line DATA = SW SDA
- P3.5 -> line CLOCK = SW SCL

they can be easily managed by the user to obtain sequences and timings defined by this standard. More easily, the user can use the high level procedures provided with programmin package that perform complete management of protocol just passing them few parameters.

On software I2C BUS line devices at slave addresses A0H and A8H are already installed, like described in paragraphs “SERIAL SRAM+RTC” and “SERIAL EEPROM”.

ACTIVITY LEDS

Control logic allows to manage three activity LEDs, using as many bits of LED register:

- LED.7 = 0 -> LD4 OFF
- LED.7 = 1 -> LD4 ON
- LED.6 = 0 -> LD2 OFF
- LED.6 = 1 -> LD2 ON
- LED.5 = 0 -> LD3 OFF
- LED.5 = 1 -> LD3 ON

LED register shares its address with other on board peripherals, so each read/write operation to this register affects the programming of these other devices.

LED register is set to 0 after reset or power on, so during these phases LEDs are all OFF.
BUZZER

Buzzer BZ1 is software managed through bit D0 of register BUZ:

- BUZ.0 = 0  ->  BZ1 OFF
- BUZ.0 = 1  ->  BZ1 ON

Main purpose of buzzer is acoustic signalation of application program status conditions to obtain attention from the user (for example to send an alert, etc).
BUZ register shares its address with other on board peripherals, so each read/write operation to this register affects the programming of these other devices.
BUZ register is set to 0 after reset or power on, so during these phases buzzer is OFF.

SERIAL EEPROM

For software management of serial EEPROM module of IC21, please refer to specific documentation or to demo programs supplied with the card. The User must realize a serial communication with I2C bus standard protocol, through two I/O microprocessor pins. The first 32 bytes of serial EEPROM are reserved for software tools use, so they can't be neither read nor written by User program.
The only necessary information is the electric connection:

- P3.3 (input/output)  ->  P3.3 DATA signal  (SW SDA)
- P3.5 (output)       ->  P3.5 CLOCK signal  (SW SCL)

Signals A0,A1,A2 of slave address are connected to the following logic levels: 0, 0, 1.
Logic status 0 means logic status low (=0 V), while logic status 1 means logic status high (=5 V).
For further information about port management modalities, please refer to CPU technical documentation.
EEPROM management lines are set to 1 after reset or power on.

DIP SWITCH DSW1

GPC® 550 has a complete 7 segment configuration inputs sattable by user in order to get them via software.
The on board DSW1 Dip Switch status can be obtained by software, through a simple "read operation" at the DIP register address.
The corrispondence between register bits and Dip Switch is as follows:

- DIP.7  ->  dip switch DSW1.8
- DIP.6  ->  0
- DIP.5  ->  dip switch DSW1.6
- DIP.4  ->  dip switch DSW1.5
- DIP.3  ->  dip switch DSW1.4
- DIP.2  ->  dip switch DSW1.3
- DIP.1  ->  dip switch DSW1.2
- DIP.0  ->  dip switch DSW1.1
Reading DIP register by software, the user obtains a complemented combination, in fact "ON" position corresponds to 0 logic status and "OFF" position corresponds to 1 logic status. Dip switch 8 of S1 features the RUN (ON) and DEBUG (OFF) function, specific for some software packaged of grifo®. To easily locate dip switch S1 please refer to figures 25 and 26.

BACKED SRAM + SERIAL RTC

The IC23 SRAM module, can be provided with on board Lithium battery and with Real Time Clock which manages time (hours, minutes, seconds) and date (day, month, year, day of the week). RTC section can also generate periodic interrupts whose period can be programmed by the user, so it can be used to awaken CPU from low consumption working modes.
For software management of serial SRAM+RTC module of IC20, please refer to specific documentation or to demo programs supplied with the card. The User must realize a serial communication with I2C bus standard protocol, through two I/O microprocessor pins. The only necessary information is the electric connection:

P3.3 (input/output) -> line DATA =SW SDA
P3.5 (output) -> line CLOCK =SW SCL

Signal A0 is connected to logic level 0, so its slave address is A0H. As the communication signals are used both for RAM+RTC and EEPROM, if IC23 is mounted then a serial EEPROM with a maximum size of 1024 bytes (24C08) can be installed on IC21.
The logic state 0 is the relative bit for low level (=0V) for the signal, otherwise the logic state 1 is the relative bit for high level (=5V) for the signal.

CPU INTERNAL PERIPHERALS

Registers description and purpose for all internal peripherals (ADC, TMR CNT, ICU, UART, I2C BUS HW, etc.) is available in the manufacturer data sheet. Please refer to chapter “BIBLIOGRAPHY” and to appendix B of this manual to easily locate such documentation.
FIGURE 45: POTENTIAL CONNECTION DIAGRAM
RS 422-485 COMMUNICATION

As described in paragraph “SERIAL COMMUNICATION SELECTION”, the RS 422 or RS 485 communication direction is enabled by software, driven by a signal called DIR which is connected to signal PWM1 of CPU.

Internal register PWM1 can set the signal, to control the communication as follows:

**Point-to-point RS 422 communication: both transmitter and receiver are enabled**

by hardware it is enough to set dip switch DSW1.7 OFF, to disconnect PWM1 signal from DIR signal and so to keep transmission enabled;

by software no management is required;

**Network RS 422 communication: transmitter is enabled in transmission, receiver is always enabled**

by hardware it is enough to set dip switch DSW1.7 ON, to connect PWM1 signal from DIR signal;

by software transmitter management is made as follows:

- \( \text{register PWM1} = \text{FFH} \rightarrow \text{DIR} = \text{logic status 0} \rightarrow \text{transmitter enabled} \)
- \( \text{register PWM1} = \text{00H} \rightarrow \text{DIR} = \text{logic status 1} \rightarrow \text{transmitter disabled} \)

**Network RS 485 communication: transmitter is enabled in transmission, receiver is always enabled, communication is half duplex**

by hardware it is enough to set dip switch S1.7 ON, to connect PWM1 signal from DIR signal;

by software transmitter management is made as follows:

- \( \text{register PWM1} = \text{FFH} \rightarrow \text{DIR} = \text{logic status 0} \rightarrow \text{reception} \)
- \( \text{register PWM1} = \text{00H} \rightarrow \text{DIR} = \text{logic status 1} \rightarrow \text{transmission} \)

Please remark that when DSW1.7 is ON, DIR signal is connected to PWM1 signal so this latter cannot be used for other purposes.

After a reset or a power on, PWM1 = DIR is at logic level high, so transmission is disabled, to avoid interference in the line.

Please refer to specific technical documentation for setting register PWM1.

SOFTWARE SERIAL LINE B

Serial line B of **GPC® 550** is a software serial line, in fact it is made using two CPU I/O signals electrically buffered in RS 232. The I/O signals are:

- \( P3.4 \) (output) \( \rightarrow \) line TXB RS232
- \( P3.2 \) (input) \( \rightarrow \) line RXB RS232 (if J5 is in position 2-4)

In conformance to standard RS 232, logic status 0 of pins is the positive status (+9 V) of signal, while logic status 1 is negative status (-9 V).

Serial B management must be done completely by the application program, that must create the correct time sequence on pin P3.4 for transmission and examine pin P3.2 for reception.

By means to simplify such management it is better to use an internal timer for time base and use interrupt /INT0 to signal automatically the beginning of a character in reception.
The user can also take advantage of some software packages (like for example **BASCOM 8051** or **BASIC 550**) that support serial software management with high level instructions; this allows to send and receive characters, using preset physical protocol, without any direct interaction with I/O lines and timing problems.

For further information about PORT signals management, please refer to CPU technical documentation. After a reset or a power on, both signals of software serial B are set to logic level high.

**PPI 82C55**

This external peripheral device is managed through 4 registers: one status register (CNT) and three data registers (PDA, PDB, PDC). The data registers are available both for read operation (to obtain signal status) and for write operation (to set signal status) with the correspondence described in figure 23. The PPI 82C55 can work in three different modes:

- **MODE 0** = it provides two 8 bits bidirectional ports (A,B) and two 4 bits bidirectional ports (C LOW, C HIGH); output signals are latched and input signals are not latched; no handshake signals are provided.

- **MODE 1** = it provides two 12 bits ports (A+C LOW and B+C HIGH) where ports A and B are used as 8 I/O lines and port C are used as 4 handshake lines. Both inputs and outputs are latched.

- **MODE 2** = it provides a 13 bits port (A+C3÷7) where port A is used as 8 I/O lines and the 5 bits of port C are used as handshake, and a 11 bits port (B+C0÷2) where port B is used as 8 I/O lines and the 3 bits of port C are used as handshakes. Both inputs and outputs are latched.

The device is programmed writing an 8 bits word in the control register RC, setting the 8 bit of the written data with the following correspondence:

\[
\begin{array}{lllllllll}
D7 & D6 & D5 & D4 & D3 & D2 & D1 & D0 \\
RC & = SF & M1 & M2 & A & CH & M3 & B & CL
\end{array}
\]

where:

- **SF** = mode Set Flag: if actived (1) the device is enabled for standard I/O operation
- **M1** M2 = mode selection:
  - 0 0 = mode 0
  - 0 1 = mode 1
  - 1 X = mode 2
- **A** = port A direction: 1=input; 0=output
- **CH** = port C HIGH direction: 1=input; 0=output
- **M3** = mode selection: 1=mode 1; 0=mode 0
- **B** = port B direction: 1=input; 0=output
- **CL** = port C LOW direction: 1=input; 0=output

After Reset or power on PPI 82C55 is programmed in mode 0 with all three ports in input; in this way any connection of PPI 82C55 signals can be used without conflict problems.
I/O SIGNALS OF CPU

Microcontroller P80C552, installed on GPC® 550, features three 8 bit ports (Port1, 4 and 5) totalizing 24 digital I/O signals.
Many of these signals are physically multiplexed inside the microprocessor and so can perform different tasks according to their software programming.
The user can decide without limitations the function of signals connected to CN1 and JP1, while must not absolutely program Port 0 and 2.
Remaining Port 3 is dedicated to software I²C BUS and serial line, so it must be programmed carefully.
Wrong programming or initialization of Port 0, 2 or 3 can cause incorrect working or hang of application program.
For further information about PORT signals management, please refer to CPU technical documentation.
After a reset or a power on, all Port signals set to logic level high as inputs.

CAN CONTROLLER

As shown in table of figure 41, CAN controller SJA 1000 is managed through a set of status and/or command registers described in detail in appendix B of this manual and used in the examples delivered with the board.
This paragraph reports only additional information to use correctly these registers.

1) Communication Bit Rate, as can be seen from information in appendix B, is calculated with following formula:

\[
\text{BAUD RATE} = \frac{\text{Freq}}{2 \times (\text{BRP} + 1) \times (3 + \text{TSEG1} + \text{TSEG2})}
\]

where:
Freq = CAN controller clock frequency in Hz (24000000 for GPC® 550).
BRP = Value of bit BRP.x or Bus Timing Register 0 (BTR0, address FF06H).
TSEG1 = Value of bit TSEG1.x or Bus Timing Register 1 (BTR1, address FF07H).
TSEG2 = Value of bit TSEG2.x or Bus Timing Register 1 (BTR1, address FF07H).

2) To interface correctly CAN controller SJA 1000 and line driver 82C250, it is essential to program Output Control Register (OCR, address INDPCS6 + 8) with value FA Hex; this configures the device for "Normal output mode", with outputs TX0 and TX1 in "Push Pull".

3) The following figure shows the flow chart of suggested initialization for CAN controller SJA 1000: it is easy to see that there is no initialization for interrupt. To eventually manage them, it is essential to program opportunistically the bits of control register (CR, address INDPSC6 + 0).
Initialization of CAN controller SJA1000

1. Writes data **01H** into Control register (CR, address FF00H): enables Reset Request
2. Reads Control Register (CR, address FF00H)

   - RM (Reset Mode, bit **0** of Control Register (CR, address FF00H) = **1**
     - NO
     - YES

3. Sets Acceptance Code Register (ACR, address FF04H)
4. Sets Acceptance Mask Register (AMR, address FF05H)
5. Sets Bus Timing Register 0 (BTR0, address FF06H)
6. Sets Bus Timing Register 1 (BTR1, address FF07H)

7. Writes data **FAH** into Output Control register (OCR, address FF08H): Normal output mode and Push-Pull.
8. Writes data **00H** into Control Register (CR, address FF00H): disables Reset mode, Normal operation and no Interrupts.
9. Read Control Register (CR, address FF00H)

   - RR (Reset Request, bit **0** of control register (CR, address FF00H) = **0**
     - NO
     - YES

10. Writes data **0EH** into Command Mode Register (CMR, address FF01H): Clear overrun, Release receive buffer and Abort transmission

**END Initialization**

**Figure 46: CAN controller initialization flow chart**
MEMORY MANAGEMENT UNIT

An efficient MMU circuitry takes care to allocate in the CPU addressing space all the memory devices that can be installed on GPC® 550. This section can be programmed through the MEM register, which is allocated in the I/O addressing space. In order to have the maximum space possible of memories, (768K) in the microcontroller logic space (64K bytes as data area and 64K as code area) the MMU divides the memories in pages in equal size that can be selected via software. This selection is made by preper register MEM located in the I/O space; the bits of MEM register have the following meaning:

MEM: Meaning of bits

<table>
<thead>
<tr>
<th>MEM.7</th>
<th>A18 x IC18</th>
</tr>
</thead>
<tbody>
<tr>
<td>MEM.6</td>
<td>A17 x IC18</td>
</tr>
<tr>
<td>MEM.5</td>
<td>A16 x IC18</td>
</tr>
<tr>
<td>MEM.4</td>
<td>A15 x IC18</td>
</tr>
<tr>
<td>MEM.3</td>
<td>A15 x IC7</td>
</tr>
<tr>
<td>MEM.2</td>
<td>A16 x IC7</td>
</tr>
<tr>
<td>MEM.1</td>
<td>A15 x IC19</td>
</tr>
<tr>
<td>MEM.0</td>
<td>A16 x IC19</td>
</tr>
</tbody>
</table>

Only the first two bits D0+D1 define which page of EPROM installed on IC19, the second group of bots D3+D2 define which page of SRAM installed IC7 and the last group of bits define which page of EPROM, FLASH EPROM, SRAM, EEPROM installed on IC18 must be addressed.

When a reset or a power on occur all the bits of MEM register are reset (all bits 0); this means to program the MMU section where the low 32K Bytes page consists of page 0 EPROM or FLASH EPROM installed on IC10 and the high 32K Bytes page consists of page 0 SRAM installed on IC18. Please refer to the following table, also remembering figures 36 and 37, for an overview of all the possible MMU section configurations.

"X" means non significant bit, that is that bit can be "1" or "0" without influencing the setting there described.
"B" and "H" suffix define the previous values of CPU are coded in binary or hexadecimal format. The distinguish of the access in the CPU addresses is referred to the two modalities that microcontroller can process, that are the CODE area (MOVC) or DATA area (MOVX).
Figure 47: MMU SECTION PAGE NUMERATION

IC19: EPROM

IC7: SRAM

IC18: SRAM, FLASH, EPROM, EEPROM
### Figure 48: MMU Mapping Programming Table 1

<table>
<thead>
<tr>
<th>PAGE</th>
<th>DEVICE ADDRESSES</th>
<th>MEM REGISTER</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>IC18: 07EFFH÷00000H</td>
<td>0000XXXXXB = 00H</td>
</tr>
<tr>
<td>1</td>
<td>IC18: 0FEFFH÷08000H</td>
<td>0001XXXXXB = 10H</td>
</tr>
<tr>
<td>2</td>
<td>IC18: 1EFFH÷10000H</td>
<td>0010XXXXXB = 20H</td>
</tr>
<tr>
<td>3</td>
<td>IC18: 1FEFFH÷18000H</td>
<td>0011XXXXXB = 30H</td>
</tr>
<tr>
<td>4</td>
<td>IC18: 2EFFH÷20000H</td>
<td>0100XXXXXB = 40H</td>
</tr>
<tr>
<td>5</td>
<td>IC18: 2FEFFH÷28000H</td>
<td>0101XXXXXB = 50H</td>
</tr>
<tr>
<td>6</td>
<td>IC18: 3EFFH÷30000H</td>
<td>0110XXXXXB = 60H</td>
</tr>
<tr>
<td>7</td>
<td>IC18: 3EFFH÷38000H</td>
<td>0111XXXXXB = 70H</td>
</tr>
<tr>
<td>8</td>
<td>IC18: 4EFFH÷40000H</td>
<td>1000XXXXXB = 80H</td>
</tr>
<tr>
<td>9</td>
<td>IC18: 4EFFH÷48000H</td>
<td>1001XXXXXB = 90H</td>
</tr>
<tr>
<td>10</td>
<td>IC18: 5EFFH÷50000H</td>
<td>1010XXXXXB = A0H</td>
</tr>
<tr>
<td>11</td>
<td>IC18: 5EFFH÷58000H</td>
<td>1011XXXXXB = B0H</td>
</tr>
<tr>
<td>12</td>
<td>IC18: 6EFFH÷60000H</td>
<td>1100XXXXXB = C0H</td>
</tr>
<tr>
<td>13</td>
<td>IC18: 6EFFH÷68000H</td>
<td>1101XXXXXB = D0H</td>
</tr>
<tr>
<td>14</td>
<td>IC18: 7EFFH÷70000H</td>
<td>1110XXXXXB = E0H</td>
</tr>
<tr>
<td>15</td>
<td>IC18: 7EFFH÷78000H</td>
<td>1111XXXXXB = F0H</td>
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<table>
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<tr>
<th>PAGE</th>
<th>DEVICE ADDRESSES</th>
<th>MEM REGISTER</th>
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</thead>
<tbody>
<tr>
<td>0</td>
<td>IC7: 07FFFH÷00000H</td>
<td>XXXX00XXXB = 00H</td>
</tr>
<tr>
<td>1</td>
<td>IC7: 0FFFFH÷08000H</td>
<td>XXXX10XXXB = 08H</td>
</tr>
<tr>
<td>2</td>
<td>IC7: 17FFFH÷10000H</td>
<td>XXXX01XXXB = 04H</td>
</tr>
<tr>
<td>3</td>
<td>IC7: 1FFFFH÷18000H</td>
<td>XXXX11XXXB = 0CH</td>
</tr>
</tbody>
</table>

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<tr>
<th>PAGE</th>
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<td>XXXXX00XXB = 00H</td>
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<td>XXXXX10XXB = 02H</td>
</tr>
<tr>
<td>2</td>
<td>IC19: 17FFFH÷10000H</td>
<td>XXXXX01XXB = 01H</td>
</tr>
<tr>
<td>3</td>
<td>IC19: 1FFFFH÷18000H</td>
<td>XXXXX11XXB = 03H</td>
</tr>
</tbody>
</table>

<table>
<thead>
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<th>MEM REGISTER</th>
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<td>0</td>
<td>IC7: 07EFFH÷00000H</td>
<td>XXXX00XXB = 00H</td>
</tr>
<tr>
<td>1</td>
<td>IC7: 0FEFFH÷08000H</td>
<td>XXXX10XXB = 08H</td>
</tr>
<tr>
<td>2</td>
<td>IC7: 1EFFH÷10000H</td>
<td>XXXX01XXB = 04H</td>
</tr>
<tr>
<td>3</td>
<td>IC7: 1FEFFH÷18000H</td>
<td>XXXX11XXB = 0CH</td>
</tr>
</tbody>
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<th>MEM REGISTER</th>
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<td>XXXXX00XXB = 00H</td>
</tr>
<tr>
<td>1</td>
<td>IC19: 0FFFFH÷08000H</td>
<td>XXXXX10XXB = 02H</td>
</tr>
<tr>
<td>2</td>
<td>IC19: 17FFFH÷10000H</td>
<td>XXXXX01XXB = 01H</td>
</tr>
<tr>
<td>3</td>
<td>IC19: 1FFFFH÷18000H</td>
<td>XXXXX11XXB = 03H</td>
</tr>
</tbody>
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## Figure 49: MMU Mapping Programming Table 2

<table>
<thead>
<tr>
<th>MEMORY MAP</th>
<th>ADDRESSES, CPU ACCESS</th>
<th>PAGE</th>
<th>DEVICE ADDRESSES</th>
<th>MEM REGISTER</th>
</tr>
</thead>
<tbody>
<tr>
<td>FEFFH÷C000H CODE</td>
<td>FEFFH÷8000H DATA</td>
<td>0</td>
<td>IC19: 07EFFH÷04000H</td>
<td>XXXXXXX00B = 00H</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td>IC19: 0FEFFH÷0C000H</td>
<td>XXXXXXX10B = 02H</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2</td>
<td>IC19: 17EFFH÷14000H</td>
<td>XXXXXXX01B = 01H</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3</td>
<td>IC19: 1FEFFH÷1C000H</td>
<td>XXXXXXX11B = 03H</td>
</tr>
<tr>
<td>MODE 2</td>
<td>FEFFH÷8000H CODE</td>
<td>0</td>
<td>IC18: 07EFFH÷00000H</td>
<td>0000XXXXXB = 00H</td>
</tr>
<tr>
<td>FEFFH÷8000H DATA</td>
<td></td>
<td>1</td>
<td>IC18: 0FEFFH÷08000H</td>
<td>0001XXXXXB = 10H</td>
</tr>
<tr>
<td>BFFFH÷8000H CODE</td>
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<td>2</td>
<td>IC18: 17EFFH÷10000H</td>
<td>0010XXXXXB = 20H</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3</td>
<td>IC18: 1FEFFH÷18000H</td>
<td>0011XXXXXB = 30H</td>
</tr>
<tr>
<td></td>
<td></td>
<td>4</td>
<td>IC18: 27EFFH÷20000H</td>
<td>0100XXXXXB = 40H</td>
</tr>
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<td>IC7: 17FFFFH÷10000H</td>
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<td>ADDRESSES, CPU ACCESS</td>
<td>PAGE</td>
<td>DEVICE ADDRESSES</td>
<td>MEM REGISTER</td>
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<td>IC18: 37EFFH÷30000H</td>
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<td>7</td>
<td>IC18: 3FEFFH÷38000H</td>
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<td>IC18: 47EFFH÷40000H</td>
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<td>IC18: 57EFFH÷50000H</td>
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<td>IC18: 5FEFFH÷58000H</td>
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<td>IC18: 67EFFH÷60000H</td>
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<td>IC18: 6FEFFH÷68000H</td>
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<td>14</td>
<td>IC18: 77EFFH÷70000H</td>
<td>1110XXXXB = E0H</td>
</tr>
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<td>IC18: 7FEFFH÷78000H</td>
<td>1111XXXXB = F0H</td>
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<td>XXXX11XXB = 0CH</td>
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<td>IC19: 19FFFFH÷18000H</td>
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</table>

**Figure 50: MMU Mapping Programming Table 3**
BIBLIOGRAPHY

In this chapter there is a complete list of technical books, where the user can find all the necessary documentations on the components mounted on **GPC® 550**.

Manual ATMEL:  
*Non volatile memory*

Manual HEWLETT PACKARD:  
*Optoelectronics Designer’s Catalog*

Manual NATIONAL SEMICONDUCTOR:  
*Linear Databook - Volume 1*

Manual NEC:  
*Microprocessors and Peripherals - Volume 3*

Manual NEC:  
*Memory Products*

Manual NEWPORT:  
*DC-DC Converters*

Manual MAXIM:  
*New Releases Data Book - Volume IV*

Manual MAXIM:  
*New Releases Data Book - Volume V*

Manual PHILIPS:  
*80C51 - Based 8-Bit Microcontrollers*

Manual PHILIPS:  
*I2C bus*

Manual PHILIPS:  
*Application notes and development tools for 80C51 microcontrollers*

Manual SGS-THOMSON:  
*Programmable Logic Manual GAL Products*

Manual TEXAS INSTRUMENTS:  
*The TTL Data Book - SN54/74 Families*

Manual TEXAS INSTRUMENTS:  
*RS-422 and RS-485 Interface Circuits*

Manual TOSHIBA:  
*Photo couplers Data Book*

Manual XICOR:  
*Data Book*

Please connect to the manufactures Web sites to get the latest version of all manuals and data sheets.
APPENDIX A: ELECTRIC DIAGRAMS

This chapter shows the electric diagram of the most frequently used interfaces for GPC® 550. Every one of these interfaces can be made by the User in autonomy, while only few of them are grifo® standard boards and can be ordered.

![Figure A1: IAC 01 Electric Diagram](image)

**Title:** IAC 01

**Date:** 13-11-98

**Rel.** 1.1

**Page:** 1 of 1
FIGURE A2: KDx x24 ELECTRIC DIAGRAM
**Title:** QTP 16P  
**Date:** 22-07-98  
**Rel.:** 1.2

**Page:** 1 of 1

**Figure A3:** QTP 16P electric diagram
Figure A4: QTP 24P Electric Diagram - Part 1
FIGURE A5: QTP 24P ELECTRIC DIAGRAM - PART 2
FIGURE A6: SPA 01 ELECTRIC DIAGRAM
**DESCRIPTION**

The 80C552/83C552 (henceforth generically referred to as 8XC552) Single-Chip 8-Bit Microcontroller is manufactured in an advanced CMOS process and is a derivative of the 80C51 microcontroller family. The 8XC552 has the same instruction set as the 80C51. Three versions of the derivative exist:

- 83C552—8k bytes mask programmable ROM
- 80C552—ROMless version of the 83C552
- 87C552—8k bytes EPROM (described in a separate chapter)

The 8XC552 contains a non-volatile 8k x 8 read-only program memory (83C552), a volatile 256 x 8 read/write data memory, five 8-bit I/O ports, one 8-bit input port, two 16-bit timer/event counters (identical to the timers of the 80C51), an additional 16-bit timer coupled to capture and compare latches, two serial interfaces (UART and I2C-bus), a “watchdog” timer and on-chip oscillator and timing circuits. For systems that require extra capability, the 8XC552 can be expanded using standard TTL compatible memories and logic.

In addition, the 8XC552 has two software selectable modes of power reduction—idle mode and power-down mode. The idle mode freezes the CPU while allowing the RAM, timers, serial ports, and interrupt system to continue functioning. The power-down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative.

The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 45 two-byte, and 17 three-byte. With a 16MHz (24MHz) crystal, 58% of the instructions are executed in 0.75µs (0.5µs) and 40% in 1.5µs (1µs). Multiply and divide instructions require 3µs (2µs).

**FEATURES**

- 80C51 central processing unit
- 8k x 8 ROM expandable externally to 64k bytes
- ROM code protection
- An additional 16-bit timer/counter coupled to four capture registers and three compare registers
- Two standard 16-bit timer/counters
- 256 x 8 RAM, expandable externally to 64k bytes
- Capable of producing eight synchronized, timed outputs
- A 10-bit ADC with eight multiplexed analog inputs
- Two 8-bit resolution, pulse width modulation outputs
- Five 8-bit I/O ports plus one 8-bit input port shared with analog inputs
- I2C-bus serial I/O port with byte oriented master and slave functions
- Full-duplex UART compatible with the standard 80C51
- On-chip watchdog timer
- Three speed ranges:
  - 3.5 to 16MHz
  - 3.5 to 24MHz (ROM, ROMless only)
  - 3.5 to 30MHz (ROM, ROMless only)
- Three operating ambient temperature ranges:
  - P83C552xBx: 0°C to +70°C
  - P83C552xFx: –40°C to +85°C (XTAL frequency max. 24 MHz)
  - P83C552xHx: –40°C to +125°C (XTAL frequency max. 16 MHz)
80C51 Family

PROGRAMMER’S GUIDE AND INSTRUCTION SET

Memory Organization

Program Memory

The 80C51 has separate address spaces for program and data memory. The Program memory can be up to 64k bytes long. The lower 4k can reside on-chip. Figure 1 shows a map of the 80C51 program memory.

The 80C51 can address up to 64k bytes of data memory to the chip. The MOVX instruction is used to access the external data memory.

The 80C51 has 128 bytes of on-chip RAM, plus a number of Special Function Registers (SFRs). The lower 128 bytes of RAM can be accessed either by direct addressing (MOV data addr) or by indirect addressing (MOV @Ri). Figure 2 shows the Data Memory organization.

Direct and Indirect Address Area

The 128 bytes of RAM which can be accessed by both direct and indirect addressing can be divided into three segments as listed below and shown in Figure 3.

1. Register Banks 0-3: Locations 0 through 1FH (32 bytes). The device after reset defaults to register bank 0. To use the other register banks, the user must select them in software. Each register bank contains eight 1-byte registers 0 through 7. Reset initializes the stack pointer to location 07H, and it is incremented once to start from location 08H, which is the first register (R0) of the second register bank. Thus, in order to use more than one register bank, the SP should be initialized to a different location of the RAM where it is not used for data storage (i.e., the higher part of the RAM).

2. Bit Addressable Area: 16 bytes have been assigned for this segment, 20H-2FH. Each one of the 128 bits of this segment can be directly addressed (0-7FH). The bits can be referred to in two ways, both of which are acceptable by most assemblers. One way is to refer to their address (i.e., 0-7FH). The other way is with reference to bytes 20H to 2FH. Thus, bits 0-7 can also be referred to as bits 20.0-20.7, and bits 8-FH are the same as 21.0-21.7, and so on. Each of the 16 bytes in this segment can also be addressed as a byte.

3. Scratch Pad Area: 30H through 7FH are available to the user as data RAM. However, if the stack pointer has been initialized to this area, enough bytes should be left aside to prevent SP data destruction.

Figure 2 shows the different segments of the on-chip RAM.
1 FEATURES

• Pin compatibility to the PCA82C200 stand-alone CAN controller
• Electrical compatibility to the PCA82C200 stand-alone CAN controller
• Software-compatibility mode to the PCA82C200 (BasicCAN mode is default)
• Extended receive buffer (64-byte FIFO)
• CAN 2.0B protocol compatibility (extended frame passive in PCA82C200 compatibility mode)
• Supports 11-bit identifier as well as 29-bit identifier
• Bit rates up to 1 Mbits/s
• PeliCAN mode extensions:
  – Error counters with read/write access
  – Programmable error warning limit
  – Last error code register
  – Error interrupt for each CAN-bus error
  – Arbitration lost interrupt with detailed bit position
  – Single-shot transmission (no re-transmission)
  – Listen only mode (no acknowledge, no active error flags)
  – Hot plugging support (software driven bit rate detection)
  – Acceptance filter extension (4-byte code, 4-byte mask)
  – Reception of ‘own’ messages (self reception request)
• 24 MHz clock frequency
• Interfaces to a variety of microprocessors
• Programmable CAN output driver configuration
• Extended ambient temperature range (−40 to +125 °C).

2 GENERAL DESCRIPTION

The SJA1000 is a stand-alone controller for the Controller Area Network (CAN) used within automotive and general industrial environments. It is designed to be hardware and software compatible to the PCA82C200 CAN controller (BasicCAN) from Philips Semiconductors. Additionally, a new mode of operation is implemented (PeliCAN) which supports the CAN 2.0B protocol specification with several new features.

3 ORDERING INFORMATION

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<td>SO28</td>
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SRAM+RTC PCF8583

Philips Semiconductors

Clock/calendar with 240 × 8-bit RAM

PCF8583

1 FEATURES

- I2C-bus interface operating supply voltage: 2.5 V to 6 V
- Clock operating supply voltage (0 to +70 °C): 1.0 V to 6.0 V
- 240 × 8-bit low-voltage RAM
- Data retention voltage: 1.0 V to 6 V
- Operating current (at \( f_{SCL} = 0 \) Hz): max. 50 µA
- Clock function with four year calendar
- Universal timer with alarm and overflow indication
- 24 or 12 hour format
- 32.768 kHz or 50 Hz time base
- Serial input/output bus (I2C)
- Automatic word address incrementing
- Programmable alarm, timer and interrupt function
- Slave address:
  - READ: A1 or A3
  - WRITE: A0 or A2.

2 GENERAL DESCRIPTION

The PCF8583 is a clock/calendar circuit based on a 2048-bit static CMOS RAM organized as 256 words by 8 bits. Addresses and data are transferred serially via the two-line bidirectional I2C-bus. The built-in word address register is incremented automatically after each written or read data byte. Address pin A0 is used for programming the hardware address, allowing the connection of two devices to the bus without additional hardware.

The built-in 32.768 kHz oscillator circuit and the first 8 bytes of the RAM are used for the clock/calendar and counter functions. The next 8 bytes may be programmed as alarm registers or used as free RAM space. The remaining 240 bytes are free RAM locations.

3 QUICK REFERENCE DATA

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<td>-</td>
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<td>V</td>
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4 ORDERING INFORMATION

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APPENDIX C: ALPHABETICAL INDEX

Simboli

.CLOOP  90  
.RS422   90  
.RS485   90  
.RTC     90  
µC/51    57  

A

A/D conversion time  12  
A/D converter  6, 30, 36  
A/D inputs cut-off frequency  12  
A/D resolution  12  
A/D total error  12  
A/D voltage reference  39  
ABACO®  15, 16, 18, 30, 49  
ABACO® BUS  49, 58  
Accessories  20, 26, 36, 37  
ADDRESSES  58  
Analog input selection  40  
Analog inputs  13, 30, 36  
Analog inputs impedance  13  
Assistance  1  

B

back up  14  
Back up current  13  
BASCOM 8051  57  
battery  13, 14, 46  
Bibliography  77  
Block diagram  7  
BT1  46  
Buzzer  65  
BZ1  65  

C

calibration  39  
CAN controller  70  
CAN controller initialization flow chart  71  
CAN Interface  54  
CAN interface connection example  34  
CAN line impedance  13  
CAN termination network  13, 54  
CCITT  20, 26  
CLOCK DEVICE  9  
Communication  20, 26  
connectors  13  
CN1  18  
CN2  16
CN3  15
CN4 + CN5  28
JP1  30
Container  1
control LOGIC  8
CPU  5
CPU INTERNAL PERIPHERALS  66
Current analog inputs  13, 30
current consumption  13
Current Loop  21, 90
current loop  36, 50
current loop network  25

D
Directive  1
Directives  1, 20, 26
Documentation  1

E
EEPROM  53
Electrostatic noises  1
EPROM  12, 53, 58
ESD  1

F
FLASH  12, 53

I
I/O CONNECTION  36
I/O digital lines  18
I/O INTERFACES  40
I/O SIGNALS OF CPU  69
I2C BUS  36
I2C BUS software interrupts  15, 48
CAN controller  48
Real Time Clock  48
Software serial line  48
Introduction  1

J
Jumpers  42
2 PINS JUMPERS  43
3 PINS JUMPERS  44
5 PINS JUMPERS  44
LEDs 64
Lithium 46
Locations 3

MAPS 58
memory configurations 58
memory Selection 52

Network 38
Normative 1, 38

port 1 18, 70
port 2 70
port 3 70
port 4 18, 70
Power supply 21, 26
power supply 13, 48
PPI 15, 16
PPI 82C55 69
Protection 1
Pull up resistors 38
PWM 36
PWM1 50, 68

Real Time Clock 46, 66
Relative humidity 13
RESET 49
RS 232 20, 26, 36, 50
RS 422 20, 36, 50, 68, 90
RS 485 20, 36, 52, 68, 90
RS 485 network 23
RTC 15, 90
Rules 1

S
S1 65, 68
Safety 1
Schemi elettrici 78
Serial communication selection 50
serial EEPROM 12, 53, 65
serial line software 48
serial SRAM  12, 66
Size    12
SJA 1000  70
SRAM    12, 53, 72, 90

T
Temperature range  13
Termination network RS 422-485  13
Trademarks  2
TRIMMERS  39
TTL      15, 16, 18, 36

U
UART     20

V
Version   3
Vref     39

W
Warranty  1
Weight    12