GPC® 323 TECHNICAL MANUAL

- Errata corrige of Edition 5.30 Rel. 20 February 2002 -

1) PAGE 32, FIGURE 24

JUMPER	CONNECTION	PURPOSE	DEF.
J2	position 1-2 and 3-4	Selects 32Kbytes FLASH EPROM.	*
	position 2-3 and 4-5	Selects 32Kbytes SRAM or EEPROM.	
	position 3-4	Selects 32Kbytes EPROM.	

FIGURE 24: 5 PINS JUMPERS TABLE

2) PAGE 32, FIGURE 25

JUMPERS	CONNECTION	PURPOSE	DEF.
J1	not connected	Does not connect pin 26 of CN1 to +5 Vdc.	
	connected	Connects pin 26 of CN1 to +5 Vdc.	*
J6	non connesso not connected	SRAM on IC4 and SRAM+RTC on IC12 are backed up only by eventual external battery.	*
	connected	SRAM on IC4 and SRAM+RTC on IC12 are backed up by internal battery and by eventual external battery.	
J8	not connected	Does not connect external Watch Dog circuitery to reset circuitery.	*
	connected	Connects external Watch Dog circuitery to reset circuitery.	
J22	not connected	Does not connect microcontroller hardware serial transmit signal to pin 2 of CN3A.	
	connected	Connects microcontroller hardware serial transmit signal to pin 2 of CN3A.	*
J23	not connected	Does not connect microcontroller hardware serial receive signal to pin 5 of CN3A.	
	connected	Connects microcontroller hardware serial receive signal to pin 5 of CN3A.	*
JS1, JS2	not connected	Do not connect termination and forcing circuitery to serial communication line A in RS 422-485.	*
	connected	Connect termination and forcing circuitery to serial communication line A in RS 422-485.	

FIGURE 25: 2 PINS JUMPERS TABLE

3) PAGE 37, PARAGRAPH INTERRUPTS MANAGEMENT

One of the most important **GPC® 323** features is the powerful interrupts management. Here is a short description of how the board's hardware interrupt signals can be managed; a more complete description of the hardware interrupts can be found in the microprocessor data sheets or in appendix B of this manual.

- CPU inside devices	->	Possible sources of internal interrupt events are: timer 0÷2; serial port 0, 1; External interrupts 0÷5; internal watch dog, etc..
- Real Time Clock	->	It is open collector wire-anded to pin /INT1 = P3.3 of CPU.
- Power failure	->	It is open collector wire-anded to pin /INT1 = P3.3 of CPU.
- Software serial line	->	It is connected in open collector to pin /INT0 = P3.2 of CPU, according to the connection of jumper J18.
- **ABACO®** I/O BUS	->	The /INT BUS signal of CN1 is connected to pin /INT0 = P3.2 of CPU, according to the connection of jumper J18. The /NMI BUS signal of CN1 is connected to pin T2 = P1.0 of CPU.

The last described connection is really important for two different reasons: each activation of /NMI BUS signal can generate an interrupt or each /NMI BUS signal change can be counted. The /NMI BUS signal management is defined by software programmation of timer 2 , so the user can select the favourite mode. This feature is really important especially when **GPC® 323** is connected to external card as **ZBT xxx** and **ZBR xxx**, in fact optocoupled digital signals can be counted or they can generate standard interrupts.
The microprocessor features a programmable priority structure that manages the case of contemporary interrupts. The addresses of the interrupt response subroutines can be software programmed by the user placing them on the proper code areas while the interrupts priority level and activation are sofware programmable through internal CPU registers. So the user program has always the possibility to react promptly to every external event, deciding also the priority of interrupts.

4) PAGE 38, PARAGRAPH MEMORY SELECTION

On **GPC® 323** can be mounted 97,25K bytes of memory divided in several configurations, as described in the following table:

IC	DEVICE	SIZE	CONFIGURATION
3	SRAM/EEPROM	32K Bytes	J2 in 2-3 and 4-5
	EPROM	32K Bytes	J2 in 3-4
	FLASH EPROM	32K Bytes	J2 in 1-2 and 3-4
4	SRAM/EEPROM	32K Bytes	-
5	EPROM	32K Bytes	-
10	Serial EEPROM	512÷1024 Bytes	-
12	SRAM+RTC	256 Bytes	-

FIGURE 30: MEMORY SELECTION TABLE

The sockets IC3, IC4 and IC5 follow the JEDEC standard, so the mounted memory devices must have JEDEC pin outs, to easily locate them please refer to figure 26. The jumpers configurations described on figure 30 only set the sockets for the indicated memory device, but there are some other jumpers that set the memory addressing map; for this information, please refer to "MEMORY ADDRESSES" paragraph.
Normally **GPC® 323** is supplied in its default configuration with 32K SRAM on IC 4 and 512 byte serial EEPROM on IC 10; each different configurations can be defined during order phase or self mounted by the user. Below are reported the abbrevation of the possible memory options:

.32K	->	32K x 8 SRAM
.32KMOD	->	32K x 8 backed SRAM
.32EE	->	32K x 8 parallel EEPROM
.32KF	->	32K x 8 parallel FLASH EPROM
.EE02	->	2K bit (256 byte) serial EEPROM
.EE08	->	8K bit (1024 byte) serial EEPROM

For further information and prices please contact directly **grifo®**.

5) PAGE 39, PARAGRAPH IN SYSTEM PROGRAMMING

One of the most important features of **GPC® 323** is the possibility to use some microcontrollers that support the in system and in application programming (ISP), as the PHILIPS 89CRx+ /2, ATMEL T89C51AC2. Below are listed the sequence of operations that must be performed by the user to use this features:

1) develop the application program through a proper software tools that generate an executable code;
2) connect jumper J19 in position 1-2 and J20 in position 1-2;
3) connect RS 232 serial line A to a personal computer free COM line;
4) power on the card;
5) program the microprocessor internal FLASH EPROM by using the specific program supplied by the manufacturer (i.e. **WINISP** by PHILIPS, **FLIP** by ATMEL, etc.).
6) power off the card;
7) connect J19 in position 2-3 and J20 in position 2-3;
8) power on the card: the programmed application programm will start execution from internal ROM.

The ISP reduces the total application cost, in fact it eliminates the requirements of EPROM, EPROM programmer, external FLASH EPROM, etc. For further informations on in system programming please refet to specific technical documentation from PHILIPS or ATMEL.

6) PAGE 40 AND 42, PARAGRAPH SERIAL COMMUNICATION SELECTION

Please remember that if not differently specified during the order phase, the card is delivered in its default configuration with two RS 232 serial line.
The serial line A is available on connector CN3A and can be buffered in RS 232, RS 422, RS 485 or current loop electric standard. By hardware can be selected which one of these electric standard is used, through jumpers connection (as described in the previous table). By software the serial line can be programmed to operate with 8, 9 bits per character, no parity, 1 stop bits at standard or no standard baud rates, through some some CPU internal register setting..
Some components necessary for RS 422 and RS 485 communication are not mounted and not tested on the default configuration card, so the first not standard configuration must always be executed by **grifo®** technician; then the user can change himself the configuration, following the below description (jumpers not mentioned in the below description have no influence on communication):

- SERIAL LINE A CONFIGURED IN RS 232 (default configuration)

			IC25	= driver MAX 202
J7	=	don't care	IC26	= no component
J22, J23	=	connected	IC27	= no component
J24	=	position 1-2	IC28	= no component
JS1, JS2	=	not connected	IC29	= no component

- SERIAL LINE A CONFIGURED IN CURRENT LOOP (**.CLOOP** option)

			IC25	= no component
J7	=	don't care	IC26	= driver HCPL 4100
J22, J23	=	not connected	IC27	= no component
J24	=	position 2-3	IC28	= driver HCPL 4200
JS1, JS2	=	not connected	IC29	= no component

Please remark that current loop serial interface is passive, so it must be connected an active Current Loop serial line, that is a line provided with its own power supply. Current loop interface can be employed to make both point to point and multi point connections through a 2 wires or a 4 wires connection as described in figures 16÷18.

- SERIAL LINE A CONFIGURED IN RS 422 (**.RS422** option)

			IC25	= no component
J7	=	position 2-3	IC26	= no component
J22, J23	=	not connected	IC27	= driver SN75176 or MAX 483
J24	=	position 2-3	IC28	= no component
JS1, JS2	=	(*)	IC29	= driver SN75176 or MAX 483

Status of signal DIR, which is software managed, allows to enable or disable the transmitter as follows:

DIR = low level = logic state 0 -> transmitter enabled
DIR = high level = logic state 1 -> transmitter disabled

In point to point connections, signal DIR can be always kept low (trasnmitter always enabled), while in multi point connections transmitter must be enabled only when a transmission is requested.

- SERIAL LINE A CONFIGURED IN RS 485 (**.RS485** option)

			IC25	=	no component
J7	=	position 1-2	IC26	=	no component
J22, J23	=	not connected	IC27	=	driver SN75176 or MAX 483
J24	=	position 2-3	IC28	=	no component
JS1, JS2	=	(*)	IC29	=	no component

In this modality the signals to use are pins 4 and 5 of connector CN3A, that become transmission or reception lines according to the status of signal DIR, managed by software, as follows:

DIR = low level = logic state 0 -> transmitter enabled
DIR = high level = logic state 1 -> transmitter disabled

This kind of serial communication can be used for multi point connections, in addition it is possible to listen to own transmission, so the user is allowed to verify the succes of transmission. In fact, any conflict on the linecan be recognized by testing the received character after each transmission.

(*) If using the RS 422 or RS 485 serial line, it is possible to connect the terminating and forcing circuit on the line by using JS1 and JS2. This circuit must be always connected in case of point to point connections, while in case of multi point connections it must be connected olny in the farest boards, that is on the edges of the commmunication line.

When a reset or a power on occour, signal DIR is kept to a logic level high, so in any of these two cases driver RS 485 is receiving or RS 422 driver is disabled, avoidng eventual conflicts in communication.

The serial line B is available on connector CN3B and it can be buffered only in RS 232. By mounting a MAX 202 driver on IC 13 this second serial line is hardware enabled and by software it can be managed as below described:

- µP 80C32 and compatible ones

The serial line B is a software serial line, managed through two I/O pins of the processor (P1.2 -> RXB and P1.3 -> TXB). In order to simplify the reception the signal RXB can be connected also to line P3.2 = /INT0, trough the jumper J18. In this condition each received character generates interrupts that can be easily serviced by microcontroller. The communication parameters (baud rate, stop bit, bit x char, etc.) are software defined through some timing and some sequence of management procedure. For further information, please refer to the software tools manuals.

- µP 80C320 and compatible ones

The serial line B is an hardware serial line, managed through the dedicated pins of the processor (P1.2 = RXD1 -> RXB and P1.3 = TXD1 -> TXB). The communication parameters (baud rate, stop bit, bit x char, etc.) are software defined through proper microprocessor registers setting. For further information, please refer to microprocessor data sheets.

For further informations about serial communication please refer to the examples of figures 12÷18 and paragraph "RS 422-485 DIRECTION".

7) PAGE 46, PARAGRAPH MEMORY CONFIGURATION 0

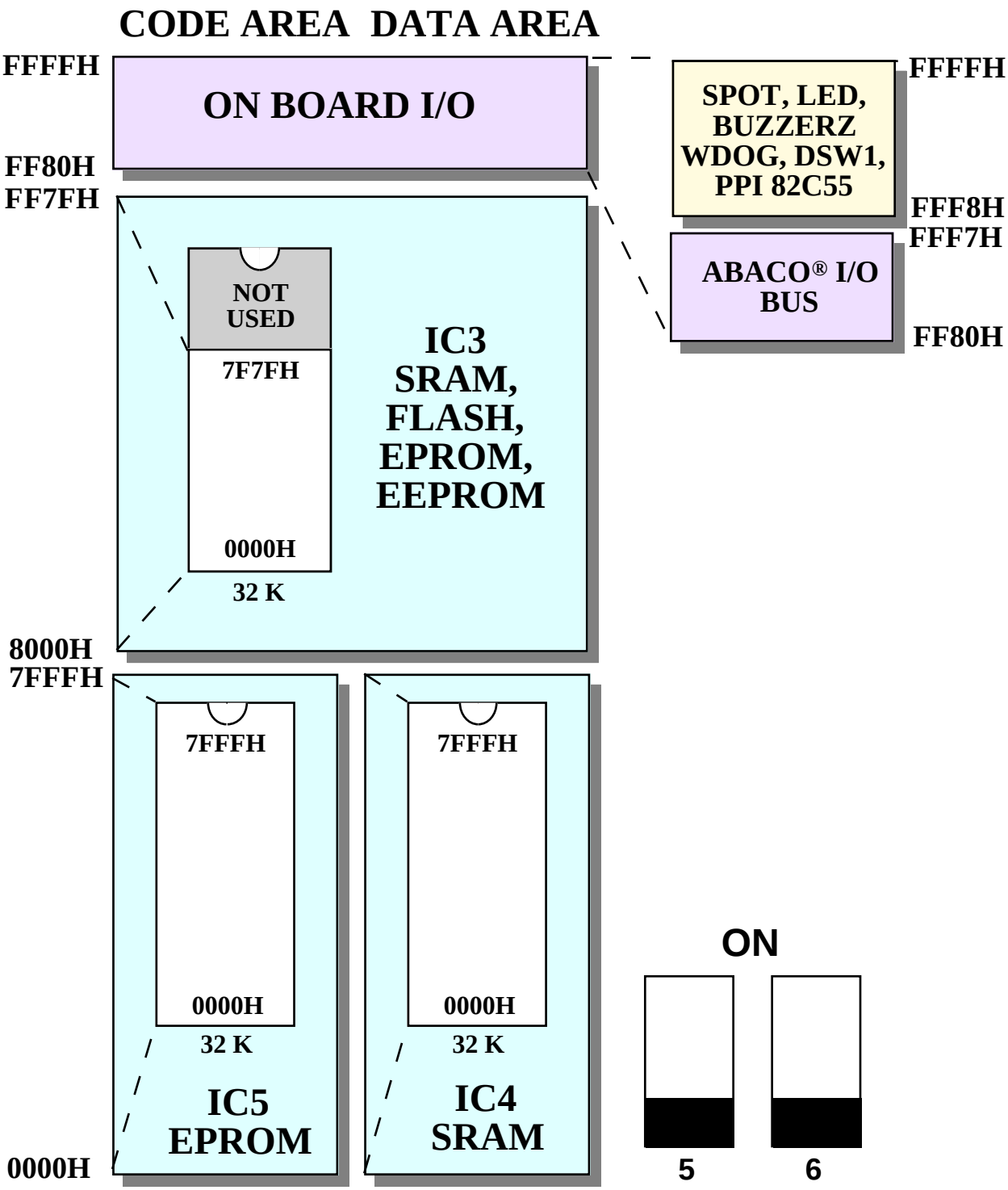

FIGURE 32: MODE 0 MEMORY CONFIGURATION

Configuration of switches 5 and 6 of DSW1: dip 5 **OFF**; dip 6 **OFF**.
Used by software tools as: BASIC 323; BXC51; HI TECH C; DDS MICRO C; µC/51; BASCOM 8051; etc.
This is the default memory configuration set on the card after the testing phase and the one received by the customer, when the card is ordered without software development tools.

8) PAGE 47, PARAGRAPH MEMORY CONFIGURATION 1

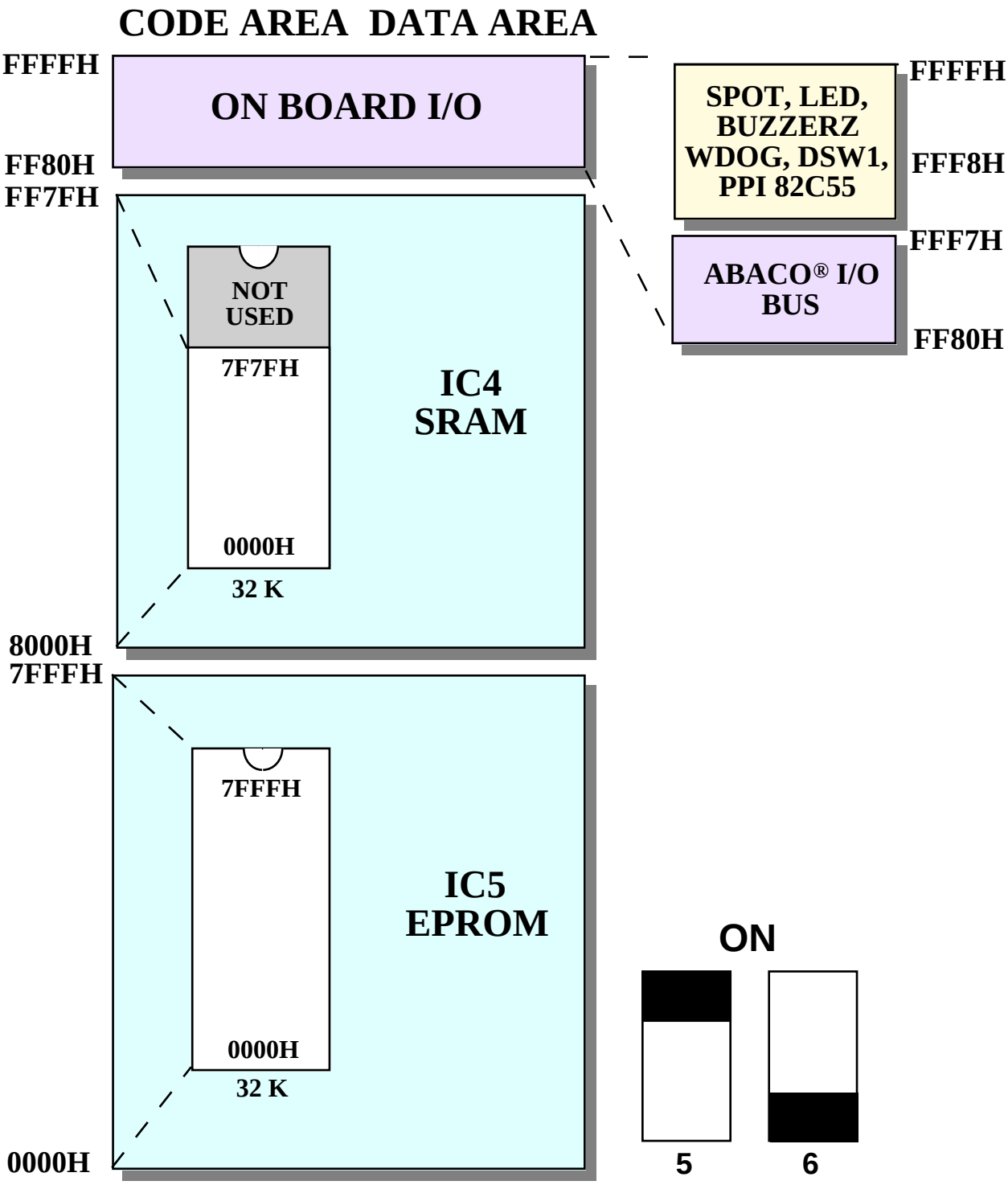

FIGURE 33: MODE 1 MEMORY CONFIGURATION

Configuration of switches 5 and 6 of DSW1: dip 5 **ON**; dip 6 **OFF**.
Used by software tools as: HI TECH C; DDS MICRO C; µC/51; BASCOM 8051; etc.

9) PAGE 48, PARAGRAPH MEMORY CONFIGURATION 3

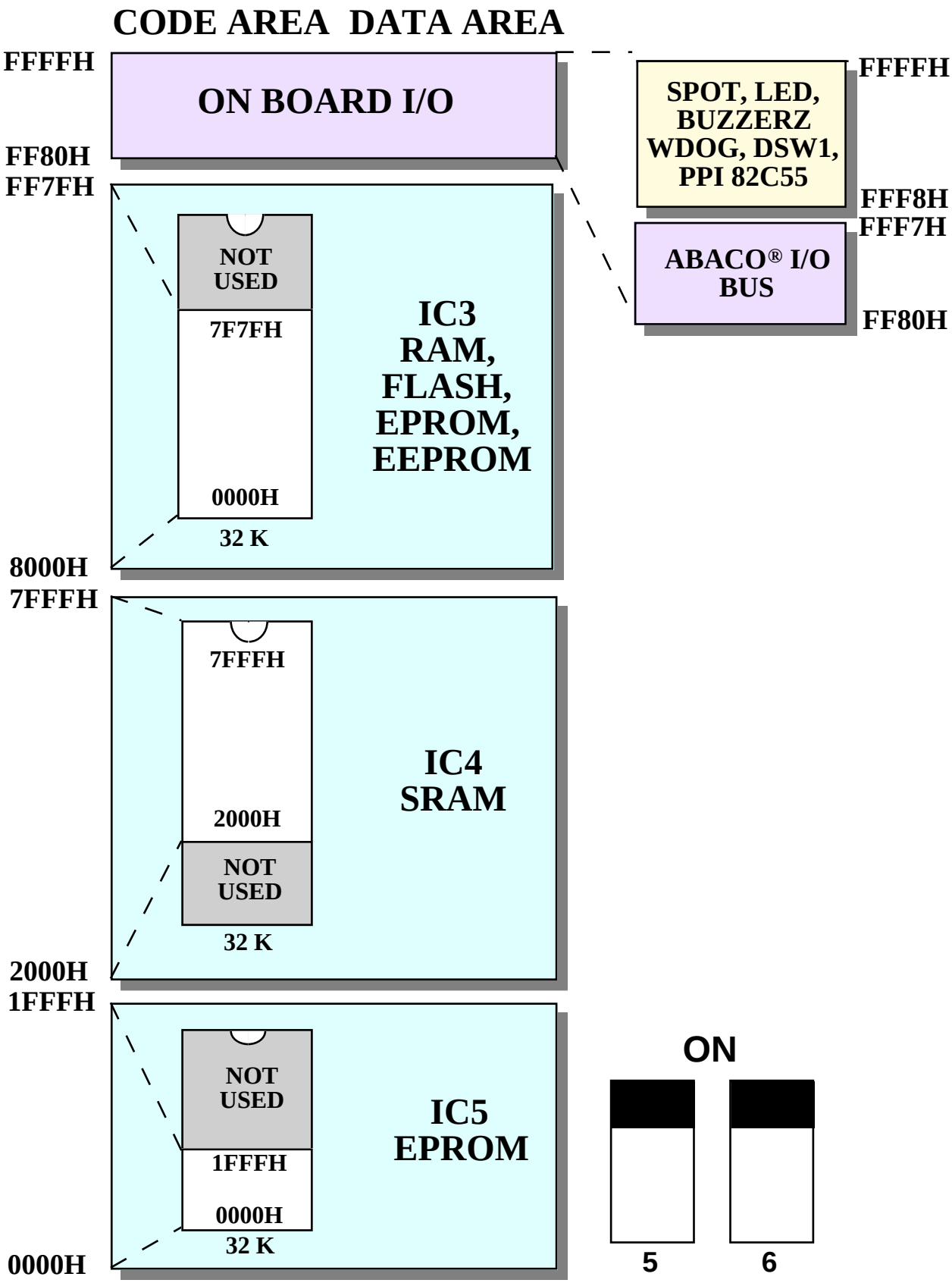

FIGURE 34: MODE 3 MEMORY CONFIGURATION

Configuration of switches 5 and 6 of DSW1: dip 5 **ON**; dip 6 **ON**.
Used by software tools as: MDP; LUCIFER HI TECH C; FMO 52;FMO 53; etc.