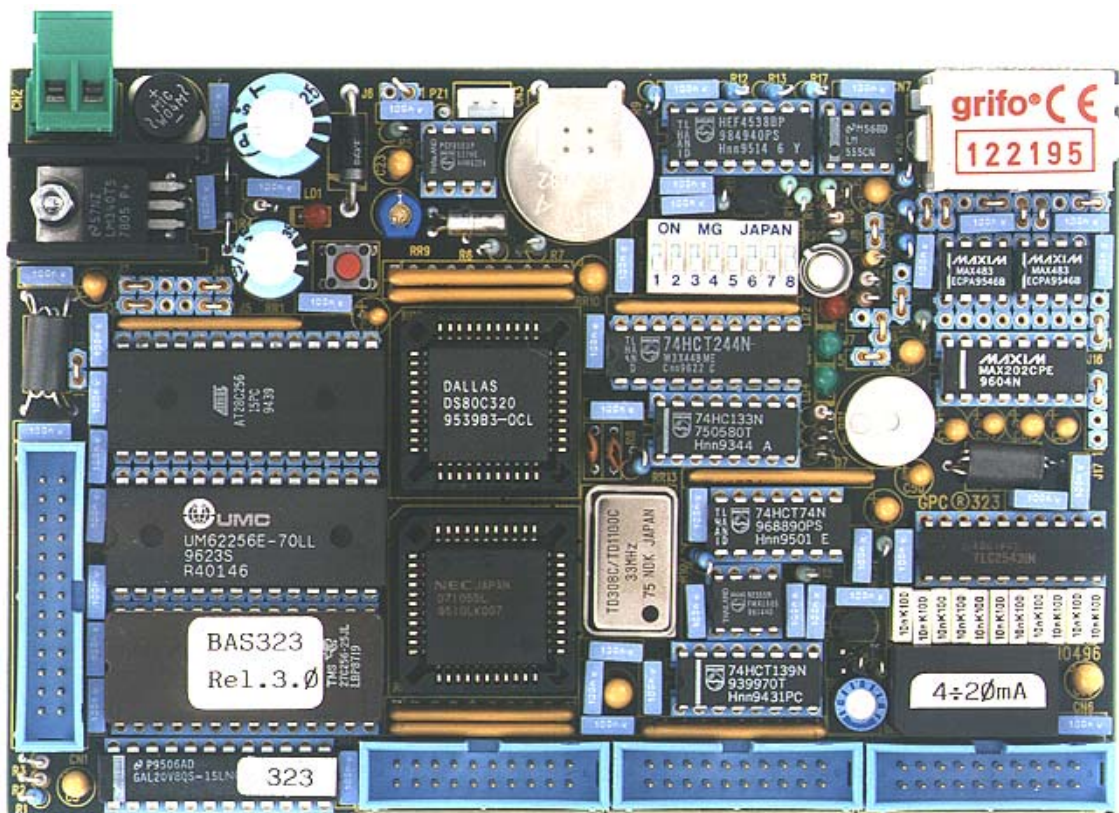


# GPC<sup>®</sup> 323

General Purpose Controller  
80C32, 80C320

## TECHNICAL MANUAL



**grifo<sup>®</sup>**

ITALIAN TECHNOLOGY

Via dell' Artigiano, 8/6  
40016 San Giorgio di Piano  
(Bologna) ITALY

E-mail: [grifo@grifo.it](mailto:grifo@grifo.it)

<http://www.grifo.it>

<http://www.grifo.com>

Tel. +39 051 892.052 (a.r.) FAX: +39 051 893.661



GPC<sup>®</sup> 323

Edition 5.20

Rel. 07 November 1999

, GPC<sup>®</sup>, grifo<sup>®</sup>, are trade marks of grifo<sup>®</sup>



# GPC<sup>®</sup> 323

General Purpose Controller  
80C32, 80C320

## TECHNICAL MANUAL

Intelligent **Abaco<sup>®</sup> BLOCK module**, 100x50 mm size; Optional plastic mount for connection to **DIN 46277-1** and **DIN 46277-3**  $\Omega$  rails; **14÷29 MHz 80C32** or **80C320 CPU**; 96 KBytes maximum addressable memory; Sockets for 32K EPROM, 32K RAM, 32K EEPROM, RAM or EPROM; **Back up** circuitry for **32 KBytes RAM** and optional **RTC with 256 Bytes RAM** through internal and external **lithium** battery; Optional serial **EEPROM 512 to 2048 Bytes** size; Eleven channels 12 Bits A/D Converter, +2,5V or 0÷20 mA full range, 10  $\mu$ s conversion time; 24 TTL I/O signals; One Dip Switch with 5 pins software readable; Three 16 bits Timer-Counter with Capture and Compare registers; Watchdog; Two RS 232 serial lines, one of which settable in RS 422-485 or Current Loop; 26 pins **Abaco<sup>®</sup>** I/O BUS expansion connector; Two 20 pins I/O **Abaco<sup>®</sup>** standard connectors; One 20 pins **Abaco<sup>®</sup>** standard A/D connector; IDLE MODE or POWER DOWN MODE; Optional **on-board power supply** or external **+5Vdc** power supply; On board protection against voltage peaks by **TransZorb<sup>™</sup>**; 4 status LEDs; 1 active buzzer.

**grifo<sup>®</sup>**

ITALIAN TECHNOLOGY

Via dell' Artigiano, 8/6  
40016 San Giorgio di Piano  
(Bologna) ITALY

E-mail: grifo@grifo.it

<http://www.grifo.it>

<http://www.grifo.com>

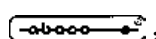
Tel. +39 051 892.052 (a.r.) FAX: +39 051 893.661



**GPC<sup>®</sup> 323**

Edition 5.20

Rel. 07 November 1999



, GPC<sup>®</sup>, grifo<sup>®</sup>, are trade marks of grifo<sup>®</sup>

## DOCUMENTATION COPYRIGHT BY grifo<sup>®</sup>, ALL RIGHTS RESERVED

No part of this document may be reproduced, transmitted, transcribed, stored in a retrieval system, or translated into any language or computer language, in any form or by any means, either electronic, mechanical, magnetic, optical, chemical, manual, or otherwise, without the prior written consent of **grifo<sup>®</sup>**.

### IMPORTANT

Although all the information contained herein have been carefully verified, **grifo<sup>®</sup>** assumes no responsibility for errors that might appear in this document, or for damage to things or persons resulting from technical errors, omission and improper use of this manual and of the related software and hardware.

**grifo<sup>®</sup>** reserves the right to change the contents and form of this document, as well as the features and specification of its products at any time, without prior notice, to obtain always the best product.

For specific informations on the components mounted on the card, please refer to the Data Book of the builder or second sources.

### SYMBOLS DESCRIPTION

In the manual could appear the following symbols:

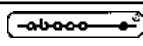


Attention: Generic danger



Attention: High voltage

### Trade Marks

, **GPC<sup>®</sup>**, **grifo<sup>®</sup>** : are trade marks of **grifo<sup>®</sup>**.

Other Product and Company names listed, are trade marks of their respective companies.

# GENERAL INDEX

<b>INTRODUCTION</b> .....	1
<b>CARD VERSION</b> .....	1
<b>GENERAL FEATURES</b> .....	2
CPU .....	3
CLOCK .....	3
POWER SUPPLY .....	4
SERIAL COMMUNICATION .....	4
MEMORY DEVICES .....	6
ON BOARD PERIPHERAL DEVICES .....	8
ABACO® I/O BUS .....	9
CONTROL LOGIC .....	9
RESET KEY .....	9
<b>TECHNICAL FEATURES</b> .....	10
GENERAL FEATURES .....	10
PHYSICAL FEATURES .....	10
ELECTRIC FEATURES .....	11
<b>INSTALLATION</b> .....	12
<b>CONNECTIONS</b> .....	12
CN 4 - POWER SUPPLY CONNECTOR .....	12
CN1 - ABACO® I/O BUS CONNECTOR .....	13
CN7 - PPI 82C55 PORT A AND C I/O CONNECTOR .....	14
CN8 - PPI 82C55 PORT B I/O CONNECTOR .....	16
CN6 - A/D CONVERTER INPUT CONNECTOR .....	18
CN3A - SERIAL LINE A CONNECTOR .....	20
CN3B - SERIAL LINE B CONNECTOR .....	26
CN2 - EXTERNAL BACK UP BATTERY CONNECTOR .....	27
OPERATOR INTERFACES .....	27
VISUAL FEEDBACK .....	28
I/O CONNECTION .....	28
RESET KEY .....	28
TEST POINT .....	29
DIP SWITCH .....	29
POWER SUPPLY VOLTAGES .....	29
INTERRUPTS MANAGEMENT .....	30
TYPE OF ANALOG INPUT SELECTION .....	30
TRIMMERS AND CALIBRATION .....	31
<b>JUMPERS</b> .....	32
2 PINS JUMPERS .....	34
3 PINS JUMPERS .....	36
6 PINS JUMPERS .....	37

NOTE .....	37
BACK UP .....	37
SERIAL COMMUNICATION TYPE SELECTION .....	37
MEMORY SELECTION .....	39
SOFTWARE .....	40
HARDWARE .....	41
INTRODUCTION .....	41
ADDRESSES .....	41
I/O ADDRESSES .....	42
MEMORY ADDRESSES .....	42
MEMORY CONFIGURATION 1 .....	43
MEMORY CONFIGURATION 3 .....	44
MEMORY CONFIGURATION 4 .....	45
PERIPHERAL DEVICES SOFTWARE DESCRIPTION .....	46
DIP SWITCH .....	46
ACTIVITY LED .....	46
EXTERNAL WATCHDOG .....	46
BUZZER .....	47
SPOT LED .....	47
PPI 82C55 .....	47
RS 422-485 COMMUNICATION DIRECTION .....	48
SERIAL EEPROM .....	48
BACKED RAM + SERIAL RTC .....	48
A/D CONVERTER .....	49
SERIAL LINES .....	49
TIMER COUNTER .....	49
INTERNAL WATCH DOG .....	49
EXTERNAL DEVICES FOR GPC® 323 .....	50
BIBLIOGRAPHY .....	54
APPENDIX A: JUMPERS LOCATION .....	A-1
APPENDIX B: ON BOARD PERIPHERAL DESCRIPTION .....	B-1
μP 80C32 .....	B-1
μP 80C320 .....	B-11
APPENDIX C: ALPHABETICAL INDEX .....	B-1

# FIGURE INDEX

FIGURE 1: BLOCK DIAGRAM .....	5
FIGURE 2: COMPONENTS MAP .....	7
FIGURE 3: CN4 - POWER SUPPLY CONNECTOR .....	12
FIGURE 4: CN1 - ABACO® I/O BUS CONNECTOR .....	13
FIGURE 5: CN7 - PPI 82C55 PORT A AND C I/O CONNECTOR .....	14
FIGURE 6: I/O SIGNALS CONNECTION DIAGRAM .....	15
FIGURE 7: CN8 - PPI 82C55 PORT B I/O CONNECTOR .....	16
FIGURE 8: LEDs, CONNECTORS, DIP SWITCH, ETC. LOCATION .....	17
FIGURE 9: CN6 - A/D CONVERTER INPUT CONNECTOR .....	18
FIGURE 10: A/D CONVERTER INPUT BLOCK DIAGRAM .....	19
FIGURE 11: CN3A - SERIAL LINE A CONNECTOR .....	20
FIGURE 12: SERIAL COMMUNICATION DIAGRAM .....	21
FIGURE 13: RS 232 PIN-OUT AND CONNECTION EXAMPLE .....	22
FIGURE 14: RS 422 PIN-OUT AND CONNECTION EXAMPLE .....	22
FIGURE 15: RS 485 PIN-OUT AND CONNECTION EXAMPLE .....	22
FIGURE 16: RS 485 NETWORK CONNECTION EXAMPLE .....	23
FIGURE 17: CURRENT LOOP PIN-OUT AND 4 WIRES CONNECTION EXAMPLE .....	24
FIGURE 18: CURRENT LOOP PIN-OUT AND 2 WIRES CONNECTION EXAMPLE .....	24
FIGURE 19: CARD PHOTO .....	25
FIGURE 20: CN3B - SERIAL LINE B CONNECTOR .....	26
FIGURE 21: CN2 - EXTERNAL BACK UP BATTERY CONNECTOR .....	27
FIGURE 22: VISUAL FEEDBACK TABLE .....	28
FIGURE 23: JUMPERS SUMMARIZING TABLE .....	32
FIGURE 24: COMPONENT SIDE JUMPERS LOCATION .....	33
FIGURE 25: 2 PINS JUMPERS TABLE .....	34
FIGURE 26: SOLDER SIDE JUMPERS LOCATION .....	35
FIGURE 27: 3 PINS JUMPERS TABLE .....	36
FIGURE 28: 6 PINS JUMPERS TABLE .....	37
FIGURE 29: MEMORY SELECTION TABLE .....	39
FIGURE 30: I/O ADDRESSES TABLE .....	42
FIGURE 31: MEMORY CONFIGURATION 1 (ASM) .....	43
FIGURE 32: MEMORY CONFIGURATION 3 (ASM) .....	44
FIGURE 33: MEMORY CONFIGURATION 4 (BASIC) .....	45
FIGURE 34: POSSIBLE CONNECTIONS DIAGRAM .....	55
FIGURE A1: MEMORY JUMPERS LOCATION .....	A-1
FIGURE A2: SERIAL COMMUNICATION JUMPERS LOCATION .....	A-2
FIGURE A3: SERIAL COMMUNICATION DRIVERS LOCATION .....	A-3





## INTRODUCTION

The use of these devices has turned - IN EXCLUSIVE WAY - to specialized personnel.

The purpose of this handbook is to give the necessary information to the cognizant and sure use of the products. They are the result of a continual and systematic elaboration of data and technical tests saved and validated from the manufacturer, related to the inside modes of certainty and quality of the information.

The reported data are destined- IN EXCLUSIVE WAY- to specialized users, that can interact with the devices in safety conditions for the persons, for the machine and for the enviroment, impersonating an elementary diagnostic of breakdowns and of malfunction conditions by performing simple functional verify operations , in the height respect of the actual safety and health norms.

The informations for the installation, the assemblage, the dismantlement, the handling, the adjustment, the reparation and the contingent accessories, devices etc. installation are destined - and then executable - always and in exclusive way from specialized warned and educated personnel, or directly from the TECHNICAL AUTHORIZED ASSISTANCE, in the height respect of the manufacturer recommendations and the actual safety and health norms.

The devices can't be used outside a box. The user must always insert the cards in a container that respect the actual safety normative. The protection of this container is not threshold to the only atmospheric agents, but specially to mechanic, electric, magnetic, etc. ones.

To be on good terms with the products, is necessary guarantee legibility and conservation of the manual, also for future references. In case of deterioration or more easily for technical updates, consult the AUTHORIZED TECHNICAL ASSISTANCE directly.

To prevent problems during card utilization, it is a good practice to read carefully all the informations of this manual. After this reading, the user can use the general index and the alphabetical index, respectly at the begining and at the end of the manual, to find information in a faster and more easy way.

## CARD VERSION

The present handbook is reported to the **GPC® 323** card release **110197** and later. The validity of the bring informations is subordinate to the number of the card release. The user must always verify the correct correspondence among the two denotations. On the card the release number is present in more points both board printed diagram (serigraph) and printed circuit (for example on the bottom right corner on the component side).

## GENERAL FEATURES

**GPC® 323** is a powerful, low cost, controller module capable of operating in stand alone mode or as an intelligent peripheral, and/or remoted, in a wider telecontrol or aquisition network. The **GPC® 323** board is secured in a plastic mount for connection to **Omega** rails **DIN 46277-1** and **DIN 46277-3**, thereby dispensing with the need of rack and allowing a cheaper mounting direct to the electrical control panel. The most intresting feature of this board is the wide choice of microcontrollers it can mount. The board can be delivered with an 80C32 or the faster 80C320, the board general features remain the same but the performance vary remarkably according to the microcontroller installed. It is also possible to supply the board in many different ways, to solve any installation problem without no need to use expansive external power supplies. **GPC® 323** board is provided with a set of **Abaco®** standard connectors, allowing the User to connect it to any of the **BLOCK** I/O module or to third parts or User made interfaces to the field.

The **Abaco® I/O BUS** connector allows to drive directly the **ZBR 324** and **ZBT 324** cards and through **ABB 03**, **ABB 05** and so on, it is possible to run all peripheral cards available on **Abaco® BUS**.

Many software development tools, both in Assembler and in high level languages, are available to allow the User to employ the **GPC® 323** board as a development system of its own applications. Noteworthy among these tools are the several **C Compilers**, the **FORTH** and the comfortable **BASIC 323**.

- Intelligent **Abaco® BLOCK module, 4 serie**, 100x50 mm size
- Optional plastic mount for connection to **DIN 46277-1** and **DIN 46277-3**  $\Omega$  rails
- **14÷20 MHz 80C32** or **80C320 CPU**, up to 96 KBytes maximum addressable memory
- Sockets for 32K EPROM, 32K RAM, 32K EEPROM, RAM or EPROM
- **Back up** circuitery for **32 KBytes RAM** through internal **lithium** battery
- Optional **RTC with 256 Bytes RAM** backed through internal and external **lithium** battery
- Optional serial **EEPROM 512 to 2048 Bytes** size, maximum size is 1024 bytes if RTC is installed
- Eleven channels **12 Bits A/D Converter**, +2,5V or 0÷20 mA full range, 10  $\mu$ s conversion time
- 24 **TTL** I/O signals
- 4 status **LEDs**, 2 of which **software programmable**, and active **BUZZER**
- One **Dip Switch** with **5 pins software readable**
- Three **16 bits Timer-Counter** with **Capture and Compare registers**
- **Watchdog**
- Two **RS 232 serial lines**, one of which settable in **RS 422**, **RS 485** or **Current Loop**
- 26 pins **Abaco® I/O BUS** expansion connector
- Two 20 pins I/O **Abaco®** standard connectors
- **IDLE MODE** or **POWER DOWN MODE** power saving features
- Optional **on-board power supply** or external **+5Vdc** power supply
- On board protection aganist voltage peaks by **TransZorb™**
- Wide availability of software development tools as **Monitor, Debugger, Assembler, GET 51 and Interpretated BASIC, BASIC Compiler, FORTH, C Compiler, HTC-51, HTC-51XA, PLM 51, PASCAL Compiler**, etc.

Here follows a description of the board's functional blocks, with an indication of the operations performed by each one. To easily locate these blocks and verify their connections please refer to figure 1.

## CPU

**GPC® 323** board is designed to employ four different types of microcontroller: **80C32** manufactured by INTEL and other several manufacturers, **80C320** manufactured by DALLAS. These 8 and 16 bits CPU feature an extended instructions set, high speed of execution, efficient vectored interrupts management and a wide range of peripherals inside the CPU.

All paragraphs of this manual report a description of the features common to all microcontrollers distinguishing where needed.

Here follow the lists of the CPU features that the User is enabled to employ, according to the type of microcontroller installed:

- μP 80C32:
- 8 bits CPU
  - 256 Bytes of internal RAM
  - One 8 bits I/O port
  - 64K + 64K directly addressable memory
  - Three 16 bits Timer/Counters
  - 6 interrupt sources with 2 priority levels
  - 1 full duplex serial line

- μP 80C320:
- 8 bits CPU
  - 256 Bytes of internal RAM
  - One 8 bits I/O port
  - 64K + 64K directly addressable memory
  - Three 16 bits Timer/Counters
  - 13 interrupt sources with 3 priority levels
  - 2 full duplex serial lines
  - Power fail circuitry
  - Watchdog timer
  - Power down and idle mode management

For further informations about these components please refer to the manufacturer documentations.

## CLOCK

On **GPC® 323** board two different circuits provide the CPU clock frequency and the Real Time Clock frequency. This solution has been chosen because using a separate circuit to generate the CPU clock allows to change it without having to make any other modification to the rest of the board. The Real Time Clock frequency is unique, its value is 32768 Hz, the CPU clock frequency may be picked from the following values:

- μP 80C32:        14.7456 MHz or 22.1184 MHz  
μP 80C320:      22.1184 MHz or 29.4912 MHz

Please remark that the CPU working frequency determines the baud rate for the serial communication line/s.

## POWER SUPPLY

The GPC® 323 board can be optionally provided with the power supply section capable to generate the unique +5 Vdc voltage needed to supply the board. Should the supply section be absent, the +5Vdc voltage is the only one needed to supply the board, otherwise two different types of supply sections are available: linear supply section, which requires an alternate input voltage in the range 6÷12 Vac; switching supply section, which requires an alternate input voltage in the range 15÷24 Vac (for further informations please refer to the paragraph “SUPPLY VOLTAGES”). The supply voltage can be supplied through proper standard connectors fast and easy to use. The power supply circuit is designed for reducing the consumption (the microprocessor power down and idle modes are available) and for increasing the electrical noise immunity.

The type of supply cannot be changed by the User so it must be specified in the order.

## SERIAL COMMUNICATION

GPC® 323 board is always provided with an hardware serial communication line (called serial A) which is completely software settable for protocol and for speed. These settings are performed programming the ASP inside the microprocessor, so for further informations, please refer to the manufacturer documentation or to appendixes of this manual. The board also provides a second serial communication line (called serial B) made as follows:

μP 80C32: software serial port managed through two microprocessor I/O signals  
μP 80C320: hardware serial port managed through microprocessor inside registers

The User can set by software also protocol and speed of serial B, in case of software serial line the software itself will have to perform all the settings (for further informations please refer to the software tools manuals or contact **grifo**®).

The serial line B is always buffered as RS 232, while for serial line A by hardware it is possible to select, through some on board jumpers, the electric communication protocol. In detail, it can be buffered as: RS 232, passive Current Loop or RS 422-485; in this last cases also full duplex or half duplex are programmable.

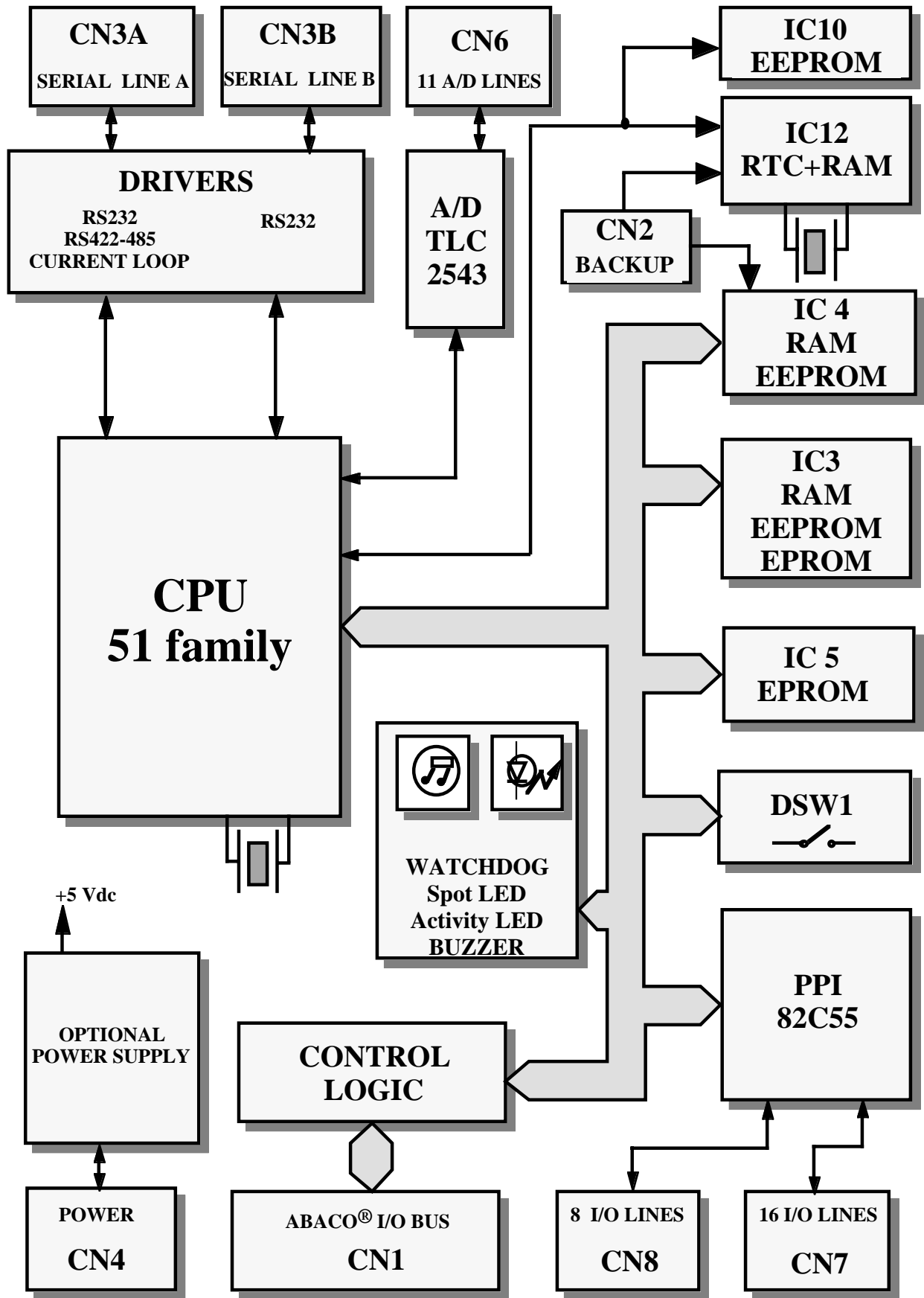


FIGURE 1: BLOCK DIAGRAM

## MEMORY DEVICES

On the card can be monted 98K bytes plus 256 bytes of memory divided with a maximum of 32K EPROM, 32K RAM or EEPROM, 32K RAM or EEPROM or EPROM, 256 bytes serial RAM+RTC and 2K serial EEPROM. The **GPC® 323** memory configuration must be chosen considering the application to realize or the specific requirements of the user. Normally the card is equipped with 32K bytes of RAM and all different configurations must be specified by the User, at the moment of the order.

With the on board back up circuit there is the possibility to keep 32K plus 256 bytes RAM, also when power supply is failed; in this way the card is always able to maintain parameters, logged data, system status and configuration, etc. without using expensive external UPS. The back up circuit is supplied by a on board lithium battery or an external battery to be connected to a specific connector. Should the amount of backed memory result insufficient, it is possible to add backed RAM modules and/or EEPROM.

The memory module to install in IC12 can also be provided with a Real Time Clock capable to manage through software time (hours, minutes, seconds) and date (day, month, year, day of week). The memory resources mapping is performed by a specific circuitry that allocates the memory devices inside the microprocessor addressing space; this control logic also provides to manage automatically the different memory mappings provided to suite the needs of the several software packages available for **GPC® 323** board.

For further informations please refer to the chapter “HARDWARE DESCRIPTION” and “PERIPHERALS SOFTWARE DESCRIPTION”.

For further informations about memory configuration, sockets description and jumpers connection, please refer to paragraph "MEMORY SELECTION".

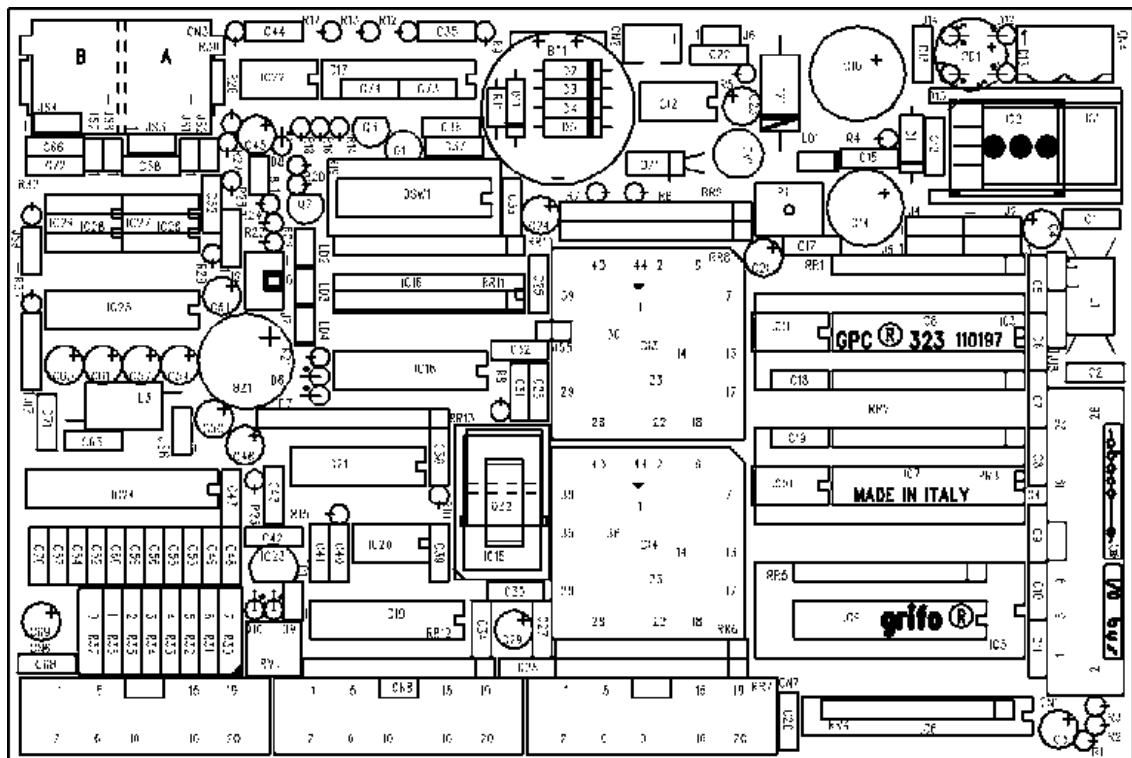
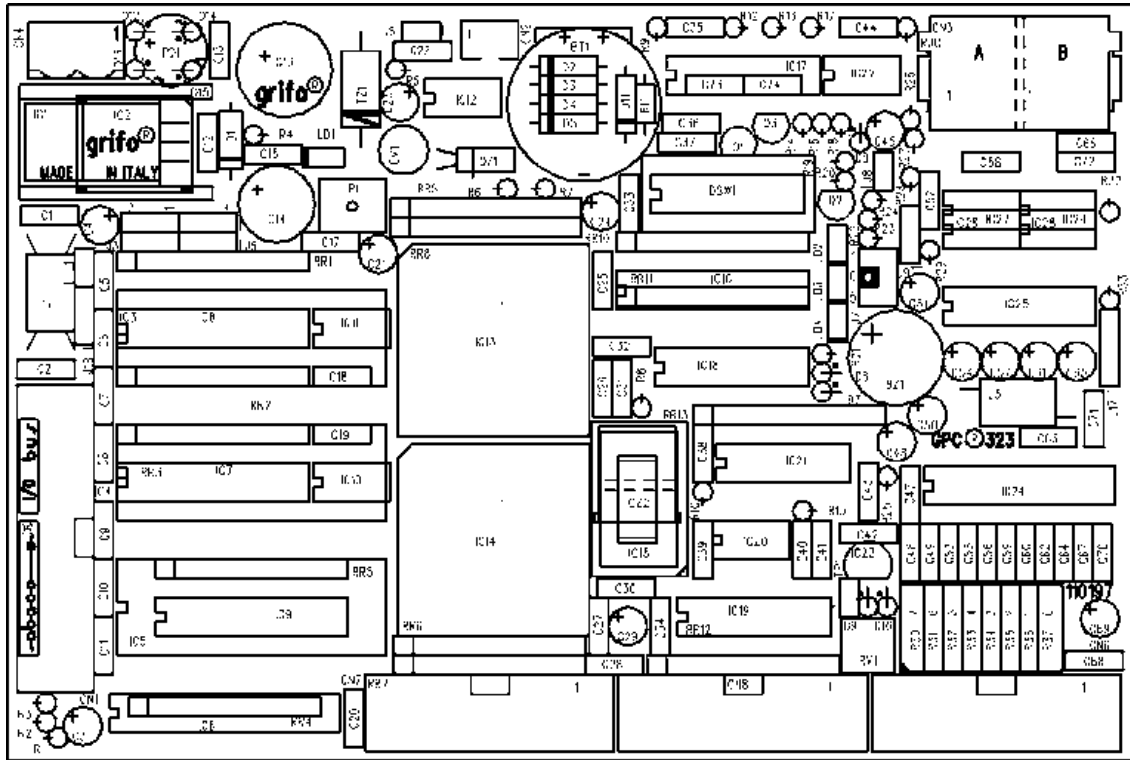


FIGURE 2: COMPONENTS MAP



## ON BOARD PERIPHERAL DEVICES

**GPC® 323** board has been designed to solve several problems of industrial automation control, so it has been provided with peripheral devices that perform an interface to the external world.

In detail:

- **A/D converter:** this peripheral can acquire 11 channels with a maximum resolution of 12 bits. By software it is possible to decide which channels to employ, to start and to stop the acquisition, etc., through a synchronous communication to the device. By means to simplify the management of this device some software packages provide utility procedures that are capable to manage all its parts. The connectable analog signals are variable voltage signals in the range 0÷2.49V (optional 0÷5V to specify in the order) or current signals in the range 0÷20 mA. This device is optional and must be explicitly requested in the order.
- **Watchdog:** a stable section not microprocessor inside with about 1.5 s of intervention time. The retrigger is completely software performed through the access to opportune registers located in the microprocessor addressing space and gives to the board an extremely high degree of safety. The intervention time can be changed on request of the User by intervening on specific RC networks (in case of need please contact **grifo®**). Should the board use microprocessors provided with a watch dog section inside the User could take advantage of two separated circuitry providing different characteristics, so the safety degree of the board would increase.
- **Board configuration:** to make the board and the applications program developed for it easier to configure an 8 pins dip switch has been installed. This dip switch has a triple configuration purpose: to select memory configuration, to select the RUN/DEBUG modality and to configure the management software. The possibility to read by software the status of some switches allows the User the chance to manage several working conditions through an unique program without no need to employ more input signals (characteristic applications are: language selection, program parameter determination, working modalities selection, etc.). On **GPC® 323** board two activity LEDs have been installed, these LEDs are software managed and the User may employ them to provide visual feedback about the system status.
- **Real Time Clock:** the backed RAM module to install on IC12 can be provided with a complete Real Time Clock module capable to manage hour, minutes, seconds, day of month, month, year and day of week as a stand alone device. This component is optional and installed only if explicitly requested in the order.
- **Serial EEPROM:** the serial EEPROM module to install on IC10 is essential to the User who needs to keep informations in memory also when power supply fails without using the backed RAM module, obtaining this way an extremely high degree of safety for data integrity. Size of this module can vary in the range 512÷2048 bytes, it is optional and must be explicitly specified in the order.
- **Buzzer:** **GPC® 323** board features a capacitive buzzer capable to produce a constant sound, driven by a circuitry that can be software enabled and/or disabled through the control logic, that can be used to generate acoustic alerts, sound feedback, etc.



- **PPI 82C55**: this peripheral can manage three 8 bits parallel ports performing 24 TTL level I/O signals whose directionality is byte-level software settable. These I/O signals provide the **GPC® 323** board more employ possibilities (for example the management of non intelligent peripherals, interfaces, etc.) also in applications where the communication handshake must be completely software managed. PPI 82C55 can be completely programmed through four registers located in the CPU addressing space.

For further informations about the above described peripherals devices, please refer to the manufacturer documentation or to appendix A of this manual.

### ABACO® I/O BUS

One of the most important features of **GPC® 323** board is its possibility to be interfaced to industrial **ABACO® I/O BUS**. Thanks to this standard connector, the card can be connected to some of the numerous **grifo®** boards, both intelligent and not. For example the user can directly use cards for analog signals acquisition, cards for analog signals generation (D/A), cards for digital I/O signals management, cards with timers and counters, cards for temperature controls, etc. also custom boards designed to satisfy specific needs of the end user.

Using **ABB 03** or **ABB 05** mother boards it is possible manage even all the **BUS ABACO®** single EURO cards. So **GPC® 884** becomes the right component for each industrial automation system, in fact **ABACO® I/O BUS** makes the card easily expandable with the best price/performance ratio.

### CONTROL LOGIC

Registers of all the peripherals installed on **GPC® 323** board are mapped through a specific control logic circuit that maps them inside the microprocessor addressing space. For further informations please refer to the paragraph "I/O MAPPING".

### RESET KEY

**GPC® 323** board features a comfortable reset key that, when pushed, restarts the board from a general reset condition. The main purpose of this key is to exit from infinite loop conditions, useful especially during the debug phase or to warrant a special starting status.

## TECHNICAL FEATURES

### GENERAL FEATURES

**Board Resources:**  
(except  $\mu$ P resources)

- 24 TTL programmable Input/Output signals
- 1 RS 232 or RS 422-485 or Current Loop bidirectional line
- 1 RS 232 bidirectional line
- 1 Hardware Watchdog
- 11 A/D converter signals
- 1 Reset key
- 1 Real Time Clock
- 2 Software manageable LEDs
- 1 Eight pins Dip Switch (5 software readables)
- 1 **Abaco<sup>®</sup> I/O BUS** expansion connector

**Addressable Memory:**

- IC 5: EPROM 32K x 8
- IC 4: RAM/EEPROM from 8K x 8 to 32K x 8
- IC 3: RAM/EEPROM/EPROM from 8K x 8 to 32K x 8
- IC 10: Serial EEPROM from 512 byte to 2048 byte
- IC 12: Serial RAM+RTC 256 byte

**CPU:** INTEL 80C32; DALLAS 80C320

**Clock Frequency:**

- $\mu$ P 80C32: 14.7456 MHz or 22.1184 MHz
- $\mu$ P 80C320: 22.1184 MHz or 29.4912 MHz

**A/D Resolution:** 12 bits

**A/D Conversion Time:** 10  $\mu$ s

### PHYSICAL FEATURES

**Size:** 100 x 149 mm

**Weight:** 170 g (complete configuration)

**Connectors:**

- CN1: 26 pins, male, vertical, low profile connector
- CN2: 2 pins, male, vertical, low profile connector
- CN3A: 6 pins, Plug, female
- CN3B: 6 pins, Plug, female
- CN4: 2 pins screw terminal connector
- CN6: 20 pins, male, vertical, low profile connector
- CN7: 20 pins, male, vertical, low profile connector
- CN8: 20 pins, male, vertical, low profile connector

**Temperature Range:** from 0 to 70 centigrad degrees

**Reactive Humidity:** 20% op tp 90% (without condense)

**Watchdog Intervent Time:** 1.5 s

### ELECTRIC FEATURES

**Power Supply:**

5 Vdc	(without power supply section)	
6 ÷ 12 Vac	(linear power supply section)	*
15 ÷ 24 Vac	(switching power supply section)	

**Consumption on 5 Vdc:**

µP 80C32:	100÷300 mA
µP 80C320:	200÷400 mA

**Current provided on +5 Vdc for external loads:**

µP 80C32:	300÷100 mA (switching)	*
	900÷700 mA (linear)	*
µP 80C320:	200÷0 mA (switching)	*
	800÷600 mA (linear)	*

**External Back up Battery:** 3.6÷5 Vdc

**Back up Current:** 15 µA

**Analog Inputs Voltage:** 0÷2.49 Vcc or 0÷5 Vcc

**Analog Inputs Current:** 0÷20 mA

**Analog Inputs Impedance:** 1 KΩ

**RS 422-485 Termination Net:**

Line termination resistance	=	120 Ω
Positive pull up resistance	=	3.3 KΩ
Negative pull down resistance	=	3.3 KΩ

\* Data here reported are referred to a 20 centigrad degreees environmental temperature (for further informations please refer to the paragraph “SUPPLY VOLTAGES”).

## INSTALLATION

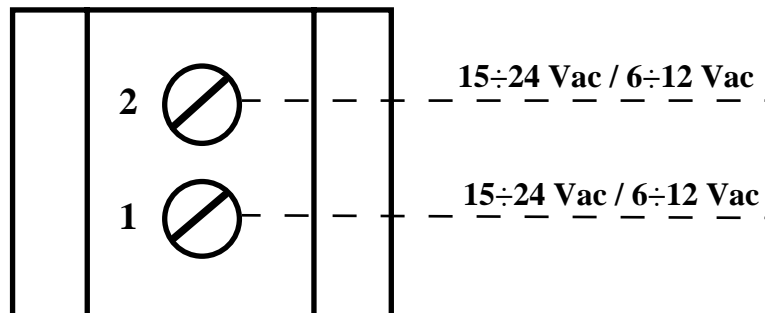
In this chapter there are the information for a right installation and correct use of the card. The user can find the location and functions of each connectors, trimmers, LEDs, jumpers and some explanatory diagrams.

### CONNECTIONS

The **GPC<sup>®</sup>323** module has 7 connectors that can be linkeded to other devices or directly to the field, according to system requirements. In this paragraph there are connectors pin outs, a short signals description (including the signals direction) and connectors location (see figure 8), plus some figures that describe how the interface signals are connected on the card.

#### **CN 4 - POWER SUPPLY CONNECTOR**

CN4 is a 2 pins screw terminal connector. The board supply voltage must be provided through this connector. When using the board without any power supply section, the +5 Vdc must be provided through pin 26 (+Vdc) and pin 25 (GND) of CN1.



**FIGURE 3: CN4 - POWER SUPPLY CONNECTOR**

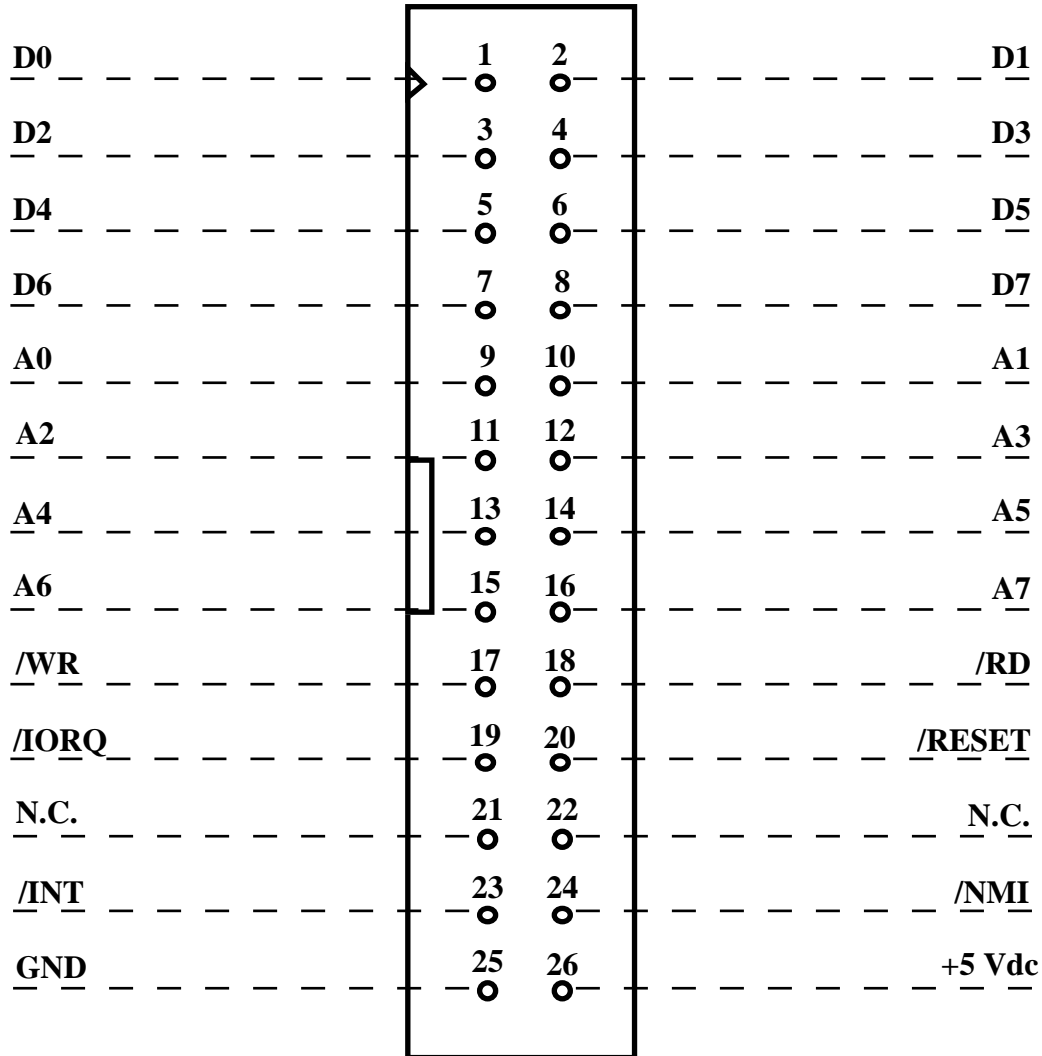
Signals description:

**15÷24 Vac / 6÷12 Vac =** I - 15÷24 Vac power supply signals (switching supply section)  
 I - 6÷12 Vac power supply signals (linear supply section)

**CN1 - ABACO® I/O BUS CONNECTOR**

CN1 is a 26 pins, male, vertical, low profile connector.

Through CN1 the card can be connected to external expansion modules developed by the user or to the numerous **grifo®** boards, both intelligent and not. All this connector's signals are at TTL level and follow the **ABACO® I/O BUS** standard.



**FIGURE 4: CN1 - ABACO® I/O BUS CONNECTOR**

Signals description;

- A0-A7** = O - Address BUS.
- D0-D7** = I/O - Data BUS.
- /INT BUS** = I - Interrupt request (open collector type).
- /NMI BUS** = I - Non maskable interrupt (open collector type).
- /IORQ** = O - Input output request.
- /RD** = O - Read cycle status.
- /WR** = O - Write cycle status.
- /RESET** = O - Reset.
- +5 Vdc** = I/O - +5 Vdc power supply.
- GND** = - Ground signal.
- N.C.** = - Not connected

## CN7 - PPI 82C55 PORT A AND C I/O CONNECTOR

CN7 is a 20 pins, male, vertical, low profile connector, 2.54 mm pitch. Through CN1 two of the three programmable peripheral PPI 82C55 8 bits parallel ports are connected to external world. All this connector's signals are at TTL level and follow the **ABACO® I/O BUS** standard.

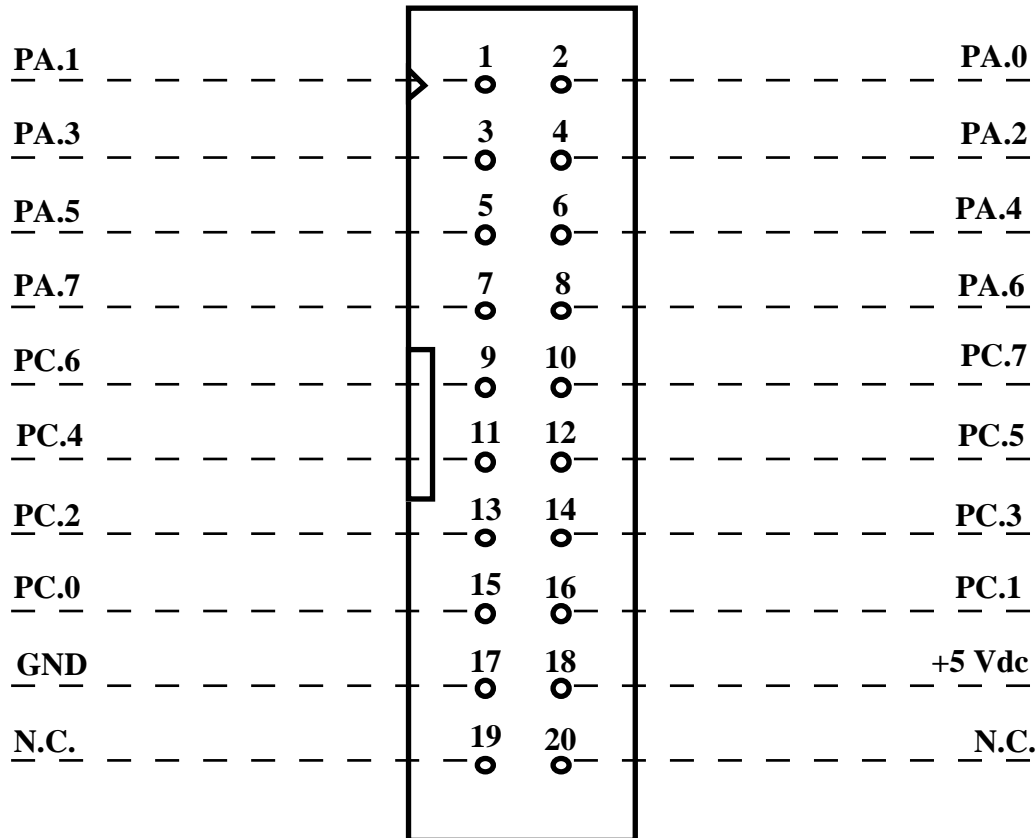


FIGURE 5: CN7 - PPI 82C55 PORT A AND C I/O CONNECTOR

Signals description:

<b>PA.n</b>	=	I/O	-	PPI 82C55 port A n-th digital signal
<b>PC.n</b>	=	I/O	-	PPI 82C55 port C n-th digital signal
<b>GND</b>	=	-	-	Ground signal
<b>+5 Vdc</b>	=	O	-	+5 Vcc signal
<b>N.C.</b>	=	-	-	Not connected

Remarkable is the possibility to connect directly through CN7 a set of interfaces designed to solve several typical problems of industrial automation. We especially would want to remark the simplicity of installation and software management of **QTP 24P**, **KDL x24**, **KDF 224**, etc., that are also supported by high level programming languages. For further informations please refer to the paragraph "OPERATOR INTERFACES".

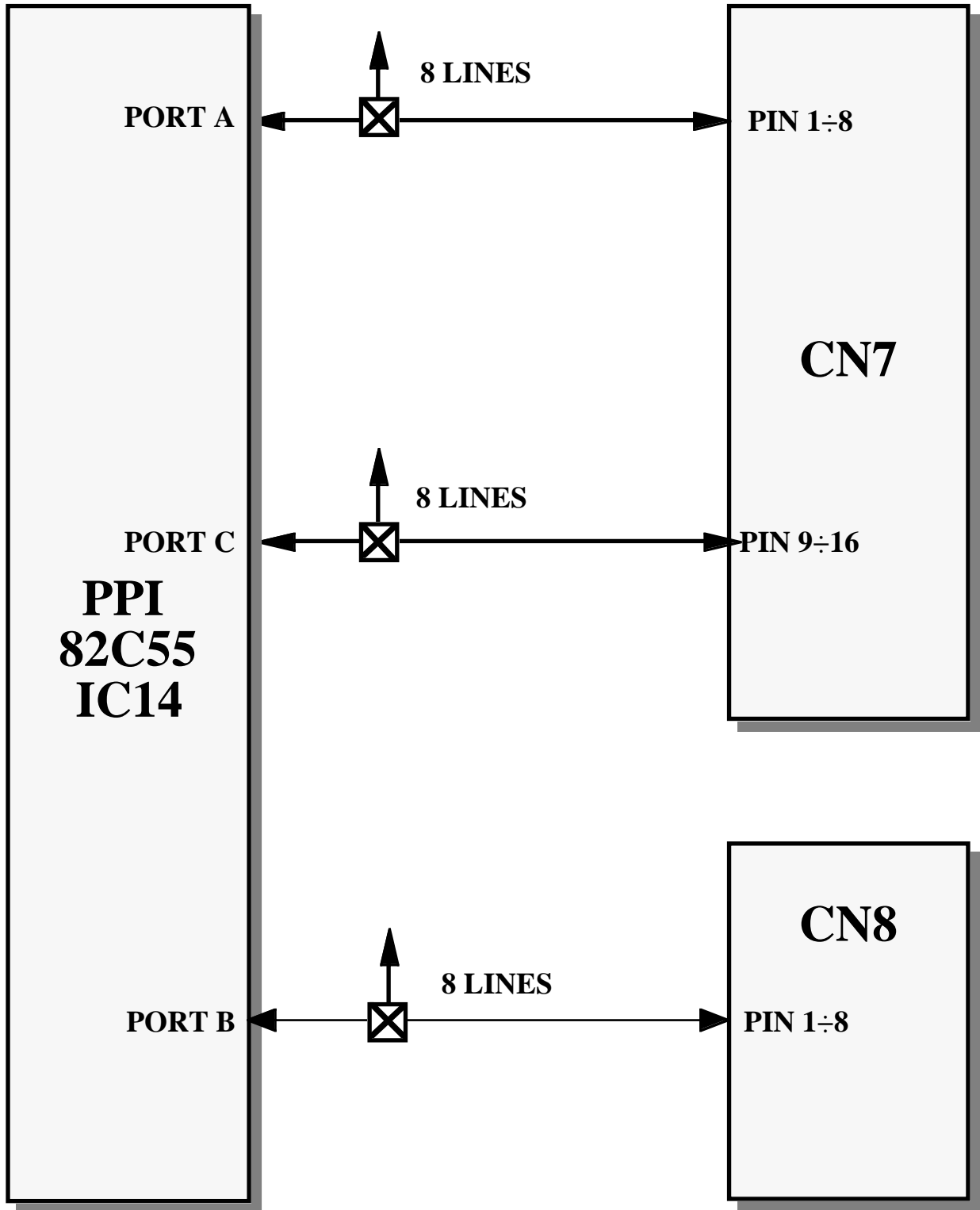


FIGURE 6: I/O SIGNALS CONNECTION DIAGRAM

## CN8 - PPI 82C55 PORT B I/O CONNECTOR

CN8 is a 20 pins, male, vertical, low profile connector, 2.54 mm pitch. Through CN8 one of the three programmable peripheral PPI 82C55 8 bits parallel ports are connected to external world. All this connector's signals are at TTL level and follow the **ABACO® I/O BUS** standard.

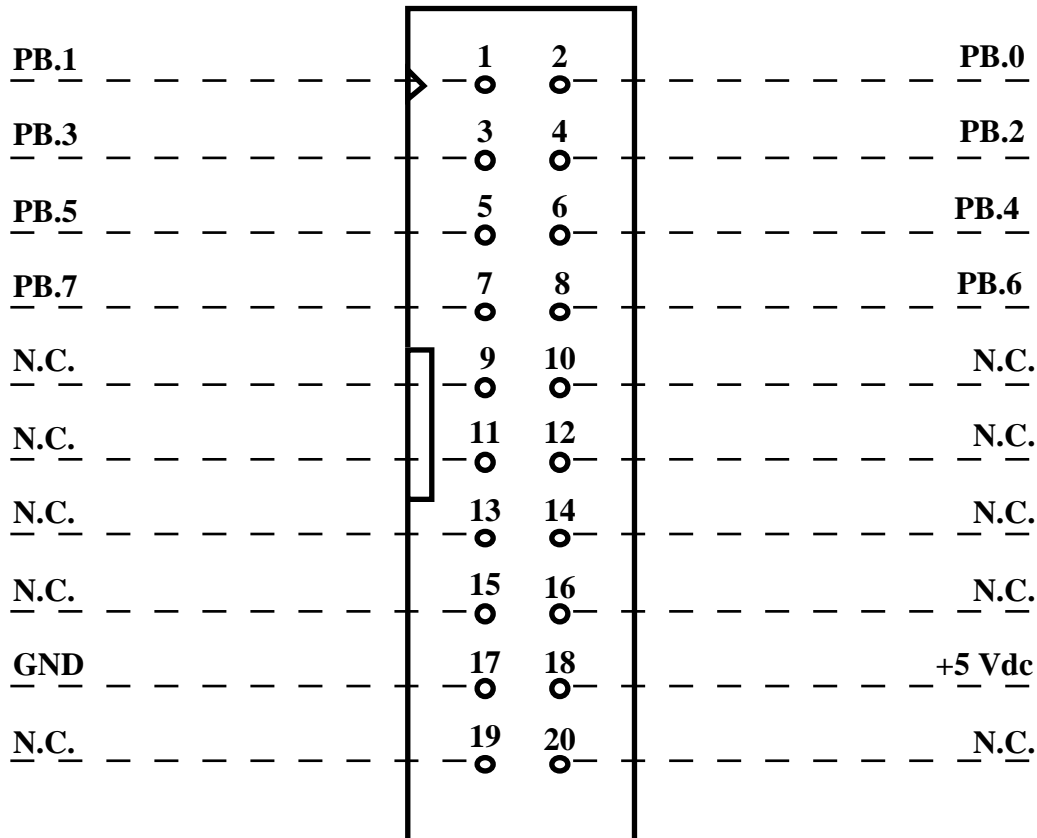


FIGURE 7: CN8 - PPI 82C55 PORT B I/O CONNECTOR

Signals description:

<b>PB.n</b>	=	I/O	-	PPI 82C55 port B n-th digital signal
<b>GND</b>	=	-	-	Ground signal
<b>+5 Vdc</b>	=	O	-	+5 Vcc signal
<b>N.C.</b>	=	-	-	Not connected



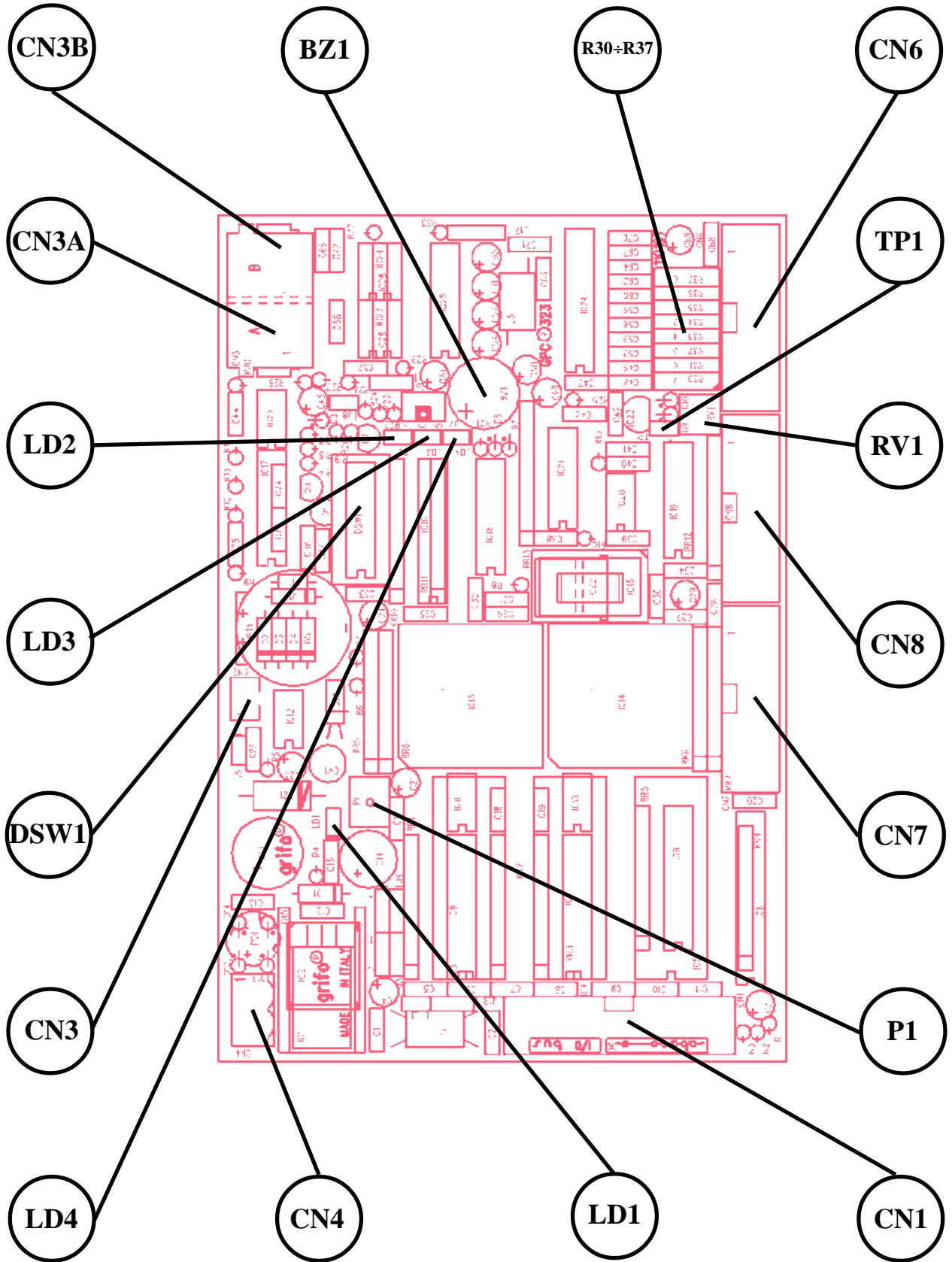
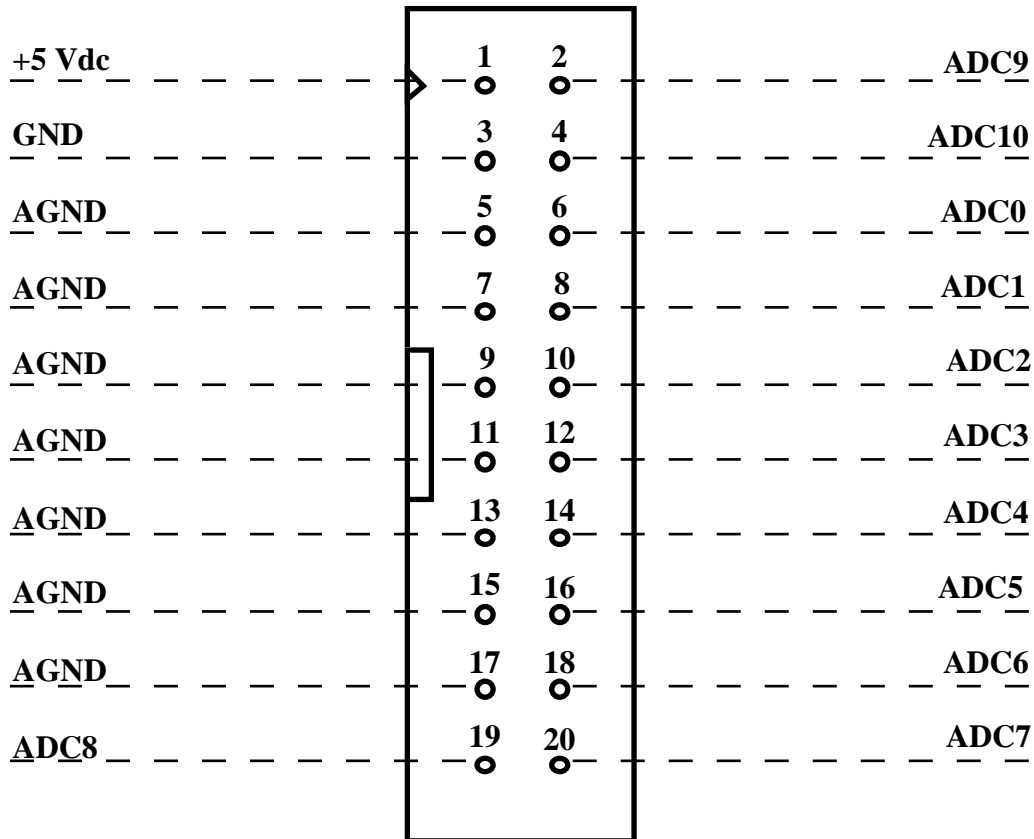


FIGURE 8: LEDs, CONNECTORS, DIP SWITCH, ETC. LOCATION

## CN6 - A/D CONVERTER INPUT CONNECTOR

CN6 is a 20 pins, male, vertical, low profile connector, 2.54 mm pitch. Through CN6 the 11 A/D converter section input signals interface to the external world.

This connector accepts voltage analog signals (0÷2.49 Vcc) or current analog signals (0÷20 mA) and follow the **A/D ABACO®** standard.



**FIGURE 9: CN6 - A/D CONVERTER INPUT CONNECTOR**

Signals description:

<b>ADCn</b>	=	I	-	A/D converter n-th channel analog input
<b>GND</b>	=		-	Digital ground signal
<b>AGND</b>	=		-	Analog ground signal
<b>+5 Vdc</b>	=	O	-	+5 Vcc signal

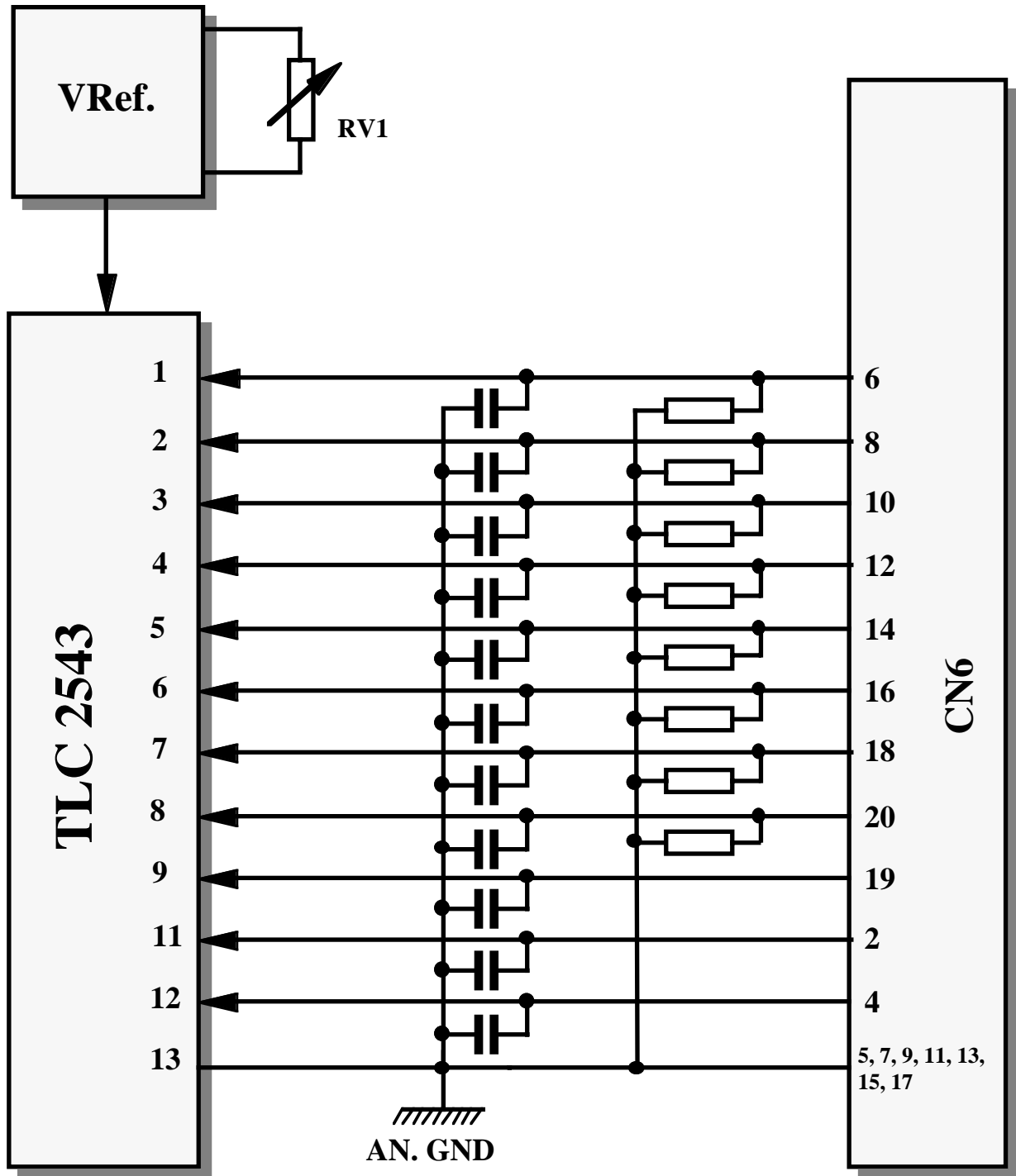


FIGURE 10: A/D CONVERTER INPUT BLOCK DIAGRAM

## CN3A - SERIAL LINE A CONNECTOR

CN3A is a 6 pins, female PLUG connector for serial communication.

Placing of the signal has been designed to reduce interference and electrical noise and to simplify connections with other systems, while the electric protocol follows the CCITT normative.

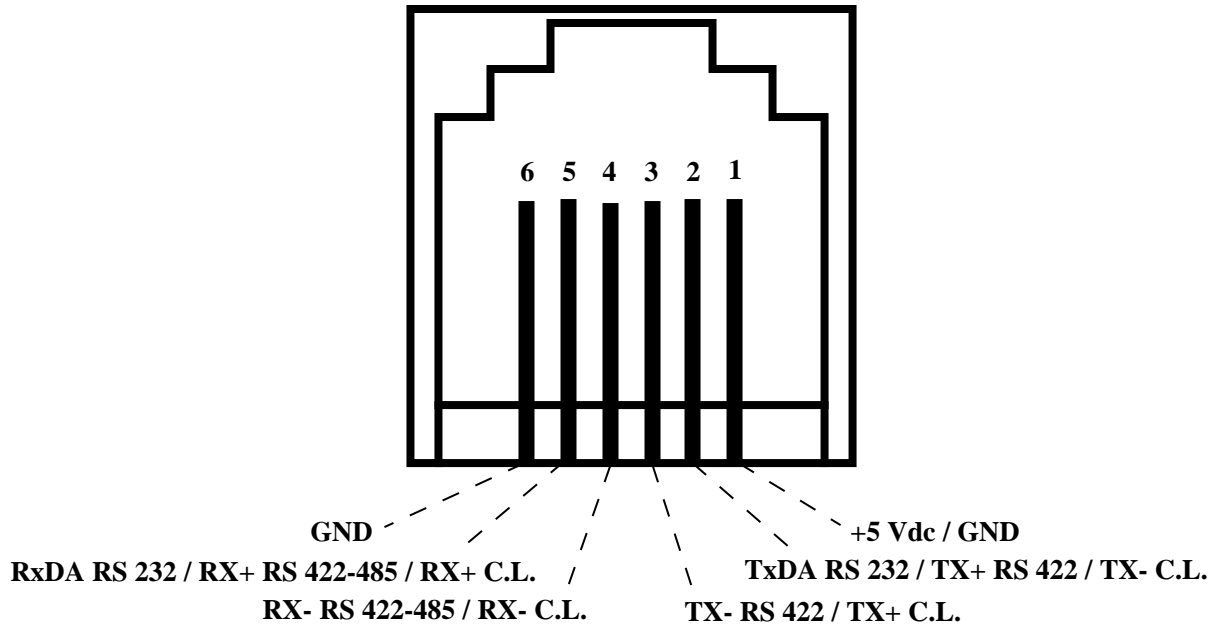


FIGURE 11: CN3A - SERIAL LINE A CONNECTOR

Legenda:

<b>RX- RS 422-485</b>	=	I	-	Receive Data Negative: negative signal for RS 422-485 serial differential receive
<b>RX+ RS 422-485</b>	=	I	-	Receive Data Positive: positive signal for RS 422-485 serial differential receive
<b>TX- RS 422</b>	=	O	-	Transmit Data Negative: negative signal for RS 422-485 serial differential transmit
<b>TX+ RS 422</b>	=	O	-	Transmit Data Positive: positive signal for RS 422-485 serial differential transmit
<b>RxD RS 232</b>	=	I	-	Receive Data: RS 232 Receive Data signal
<b>TxD RS 232</b>	=	O	-	Transmit Data: RS 232 Transmit Data signal
<b>RX- C.L.</b>	=	I	-	Receive Data Negative: negative signal for Current Loop serial differential receive
<b>RX+ C.L.</b>	=	I	-	Receive Data Positive: positive signal for Current Loop serial differential receive
<b>TX- C.L.</b>	=	O	-	Transmit Data Negative: negative signal for Current Loop serial differential transmit
<b>TX+ C.L.</b>	=	O	-	Transmit Data Positive: positive signal for Current Loop serial differential transmit
<b>+5 Vdc/GND</b>	=	I		+5 Vcc or ground signal
<b>GND</b>	=			Ground signal

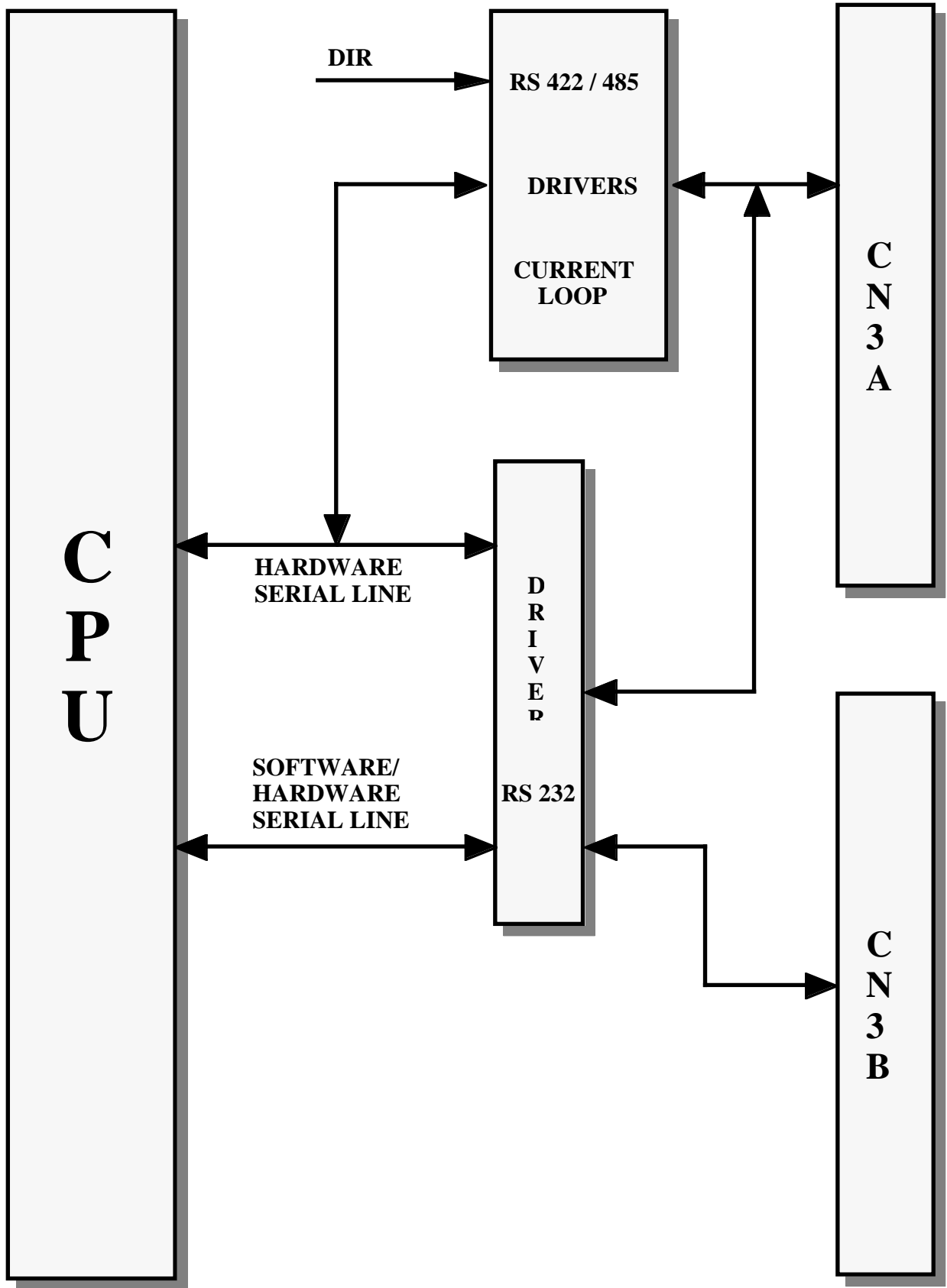


FIGURE 12: SERIAL COMMUNICATION DIAGRAM

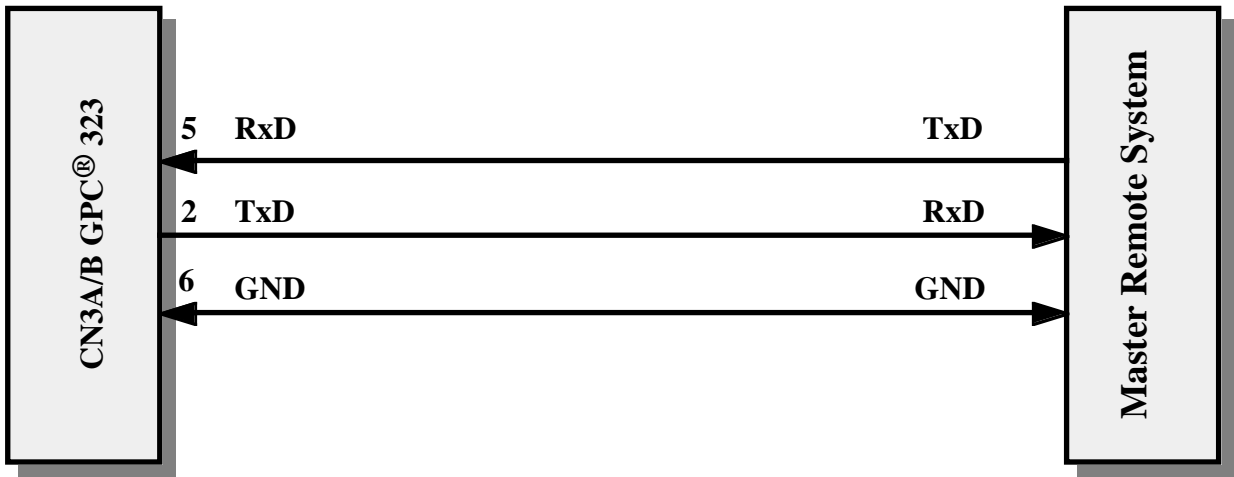


FIGURE 13: RS 232 PIN-OUT AND CONNECTION EXAMPLE

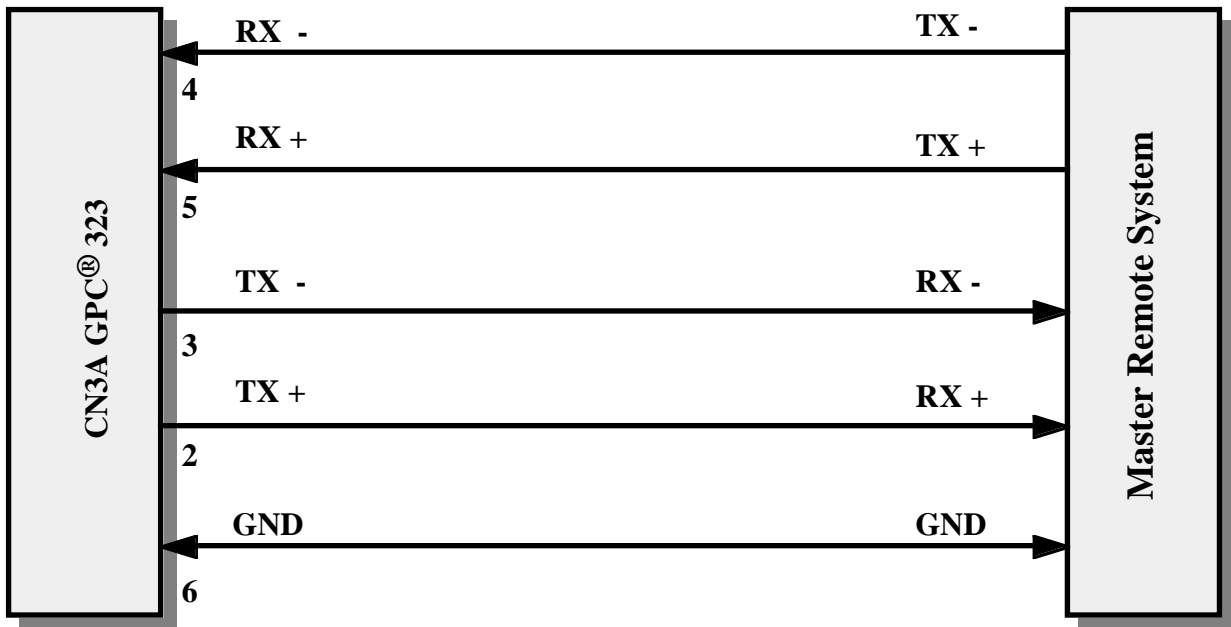


FIGURE 14: RS 422 PIN-OUT AND CONNECTION EXAMPLE

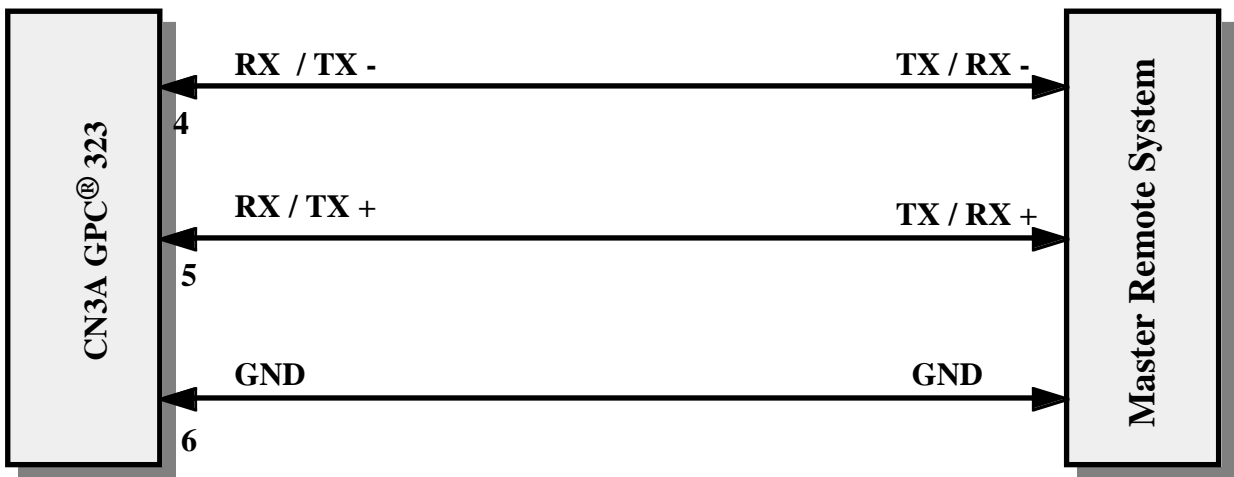


FIGURE 15: RS 485 PIN-OUT AND CONNECTION EXAMPLE

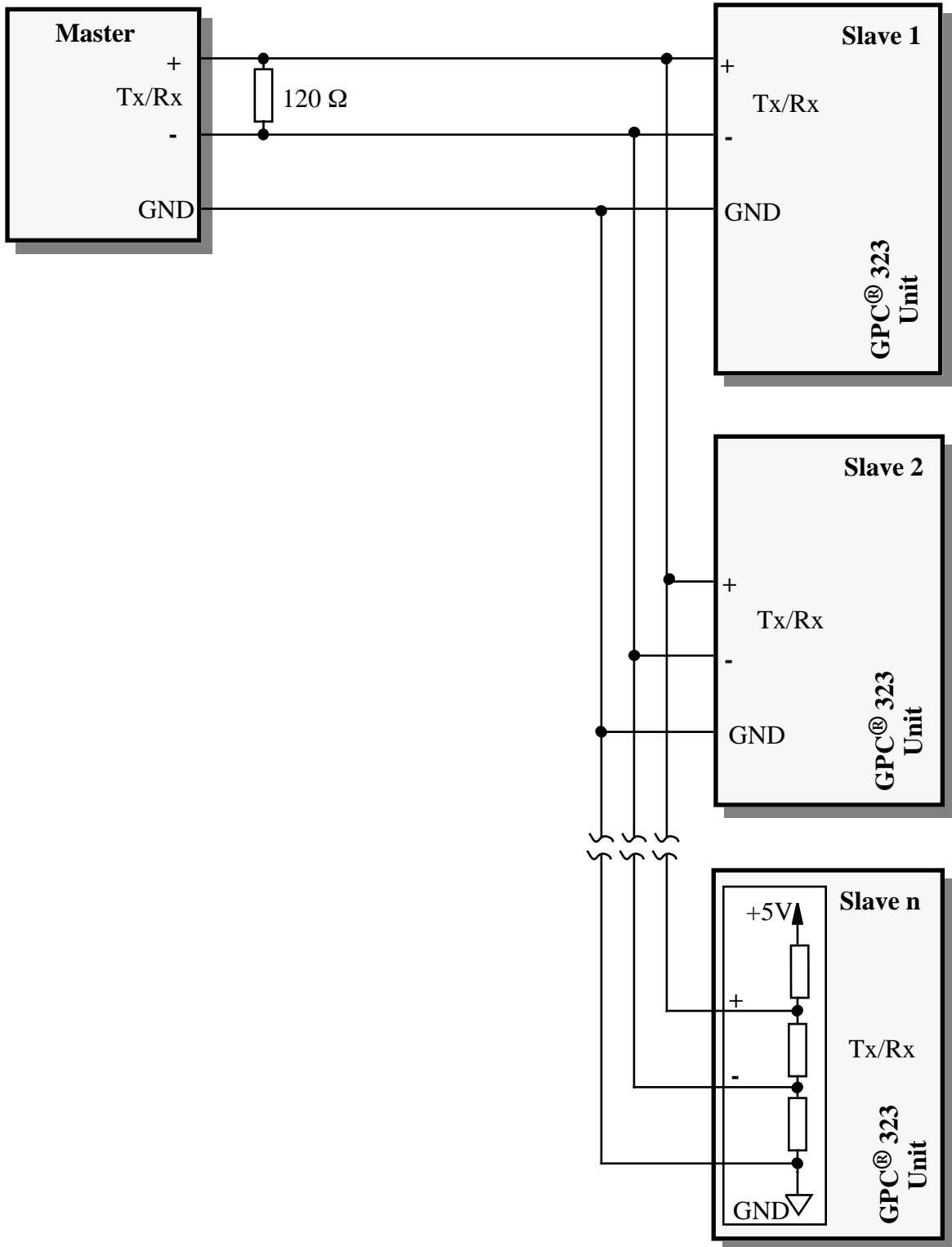


FIGURE 16: RS 485 NETWORK CONNECTION EXAMPLE

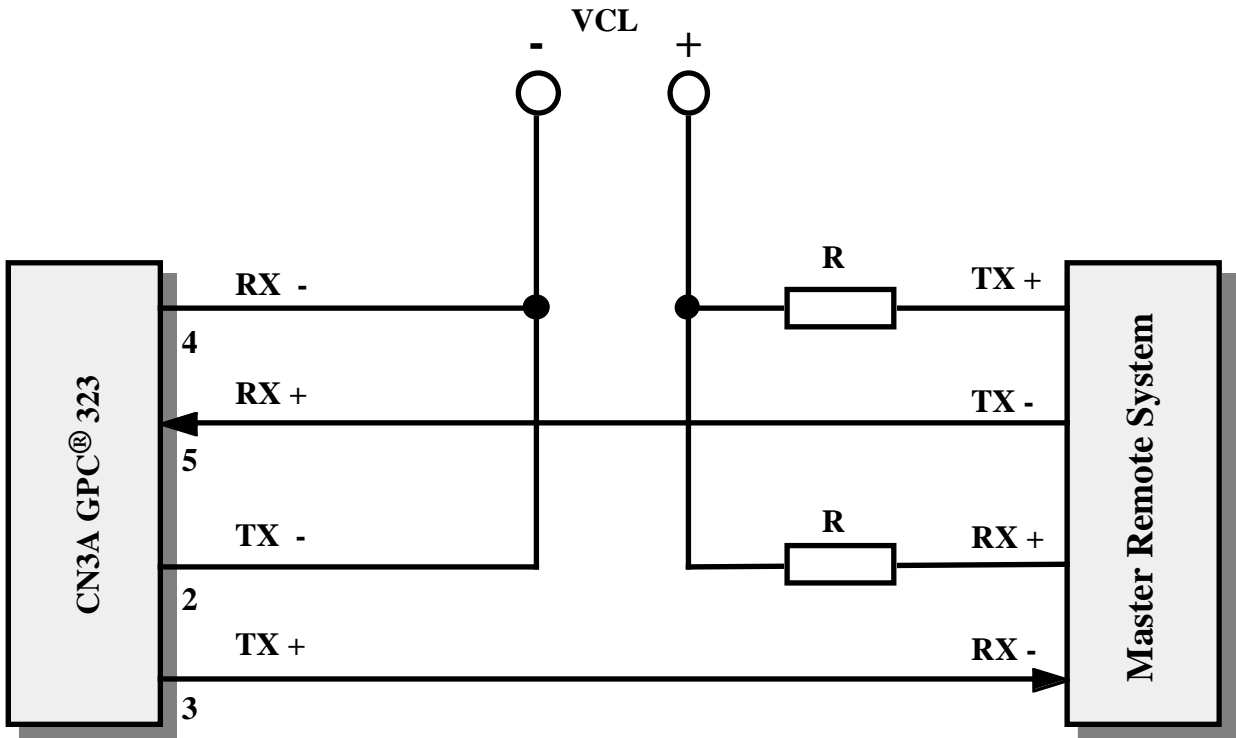


FIGURE 17: CURRENT LOOP PIN-OUT AND 4 WIRES CONNECTION EXAMPLE

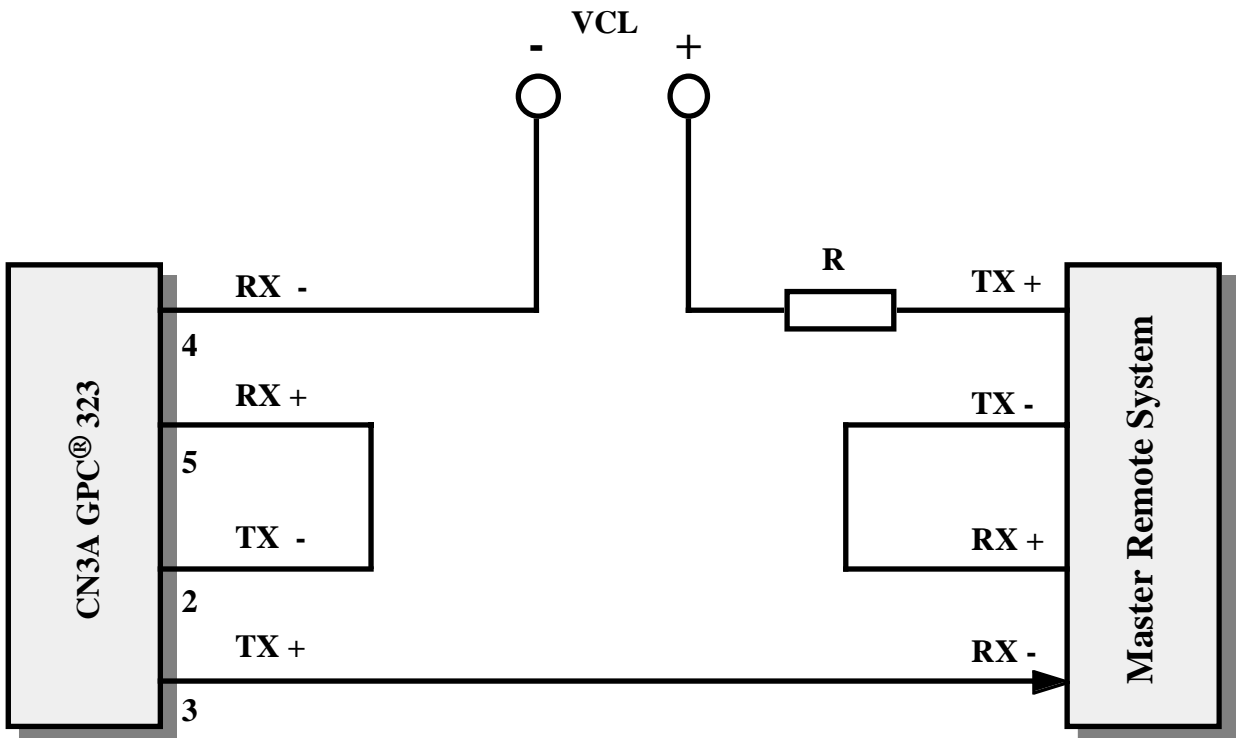


FIGURE 18: CURRENT LOOP PIN-OUT AND 2 WIRES CONNECTION EXAMPLE





## CN3B - SERIAL LINE B CONNECTOR

CN3B is a 6 pins, female PLUG connector for serial communication.

Placing of the signal has been designed to reduce interference and electrical noise and to simplify connections with other systems, while the electric protocol follows the CCITT normative.

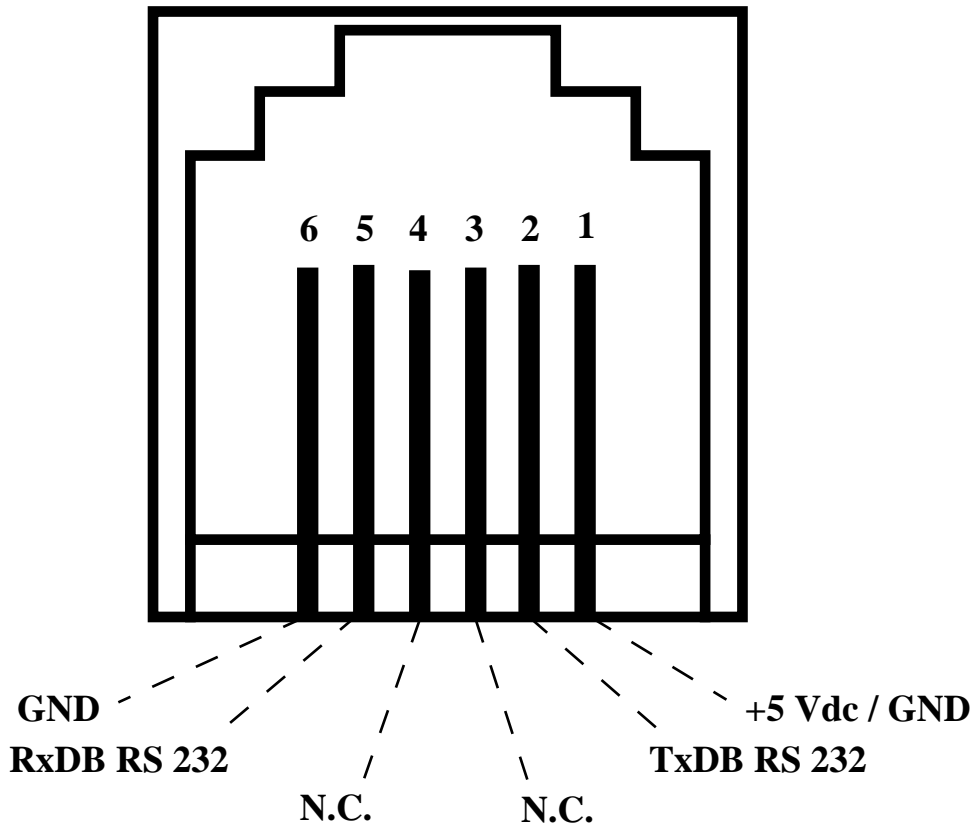


FIGURE 20: CN3B - SERIAL LINE B CONNECTOR

Signals description:

<b>RxDB RS 232</b>	=	I	-	Receive Data: RS 232 Receive Data signal
<b>TxDB RS 232</b>	=	O	-	Transmit Data: RS 232 Transmit Data signal
<b>+5 Vdc/GND</b>	=	I		+5 Vcc or ground signal
<b>GND</b>	=			Ground signal
<b>N.C.</b>	=		-	Not connected

## CN2 - EXTERNAL BACK UP BATTERY CONNECTOR

CN2 is a 2 pins, male, vertical, low profile connector, 2.54 mm pitch. Through CN2 the external back up battery that keeps on board RAM data integer and feeds the optional Real Time Clock also when power supply fails must be connected (for further informations please refer to the paragraph “BACK UP”).

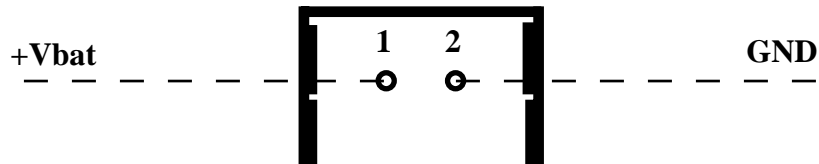


FIGURE 21: CN2 - EXTERNAL BACK UP BATTERY CONNECTOR

Signals description:

<b>+Vbat</b>	=	I	-	Positive terminal of external back up battery
<b>GND</b>	=	-	-	Negative terminal of external back up battery

## OPERATOR INTERFACES

Through CN7 (I/O Abaco® standard connector) GPC® 323 board can be connected to several grifo® cards featuring the same pin out. Especially remarkable is the possibility to connect directly modules as QTP 24P, KDL x24, KDF 224, etc. that may solve any operator interfacement problems. These modules are provided with the resources (alphanumeric display, matrix keycoard and LEDs) essential to manage an high level human-to-machine interfacement at a small distance to GPC® 323. To install one of these interfaces the User needs just a 20 pins flat cable, which transports both the signals and the interface power supply, while the software management can be easily performed through the procedures provided by any software packages suitable to GPC® 323. These procedures for most of the software packages are “software drivers” added to the programming language, that allow to use directly the “console management instructions” provided by the language itself. For further informations please refer to the chapter “EXTERNAL CARDS” and to the documentation of the software development tool being used.

## VISUAL FEEDBACK

GPC® 323 board is provided with four LEDs to signal status conditions, as described in the following table:

LED	COLOUR	FUNCTION
LD1	Red	It signals the presence of +5 Vcc power supply.
LD2	Red	It signals the external watchdog circuitry activity.
LD3	Green	Software managed timed activity LED (spot).
LD4	Green	Software managed activity LED.

**FIGURE 22: VISUAL FEEDBACK TABLE**

The main purpose of these LEDs is to give a visual indication of the board status, making easier the operations of system working verify. To easily locate these LEDs on the board, please refer to figure 8.

## I/O CONNECTION

To prevent possible connecting problems between GPC® 323 and the external systems, the user has to read carefully the information of the previous paragraphs and he must follow these instructions:

- For RS 232, RS 422, Current Loop or RS 485 communication signals the User must follow the standard rules of these protocols.
- For all TTL signals the user must follow the rules of this electric standard. The connected digital signal must be always referred to card digital ground (GND). For TTL signals, the 0 Vdc level corresponds to logic state "0", while 5Vdc level corresponds to logic state "1".
- The analog inputs (A/D section) must be connected to low impedance signals in the following ranges: 0÷2,490 V or 0÷5,000 V according to selected voltage reference (Vref). Remember that the four analog inputs available on CN5 are provided of filter capacitors that ensure an higher stability of the acquired signals, but reduce at the same time the bandwidth frequency. For further informations please refer to the paragraph "TYPE OF ANALOG INPUT SELECTION".

## RESET KEY

P1 reset key of the GPC® 323 board allows the user to reset the board and restarting it in a general clearing condition.

The main purpose of this key is to come out of infinite loop conditions, useful especially during debug and develop phases, or to ensure a particular initial status. Please see figure 8 for an easy localization of this contact.

## TEST POINT

The board is provided with a test point called TP1, that allows to read, through a galvanically isolated multimeter, the reference voltage which is calibrated in laboratory and whose value is  $V_{ref}=2.4900$  V. TP1 is made of two contacts:

pin 1	->	Vref
pin 2	->	GND

To easily locate the test point contacts please refer to figure 8, while for further informations about Vref signal please refer to the paragraph “TRIMMER AND CALIBRATION”.

## DIP SWITCH

**GPC® 323** board is provided with one 8 pins dip switch (DSW1), typically used for system configuration, five of its pins are software readable by the User (DIP 1÷4, 8), two pins are used for memory configuration selection (DIP 5, 6), one pin is not used (DIP 7). The most frequent applications are: working condition selection or on board firmware parameters setting. The combination present on dip switch is in complemented logic (0 -> dip On and 1 -> dip OFF) and can be read performing a read operation at the address decided by the on board control logic for the dip switch. For further informations please refer to the paragraphs “I/O MAPPING” and “MEMORY MAPPING”, while to easily locate the dip switch please refer to figure 8.

## POWER SUPPLY VOLTAGES

**GPC® 323** board is provided with an efficient circuitry that solves in an efficient and comfortable way the problem of power supply in any employ condition. Here follows the list of the possible configurations for power supply section:

- No power supply section:

The board must be supplied by a +5 Vdc voltage provided directly on the specific pins of CN1, CN3A or CN3B.

- Linear power supply section:

The board must be supplied by a 6÷12 Vac alternate voltage, or the corresponding continuous voltage, that must be provided to pins 1 and 2 of CN4. This is the high efficiency linear supply section.

It is also available a normal efficiency linear supply section, which requires 8÷12 Vac, or the corresponding continuous voltage, as input supply.

- Switching power supply section:

The board must be supplied by a 15÷24 Vac alternate voltage, or the corresponding continuous voltage, that must be provided to pin 1 and 2 of CN4.

Regardless the type of supply section chosen, the **GPC® 323** board is always provided with an efficient protection circuitry that protects the board against voltage peaks or noise. Please remark that the desired supply section must be explicitly specified in the order; in fact the choice implies a different hardware configuration that must be performed by the grifo® technical personnel.

## INTERRUPTS MANAGEMENT

One of the most important **GPC® 323** features is the powerful interrupts management. Here is a short description of how the board's hardware interrupt signals can be managed; a more complete description of the hardware interrupts can be found in the microprocessor data sheets or in appendixes of this manual.

**/INT ABACO® I/O BUS** -> generates an interrupt on CPU pin 14 (/INT0)

**/NMI ABACO® I/O BUS** -> generates an interrupt on CPU pin 2 (T2)

This connections allow to generate an interrupt when the /NMI CPU signals is activated, through an opportune programming of microprocessor inside timer 2 and is remarkable the possibility to use this feature with **ZBT xxx** and **ZBR xxx** board. In fact optocoupled input signals of these two boards can generate interrupts or simply be counted.

There are also microprocessor inside resources that can generate interrupts.

## TYPE OF ANALOG INPUT SELECTION

**GPC® 323** board can accept analog voltage and/or current inputs, as described in the previous paragraphs and chapters. The input type selection can be made only for 8 out of 11 input analog channels during the order phase and is performed mounting a specific voltage-current conversion module made by precision resistors. In detail:

R37	->	channel 0
R36	->	channel 1
R35	->	channel 2
R34	->	channel 3
R33	->	channel 4
R32	->	channel 5
R31	->	channel 6
R30	->	channel 7

Should the voltage-current conversion module not to be mounted (default case) the corresponding channel accepts a voltage input signal in the range 0÷2.49 V; otherwise a current input signal is accepted.

The value of the above mentioned resistors is obtained by the following spread;

$$R = 2.49 \text{ V} / I_{\text{max}}$$

Usually the voltage-current conversion modules are made using 124  $\Omega$  precision resistors, corresponding to 4÷20 mA or 0÷20 mA.

To easily locate the voltage-current conversion module please refer to figure 8.

## TRIMMERS AND CALIBRATION

On **GPC® 323** is available a trimmer, named **RV1**, that calibrates the  $V_{ref}$  voltage of the A/D converter section. The **GPC® 323** is subjected to a careful test that verifies and calibrates all the card sections. To easily locate the trimmer, please refer to figure 8. The calibration is executed in laboratory, with a controlled  $+20\text{ C}^\circ$  room temperature, following these steps:

- The A/D voltage reference ( $V_{ref}$ ) is calibrated through RV1 trimmer, by using a 5 digits precision multimeter, to a value of  $+2,4900\text{ Vdc}$  or  $+5,0000\text{ Vdc}$ .
- The correspondance between the analog input signal and the combination read from A/D is verified. This check is performed with a reference signal connected to A/D inputs and testing that the A/D combination and the theoretic combination differ at maximum of the A/D section errors sum.
- The trimmer is blocked with paint.

The analog interfaces use high precision components that are selected during mounting phase to avoid complicate and long calibration procedures. After the calibration, the on board trimmer is blocked with paint to maintain calibration also in presence of mechanic stresses (vibrations, movings, delivery, etc.).

The user must not modify the card calibration, but if thermic drifts, time drifts and so on, make necessary a new calibration, the user must strictly follow the previous described procedure.

## JUMPERS

On **GPC® 323** there are 17 jumpers for card configuration, 8 of them are solder jumpers. Thanks to these jumpers, the user can define for example the memory type and size, the peripheral devices functionality and so on. Below there is the jumpers list, location and function.

JUMPER	N. PINS	USE
J1	2	Connects to + 5 Vcc CN1 pin 26.
J2	3	Selects memory device type for IC 3.
J3	3	Selects memory device type and size for IC 3.
J4	3	Selects memory device type and size for IC 3.
J5	3	Selects memory device size for IC 4.
J6	2	Configures back up circuitry for RAM and RTC.
J7	6	Selects direction and activation modality for RS 422-485 serial line.
J8	2	Connects watchdog external circuitry.
J18	3	Selects the connection type for CPU pin 14 (/INT0).
JS1, JS2	2	Connect the termination and forcing circuitry for RS 422-485 serial communication line.
JS3	3	Selects the connection type for CN3A pin 1.
JS4	3	Selects the connection type for CN3B pin 1.
JS5	2	Selects internal or external ROM code area.
JS7, JS8	2	Connect RS 232 driver of serial A to CN3A.
JS9	3	Selects the communication type for serial A reception line.

**FIGURE 23: JUMPERS SUMMARIZING TABLE**

The following tables describe all the right connections of **GPC® 323** jumpers with their relative functions. To recognize these valid connections, please refer to the board printed diagram (serigraph) or to figure 2 of this manual, where the pins numeration is listed; for recognizing jumpers location, please refer to figures 24 and 26. The "\*" used in the following tables, denotes the default connection, or on the other hand the connection set up at the end of testing phase, that is the configuration the user receives.



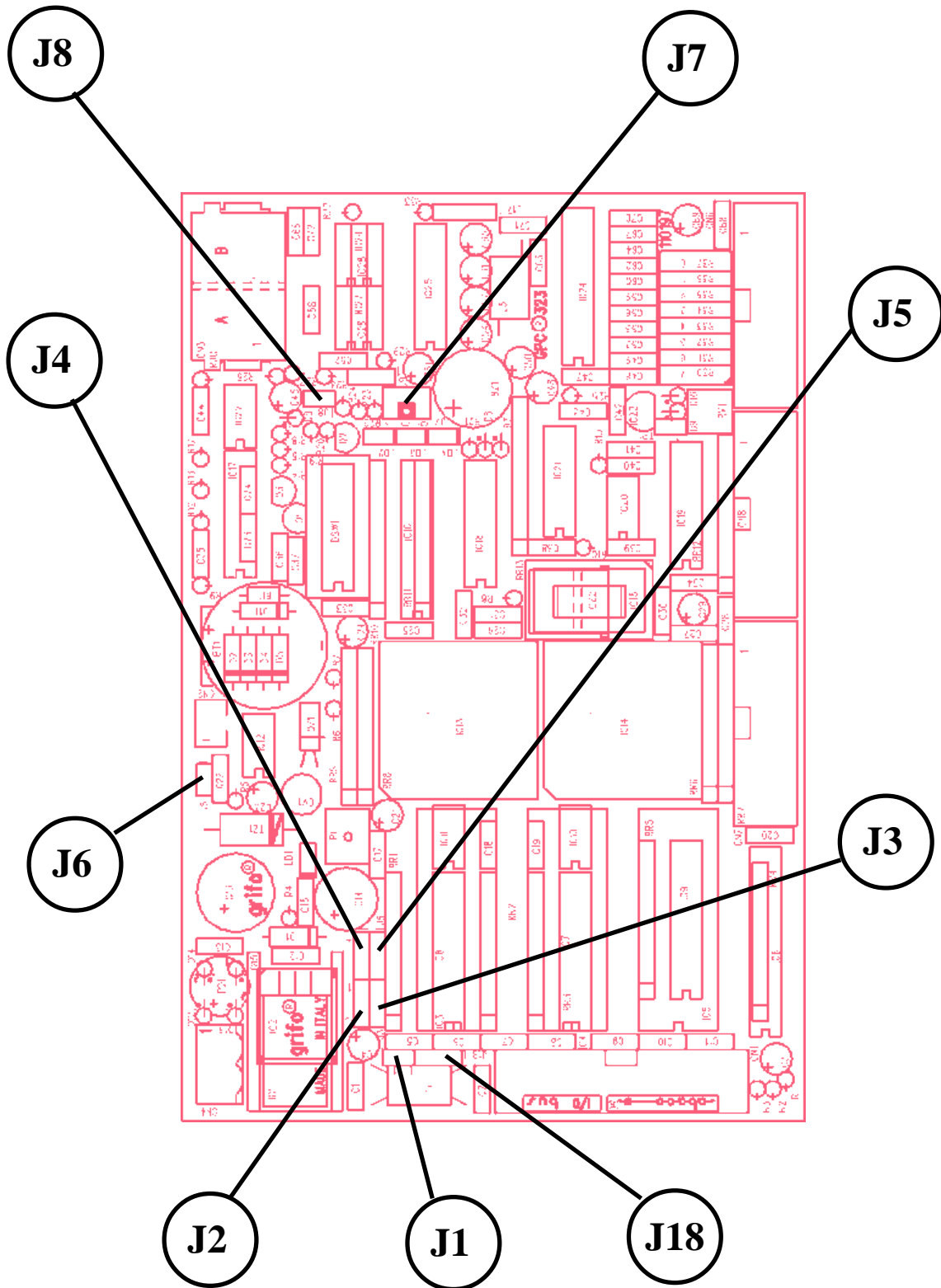


FIGURE 24: COMPONENT SIDE JUMPERS LOCATION

**2 PINS JUMPERS**

JUMPER	CONNECTION	USE	DEF.
J1	not conncted	Does not connect CN1 pin 26 to +5 Vcc.	
	connected	Connects CN1 pin 26 to +5 Vcc.	*
J6	not conncted	IC 4 RAM backed only by an eventual external battery. IC12 RAM +RTC backed only by on board battery BT1.	*
	connected	IC 4 RAM backed by an eventual external battery and the eventual on board battery BT1. IC12 RAM +RTC backed by on board battery BT1 and an eventual external battery.	
J8	not conncted	Does not connect external watchdog circuitry to reset circuitry.	*
	connected	Connects external watchdog circuitry to reset circuitry.	
JS1, JS2	not conncted	Do not connect the termination and forcing circuitry RS 422-485 serial A.	*
	connected	Connect the termination and forcing circuitry RS 422-485 serial A.	
JS5	not conncted	Enables microprocessor inside ROM code.	
	connected	Enables external ROM = on board EPROM	*
JS7, JS8	not conncted	Do not connect RS 232 driver of serial A to CN3A.	
	connected	Connect RS 232 driver of serial A to CN3A.	*

**FIGURE 25: 2 PINS JUMPERS TABLE**

The "\*" used in the following tables, denotes the default connection, or on the other hand the connection set up at the end of testing phase, that is the configuration the user receives.

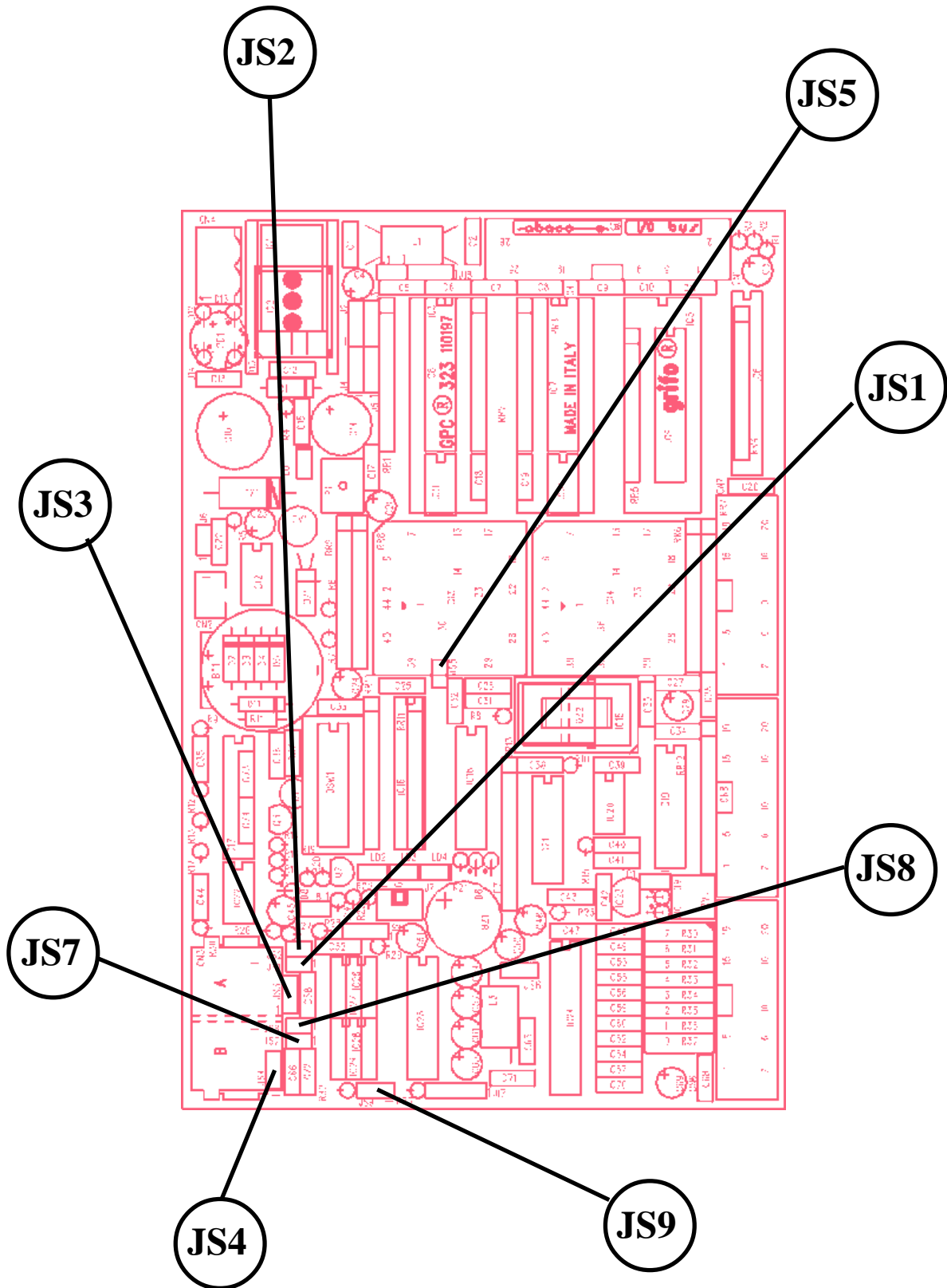


FIGURE 26: SOLDER SIDE JUMPERS LOCATION

**3 PINS JUMPERS**

JUMPER	CONNECTION	USE	DEF.
J2	position 1-2	Sets IC3 to accept EPROM.	
	position 2-3	Sets IC3 to accept RAM/EEPROM.	*
J3	position 1-2	Sets IC3 to accept EPROM	
	position 2-3	Sets IC3 to accept 32K RAM/EEPROM.	*
	not connected	Sets IC3 to accept 8K RAM/EEPROM.	
J4	position 1-2	Sets IC3 to accept 32K RAM/EEPROM/EPROM.	*
	position 2-3	Sets IC3 to accept 8K RAM/EEPROM.	
	not connected	Sets IC3 to accept 8K EPROM.	
J5	position 1-2	Sets IC4 to accept 32K RAM/EEPROM.	*
	position 2-3	Sets IC4 to accept 8K RAM/EEPROM.	
J18	position 1-2	Connects CPU pin 14 (/INT0) to CN1 pin 23 (/INT).	
	position 2-3	Connects CPU pin 14 (/INT0) to IC25 pin 12 (serial B reception signal).	*
JS3	position 1-2	Connects CN3A pin 1 to GND.	*
	posizione 2-3	Connects CN3A pin 1 to +5 Vdc.	
JS4	position 1-2	Connects CN3B pin 1 to GND.	*
	position 2-3	Connects CN3B pin 1 to +5 Vdc.	
JS9	position 1-2	Connects serial A reception signal to RS 232 driver.	*
	position 2-3	Connects serial A reception signal to Current Loop or RS 422-485 driver.	

**FIGURE 27: 3 PINS JUMPERS TABLE**

The "\*" used in the following tables, denotes the default connection, or on the other hand the connection set up at the end of testing phase, that is the configuration the user receives.

## 6 PINS JUMPERS

JUMPER	CONNECTION	USE	DEF.
J7	position 1-2 and 3-4	Selects RS 485 serial communication (2 wires half duplex)	*
	position 2-3 and 4-5	Selects RS 422-485 serial communication (4 wires full duplex or half duplex)	
	position 1-6	Connects the il RTC interrupt signal to CPU pin 15 (P3.3 - /INT1).	

**FIGURE 28: 6 PINS JUMPERS TABLE**

The "\*" used in the following tables, denotes the default connection, or on the other hand the connection set up at the end of testing phase, that is the configuration the user receives.

### NOTE

Here follow some indications about how to configure properly the board.

### **BACK UP**

Please remark that lithium battery BT1 is optional and is provided only with IC12 RAM+RTC:

- If the User needs to back up IC14 RAM then he/she must connect an external battery to CN2. Through jumper J6 it is also possible to back up the optional IC12 RAM+RTC module, saving the on board battery BT1.
- If the board is provided with on board battery BT1, through jumper J6 the User can also back up IC4 RAM, but only for short time periods, like, for example, to perform the replacement of the external battery.

No other combination has been considered therefore no other combination can be used. To choose the external battery please follow the indications at the paragraph "ELECTRIC FEATURES".

### **SERIAL COMMUNICATION TYPE SELECTION**

The serial line A is available on connector CN3A and can be buffered in RS 232, RS 422, RS 485 or Current Loop electric standard. By hardware can be selected which one of these electric standard is used, through jumpers connection. By software the serial line can be programmed to operate with the desired physical communication protocol acting on the CPU internal registers. In the following paragraphs there are all the informations on serial communication configurations; please note that jumpers which are not mentioned below do not affect the serial communication whatever their configuration is.

#### - RS 232 SERIAL LINE

MAX 232 serial driver must be installed on IC25, while on IC26, IC27, IC28, IC29 no driver must be installed. Jumper JS9 must be connected in position 1-2, jumpers JS7 and JS8 must be connected.

#### - CURRENT LOOP SERIAL LINE

HCPL 4100 must be installed on IC26, HCPL4200 must be installed on IC28, while on IC17 and IC29 no driver must be installed. Jumper JS9 must be connected in position 2-3, jumpers JS7 and JS8 must be not connected..

#### - RS 485 SERIAL LINE

SN75176 serial driver must be installed on IC27, while no driver must be installed on IC26 and IC28. Jumper J7 must be connected in position 1-2 and 3-4, jumper JS9 must be connected in position 2-3, jumpers JS7 and JS8 must be not connected. CN3A pins 4 and 5 are the signals employed to receive and transmit according to the status of DIR signal (0=level low=reception, 1=level high=transmission), which is software manageable

This kind of serial communication can be used for multi-point connections, in addition it is possible to listen to own transmission, so the user is allowed to verify the success of transmission. In fact, any conflict on the line can be recognized by testing the received character after each transmission.

#### - RS 422 SERIAL LINE

SN75176 serial drivers must be installed on IC27 and IC29 while no driver must be installed on IC26 and IC28. Jumper J7 must be connected in position 2-3 and 4-5, jumper JS9 must be connected in position 2-3, jumpers JS7 and JS8 must be not connected.

DIR signal can be kept always high (active transmitter) for point-to-point connections, while for multi-point connections the transmitter must be activated only before the transmission (DIR =1=high=transmitter activated).

If using the RS 422-485 serial line, it is possible to connect the terminating and forcing circuit on the line by using JS1 and JS2. This circuit must be always connected in case of point-to-point connections, while in case of multi-point connections it must be connected only in the farthest boards, that is on the edges of the communication line.

To easily locate jumpers and serial drivers please refer to appendix A.

**GPC® 323** board is provided with a second serial line (B) that can be buffered only as RS 232. Serial line B is software managed through two microcontroller I/O signals, so communication parameters can be set programming the management firmware (for further information please refer to the software tool manual). Please remark that Rx/B reception signal can be connected to CPU /INT0 signal connecting jumper J18 in position 2-3 allowing to manage the reception via interrupt.

## MEMORY SELECTION

On **GPC® 323** can be mounted 98K and 256 bytes of memory divided in several configurations, as described in the following table:

IC	DEVICE	SIZE	JUMPERS CONNECTION
3	RAM/EEPROM	8K Bytes	J2 in 2-3; J3 not connected; J4 in 2-3
	RAM/EEPROM	32K Bytes	J2 in 2-3; J3 in 2-3; J4 in 1-2
	EPROM	8K Bytes	J2 in 1-2; J3 in 1-2; J4 not connected
	EPROM	32K Bytes	J2 in 1-2; J3 in 1-2; J4 in 1-2
4	RAM/EEPROM	8K Bytes	J5 in 2-3
	RAM/EEPROM	32K Bytes	J5 in 1-2
5	EPROM	32K Bytes	
10	EEPROM	512÷2048 Bytes	
12	RAM+RTC	256 Bytes	

**FIGURE 29: MEMORY SELECTION TABLE**

The sockets described above follow the JEDEC standard, so the mounted memory devices must have JEDEC pin outs; exceptions are the serial EEPROM on IC10 and the serial RAM+RTC on IC12 devices that must be specified at the moment of the order and can be mounted only by **grifo®** technician. For further information about the memory devices please refer to the manufacturer documentation. We would want to remark that in case the IC12 component is mounted, the maximum size of IC10 is 1024 bytes.

RAM modules on IC12 and IC13 can be backed on request.

## SOFTWARE

A wide selection of software development tools can be obtained, allowing use of the module as a system for its own development, both in assembler and in other high level languages; in this way the User can easily develop all the requested application programs in a very short time. Generally all software packages available for the mounted microprocessor, or for the 51 family, can be used. For example:

**MDP:** monitor debugger program able to load and debug each HEX Intel files for 51 microprocessor family. It is provided of the standard commands available on in circuit emulator and requires only an external P.C. connected through a serial line.

**FORTH:** complete software development tools to program the card with FORTH high level language. It needs a P.C. for User interface and it is really interesting for its fast execution and small size, of the generated code.

**BASIC 323:** complete development tools for BASIC (interpreted BASIC language for industrial application). It needs a P.C. for console and program saving operations, while the debug, test and program operations are performed on the card. Special instructions which manage the on board peripheral devices have been added.

**BXC51:** cross compiler for source files written in MCS BASIC 552. It allows a considerable speed increment of the starting MCS BASIC program and it is completely executed on external P.C.

**OS552:** powerful macro cross assembler composed by communication program, editor, macro assembler, symbolic linker and a source remote debugger..

**MICRO/ASM-51:** macro cross assembler available for MS-DOS operating system in absolute and relocatable version. In this relocatable version is supplied with a linker and a library manager.

**MICRO/C-51:** integer cross compiler for source files in standard ANSI C. It produces a source assembly file compatible with MICRO/ASM 51 or with Intel macro relocatable assembler MCS 51.

**MICRO/SLD-51:** source level debugger and simulator. It is executed on P.C. without any additional hardware and it allows loading of HEX and SYMBOLIC files, breakpoint setting, instruction execution in trace mode, registers and memory dump, etc.

**HI-TECH C:** cross compiler for C source program. It is a powerful software tool that includes editor, C compiler, assembler, optimizer, linker, library, and remote symbolic debugger, in one easy to use integrated development environment.

**XPAS51:** cross compiler for PASCAL source program , executable on P.C. with MS-DOS operating system.

**RSD 323:** Powerful structure including a Remote Symbolic Debugger and a cross assembler. It needs a P.C. for console and program saving operations, while the debug, test and program operations are performed on the card. The user interface is developed and capable to show all the microprocessor status informations.



## HARDWARE

### INTRODUCTION

In this chapter are reported all information about card use, related to hardware features of **GPC® 323**. For example the registers addresses, the memory allocation and peripheral devices software management are described below.

### ADDRESSES

The card devices addresses are managed from a control logic, realized with programmable logic. This control logic allocates memory and peripheral devices with very low power consumption, in two separate manners. The acceptable microprocessors address 64K bytes of code memory and 64K bytes of data memory and the control logic provides on board memory and peripheral devices allocation

Inside these addresses space. Control logic sets size, type and addresses of memory device through jumpers J2, J3, J4 and J5 plus two dips of DSW1, while it sets I/O addresses always in its reserved memory area to avoid conflicts. Summarizing the control logic allocates:

- Up to 32K bytes of EPROM on IC 1
- Up to 32K bytes of RAM, EEPROM on IC 4
- Up to 32K bytes of RAM, EEPROM, EPROM on IC 3
- PPI 82C55
- **Abaco® I/O BUS**
- DSW1 dip switch
- Watchdog circuitry
- Buzzer
- Activity LED

The addresses of all these devices are described in the following two paragraphs and can't be set with different value.

Other devices such EEPROM on IC10 and RAM+RTC on IC12, A/D conversion section and DIR signal are always managed by the control logic but don't occupy room in the addressing space because they use a synchronous serial communication based on the CPU I/O lines.

## I/O ADDRESSES

I/O addresses are located in the last 128 bytes of the 64K bytes microprocessor area code, to avoid conflict problems. Next table shows addresses, meanings and direction of peripheral device registers (only the external ones to microprocessor):

DEVICE	REG.	ADDRESS	R/W	MEANING
<b>Abaco® I/O BUS</b>	I/OBUS	FF80H÷FFF7H	R/W	ABACO® I/O BUS addresses
<b>Spot LED</b>	SPOT	FFF8H	W	LD3 spot LED register
<b>Activity LED and buzzer</b>	LD4BZ	FFF9H	W	LD4 Activity LED and buzzer register
<b>Watchdog</b>	WDOG	FFF8H	R	Watchdog retrigger register
<b>Dip switch</b>	DSW1	FFF9H	R	DSW1 (dip 1, 2, 3, 4, 8) data register
<b>PPI 82C55</b>	PDA	FFFCH	R/W	Port A data register
	PDB	FFFDH	R/W	Port B data register
	PDC	FFFEH	R/W	Port C data register
	CNT	FFFFH	R/W	Control register

**FIGURE 30: I/O ADDRESSES TABLE**

For further information about register meanings, please refers to next paragraph called "PERIPHERAL DEVICES SOFTWARE DESCRIPTION".

## MEMORY ADDRESSES

On the **GPC® 323** three different memory configurations can be selected. The configuration must be selected both according to used software tools and User requests and/or application features. Here follows a schematization of memory disposition and the indication about how to configure dip 5 and dip 6 of DSW1 to perform this selection.

Memory type and size selection is performed through a set of comfortable jumpers as described in figure 28.

MEMORY CONFIGURATION 1

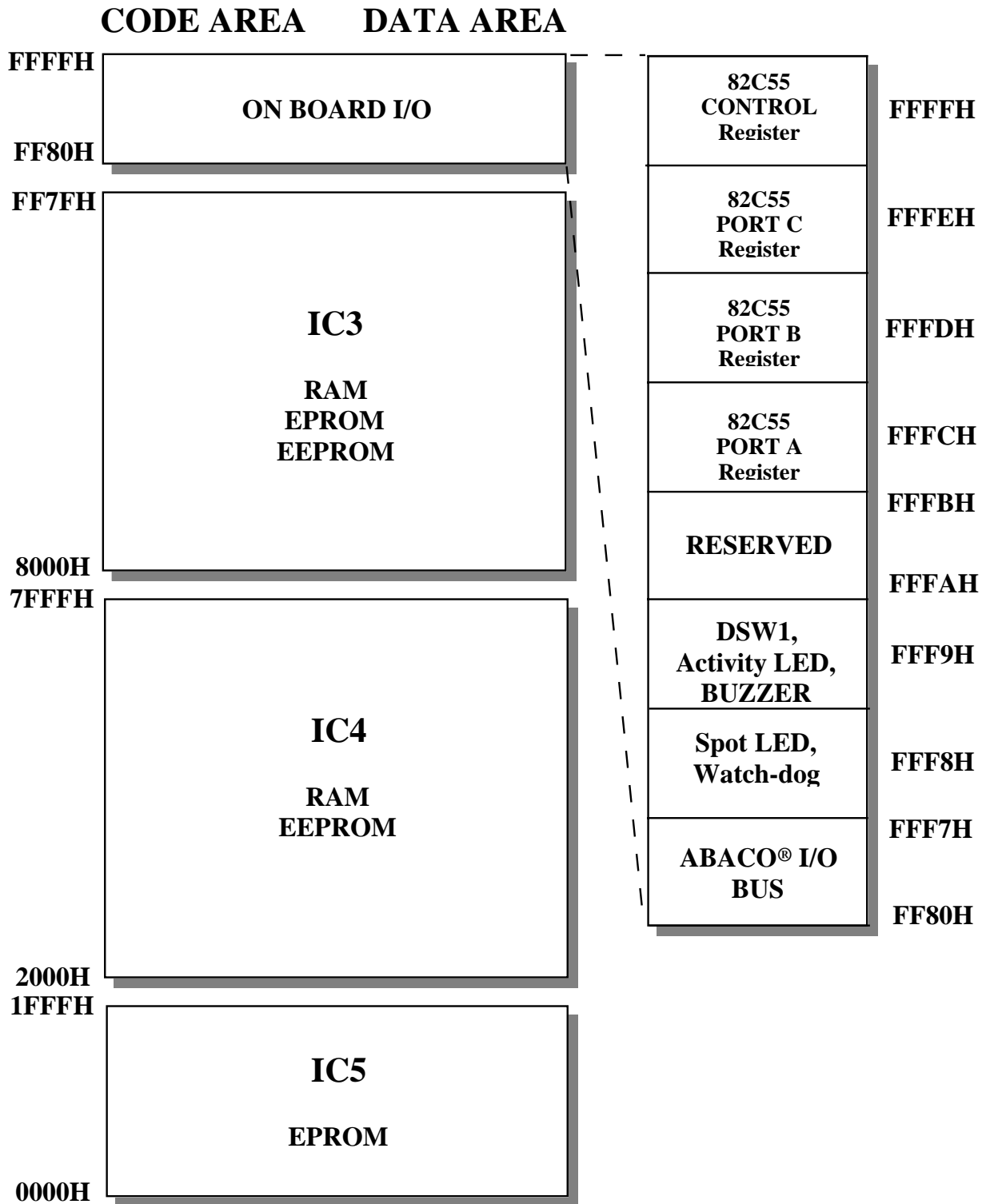
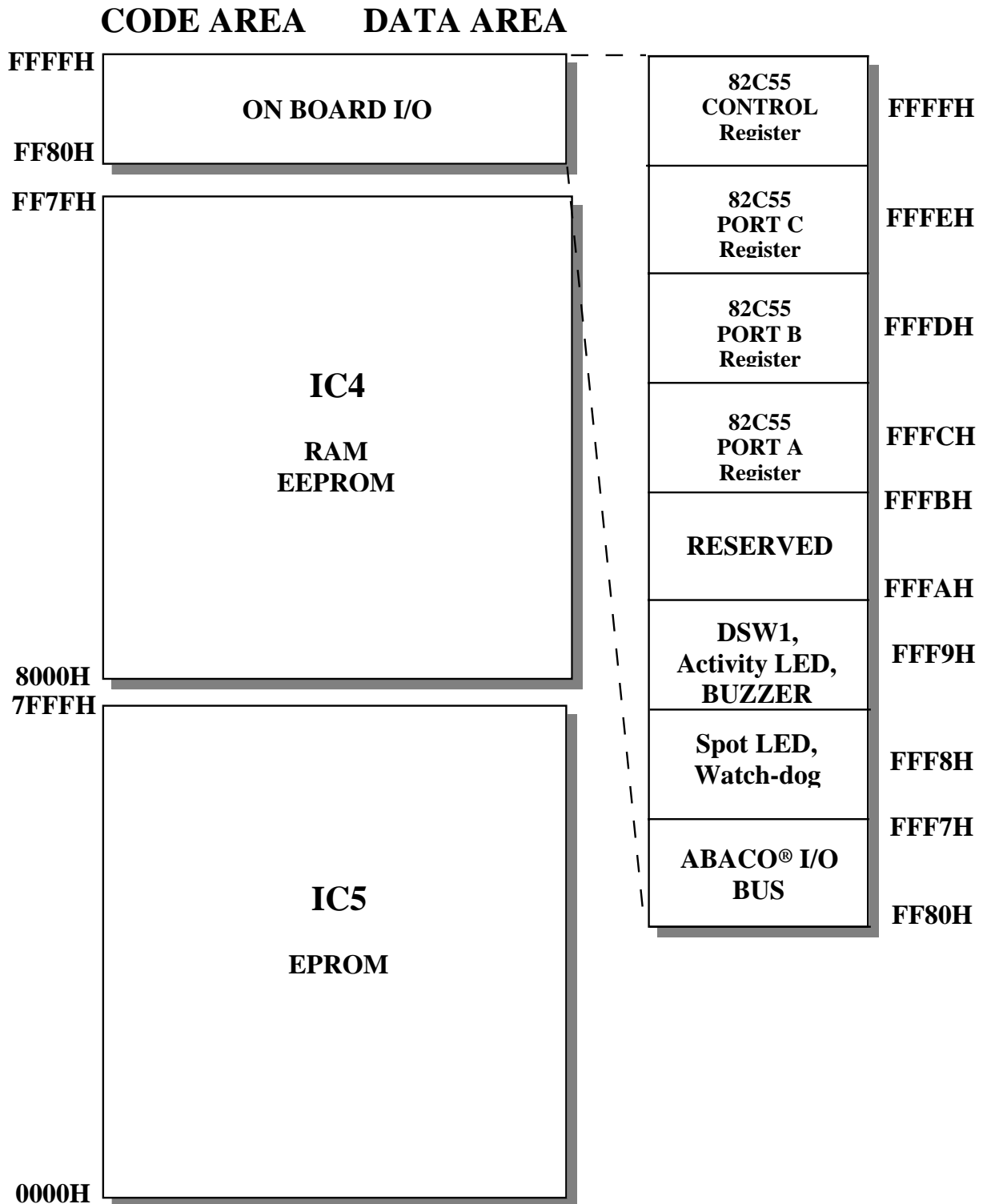


FIGURE 31: MEMORY CONFIGURATION 1 (ASM)

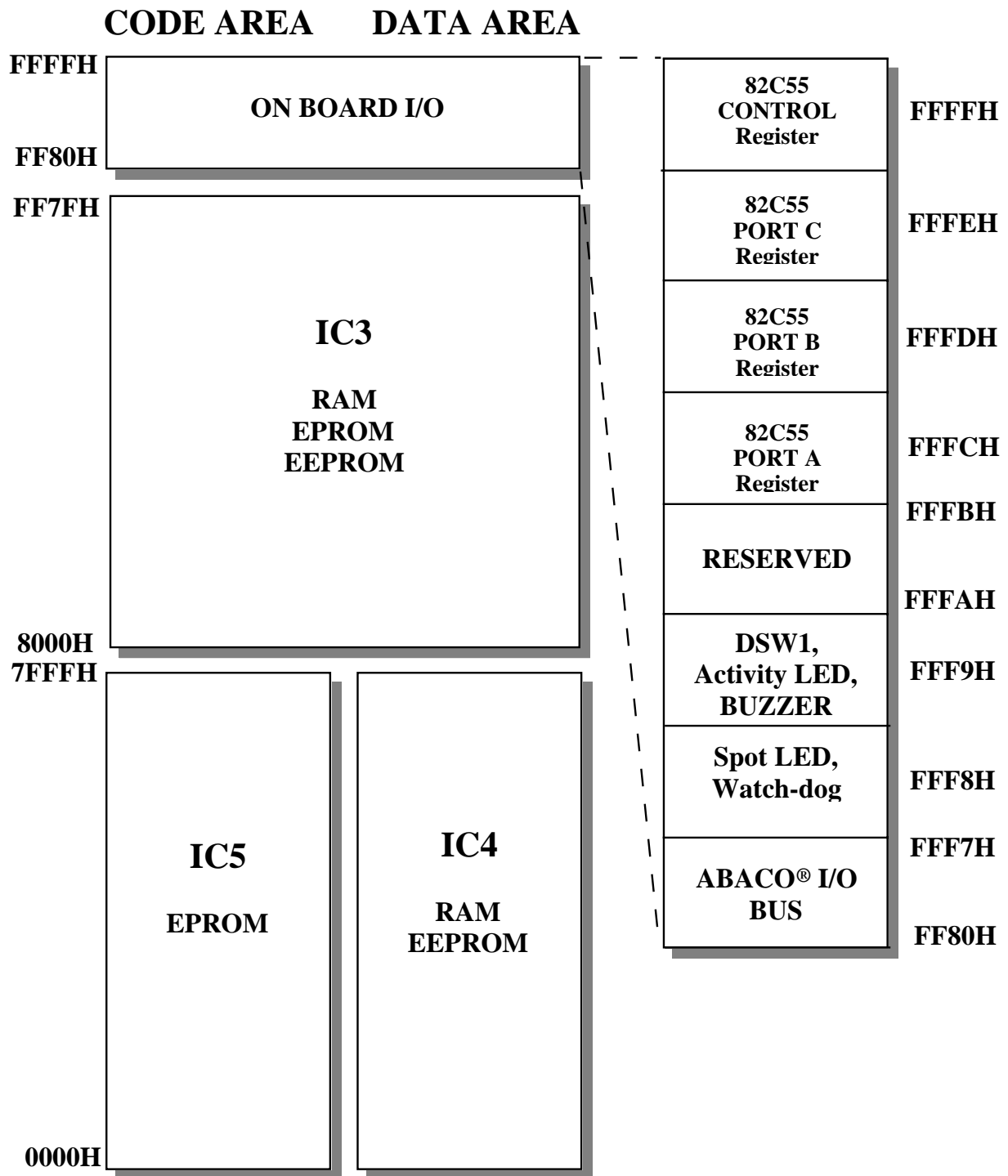
DSW1 dip 5 and 6 configuration: dip 5 ON; dip 6 ON  
 Used by software packages like: HI TECH C; DDS C; etc.



**MEMORY CONFIGURATION 3**

**FIGURE 32: MEMORY CONFIGURATION 3 (ASM)**

**DSW1 dip 5 and 6 configuration: dip 5 ON; dip 6 OFF**  
 Used by software packages like: HI TECH C; DDS C; etc.

**MEMORY CONFIGURATION 4**



**FIGURE 33: MEMORY CONFIGURATION 4 (BASIC)**

**DSW1 dip 5 and 6 configuration: dip 5 OFF; dip 6 OFF**

Used by software packages like: BASIC 323; BXC51; HI TECH C; DDS C; etc.



## PERIPHERAL DEVICES SOFTWARE DESCRIPTION

In the previous paragraphs are described the external registers addresses, while in this one is described a specific description of registers meaning and function (please refer to the I/O addressing table). Should the informations here reported be insufficient please refer to the manufacturer technical manual. This paragraph doesn't describe the microprocessor inside sections, for further informations about these sections please refer to appendix A of this manual.

### DIP SWITCH

The on board DSW1 dip switch state can be obtained by software, through a simple "read operation" at the DSW1 register address. The correspondence between register bits and dip switch is as follows:

bit D7	->	DSW1.8 (RUN/DEBUG under BASIC 323)
bit D3	->	DSW1.4
bit D2	->	DSW1.3
bit D1	->	DSW1.2
bit D0	->	DSW1.1

Reading DSW1 register by software, the User obtains a negated 8 bits combination, in fact "ON" position corresponds to **0** logic state and "OFF" position corresponds to **1** logic state.

### ACTIVITY LED

Activity LED LD4 is enabled by performing a "write operation" with bit D7=1 at the address of register LD4BZ; vice versa LED is disabled by performing the same operation with bit D7=0. The remaining 7 bits of register LD4BZ must be defined according to previous setting, for avoiding modifications on other devices.

LD4BZ register is reset (all bits to 0) after Reset or power on, maintaining disabled the activity LED.

### EXTERNAL WATCHDOG

To retrigger the external watchdog circuitry installed on **GPC® 323** board, simply perform a read operation to the WDOG register. This register shares the same addressing space of the LED management registers, this fact creates no conflict because retriggering requires only a read operation and the read data is meaningless. To prevent the external watchdog circuitry from intervening, it must be regularly retriggered at time intervals shorter than the circuit intervent time. If this doesn't happen and jumper J8 connects the watchdog to the reset circuitry, the board is reset. The default intervent time is 1.5 s.

## **BUZZER**

Buzzer is activated by performing a "write operation" with bit D0=1 at the address of register LD4BZ; vice versa buzzer is disabled by performing the same operation with bit D0=0. The remaining 7 bits of register LD4BZ must be defined according to previous setting, for avoiding modifications on other devices.

BUZ register is reset (all bits to 0) after Reset or power on, maintaining disabled the buzzer circuit.

## **SPOT LED**

Spot LED LD3 is enabled by performing a "write operation" to the address of register SPOT. This operation enables the LED for an interval of about 300 msec then the LED turns off automatically. The value to write to the SPOT register is meaningless and so can be any value.

The main purpose of this LED is to indicate the working condition of application program without introducing programming difficulties or to signal efficiently the presence of an event that requires a prompt reaction.

## **PPI 82C55**

This external peripheral device is managed through 4 registers: one status register (CNT) and three data registers (PDA, PDB, PDC). The data registers are available both for read operation (to obtain signal status) and for write operation (to set signal status) with the correspondence described in figure 23. The PPI 82C55 can work in three different modes:

MODE 0 = it provides two 8 bits bidirectional ports (A,B) and two 4 bits bidirectional ports (C LOW, C HIGH); output signals are latched and input signals are not latched; no handshake signals are provided.

MODE 1 = it provides two 12 bits ports (A+C LOW and B+C HIGH) where ports A and B are used as 8 I/O lines and port C are used as 4 handshake lines. Both inputs and outputs are latched.

MODE 2 = it provides a 13 bits port (A+C $\div$ 7) where port A is used as 8 I/O lines and the 5 bits of port C are used as handshake, and a 11 bits port (B+C0 $\div$ 2) where port B is used as 8 I/O lines and the 3 bits of port C are used as handshakes. Both inputs and outputs are latched.

The device is programmed writing an 8 bits word in the status register CNT, with the following bit meaning:

CNT = SF M1 M2 A CH M3 B CL

where

SF = mode Set Flag: if actived (1) the device is enabled for standard I/O operation

M1 M2 = mode selection:

0 0 = mode 0

0 1 = mode 1

1 X = mode 2

A = port A direction: 1=input; 0=output

CH = port C HIGH direction: 1=input; 0=output

M3 = mode selection: 1=mode 1; 0=mode 0

B = port B direction: 1=input; 0=output

CL = port C LOW direction: 1=input; 0=output

After Reset or power on PPI 82C55 is programmed in mode 0 with all three ports in input; in this way any connection of PPI 82C55 signals can be used without conflict problems.

### **RS 422-485 COMMUNICATION DIRECTION**

Bit D1 of DIR microprocessor signal (CPU pin 15, P3.3) sets the status of RS 485 communication direction or RS 422 communication enable as described in paragraph "SERIAL COMMUNICATION TYPE SELECTION".

The DIR signal has the following meaning:

- RS485: DIR = 0 --> RS 485 serial line in reception
- DIR = 1 --> RS 485 serial line in transmission
- RS 422: DIR = 0 --> RS 422 transmitter disabled
- DIR = 1 --> RS 422 transmitter enabled

During Reset or power DIR signal is locked to a low level (DIR = 0) so RS 485 driver is receiving or RS 422 driver is disabled to avoid communication conflicts.

### **SERIAL EEPROM**

For software management of serial EEPROM module of IC 10, please refer to specific documentation or to demo programs supplied with the card. No other information is provided by this manual because the use of this component requires a deep knowledge of its management techniques, and, however, the User can take advantage of the high level routines provided with the programming tool. The first 30 bytes of serial EEPROM are reserved for software tools use, so they can't be read or written by User program.

The electric connection is:

DATA signal (SDA) --> CPU pin 16 (P3.4)  
CLOCK signal (SCL) --> CPU pin 9 (P1.7)

We also would remark that, due to our implementation of the management circuitry of EEPROM module, signals A2, A1, A0 of slave address are respectively set to 1, 0, 0.

### **BACKED RAM + SERIAL RTC**

For software management of serial RAM+RTC module of IC 12, please refer to specific documentation or to demo programs supplied with the card. No other information is provided by this manual because the use of this component requires a deep knowledge of its management techniques, and, however, the User can take advantage of the high level routines provided with the programming tool. We would remark that the maximum size of EEPROM must be 1024 bytes if this RAM+RTC component is installed on IC12.

The electric connection is:

DATA signal (SDA) --> CPU pin 27 (P3.3)  
CLOCK signal (SCL) --> CPU pin 29 (P3.5)

We also would remark that, due to our implementation of the management circuitry of RAM+RTC module, signal A0 of slave address is set to 0.



## **A/D CONVERTER**

For software management of A/D converter channels, please refer to specific documentation. No other information is provided by this manual because the use of this component requires a deep knowledge of its management techniques, and, however, the User can take advantage of the high level routines provided with the programming tool.

The electric connection is:

DATA IN signal	->	CPU pin 16 (P3.4)
DATA OUT signal	->	CPU pin 17 (P3.5)
I/O CLOCK signal	->	CPU pin 3 (P1.1)
/CS signal	->	CPU pin 8 (P1.6)

## **SERIAL LINES**

Please refer to proper technical documentation or to "APPENDIX B".

## **TIMER COUNTER**

Please refer to proper technical documentation or to "APPENDIX B".

## **INTERNAL WATCH DOG**

Please refer to proper technical documentation or to "APPENDIX B".

## EXTERNAL DEVICES FOR GPC® 323

**GPC® 323** can be connected to a wide range of **grifo®** cards and to many system of other companies. Hereunder these cards are listed, for further information please call **grifo®**.

### **QTP 24 - QTP 24P**

Quick Terminal Panel 24 keys with Parallel interface

Intelligent user panel equipped with Fluorescent or LCD display, LEDs backlit, 20x2 or 20x4 characters; RS 232, RS 422, RS 485 or current loop serial line; serial E2 for set up and message. Possibility of re-naming keys, LEDs and panel name by inserting label with new name into the proper slot; 24 Keys and 16 LEDs with blinking attribute and buzzer manageable by software; built in power supply; RTC option, reader of magnetic badge and relay. The QTP 24P is low cost no intelligent (passive) version. It is directly driven from 16 TTL I/O lines; high level languages supported.

### **QTP G26**

Quick Terminal Panel - LCD Graphic, 26 keys

Intelligent user panel equipped with graphic LCD display 240x128 pixel, CFC backlit; optocoupled RS 232 line and additional RS 232, RS 422, RS 485 or current loop serial line. Independent optional CAN line controller; serial E2 for set up; RTC and RAM Lithium backed; primary graphic objects; possibility of re-naming keys, LEDs and panel name by inserting label with new name into the proper slot; 26 Keys and 16 LEDs with blinking attribute and buzzer manageable by software; built in power supply; reader of magnetic badge, smart-card and relay option.

### **MCI 64**

Memory Cards Interfaces 64 MBytes

Interfacing card for managing 68 pins PCMCIA Memory cards, it is directly driven from any **Abaco®** I/O standard connector; High level languages GDOS supported.

### **RBO 08 TBO 08**

Relays or Transistor BLOCK Output

Interface for **Abaco®** standard I/O 20 pins connector; 8 displayed Relays 3 A with MOV or 8 optocoupled Transistors 3 A open collectors; screw terminal; Connection for DIN C Type and  $\Omega$  rails.

### **RBO 16**

Relays BLOCK Output

Interface for **Abaco®** standard I/O 20 pins connector; 16 displayed Relays 3 A with MOV; screw terminal; Connection for DIN C Type and  $\Omega$  rails.

### **XBI R4 XBI T4**

miXed BLOCK Input-Output

Interface for **Abaco®** standard I/O 20 pins connector; 4 Relays 3 A with MOV or 4 optocoupled Transistors 3 A open collectors; 4 input lines optocoupled; I/O lines displayed; screw terminal; Connection for DIN C Type and  $\Omega$  rails.

**FBC xxx**

## Flat BLOCK Contact

This interconnection system “wires to board” allows the connection to many types of flat cable connectors to a terminal for external connections.

Other interfacing for most popular connectors such as D, mini DIN, ACCESS.bus™, and so on, are available. Connection for DIN C Type and  $\Omega$  rails.

**IPC 51**

## Intelligent Peripheral Controller

This Intelligent peripheral card acquires 8 temperature sensors PT 100 type or thermo couple J, K, S, T type; BUS interfacing or through RS 232, RS 422-485 or Current Loop line; 16 Bits + sign A/D section; 5 or 8 conversion per second; 0,1 °C resolution.

**UAR 24**

## Universal Analog Regulator

This Intelligent peripheral card acquires 2 temperature sensors PT 100 type or 2 thermo couple J, K, S, T type; 4 3 A relays output; 2 D/A outputs 12 bits 0÷10 Vdc each; BUS interfacing or through RS 232, RS 422-485 or Current Loop line; 16 Bits + sign A/D section

**QTP 22**

## Quick Terminal Panel 22 keys

Intelligent user panel equipped with alphanumeric LCD or fluorescent display (40x1, 40x2 or 40x4 characters); RS 232, RS 422-485 or Current Loop serial lines; serial EEPROM for set-up and messages; Possibility of re-naming the 22 keys and name panel by inserting label with new name into the proper slot ; 22 LEDs with blinking attribute and Buzzer manageable by software ; built-in 24 Vac power supply; RTC option, reader of magnetic badge and relays.

**QTP 24**

## Quick Terminal Panel 24 keys

Intelligent user panel equipped with Fluorescent 20x2 or LCD display, LEDs backlit, 20x2 or 20x4 characters; RS 232, RS 422-485 or Current Loop serial lines; serial EEPROM for set-up and messages; Possibility of re-naming keys, LEDs and panel name by inserting label with new name into the proper slot ; 24 keys and 16 LEDs with blinking attribute and Buzzer manageable by software ; built-in power supply; RTC option, reader of magnetic badge and relays.

**QTP G26**

## Quick Terminal Panel LCD Graphic

Intelligent user panel equipped with graphic LCD display 240x120 pixels, LEDs backlit; 1RS 232 line , additional RS 232, RS 422-485 or Current Loop lines; serial EEPROM for set-up; 256K EPROM, FLASH and EEPROM; RTC and 128K RAM; primary graphic object; Possibility of re-naming keys, LEDs and panel name by inserting label with new name into the proper slot , 16 keys and 16 LEDs, Buzzer, built-in power supply.

**OBI 01 - OBI 02**

Opto BLOCK Input NPN-PNP

Interface between 16 NPN, PNP optocoupled and displayed input lines, screw terminal, and **Abaco**<sup>®</sup> standard I/O 20 pins connector; power supply section; connection for DIN C type and  $\Omega$  rails.

**OBI N8 - OBI P8**

Opto BLOCK Input NPN-PNP

Interface between 8 NPN, PNP optocoupled and displayed input lines, screw terminal, and **Abaco**<sup>®</sup> standard I/O 20 pins connector; power supply section; connection for DIN C type and  $\Omega$  rails.

**TBO 01**

Transistor BLOCK Output

Interface between **ABACO**<sup>®</sup> standard I/O 20 pins connector and 16 transistor output lines; 45 Vdc 3 A open collector; screw terminal; optocoupled and displayed signals; connection for DIN C type and  $\Omega$  rails.

**RBO 01**

Relays BLOCK Output

Interface between **ABACO**<sup>®</sup> standard I/O 20 pins connector and 8 relay output lines; 5 or 10 A outputs; N.O. or N.C. contact; screw terminal; displayed signals; connection for DIN C type and  $\Omega$  rails.

**XBI 01**

miXed BLOCK Input-Output

Interface for **ABACO**<sup>®</sup> standard I/O 20 pins connector; 8 transistor output lines 45 Vdc 3 A; 8 input lines; screw terminal; optocoupled and displayed signals; connection for DIN C type and  $\Omega$  rails.

**IBC 01**

Interface Block Communication

Conversion card for serial communication, 2 RS 232 lines; 1 RS 422-485 line; 1 optical fibre line; selectable DTE/DCE interface; quick connection for DIN C type and  $\Omega$  rails.

**DEB 01**

Didactis Experimental Board

Supporting card for 16 TTL I/O lines use. It includes: 16 keys, 16 LEDs, 4 digits, 16 keys matrix keyboard, Centronics printer interface, LCD display and fluorescent display interface, **GPC**<sup>®</sup> 68 I/O connector, field connection with screw terminal.

**KDI LT - KDI L32 - KDI L33 - KDI FF - KDI F32 - KDI F33**

Keyboard Display Interface 32 Key

Interface for **Abaco**<sup>®</sup> standard I/O 20 pins connector; 32 keys matrix keyboard (short key for 32 types, long keys for 33 types and external keyboard for LT, FF types); 8 LEDs; buzzer; fluorescentor LCD alphanumeric display.

**CBT 420**

Current Block Transmitter 4÷20mA

Interface between 4 input lines 0÷5, 0÷10 Vdc and 4 current output channels 4÷20 mA; signals on screw terminal; 14 bit resolution; quick connection for DIN C type and  $\Omega$  rails.

**KDL 224 - KDL 424**

## Keyboard Display LCD

Interface for **Abaco**® standard I/O 20 pins connector; 24 keys matrix keyboard (compatible pin out with 3x4 and 4x4 telephone keyboards); LCD alphanumeric display with 20x2 or 20x4 characters.

**KDF 224**

## Keyboard Display FUTABA

Interface for **Abaco**® standard I/O 20 pins connector; 24 keys matrix keyboard (compatible pin out with 3x4 and 4x4 telephone keyboards); fluorescent alphanumeric display with 20x2 or 20x4 characters.

**IAC 01**

## Interface Adapter Centronics

Interface between **Abaco**® standard I/O 20 pins connector and D 25 pins connector with Centronics standard pin out.

## BIBLIOGRAPHY

In this chapter there is a complete list of technical books, where the user can find all the necessary documentations on the components mounted on **GPC® 323**.

Data book MAXIM:	<i>New Releases Data Book - Volume 4</i>
Data book HEWLETT PACKARD:	<i>Optoelectronic Designer's Catalog</i>
Data book NEC:	<i>Memory Products</i>
Data book NEC:	<i>Microprocesors and Peripherals - Volume 3</i>
Data book TEXAS INSTRUMENTS:	<i>The TTL Data Book - SN54/74 Families</i>
Data book TEXAS INSTRUMENTS:	<i>Linear Circuits Dtata Book - Volumi 1 e 3</i>
Data book TEXAS INSTRUMENTS:	<i>RS-422 and RS-485 Interface Circuits</i>
Data book TEXAS INSTRUMENTS:	<i>Data acquisition circuits Data Book</i>
Data book XICOR:	<i>Data Book</i>
Data book PHILIPS:	<i>80C51 - Based 8-Bit Microcontrollers</i>
Data book PHILIPS:	<i>IC12 - I<sup>2</sup>C Bus</i>
Data book NATIONAL SEMICONDUCTOR:	<i>Linear Databook - Volume1</i>

For further informations and upgrades please refer to specific internet web pages of the manufacturing companies.

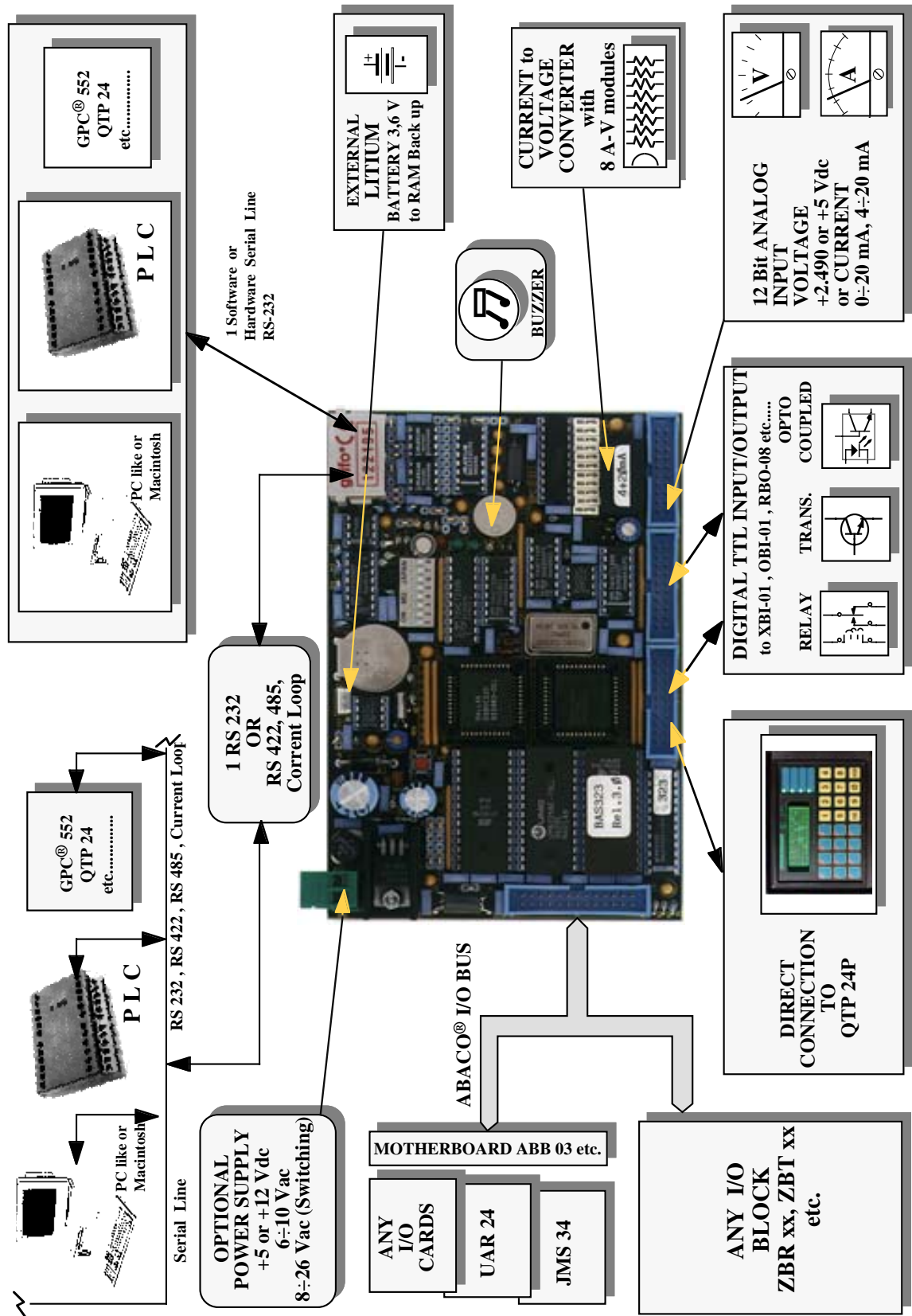


FIGURE 34: POSSIBLE CONNECTIONS DIAGRAM





APPENDIX A: JUMPERS AND DRIVERS LOCATION

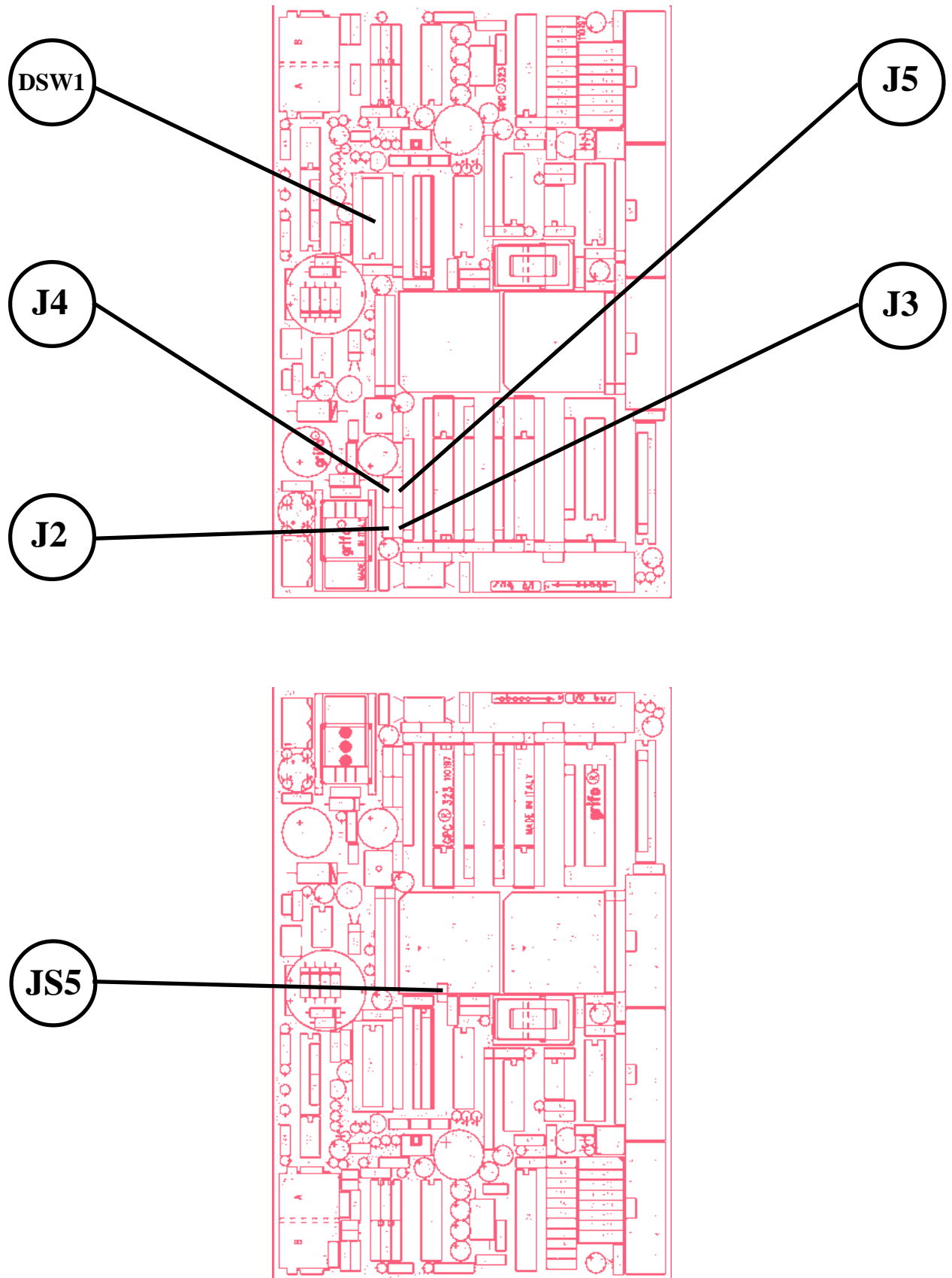


FIGURE A1: MEMORY JUMPERS LOCATION

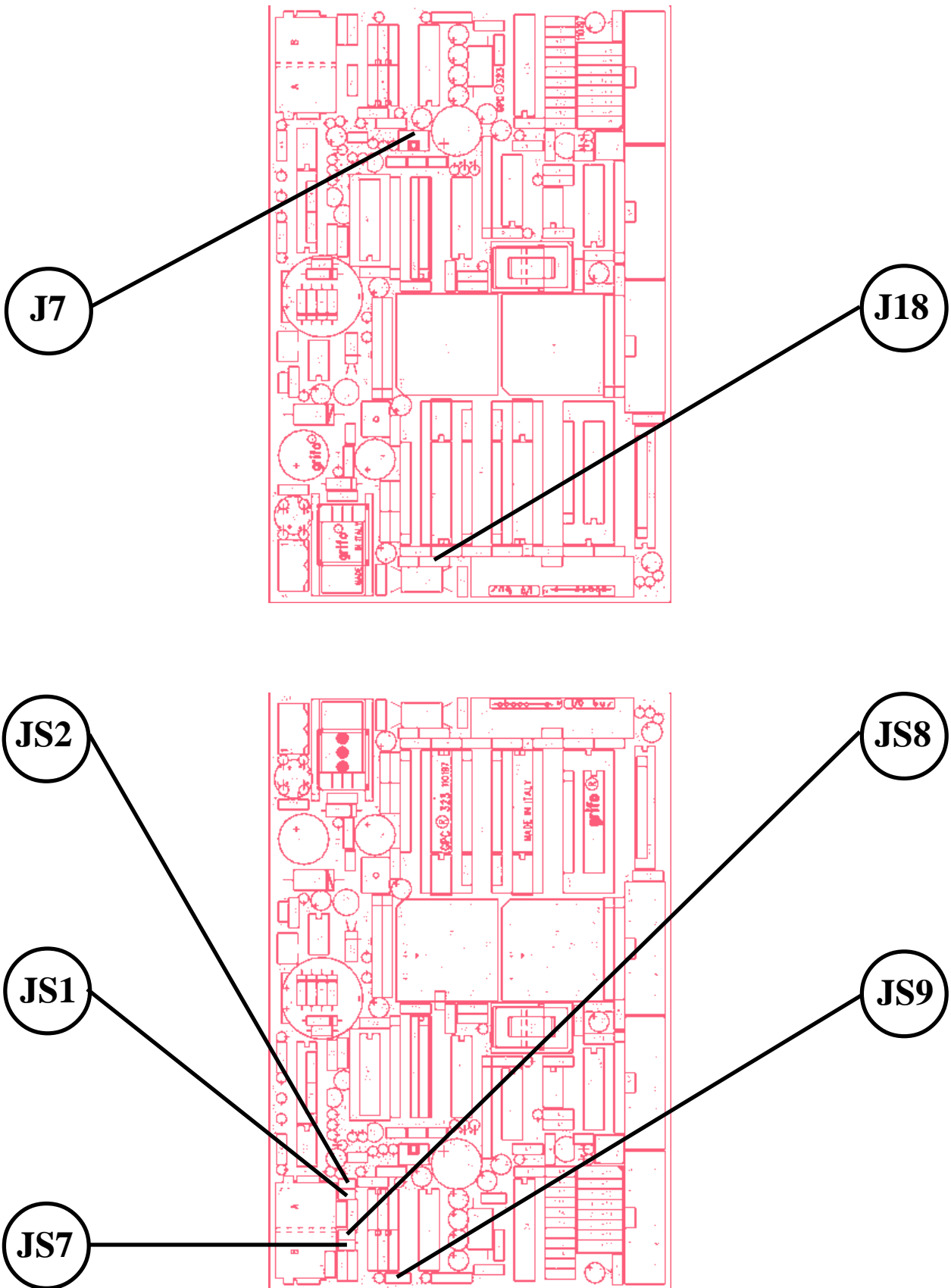
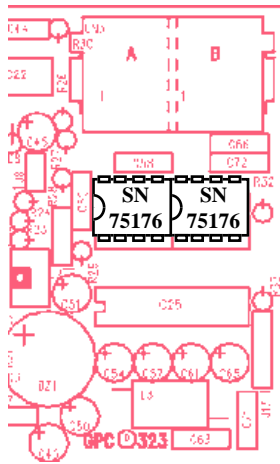
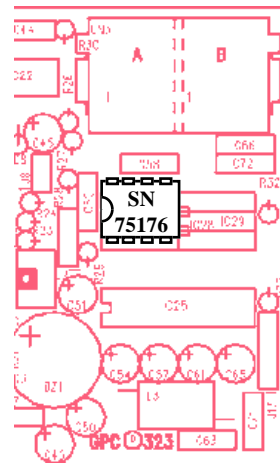


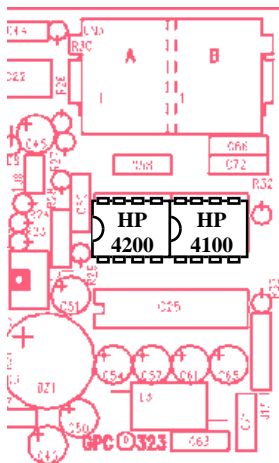
FIGURE A2: SERIAL COMMUNICATION JUMPERS LOCATION



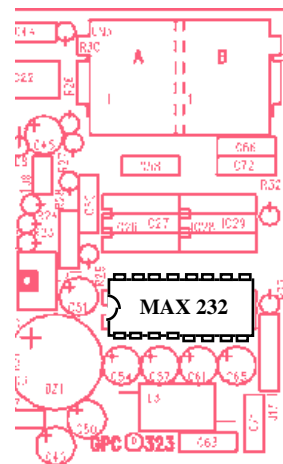
Serial = RS 422



Serial = RS 485



Serial = Current Loop



Serial = RS 232

FIGURA A3: SERIAL COMMUNICATION DRIVERS LOCATION



# APPENDIX B: ON BOARD PERIPHERAL DESCRIPTION

## µP 80C32

Philips Semiconductors

Product specification

### CMOS single-chip 8-bit microcontrollers

### 80C32/87C52

#### DESCRIPTION

The Philips 80C32/87C52 is a high-performance microcontroller fabricated with Philips high-density CMOS technology. The Philips CMOS technology combines the high speed and density characteristics of HMOS with the low power attributes of CMOS. Philips epitaxial substrate minimizes latch-up sensitivity.

The 87C52 contains an 8k × 8 EPROM and the 80C32 is ROMless. Both contain a 256 × 8 RAM, 32 I/O lines, three 16-bit counter/timers, a six-source, two-priority level nested interrupt structure, a serial I/O port for either multi-processor communications, I/O expansion or full duplex UART, and on-chip oscillator and clock circuits.

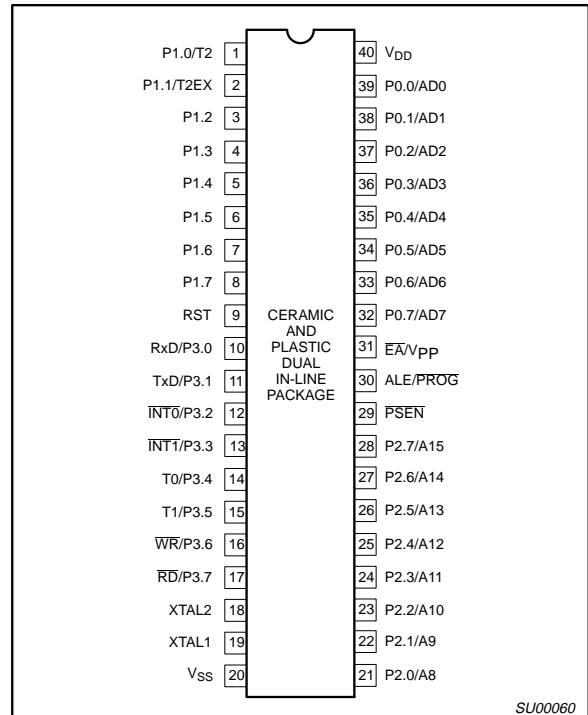
In addition, the 80C32/87C52 has two software selectable modes of power reduction—idle mode and power-down mode. The idle mode freezes the CPU while allowing the RAM, timers, serial port, and interrupt system to continue functioning. The power-down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative.

See 80C52/80C54/80C58 datasheet for ROM device specifications.

#### FEATURES

- 80C51 based architecture
- 8032 compatible
  - 8k × 8 EPROM (87C52)
  - ROMless (80C32)
  - 256 × 8 RAM
  - Three 16-bit counter/timers
  - Full duplex serial channel
  - Boolean processor
- Memory addressing capability
  - 64k ROM and 64k RAM
- Power control modes:
  - Idle mode
  - Power-down mode
- CMOS and TTL compatible
- Three speed ranges:
  - 3.5 to 16MHz
  - 3.5 to 24MHz
  - 3.5 to 33MHz
- Five package styles
- Extended temperature ranges
- OTP package available

#### PIN CONFIGURATIONS



SU00060



CMOS single-chip 8-bit microcontrollers

80C32/87C52

CERAMIC AND PLASTIC LEADED CHIP CARRIER PIN FUNCTIONS

Pin	Function	Pin	Function	Pin	Function
1	NC*	16	T0/P3.4	31	P2.7/A15
2	T2/P1.0	17	T1/P3.5	32	PSEN
3	T2EX/P1.1	18	WR/P3.6	33	ALE/PROG
4	P1.2	19	RD/P3.7	34	NC*
5	P1.3	20	XTAL2	35	EA/Vpp
6	P1.4	21	XTAL1	36	P0.7/AD7
7	P1.5	22	Vss	37	P0.6/AD6
8	P1.6	23	NC*	38	P0.5/AD5
9	P1.7	24	P2.0/A8	39	P0.4/AD4
10	RST	25	P2.1/A9	40	P0.3/AD3
11	RxD/P3.0	26	P2.2/A10	41	P0.2/AD2
12	NC*	27	P2.3/A11	42	P0.1/AD1
13	TxD/P3.1	28	P2.4/A12	43	P0.0/AD0
14	INT0/P3.2	29	P2.5/A13	44	Vcc
15	INT1/P3.3	30	P2.6/A14		

\* DO NOT CONNECT

SU00061

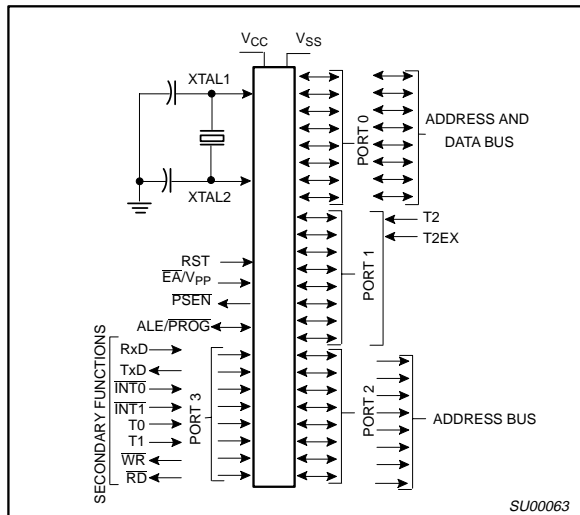
PLASTIC QUAD FLAT PACK PIN FUNCTIONS

Pin	Function	Pin	Function	Pin	Function
1	P1.5	16	Vss	31	P0.6/AD6
2	P1.6	17	NC*	32	P0.5/AD5
3	P1.7	18	P2.0/A8	33	P0.4/AD4
4	RST	19	P2.1/A9	34	P0.3/AD3
5	RxD/P3.0	20	P2.2/A10	35	P0.2/AD2
6	NC*	21	P2.3/A11	36	P0.1/AD1
7	TxD/P3.1	22	P2.4/A12	37	P0.0/AD0
8	INT0/P3.2	23	P2.5/A13	38	Vcc
9	INT1/P3.3	24	P2.6/A14	39	NC*
10	T0/P3.4	25	P2.7/A15	40	T2/P1.0
11	T1/P3.5	26	PSEN	41	T2EX/P1.1
12	WR/P3.6	27	ALE/PROG	42	P1.2
13	RD/P3.7	28	NC*	43	P1.3
14	XTAL2	29	EA/Vpp	44	P1.4
15	XTAL1	30	P0.7/AD7		

\* DO NOT CONNECT

SU00062

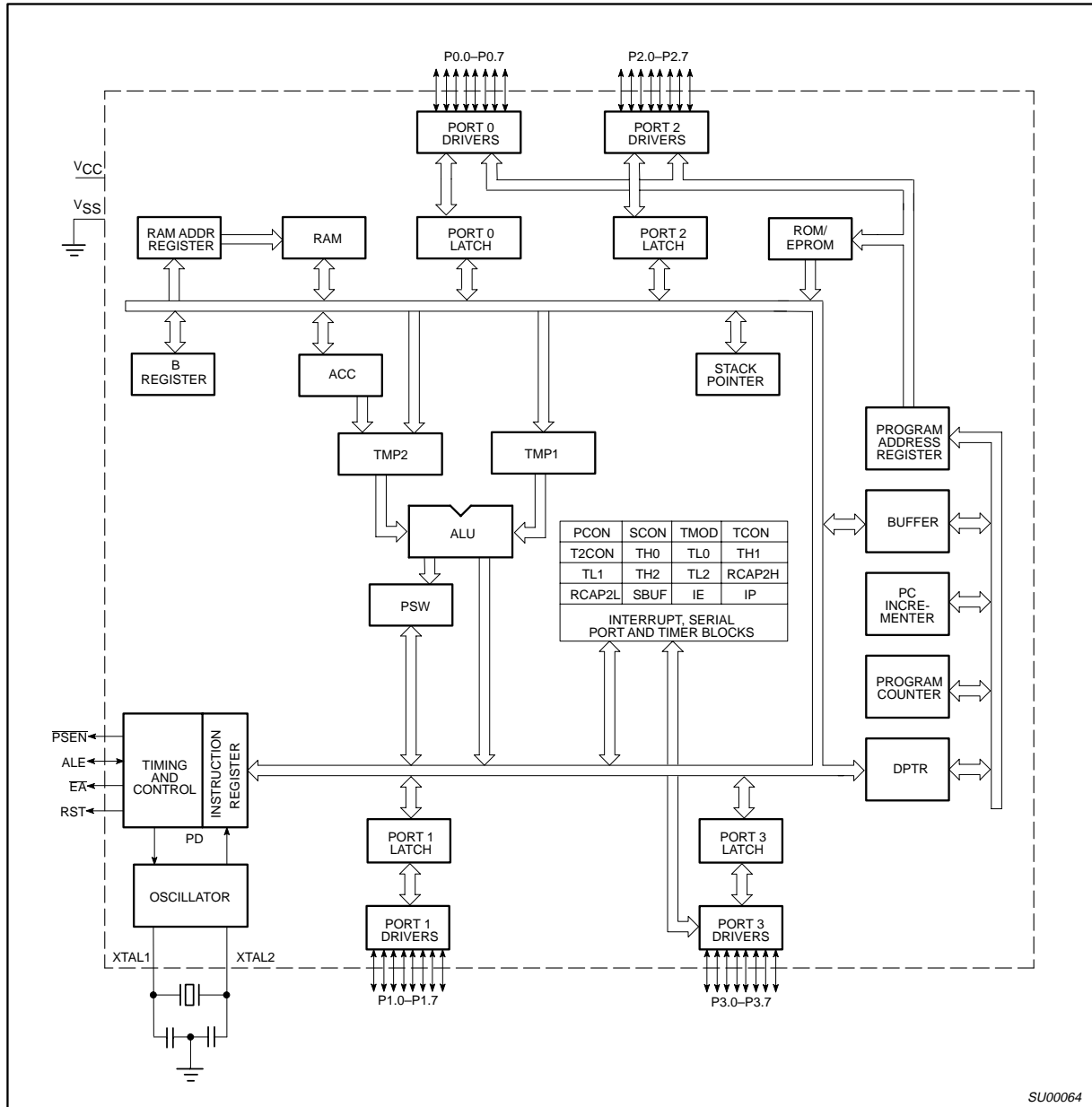
LOGIC SYMBOL



CMOS single-chip 8-bit microcontrollers

80C32/87C52

BLOCK DIAGRAM



## CMOS single-chip 8-bit microcontrollers

## 80C32/87C52

**Table 1. 8XC52 Special Function Registers**

SYMBOL	DESCRIPTION	DIRECT ADDRESS	BIT ADDRESS, SYMBOL, OR ALTERNATIVE PORT FUNCTION								RESET VALUE
			MSB				LSB				
ACC*	Accumulator	E0H	E7	E6	E5	E4	E3	E2	E1	E0	00H
B*	B register	F0H	F7	F6	F5	F4	F3	F2	F1	F0	00H
DPTR: DPH DPL	Data pointer (2 bytes) Data pointer high Data pointer low	83H 82H									00H 00H
IE*	Interrupt enable	A8H	AF	AE	AD	AC	AB	AA	A9	A8	0x000000B
			EA	–	ET2	ES	ET1	EX1	ET0	EX0	
IP*	Interrupt priority	B8H	BF	BE	BD	BC	BB	BA	B9	B8	xx000000B
			–	–	PT2	PS	PT1	PX1	PT0	PX0	
P0*	Port 0	80H	87	86	85	84	83	82	81	80	FFH
			AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	
P1*	Port 1	90H	97	96	95	94	93	92	91	90	FFH
			–	–	–	–	–	–	T2EX	T2	
P2*	Port 2	A0H	A7	A6	A5	A4	A3	A2	A1	A0	FFH
			A15	A14	A13	A12	A11	A10	A9	A8	
P3*	Port 3	B0H	B7	B6	B5	B4	B3	B2	B1	B0	FFH
			RD	WR	T1	T0	INT1	INT0	TxD	RxD	
PCON <sup>1</sup>	Power control	87H	SMOD	–	–	–	GF1	GF0	PD	IDL	0xxxxxxxB
			D7	D6	D5	D4	D3	D2	D1	D0	
PSW*	Program status word	D0H	CY	AC	F0	RS1	RS0	OV	–	P	00H
RCAP2H# RCAPL#	Capture high Capture low	CBH CAH									00H 00H
SBUF	Serial data buffer	99H	9F	9E	9D	9C	9B	9A	99	98	xxxxxxxB
			SM0	SM1	SM2	REN	TB8	RB8	TI	RI	
SCON*	Serial controller	98H									00H
SP	Stack pointer	81H	8F	8E	8D	8C	8B	8A	89	88	07H
			TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	
TCON*	Timer control	88H	CF	CE	CD	CC	CB	CA	C9	C8	00H
			TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2	
T2CON*#	Timer 2 control	C8H									00H
TH0	Timer high 0	8CH									00H
TH1	Timer high 1	8DH									00H
TH2#	Timer high 2	CDH									00H
TL0	Timer low 0	8AH									00H
TL1	Timer low 1	8BH									00H
TL2#	Timer low 2	CCH									00H
TMOD	Timer mode	89H	GATE	C/T	M1	M0	GATE	C/T	M1	M0	00H

\* Bit addressable

# SFRs are modified from or added to the 80C51 SFRs.

1. Bits GF1, GF0, PD, and IDL of the PCON register are not implemented in the NMOS 8XC52.



CMOS single-chip 8-bit microcontrollers

80C32/87C52

PIN DESCRIPTION

MNEMONIC	PIN NO.			TYPE	NAME AND FUNCTION
	DIP	LCC	QFP		
V <sub>SS</sub>	20	22	16	I	<b>Ground:</b> 0V reference.
V <sub>CC</sub>	40	44	38	I	<b>Power Supply:</b> This is the power supply voltage for normal, idle, and power-down operation.
P0.0–P0.7	39–32	43–36	37–30	I/O	<b>Port 0:</b> Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application, it uses strong internal pull-ups when emitting 1s. Port 0 also outputs the code bytes during program verification in the 87C52. External pull-ups are required during program verification.
P1.0–P1.7	1–8	2–9	40–44 1–3	I/O	<b>Port 1:</b> Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 1 pins that are externally pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I <sub>IL</sub> ). Pins P1.0 and P1.1 also. Port 1 also receives the low-order address byte during program memory verification. Port 1 also serves alternate functions for timer 2: <b>T2 (P1.0):</b> Timer/counter 2 external count input. <b>T2EX (P1.1):</b> Timer/counter 2 trigger input.
P2.0–P2.7	1 2 21–28	2 3 24–31	40 41 18–25	I I I/O	<b>Port 2:</b> Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 2 pins that are externally being pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I <sub>IL</sub> ). Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application, it uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOV @Ri), port 2 emits the contents of the P2 special function register.
P3.0–P3.7	10–17	11, 13–19	5, 7–13	I/O	<b>Port 3:</b> Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 3 pins that are externally being pulled low will source current because of the pull-ups. (See DC Electrical Characteristics: I <sub>IL</sub> ). Port 3 also serves the special features of the 80C51 family, as listed below: <b>RxD (P3.0):</b> Serial input port <b>TxD (P3.1):</b> Serial output port <b>INT0 (P3.2):</b> External interrupt <b>INT1 (P3.3):</b> External interrupt <b>T0 (P3.4):</b> Timer 0 external input <b>T1 (P3.5):</b> Timer 1 external input <b>WR (P3.6):</b> External data memory write strobe <b>RD (P3.7):</b> External data memory read strobe
RST	9	10	4	I	<b>Reset:</b> A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to V <sub>SS</sub> permits a power-on reset using only an external capacitor to V <sub>CC</sub> .
ALE/PROG	30	33	27	I/O	<b>Address Latch Enable/Program Pulse:</b> Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. This pin is also the program pulse input (PROG) during EPROM programming.
PSEN	29	32	26	O	<b>Program Store Enable:</b> The read strobe to external program memory. When the device is executing code from the external program memory, PSEN is activated twice each machine cycle, except that two PSEN activations are skipped during each access to external data memory. PSEN is not activated during fetches from internal program memory.
EA/V <sub>PP</sub>	31	35	29	I	<b>External Access Enable/Programming Supply Voltage:</b> EA must be externally held low to enable the device to fetch code from external program memory locations 0000H to 1FFFH. If EA is held high, the device executes from internal program memory unless the program counter contains an address greater than 1FFFH. This pin also receives the 12.75V programming supply voltage (V <sub>PP</sub> ) during EPROM programming.
XTAL1	19	21	15	I	<b>Crystal 1:</b> Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	18	20	14	O	<b>Crystal 2:</b> Output from the inverting oscillator amplifier.



## CMOS single-chip 8-bit microcontrollers

## 80C32/87C52

### DIFFERENCES FROM THE 80C51

#### Special Function Registers

The special function register space is the same as the 80C51 except that the 80C32/87C52 contains the additional special function registers T2CON, RCAP2L, RCAP2H, TL2, and TH2. Since the standard 80C51 on-chip functions are identical in the 8XC52, the SFR locations, bit locations, and operation are likewise identical. The only exceptions are in the interrupt mode and interrupt priority SFRs (see Table 1).

#### Timer/Counters

In addition to timer/counters 0 and 1 of the 80C51, the 80C32/87C52 contains timer/counter 2. Like timers 0 and 1, timer 2 can operate as either an event timer or as an event counter. This is selected by bit C/T2 in the special function register T2CON (see Figure 1). It has three operating modes: capture, auto-load, and baud rate generator, which are selected by bits in the T2CON as shown in Table 2.

In the Capture Mode there are two options which are selected by bit EXEN2 in T2CON. If EXEN2 = 0, then Timer 2 is a 16-bit timer or counter which upon overflowing sets bit TF2, the Timer 2 overflow bit, which can be used to generate an interrupt. If EXEN2 = 1, then Timer 2 still does the above, but with the added feature that a 1-to-0 transition at external input T2EX causes the current value in the Timer 2 registers, TL2 and TH2, to be captured into registers RCAP2L and RCAP2H, respectively. (RCAP2L and RCAP2H are new special function registers in the 80C52.) In addition, the transition at T2EX causes bit EXF2 in T2CON to be set, and EXF2 like TF2 can generate an interrupt. The Capture Mode is illustrated in Figure 2.

In the auto-reload mode, there are again two options, which are selected by bit EXEN2 in T2CON. If EXEN2 = 0, then when Timer 2 rolls over it not only sets TF2 but also causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2L and RCAP2H, which are preset by software. If EXEN2 = 1, then Timer 2 still does the above, but with the added feature that a 1-to-0

transition at external input T2EX will also trigger the 16-bit reload and set EXF2. The auto-reload mode is illustrated in Figure 3.

The baud rate generation mode is selected by RCLK = 1 and/or TCLK = 1. It will be described in conjunction with the serial port.

#### Serial Port

The serial port of the 8XC52 is identical to that of the 80C51 except that counter/timer 2 can be used to generate baud rates.

In the 8XC52, Timer 2 is selected as the baud rate generator by setting TCLK and/or RCLK in T2CON (see Figure 1). Note that the baud rate for transmit and receive can be simultaneously different. Setting RCLK and/or TCLK puts Timer into its baud rate generator mode, as shown in Figure 4.

The baud rate generator mode is similar to the auto-reload mode, in that a rollover in TH2 causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2H and RCAP2L, which are preset by software.

Now, the baud rates in Modes 1 and 3 are determined by Timer 2's overflow rate as follows:

$$\text{Modes 1, 3 Baud Rate} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

The timer can be configured for either "timer" or "counter" operation. In the most typical applications, it is configured for "timer" operation (C/T2 = 0). "Timer" operation is a little different for Timer 2 when it's being used as a baud rate generator. Normally, as a timer it would increment every machine cycle (thus at 1/12 the oscillator frequency). As a baud rate generator, however, it increments every state time (thus at 1/2 the oscillator frequency). In that case the baud rate is given by the formula:

$$\text{Modes 1, 3 Baud Rate} = \frac{\text{Oscillator Frequency}}{32 [65536 (\text{RCAP2H}, \text{RCAP2L})]}$$

where (RCAP2H, RCAP2L) is the content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

		(MSB)						(LSB)	
		TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2
Symbol	Position	Name and Significance							
TF2	T2CON.7	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK or TCLK = 1.							
EXF2	T2CON.6	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software.							
RCLK	T2CON.5	Receive clock flag. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in modes 1 and 3. RCLK = 0 causes Timer 1 overflow to be used for the receive clock.							
TCLK	T2CON.4	Transmit clock flag. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.							
EXEN2	T2CON.3	Timer 2 external enable flag. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.							
TR2	T2CON.2	Start/stop control for Timer 2. A logic 1 starts the timer.							
C/T2	T2CON.1	Timer or counter select. (Timer 2) 0 = Internal timer (OSC/12) 1 = External event counter (falling edge triggered).							
CP/RL2	T2CON.0	Capture/Reload flag. When set, captures will occur on negative transitions at T2EX if EXEN2 = 1. When cleared, auto-reloads will occur either with Timer 2 overflows or negative transitions at T2EX when EXEN2 = 1. When either RCLK = 1 or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.							

SU00065

Figure 1. Timer/Counter 2 (T2CON) Control Register

CMOS single-chip 8-bit microcontrollers

80C32/87C52

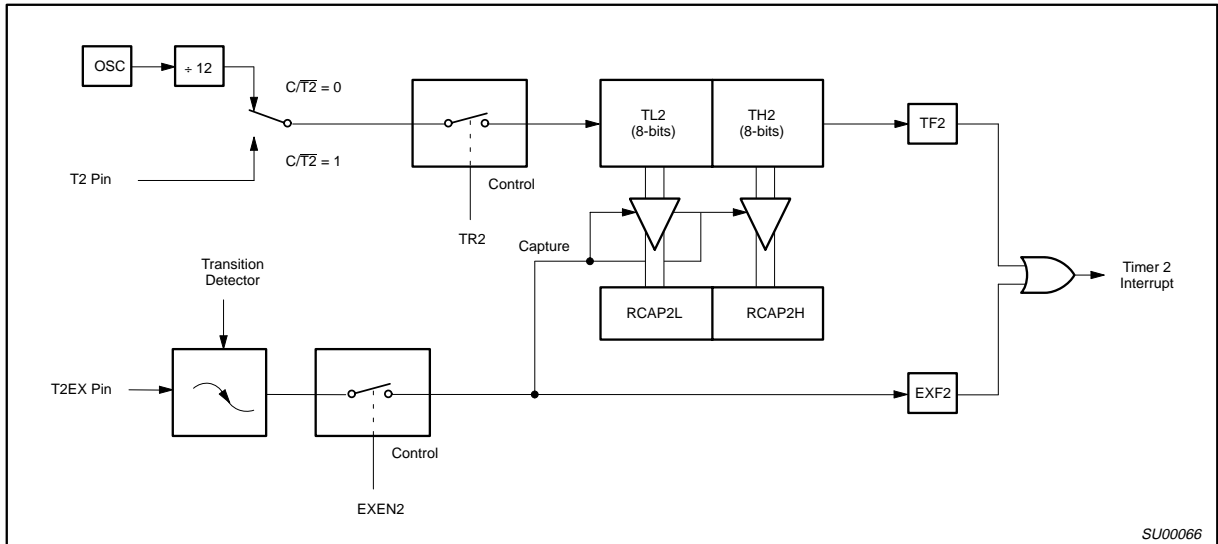


Figure 2. Timer 2 in Capture Mode

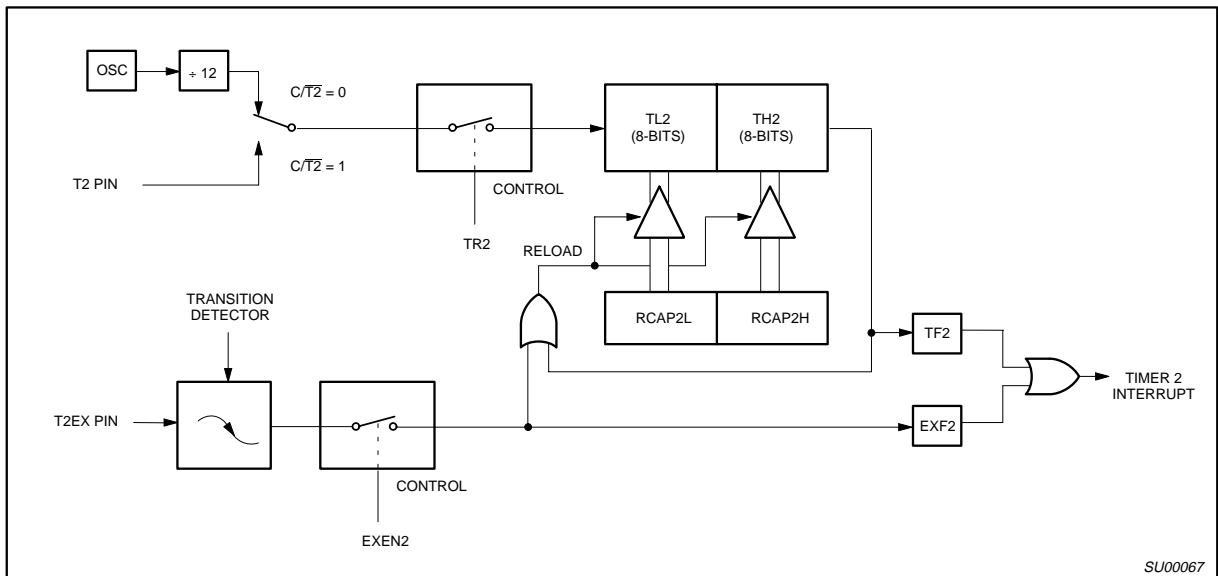


Figure 3. Timer 2 in Auto-Reload Mode



CMOS single-chip 8-bit microcontrollers

80C32/87C52

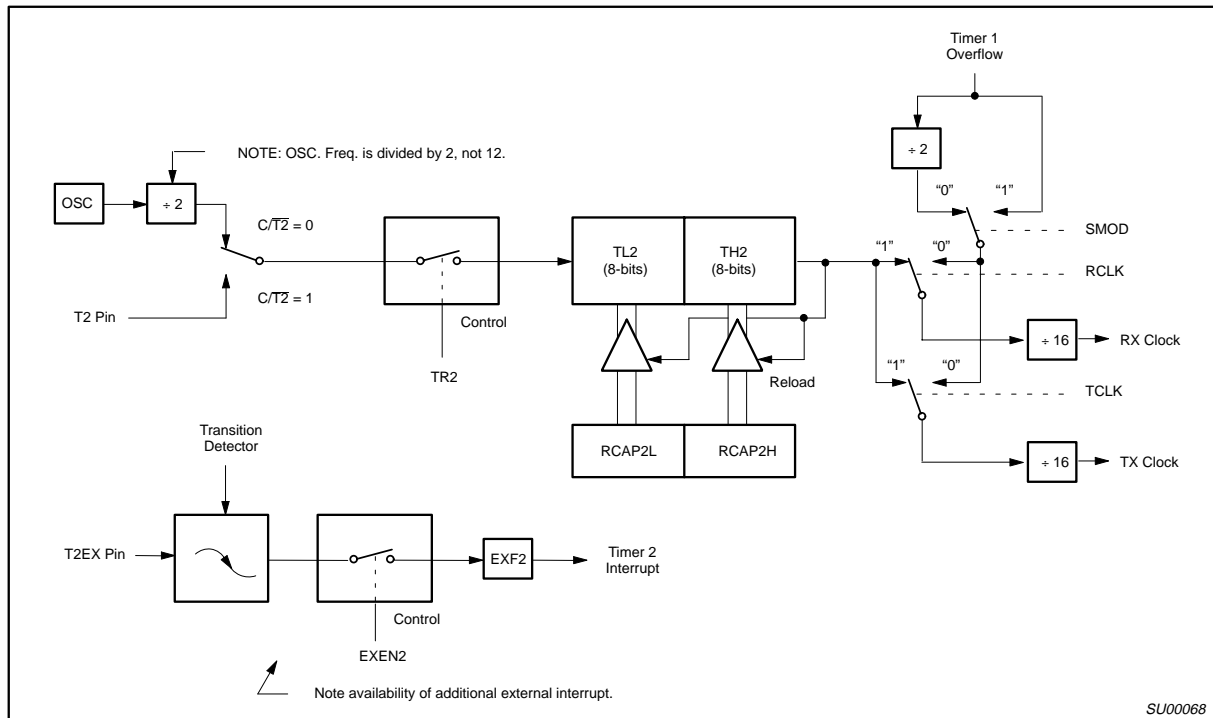


Figure 4. Timer 2 in Baud Rate Generator Mode

Table 2. Timer 2 Operating Modes

RCLK + TCLK	CP/RL2	TR2	MODE
0	0	1	16-bit Auto-reload
0	1	1	16-bit Capture
1	X	1	Baud rate generator
X	X	0	(off)

Timer 2 as a baud rate generator is shown in Figure 4. This figure is valid only if RCLK + TCLK = 1 in T2CON. Note that a rollover in TH2 does not set TF2, and will not generate an interrupt. Therefore, the Timer 2 interrupt does not have to be disabled when Timer 2 is in the baud rate generator mode. Note too, that if EXEN2 is set, a 1-to-0 transition in T2EX will set EXF2 but will not cause a reload from (RCAP2H, RCAP2L) to (TH2, TL2). Thus when Timer 2 is in use as a baud rate generator, T2EX can be used as an extra external interrupt, if desired.

It should be noted that when Timer 2 is running (TR2 = 1) in "timer" function in the baud rate generator mode, one should not try to read or write TH2 or TL2. Under these conditions the timer is being incremented every state time, and the results of a read or write may not be accurate. The RCAP registers may be read, but should not be written to, because a write might overlap a reload and cause write and/or reload errors. Turn the timer off (clear TR2) before accessing the Timer 2 or RCAP registers, in this case.

Timer/Counter 2 Set-up

Except for the baud rate generator mode, the values given for T2CON do not include the setting of the TR2 bit. Therefore, bit TR2 must be set, separately, to turn the timer on. See Table 3 for set-up of timer 2 as a timer. See Table 4 for set-up of timer 2 as a counter.

Using Timer/Counter 2 to Generate Baud Rates

For this purpose, Timer 2 must be used in the baud rate generating mode. If Timer 2 is being clocked through pin T2 (P1.0) the baud rate is:

$$\text{Baud Rate} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

And if it is being clocked internally, the baud rate is:

$$\text{Baud Rate} = \frac{\text{Oscillator Frequency}}{32 \cdot [65536 \cdot (\text{RCAP2H}, \text{RCAP2L})]}$$

To obtain the reload value for RCAP2H and RCAP2L, the above equation can be rewritten as:

$$\text{RCAP2H, RCAP2L} = 65536 \cdot \frac{\text{Oscillator Frequency}}{32 \cdot \text{Baud Rate}}$$



CMOS single-chip 8-bit microcontrollers

80C32/87C52

**Interrupts**

The 80C32/87C52 has 6 interrupt sources. All except TF2 and EXF2 are identical sources to those in the 80C51.

The Interrupt Enable Register and the Interrupt Priority Register are modified to include the additional 80C32/87C52 interrupt sources. The operation of these registers is identical to the 80C51.

In the 80C32/87C52, the Timer 2 Interrupt is generated by the logical OR of TF2 and EXF2. Neither of these flags is cleared by hardware when the service routine is vectored to. In fact, the service routine may have to determine whether it was TF2 or EXF2 that generated the interrupt, and the bit will have to be cleared in software.

All of the bits that generate interrupts can be set or cleared by software, with the same result as though it has been set or cleared

by hardware. That is, interrupts can be generated or pending interrupts can be canceled in software.

The interrupt vector addresses and the interrupt priority for requests in the same priority level are given in the following:

Source	Vector Address	Priority Within Level
1. IE0	0003H	(highest)
2. TF0	000BH	
3. IE1	0013H	
4. TF1	001BH	
5. RI + TI	0023H	
6. TF2 + EXF2	002BH	(lowest)

Note that they are identical to those in the 80C51 except for the addition of the Timer 2 (TF1 and EXF2) interrupt at 002BH and at the lowest priority within a level.

**Table 3. Timer 2 as a Timer**

MODE	T2CON	
	INTERNAL CONTROL (Note 1)	EXTERNAL CONTROL (Note 2)
16-bit Auto-Reload	00H	08H
16-bit Capture	01H	09H
Baud rate generator receive and transmit same baud rate	34H	36H
Receive only	24H	26H
Transmit only	14H	16H

**Table 4. Timer 2 as a Counter**

MODE	TMOD	
	INTERNAL CONTROL (Note 1)	EXTERNAL CONTROL (Note 2)
16-bit	02H	0AH
Auto-Reload	03H	0BH

**NOTES:**

1. Capture/reload occurs only on timer/counter overflow.
2. Capture/reload occurs on timer/counter overflow and a 1-to-0 transition on T2EX (P1.1) pin except when timer 2 is used in the baud rate generator mode.



## CMOS single-chip 8-bit microcontrollers

## 80C32/87C52

**OSCILLATOR CHARACTERISTICS**

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier. The pins can be configured for use as an on-chip oscillator, as shown in the Logic Symbol, page 4.

To drive the device from an external clock source, XTAL1 should be driven while XTAL2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, because the input to the internal clock circuitry is through a divide-by-two flip-flop. However, minimum and maximum high and low times specified in the data sheet must be observed.

**RESET**

A reset is accomplished by holding the RST pin high for at least two machine cycles (24 oscillator periods), while the oscillator is running. To insure a good power-up reset, the RST pin must be high long enough to allow the oscillator time to start up (normally a few milliseconds) plus two machine cycles.

**IDLE MODE**

In idle mode, the CPU puts itself to sleep while all of the on-chip peripherals stay active. The instruction to invoke the idle mode is the last instruction executed in the normal operating mode before the idle mode is activated. The CPU contents, the on-chip RAM, and all

of the special function registers remain intact during this mode. The idle mode can be terminated either by any enabled interrupt (at which time the process is picked up at the interrupt service routine and continued), or by a hardware reset which starts the processor in the same manner as a power-on reset.

**POWER-DOWN MODE**

In the power-down mode, the oscillator is stopped and the instruction to invoke power-down is the last instruction executed. Only the contents of the on-chip RAM are preserved. A hardware reset is the only way to terminate the power-down mode. The control bits for the reduced power modes are in the special function register PCON.

**DESIGN CONSIDERATIONS**

At power-on, the voltage on  $V_{CC}$  and RST must come up at the same time for a proper start-up.

Table 5 shows the state of I/O ports during low current operating modes.

As a precaution to coming out of an unexpected power down,  $INT0$  and  $INT1$  should be disabled prior to entering power down.

**Table 5. External Pin Status During Idle and Power-Down Modes**

MODE	PROGRAM MEMORY	ALE	PSEN	PORT 0	PORT 1	PORT 2	PORT 3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

**μP 80C320**

DS80C320

**DALLAS**  
SEMICONDUCTOR

**DS80C320**  
High-Speed Micro

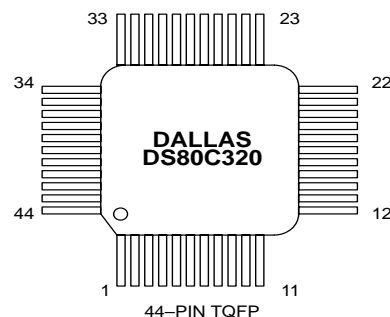
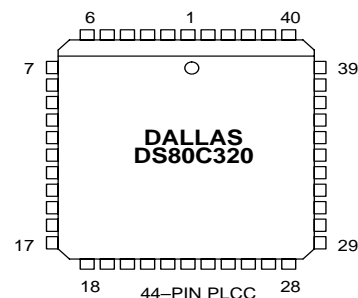
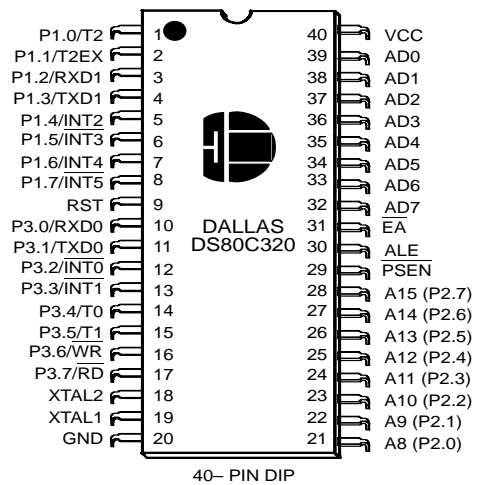
**FEATURES**

- 80C32-Compatible
  - Pin-compatible
  - Standard 8051 instruction set
  - Four 8-bit I/O ports
  - Three 16-bit timer/counters
  - 256 bytes scratchpad RAM
  - Multiplexed address/data bus
  - Addresses 64KB ROM and 64KB RAM
- High-speed architecture
  - 4 clocks/machine cycle (8032=12)
  - Wasted cycles removed
  - Runs DC to 33 MHz clock rates
  - Single-cycle instruction in 121 ns
  - Uses less power for equivalent work
  - Dual data pointer
  - Optional variable length MOVX to access fast/slow RAM /peripherals
- High integration controller includes:
  - Power-fail reset
  - Programmable Watchdog timer
  - Early-warning power-fail interrupt
- Two full-duplex hardware serial ports
- 13 total interrupt sources with six external
- Available in 40-pin DIP, 44-pin PLCC and TQFP

**DESCRIPTION**

The DS80C320 is a fast 80C31/80C32-compatible microcontroller. Wasted clock and memory cycles have been removed using a redesigned processor core. As a result, every 8051 instruction is executed between 1.5 and 3 times faster than the original for the same crystal speed. Typical applications will see a speed improvement of 2.5 times using the same code and same crystal. The DS80C320 offers a maximum crystal rate of 33 MHz, resulting in apparent execution speeds of 82.5 MHz (approximately 2.5X).

**PIN ASSIGNMENT**



Copyright 1995 by Dallas Semiconductor Corporation. All Rights Reserved. For important information regarding patents and other intellectual property rights, please refer to Dallas Semiconductor data books.



The DS80C320 is pin compatible with all three packages of the standard 80C32 and offers the same timer/counters, serial port, and I/O ports. In short, the DS80C320 is extremely familiar to 8051 users but provides the speed of a 16-bit processor.

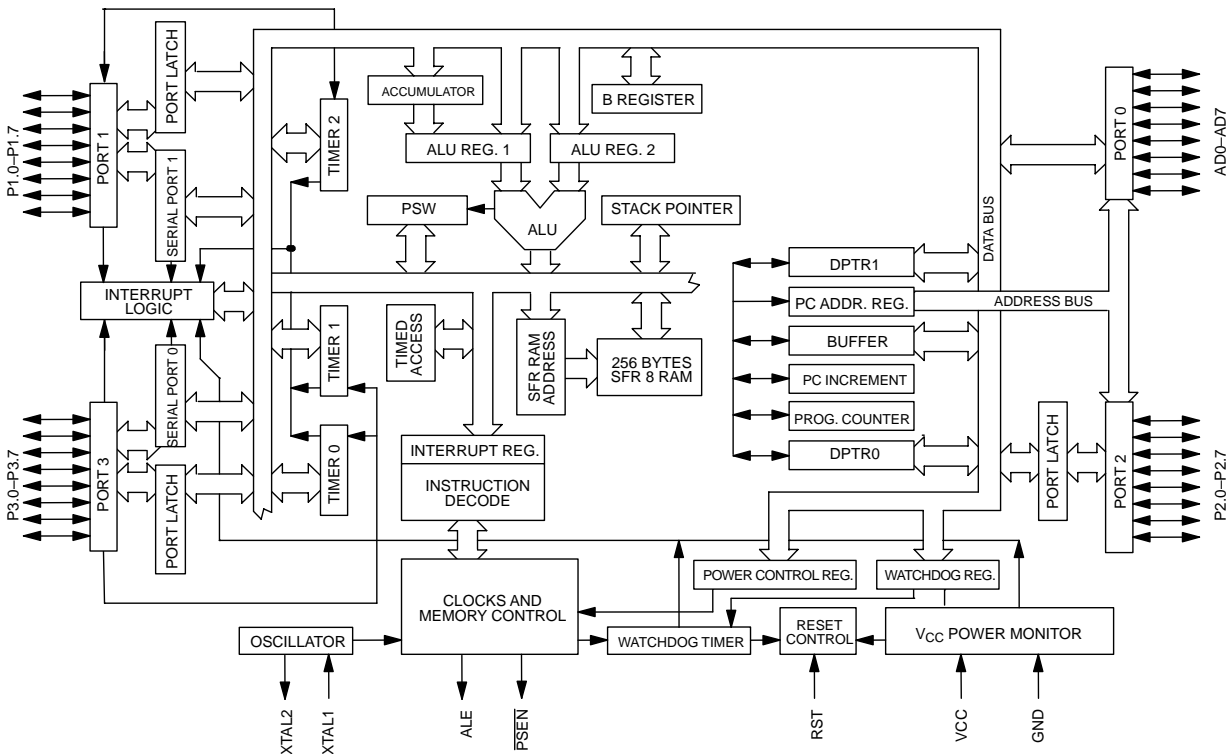
The DS80C320 provides several extras in addition to greater speed. These include a second full hardware

serial port, seven additional interrupts, programmable watchdog timer, power-fail interrupt and reset. The DS80C320 also provides dual data pointers (DPTRs) to speed block data memory moves. It can also adjust the speed of off-chip data memory access to between two and nine machine cycles for flexibility in selecting memory and peripherals.

**ORDERING INFORMATION**

PART NUMBER	PACKAGE	MAX CLOCK SPEED	TEMPERATURE RANGE
DS80C320-MCG	40-pin plastic DIP	25 MHz	0°C to +70°C
DS80C320-QCG	44-pin PLCC	25 MHz	0°C to +70°C
DS80C320-ECG	44-pin TQFP	25 MHz	0°C to +70°C
DS80C320-MNG	40-pin plastic DIP	25 MHz	-40°C to +85°C
DS80C320-QNG	44-pin PLCC	25 MHz	-40°C to +85°C
DS80C320-ENG	44-pin TQFP	25 MHz	-40°C to +85°C
DS80C320-MCL	40-pin plastic DIP	33 MHz	0°C to +70°C
DS80C320-QCL	44-pin PLCC	33 MHz	0°C to +70°C
DS80C320-ECL	44-pin TQFP	33 MHz	0°C to +70°C
DS80C320-MNL	40-pin plastic DIP	33 MHz	-40°C to +85°C
DS80C320-QNL	44-pin PLCC	33 MHz	-40°C to +85°C
DS80C320-ENL	44-pin TQFP	33 MHz	-40°C to +85°C

**DS80C320 BLOCK DIAGRAM** Figure 1





### HIGH-SPEED OPERATION

The DS80C320 is built around a high speed 80C32 compatible core. Higher speed comes not just from increasing the clock frequency, but from a newer, more efficient design.

In this updated core, dummy memory cycles have been eliminated. In a conventional 80C32, machine cycles are generated by dividing the clock frequency by 12. In the DS80C320, the same machine cycle is performed in 4 clocks. Thus the fastest instruction, 1 machine cycle, is executed three times faster for the same crystal frequency. Note that these are identical instructions. A comparison of the timing differences is shown in Figure 2. The majority of instructions on the DS80C320 will see the full 3 to 1 speed improvement. Some instructions will get between 1.5 and 2.4 X improvement. Note that all instructions are faster than the original 80C51. Table 2 below shows a summary of the instruction set including the speed.

The numerical average of all opcodes is approximately a 2.5 to 1 speed improvement. Individual programs will be affected differently, depending on the actual instructions used. Speed sensitive applications would make the most use of instructions that are three times faster. However, the sheer number of 3 to 1 improved opcodes makes dramatic speed improvements likely for any code. When these architecture improvements are combined with 0.8  $\mu\text{m}$  CMOS, the result is a single cycle instruction execution in 160 ns. The Dual Data Pointer feature also allows the user to eliminate wasted instructions when moving blocks of memory.

### INSTRUCTION SET SUMMARY

All instructions in the DS80C320 perform the same functions as their 80C32 counterparts. Their affect on bits, flags, and other status functions is identical. However, the timing of each instruction is different. This applies both in absolute and relative number of clocks.

For absolute timing of real-time events, the timing of software loops will need to be calculated using the table

below. However, counter/timers default to run at the older 12 clocks per increment. Therefore, while software runs at higher speed, timer-based events need no modification to operate as before. Timers can be set to run at 4 clocks per increment cycle to take advantage of higher speed operation.

The relative time of two instructions might be different in the new architecture than it was previously. For example, in the original architecture, the "MOVX A, @DPTR" instruction and the "MOV direct, direct" instruction used two machine cycles or 24 oscillator cycles. Therefore, they required the same amount of time. In the DS80C320, the MOVX instruction can be done in two machine cycles or eight oscillator cycles but the "MOV direct, direct" uses three machine cycles or 12 oscillator cycles. While both are faster than their original counterparts, they now have different execution times from each other. This is because in most cases, the DS80C320 uses one cycle for each byte. The user concerned with precise program timing should examine the timing of each instruction for familiarity with the changes. Note that a machine cycle now requires just four clocks, and provides one ALE pulse per cycle. Many instructions require only one cycle, but some require five. In the original architecture, all were one or two cycles except for MUL and DIV.

### INSTRUCTION SET SUMMARY Table 2

#### Legends:

A	–	Accumulator
Rn	–	Register R7–R0
direct	–	Internal Register address
@Ri	–	Internal Register pointed-to by R0 or R1 (except MOVX)
rel	–	2's complement offset byte
bit	–	direct bit-address
#data	–	8-bit constant
#data 16	–	16-bit constant
addr 16	–	16-bit destination address
addr 11	–	11-bit destination address

INSTRUCTION	BYTE	OSCILLATOR CYCLES	INSTRUCTION	BYTE	OSCILLATOR CYCLES
<b>Arithmetic Instructions:</b>					
ADD A, Rn	1	4	INC A	1	4
ADD A, direct	2	8	INC Rn	1	4
ADD A, @Ri	1	4	INC direct	2	8
ADD A, #data	2	8	INC @Ri	1	4
ADDC A, Rn	1	4	INC DPTR	1	12
ADDC A, direct	2	8	DEC A	1	4
ADDC A, @Ri	1	4	DEC Rn	1	4
ADDC A, #data	2	8	DEC direct	2	8
SUBB A, Rn	1	4	DEC @Ri	1	4
SUBB A, direct	2	8	MUL AB	1	20
SUBB A, @Ri	1	4	DIV AB	1	20
SUBB A, #data	2	8	DA A	1	4
<b>Logical Instructions:</b>					
ANL A, Rn	1	4	XRL A, Rn	1	4
ANL A, direct	2	8	XRL A, direct	2	8
ANL A, @Ri	1	4	XRL A, @Ri	1	4
ANL A, #data	2	8	XRL A, #data	2	8
ANL direct, A	2	8	XRL direct, A	2	8
ANL direct, #data	3	12	XRL direct, #data	3	12
ORL A, Rn	1	4	CLR A	1	4
ORL A, direct	2	8	CPL A	1	4
ORL A, @Ri	1	4	RL A	1	4
ORL A, #data	2	8	RLC A	1	4
ORL direct, A	2	8	RR A	1	4
ORL direct, #data	3	12	RRC A	1	4
			SWAP A	1	4
<b>Data Transfer Instructions:</b>					
MOV A, Rn	1	4	MOVC A, @A+DPTR	1	12
MOV A, direct	2	8	MOVC A, @A+PC	1	12
MOV A, @Ri	1	4	MOVX A, @Ri	1	8-36 *
MOV A, #data	2	8	MOVX A, @DPTR	1	8-36 *
MOV Rn, A	1	4	MOVX @Ri, A	1	8-36 *
MOV Rn, direct	2	8	MOVX @DPTR, A	1	8-36 *
MOV Rn, #data	2	8	PUSH direct	2	8
MOV direct, A	2	8	POP direct	2	8
MOV direct, Rn	2	8	XCH A, Rn	1	4
MOV direct1, direct2	3	12	XCH A, direct	2	8
MOV direct, @Ri	2	8	XCH A, @Ri	1	4
MOV direct, #data	3	12	XCHD A, @Ri	1	4
MOV @Ri, A	1	4			
MOV @Ri, direct	2	8			
MOV @Ri, #data	2	8			
MOV DPTR, #data 16	3	12			

\*User Selectable

**Bit Manipulation**

**Instructions:**

CLR C	1	4	ANL C, bit	2	8
CLR bit	2	8	ANL C, $\overline{\text{bit}}$	2	8
SETB C	1	4	ORL C, bit	2	8
SETB bit	2	8	ORL C, $\overline{\text{bit}}$	2	8
CPL C	1	4	MOV C, bit	2	8
CPL bit	2	8	MOV bit, C	2	8

**Program Branching**

**Instructions:**

ACALL addr 11	2	12	CJNE A, direct, rel	3	16
LCALL addr 16	3	16	CJNE A, #data, rel	3	16
RET	1	16	CJNE Rn, #data, rel	3	16
RETI	1	16	CJNE Ri, #data, rel	3	16
AJMP addr 11	2	12	NOP	1	4
LJMP addr 16	3	16	JC rel	2	12
SJMP rel	2	12	JNC rel	2	12
JMP @A+DPTR	1	12	JB bit, rel	3	16
JZ rel	2	12	JNB bit, rel	3	16
JNZ rel	2	12	JBC bit, rel	3	16
DJNZ Rn, rel	2	12			
DJNZ direct, rel	3	16			

The table above shows the speed for each class of instruction. Note that many of the instructions have multiple opcodes. There are 255 opcodes for 111 instructions. Of the 255 opcodes, 159 are three times faster than the original 80C32. While a system that emphasizes those instructions will see the most improvement, the large total number that receive a 3 to 1 improvement assure a dramatic speed increase for any system. The speed improvement summary is provided below.

**SPEED ADVANTAGE SUMMARY**

#Opcodes	Speed Improvement
159	3.0 x
51	1.5 x
43	2.0 x
<u>2</u>	<u>2.4 x</u>
255	Average: 2.5

**MEMORY ACCESS**

The DS80C320 contains no on-chip ROM and 256 bytes of scratchpad RAM. Off-chip memory is accessed using the multiplexed address/data bus on P0 and the MSB address on P2. A typical memory connection is shown in Figure 3. Timing diagrams are provided in the Electrical Specifications. Program memory (ROM) is accessed at a fixed rate determined by the crystal frequency and the actual instructions. As mentioned above, an instruction cycle requires four clocks. Data memory (RAM) is accessed according to a variable speed MOVX instruction as described below.



**DATA MEMORY CYCLE STRETCH VALUES** Table 3

CKCON.2-0			MEMORY CYCLES	$\overline{RD}$ or $\overline{WR}$ STROBE WIDTH IN CLOCKS	STROBE WIDTH TIME @ 25 MHz
MD2	MD1	MD0			
0	0	0	2	2	80 ns
0	0	1	3 (default)	4	160 ns
0	1	0	4	8	320 ns
0	1	1	5	12	480 ns
1	0	0	6	16	640 ns
1	0	1	7	20	800 ns
1	1	0	8	24	960 ns
1	1	1	9	28	1120 ns

**DUAL DATA POINTER**

Data memory block moves can be accelerated using the DS80C320 Dual Data Pointer (DPTR). The standard 8032 DPTR is a 16-bit value that is used to address off-chip data RAM or peripherals. In the DS80C320, the standard data pointer is called DPTR 0 and is located at SFR addresses 82h and 83h. These are the standard locations. No modification of standard code is needed to use DPTR. The new DPTR is located at SFR 84h and 85h and is called DPTR1. The DPTR Select bit (DPS) chooses the active pointer and is located at the LSB of the SFR location 86h. No other bits in register 86h have any effect and are set to 0. The user switches between data pointers by toggling the LSB of register 86h. The increment (INC) instruction is the fastest way to accomplish this. All DPTR-related instructions use the currently selected DPTR for any activity. Therefore only one instruction is required to switch from a source to a destination address. Using the Dual-Data Pointer saves code from needing to save source and destination addresses when doing a block move. Once

loaded, the software simply switches between DPTR and 1. The relevant register locations are as follows.

DPL	82h	Low byte original DPTR
DPH	83h	High byte original DPTR
DPL1	84h	Low byte new DPTR
DPH1	85h	High byte new DPTR
DPS	86h	DPTR Select (LSB)

Sample code listed below illustrates the saving from using the dual DPTR. The example program was original code written for an 8051 and requires a total of 1869 machine cycles on the DS80C320. This takes 299  $\mu$ s to execute at 25 MHz. The new code using the Dual DPTR requires only 1097 machine cycles taking 175.5  $\mu$ s. The Dual DPTR saves 772 machine cycles or 123.5  $\mu$ s for a 64 byte block move. Since each pass through the loop saves 12 machine cycles when compared to the single DPTR approach, larger blocks gain more efficiency using this feature.

**64 BYTE BLOCK MOVE WITHOUT DUAL DATA POINTER**

; SH and SL are high and low byte source address.  
; DH and DL are high and low byte of destination address.

# CYCLES

```

MOV     R5, #64d      ; NUMBER OF BYTES TO MOVE          2
MOV     DPTR, #SHSL   ; LOAD SOURCE ADDRESS          3
MOV     R1, #SL       ; SAVE LOW BYTE OF SOURCE        2
MOV     R2, #SH       ; SAVE HIGH BYTE OF SOURCE        2
MOV     R3, #DL       ; SAVE LOW BYTE OF DESTINATION    2
MOV     R4, #DH       ; SAVE HIGH BYTE OF DESTINATION    2
    
```

MOVE:

; THIS LOOP IS PERFORMED THE NUMBER OF TIMES LOADED INTO R5, IN THIS EXAMPLE 64

```

MOVX   A, @DPTR      ; READ SOURCE DATA BYTE          2
MOV     R1, DPL       ; SAVE NEW SOURCE POINTER        2
MOV     R2, DPH       ;                               2
    
```

```

MOV     DPL, R3           ; LOAD NEW DESTINATION                2
MOV     DPH, R4           ;                                  2
MOVX    @DPTR, A          ; WRITE DATA TO DESTINATION        2
INC     DPTR              ; NEXT DESTINATION ADDRESS          3
MOV     R3, DPL           ; SAVE NEW DESTINATION POINTER      2
MOV     R4, DPH           ;                                  2
MOV     DPL, R1           ; GET NEW SOURCE POINTER        2
MOV     DPH, R2           ;                                  2
INC     DPTR              ; NEXT SOURCE ADDRESS              3
DJNZ    R5, MOVE         ; FINISHED WITH TABLE?              3

```

#### 64 BYTE BLOCK MOVE WITH DUAL DATA POINTER

```

; SH and SL are high and low byte source address.
; DH and DL are high and low byte of destination address.
; DPS is the data pointer select. Reset condition is DPS=0, DPTR0 is selected.
# CYCLES

```

```

EQU     DPS, #86h        ; TELL ASSEMBLER ABOUT DPS

MOV     R5, #64          ; NUMBER OF BYTES TO MOVE                2
MOV     DPTR, #DHDL     ; LOAD DESTINATION ADDRESS              3
INC     DPS              ; CHANGE ACTIVE DPTR                            2
MOV     DPTR, #SHSL     ; LOAD SOURCE ADDRESS                  2

```

MOVE:

```

; THIS LOOP IS PERFORMED THE NUMBER OF TIMES LOADED INTO R5, IN THIS EXAMPLE 64

```

```

MOVX    A, @DPTR        ; READ SOURCE DATA BYTE                2
INC     DPS              ; CHANGE DPTR TO DESTINATION                2
MOVX    @DPTR, A        ; WRITE DATA TO DESTINATION            2
INC     DPTR            ; NEXT DESTINATION ADDRESS                  3
INC     DPS              ; CHANGE DATA POINTER TO SOURCE            2
INC     DPTR            ; NEXT SOURCE ADDRESS                      3
DJNZ    R5, MOVE        ; FINISHED WITH TABLE?                    3

```

#### PERIPHERAL OVERVIEW

Peripherals in the DS80C320 are accessed using Special Function Registers (SFRs). The DS80C320 provides several of the most commonly needed peripheral functions in microcomputer-based systems. These functions are new to the 80C32 family and include a second serial port, Power-fail Reset, Power-fail Interrupt, and a programmable Watchdog Timer. These are described below, and more details are available in the High-Speed Microcontroller User's Guide.

The second serial port operates in a comparable manner with the first. Both can operate simultaneously but can be at different baud rates.

The second serial port has similar control registers (SCON1 at C0h, SBUF1 at C1h) to the original. One difference is that for timer based baud rates, the original serial port can use Timer 1 or Timer 2 to generate baud rates. This is selected via SFR bits. The new serial port can only use Timer 1.

#### SERIAL PORTS

The DS80C320 provides a serial port (UART) that is identical to the 80C32. Many applications require serial communication with multiple devices. Therefore the DS80C320 provides a second hardware serial port that is a full duplicate of the standard one. It optionally uses pins P1.2 (RXD1) and P1.3 (TXD1). This port has duplicate control functions included in new SFR locations.

#### TIMER RATE CONTROL

One important difference exists between the DS80C320 and 80C32 regarding timers. The original 80C32 used a 12 clock per cycle scheme for timers and consequently for some serial baud rates (depending on the mode). The DS80C320 architecture normally runs using 4 clocks per cycle. However, in the area of timers, the DS80C320 will default to a 12 clock per cycle

scheme on a reset. This allows existing code with real-time dependencies such as baud rates to operate properly. If an application needs higher speed timers or serial baud rates, the timers can be set to run at the 4 clock rate.

The Clock Control register (CKCON – 8Eh) determines these timer speeds. When the relevant CKCON bit is a logic 1, the DS80C320 uses 4 clocks per cycle to generate timer speeds. When the control bit is set to a 0, the DS80C320 uses 12 clocks for timer speeds. The reset condition is a 0. CKCON.5 selects the speed of Timer 2. CKCON.4 selects Timer 1 and CKCON.3 selects Timer 0. Note that unless a user desires very fast timing, it is unnecessary to alter these bits. Note that the timer controls are independent.

### POWER FAIL RESET

The DS80C320 incorporates a precision band-gap voltage reference to determine when  $V_{CC}$  is out-of-tolerance. While powering up, internal circuits will hold the DS80C320 in a reset state until  $V_{CC}$  rises above the  $V_{RST}$  reset threshold. Once  $V_{CC}$  is above this level, the oscillator will begin running. An internal reset circuit will then count 65536 clocks to allow time for power and the oscillator to stabilize. The microcontroller will then exit the reset condition. No external components are needed to generate a power on reset. During power down or during a severe power glitch, as  $V_{CC}$  falls below  $V_{RST}$ , the microcontroller will also generate its own reset. It will hold the reset condition as long as power remains below the threshold. This reset will occur automatically, needing no action from the user or from the software. Refer to the Electrical Specifications for the exact value of  $V_{RST}$ .

### POWER FAIL INTERRUPT

The same reference that generates a precision reset threshold can also generate an optional early warning

Power-fail Interrupt (PFI). When enabled by the application software, this interrupt always has the highest priority. On detecting that the  $V_{CC}$  has dropped below  $V_{PFW}$  and that the PFI is enabled, the processor will vector to ROM address 0033h. The PFI enable is located in the Watchdog Control SFR (WDCON – D8h). Setting WDCON.5 to a logic one will enable the PFI. The application software can also read a flag at WDCON.4. This bit is set when a PFI condition has occurred. The flag is independent of the interrupt enable and software must manually clear it.

### WATCHDOG TIMER

For applications that can not afford to run out-of-control, the DS80C320 incorporates a programmable Watchdog Timer circuit. It resets the uC if software fails to reset the Watchdog before the selected time interval has elapsed. The user selects one of four time-out values. After enabling the Watchdog, software must reset the timer prior to expiration of the interval, or the CPU will be reset. Both the Watchdog Enable and the Watchdog Reset bits are protected by a “Timed Access” circuit. This prevents accidentally clearing the Watchdog. Time-out values are precise since they are related to the crystal frequency as shown below in Table 4. For reference, the time periods at 25 MHz are also shown.

The DS80C320 Watchdog also provides a useful option for systems that may not require a reset. If enabled, then 512 clocks before giving a reset, the Watchdog will give an interrupt. The interrupt can also serve as a convenient time-base generator, or be used to wake-up the processor from Idle mode. The Watchdog function is controlled in the Clock Control (CKCON – 8Eh), Watchdog Control (WDCON – D8h), and Extended Interrupt Enable (EIE – E8h) SFRs. CKCON.7 and CKCON.6 are called WD1 and WD0 respectively and are used to select the Watchdog time-out period as shown in Table 4.

**WATCHDOG TIME-OUT VALUES** Table 4

WD1	WD0	INTERRUPT TIME-OUT	TIME (@ 25 MHz)	RESET TIME-OUT	TIME (@ 25 MHz)
0	0	$2^{17}$ clocks	5.243 ms	$2^{17} + 512$ clocks	5.263 ms
0	1	$2^{20}$ clocks	41.94 ms	$2^{20} + 512$ clocks	41.96 ms
1	0	$2^{23}$ clocks	335.54 ms	$2^{23} + 512$ clocks	335.56 ms
1	1	$2^{26}$ clocks	2684.35 ms	$2^{26} + 512$ clocks	2684.38 ms

As shown above, the Watchdog Timer uses the crystal frequency as a time base. A user selects one of four counter values to determine the time-out. These clock counter lengths are  $2^{17} = 131,072$  clocks;  $2^{20} = 1,048,576$ ;  $2^{23} = 8,388,608$  clocks; or  $2^{26} = 67,108,864$  clocks. The times shown in Table 4 above are with a 25 MHz crystal frequency. Note that once the counter chain has reached a conclusion, the optional interrupt is generated. Regardless of whether the user enables this interrupt, there are then 512 clocks left until a reset occurs. There are five control bits in special function registers that affect the Watchdog Timer and two status flags that report to the user.

WDIF (WDCON.3) is the interrupt flag that is set when there are 512 clocks remaining until a reset occurs. WTRF (WDCON.2) is the flag that is set when a Watchdog reset has occurred. This allows the application software to determine the source of a reset.

EWT (WDCON.1) is the enable for the Watchdog Timer. Software sets this bit to enable the timer. The bit is pro-

ected by Timed Access discussed below. RWT (WDCON.0) is the bit that software uses to restart the Watchdog Timer. Setting this bit restarts the timer for another full interval. Application software must set this bit prior to the time-out. As mentioned previously, WD1 and 0 (CKCON .7 and 6) select the time-out. Finally, the Watchdog Interrupt is enabled using EWDI (EIE.4). The Special Function Register map is shown below.

**INTERRUPTS**

The DS80C320 provides 13 sources of interrupt with three priority levels. The Power-fail Interrupt (PFI), if enabled, always has the highest priority. There are two remaining user selectable priorities: high and low. If two interrupts that have the same priority occur simultaneously, the natural precedence given below determines which is acted upon. Except for the PFI, all interrupts that are new to the 8051 family have a lower natural priority than the originals.

**INTERRUPT PRIORITY Table 5**

NAME	DESCRIPTION	VECTOR	NATURAL PRIORITY	OLD/NEW
PFI	Power Fail Interrupt	33h	1	NEW
INT0	External Interrupt 0	03h	2	OLD
TF0	Timer 0	0Bh	3	OLD
INT1	External Interrupt 1	13h	4	OLD
TF1	Timer 1	1Bh	5	OLD
SCON0	TI0 or RI0 from serial port 0	23h	6	OLD
TF2	Timer 2	2Bh	7	OLD
SCON1	TI1 or RI1 from serial port 1	3Bh	8	NEW
INT2	External Interrupt 2	43h	9	NEW
INT3	External Interrupt 3	4Bh	10	NEW
INT4	External Interrupt 4	53h	11	NEW
INT5	External Interrupt 5	5Bh	12	NEW
WDTI	Watchdog Time-out Interrupt	63h	13	NEW

**POWER MANAGEMENT**

The DS80C320 provides the standard Idle and power down (Stop) that are available on the standard 80C32. However the DS80C320 has enhancements that make these modes more useful, and allow more power saving.

The Idle mode is invoked by setting the LSB of the Power Control register (PCON – 87h). Idle will leave internal clocks, serial port and timer running. No memory access will be performed so power is dramati-

cally reduced. Since clocks are running, the Idle power consumption is related to crystal frequency. It should be approximately 1/2 of the operational power. The CPU can exit the Idle state with any interrupt or a reset.

The power-down or Stop mode is invoked by setting the PCON.1 bit. Stop mode is a lower power state than Idle since it turns off all internal clocking. The I<sub>CC</sub> of a standard Stop mode is approximately 1 μA but is specified in the Electrical Specifications. The CPU will exit Stop mode from an external interrupt or a reset condition.



Note that internally generated interrupts (timer, serial port, watchdog) are not useful since they require clocking activity.

### IDLE MODE ENHANCEMENTS

A simple enhancement to Idle mode makes it substantially more useful. The innovation involves not the Idle mode itself, but the watchdog timer. As mentioned above, the Watchdog Timer provides an optional interrupt capability. This interrupt can provide a periodic interval timer to bring the DS80C320 out of Idle mode. This can be useful even if the Watchdog is not normally used. By enabling the Watchdog Timer and its interrupt prior to invoking Idle, a user can periodically come out of Idle perform an operation, then return to Idle until the next operation. This will lower the overall power consumption. When using the Watchdog Interrupt to cancel the Idle state, make sure to restart the Watchdog Timer or it will cause a reset.

### STOP MODE ENHANCEMENTS

The DS80C320 provides two enhancements to the Stop mode. As documented above, the DS80C320 provides a band-gap reference to determine Power-fail Interrupt and Reset thresholds. The default state is that the band-gap reference is off when Stop mode is invoked. This allows the extremely low power state mentioned above. A user can optionally choose to have the band-gap enabled during Stop mode. This means that PFI and power-fail reset will be activated and are valid means for leaving Stop mode.

In Stop mode with the band-gap on,  $I_{CC}$  will be approximately 50  $\mu$ A compared with 1  $\mu$ A with the band-gap off. If a user does not require a Power-fail Reset or Interrupt while in Stop mode, the band-gap can remain turned off. Note that only the most power sensitive applications should turn off the band-gap, as this results in an uncontrolled power down condition.

The control of the band-gap reference is located in the Extended Interrupt Flag register (EXIF – 91h). Setting BGS (EXIF.0) to a one will leave the band-gap reference enabled during Stop mode. The default or reset condition is with the bit at a logic 0. This results in the band-gap being turned off during Stop mode. Note that

this bit has no control of the reference during full power or Idle modes.

The second feature allows an additional power saving option. This is the ability to start instantly when exiting Stop mode. It is accomplished using an internal ring oscillator that can be used when exiting Stop mode in response to an interrupt. The benefit of the ring oscillator is as follows.

Using Stop mode turns off the crystal oscillator and all internal clocks to save power. This requires that the oscillator be restarted when exiting Stop mode. Actual start-up time is crystal dependent, but is normally at least 4 ms. A common recommendation is 10 ms. In an application that will wake-up, perform a short operation, then return to sleep, the crystal start-up can be longer than the real transaction. However, the ring oscillator will start instantly. The user can perform a simple operation and return to sleep before the crystal has even stabilized. If the ring is used to start and the processor remains running, hardware will automatically switch to the crystal once a power-on reset interval (65536 clocks) has expired. This value is used to guarantee stability even though power is not being cycled.

If the user returns to Stop mode prior to switching of crystal, then all clocks will be turned off again. The ring oscillator runs at approximately 4 MHz but will not be a precision value. No real-time precision operations (including serial communication) should be conducted during this ring period. Figure 7 shows how the operation would compare when using the ring, and when starting up normally. The default state is to come out of Stop mode without using the ring oscillator.

This function is controlled using the RGSL – Ring Select bit at EXIF.1 (EXIF – 91h). When EXIF.1 is set, the ring oscillator will be used to come out of Stop mode quickly. As mentioned above, the processor will automatically switch from the ring (if enabled) to the crystal after a delay of 65536 crystal clocks. For a 3.57 MHz crystal, this is approximately 18 ms. The processor sets a flag called RGMD – Ring Mode to tell software that the ring is being used. This bit at EXIF.2 will be a logic 1 when the ring is in use. No serial communication or precision timing should be attempted while this bit is set, since the operating frequency is not precise.



**RING OSCILLATOR START-UP Figure 4**

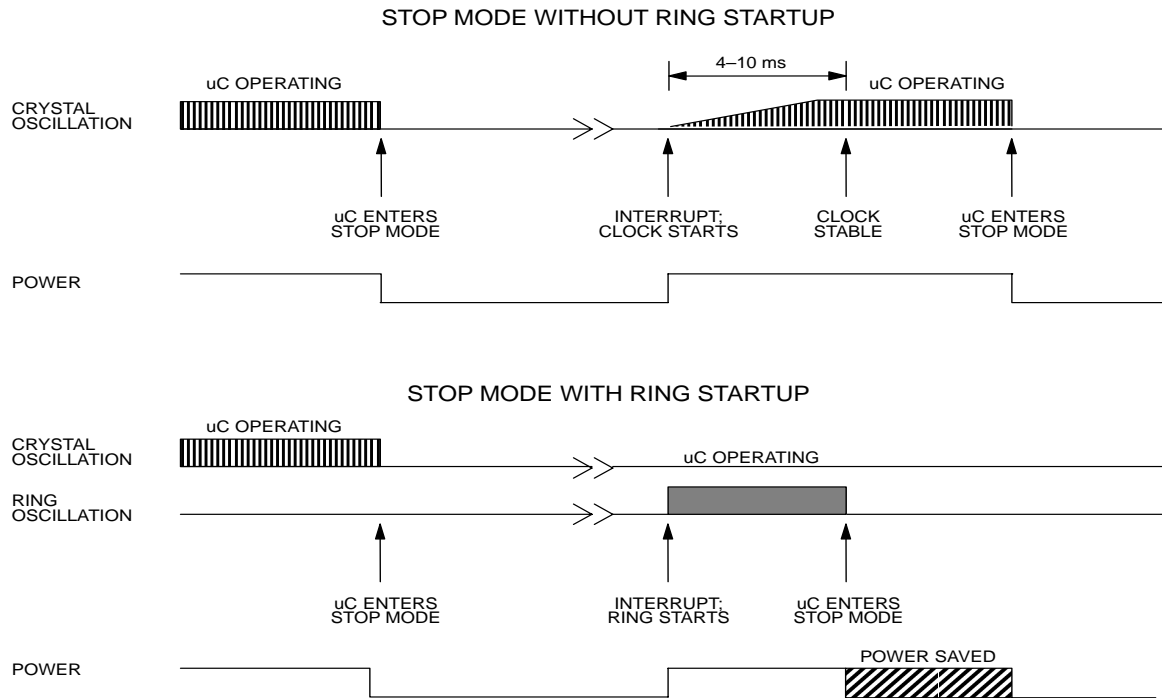


Diagram assumes that the operation following Stop requires less than 18 ms complete.

**TIMED ACCESS PROTECTION**

Selected SFR bits are critical to operation, making it desirable to protect against an accidental write operation. The Timed Access procedure prevents an errant cpu from accidentally altering a bit that would cause difficulty. The Timed Access procedure requires that the write of a protected bit be preceded by the following instructions :

```
MOV    0C7h, #0AAh
MOV    0C7h, #55h
```

By writing an AAh followed by a 55h to the Timed Access register (location C7h), the hardware opens a two cycle window that allows software to modify one of the protected bits. If the instruction that seeks to modify the protected bit is not immediately preceded by these instructions, the write will not take effect. The protected bits are:

- |         |                              |
|---------|------------------------------|
| EXIF.0  | BGS Band-gap Select          |
| WDCON.6 | POR Power-on Reset flag      |
| WDCON.1 | EWT Enable Watchdog          |
| WDCON.0 | RWT Reset Watchdog           |
| WDCON.3 | WDIF Watchdog Interrupt Flag |

**SPECIAL FUNCTION REGISTERS**

Most special features of the DS80C320 or 80C32 are controlled by bits in special function registers (SFRs). This allows the DS80C320 to add many features but use the same instruction set. When writing software to use a new feature, the SFR must be defined to an assembler or compiler using an equate statement. This is the only change needed to access the new function. The DS80C320 duplicates the SFRs that are contained in the standard 80C32. Table 6 shows the register addresses and bit locations. Many are standard 80C32 registers. The High-Speed Microcontroller User's Guide describes all SFRs.



**SPECIAL FUNCTION REGISTER LOCATIONS** Table 6

REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	ADDRESS
SP									81h
DPL									82h
DPH									83h
DPL1									84h
DPH1									85h
DPS	0	0	0	0	0	0	0	SEL	86h
PCON	SMOD_0	SMOD0	–	–	GF1	GF0	STOP	IDLE	87h
TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	88h
TMOD	GATE	C/T	M1	M0	GATE	C/T	M1	M0	89h
TL0									8Ah
TL1									8Bh
TH0									8Ch
TH1									8Dh
CKCON	WD1	WD0	T2M	T1M	T0M	MD2	MD1	MD0	8Eh
P1	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0	90h
EXIF	IE5	IE4	IE3	IE2	–	RGMD	RGSL	BGS	91h
SCON0	SM0/FE_0	SM1_0	SM2_0	REN_0	TB8_0	RB8_0	TI_0	RI_0	98h
SBUF0									99h
P2	P2.0	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0	A0h
IE	EA	ES1	ET2	ES0	ET1	EX1	ET0	EX0	A8h
SADDR0									A9h
SADDR1									AAh
P3	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0	B0h
IP	–	PS1	PT2	PS0	PT1	PX1	PT0	PX0	B8h
SADEN0									B9h
SADEN1									BAh
SCON1	SM0/FE_0	SM1_0	SM2_0	REN_0	TB8_0	RB8_0	TI_0	RI_0	C0h
SBUF1									C1h
STATUS	PIP	HIP	LIP	1	1	1	1	1	C5h
TA									C7h
T2CON	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2	C8h
T2MOD	–	–	–	–	–	–	T2OE	DCEN	C9h
RCAP2L									CAh
RCAP2H									CBh
TL2									CCh
TH2									CDh
PSW	CY	AC	F0	RS1	RS0	OV	FL	P	D0h
WDCON	SMOD_1	POR	EPFI	PFI	WDIF	WTRF	EWT	RWT	D8h
ACC									E0h
EIE	–	–	–	EWDI	EX5	EX4	EX3	EX2	E8h
B									F0h
EIP	–	–	–	PWDI	PX5	PX4	PX3	PX2	F8h

## APPENDIX C: ALPHETICAL INDEX

**SYMBOLS**

80C32 2, 3, 4  
80C320 2, 3, 4

**A**

A/D 2, 8, 10, 18, 28, 31, 41, 49  
A/D CONVERSION TIME 10  
A/D RESOLUTION 10  
**ABACO® BLOCK** 2  
**ABACO® I/O BUS** 2, 9, 41  
ACTIVITY LED 46  
ADDRESSES 41  
ANALOG INPUT 30  
ANALOG INPUTS CURRENT 11  
ANALOG INPUTS IMPEDANCE 11  
ANALOG INPUTS VOLTAGE 11

**B**

BACK UP 2, 27, 37  
BACK UP CURRENT 11  
BACKED RAM 48  
BATTERY 2, 11, 27, 37  
BOARD CONFIGURATION 8  
BOARD RESOURCES 10  
BT1 37  
BUZZER 2, 8, 47

**C**

CLOCK 3  
CLOCK FREQUENCY 10  
COMPILER 2  
CONNECTIONS 12  
CONNECTORS 10  
  CN1 10, 13, 29  
  CN2 10, 27  
  CN3A 10, 20, 29  
  CN3B 10, 26, 29  
  CN4 10, 12, 29  
  CN6 10, 18  
  CN7 10, 14  
  CN8 10, 16  
CONSUMPTION ON 5 VDC 11

CPU 2  
CURRENT LOOP 2, 4, 20, 28, 37, 38  
CURRENT PROVIDED ON +5 VDC 11

## D

DIP SWITCH 29, 46  
DSW1 29, 41, 46

## E

EEPROM 2, 6, 10, 39, 41  
ELECTRIC FEATURES 11  
EPROM 2, 6, 10, 41  
EXTERNAL DEVICES FOR GPC® 323 50  
EXTERNAL WATCHDOG 46

## G

GENERAL FEATURES 10

## H

HARDWARE 41

## I

I/O 2  
I/O ADDRESSES 42  
I/O CONNECTION 28  
IDLE MODE 2  
INSTALLATION 12  
INTERNAL WATCH DOG 49  
INTERRUPTS MANAGEMENT 30

## J

JEDEC 39  
JUMPERS 32  
    2 PINS 34  
    3 PINS 36  
    6 PINS 37

## L

LD4BZ 46, 47  
LEDS 2, 28  
LITHIUM 2

**M**

MEMORY ADDRESSES	42
MEMORY CONFIGURATION	43
MEMORY CONFIGURATION 1	43
MEMORY CONFIGURATION 3	44
MEMORY CONFIGURATION 4	45
MEMORY DEVICES	6
MEMORY SELECTION	39

**N**

NOTE	37
------	----

**O**

ON BOARD PERIPHERAL DEVICES	8
OPERATOR INTERFACES	27

**P**

PDA	47
PDB	47
PDC	47
PERIPHERAL DEVICES SOFTWARE DESCRIPTION	46
POWER DOWN MODE	2
POWER SUPPLY	4, 11
POWER SUPPLY	12, 29
PPI 82C55	14, 16, 47

**R**

RAM	2, 6, 27, 39, 41, 48
REAL TIME CLOCK	8, 10, 27
REATIVE HUMIDITY	11
RESET KEY	9, 28
RS 232	2, 4, 20, 26, 28, 37, 38
RS 422	2, 28, 37, 38
RS 422-485	4, 20
RS 422-485 COMMUNICATION DIRECTION	48
RS 422-485 TERMINATION NET	11
RS 485	2, 28, 37, 38
RTC	2, 37, 39, 41, 48
RUN/DEBUG	46

**S**

SERIAL COMMUNICATION TYPE SELECTION	37
SERIAL EEPROM	2, 8, 10, 48
SERIAL LINE A	20

SERIAL LINE B 26  
SERIAL LINES 49  
SERIAL RTC 48  
SIZE 10  
SOFTWARE 2, 40  
SPOT LED 47

**T**

TECHNICAL FEATURES 10  
TEMPERATURE RANGE 10  
TEST POINT 29  
TIMER COUNTER 49  
TP1 29  
TRANSZORB™ 2

**V**

VISUAL FEEDBACK 28  
VREF 29, 31

**W**

WATCHDOG 2, 8  
WATCHDOG INTERVENT TIME 11