GPC® 184

General Purpose Controller Z180

TECHNICAL MANUAL

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Intelligent Module **Abaco**® **BLOCK**, **Serie 4**, size 100x50 mm; Optional container, format **DIN 46277-1 and 3** rails compliant; **CPU Z180**, with **18,432 MHz** quartz; **Configuration Jumper** used to select **RUN/DEBUG** mode; Up to **512K** of **EPROM** or **FLASH** and up to **512K** of **RAM**; **Real Time Clock** capable to generate **INT**errupts; **Back Up** circuitry for RAM and RTC, through on-board **LITHIUM** battery or external battery; Clocked Serial I/O interface, available to the User, on the I/O connetor; **2** internal 16 bits wide Programmable Reload **Timer** channels; 2 **RS232** serial lines, one of which settable as **RS422**, **RS485** or **Current Loop**; double **Baud Rate** generator, software programmable; **Watch Dog** circuitery, hardware manageable; **Abaco**® **I/O BUS** da 26 pins expansion connector; **4** different power saving modes: **Halt**,**STOP**, **Sleep** and **System Stop**; **Power Failure** circuitry capable to generate interrupts; Consumption extermy reduced: only as low as **60 mA** on **5Vdc**; on-board logic protected against transients by **TransZorb™;** Wide range of development software available such as **Remote Symbolic Debugger**; **Macro Assembler**; **GET 80**; **C compilers** (**HI TECH C 80**, **DDS MICRO C 85**); **PASCAL compilers** (**PASCAL 80**, **EMBEDDED PASCAL**); **FGDOS184**; etc.

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IMPORTANT

SYMBOLS DESCRIPTION

In the manual could appear the following symbols:
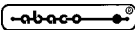
Attention: Generic danger

Attention: High voltage

Trade Marks

GENERAL INDEX

FIGURES INDEX

INTRODUCTION

The use of these devices has turned - IN EXCLUSIVE WAY - to specialized personnel.

The purpose of this handbook is to give the necessary information to the cognizant and sure use of the products. They are the result of a continual and systematic elaboration of data and technical tests saved and validated from the manufacturer, related to the inside modes of certainty and quality of the information.

The reported data are destined- IN EXCLUSIVE WAY- to specialized users, that can interact with the devices in safety conditions for the persons, for the machine and for the enviroment, impersonating an elementary diagnostic of breakdowns and of malfunction conditions by performing simple functional verify operations , in the height respect of the actual safety and health norms.

The informations for the installation, the assemblage, the dismantlement, the handling, the adjustment, the reparation and the contingent accessories, devices etc. installation are destined - and then executable - always and in exclusive way from specialized warned and educated personnel, or directly from the TECHNICAL AUTHORIZED ASSISTANCE, in the height respect of the manufacturer recommendations and the actual safety and health norms.

The devices can't be used outside a box. The user must always insert the cards in a container that rispect the actual safety normative. The protection of this container is not threshold to the only atmospheric agents, but specially to mechanic, electric, magnetic, etc. ones.

To be on good terms with the products, is necessary guarantee legibility and conservation of the manual, also for future references. In case of deterioration or more easily for technical updates, consult the AUTHORIZED TECHNICAL ASSISTANCE directly.

To prevent problems during card utilization, it is a good practice to read carefully all the informations of this manual. After this reading, the user can use the general index and the alphabetical index, respectly at the begining and at the end of the manual, to find information in a faster and more easy way.

CARD VERSION

The present handbook is reported to the **GPC® 184** card release **100997** and later. The validity of the bring informations is subordinate to the number of the card release. The user must always verify the correct correspondence among the two denotations. On the card the release number is present in more points both board printed diagram (serigraph) and printed circuit (for example between the CPU an the memoriey devices on the component side).

GENERAL FEATURES

GPC® 184 board is a powerful control **low cost** module capable of operating in stand alone mode or as an intelligent peripheral, and/or remoted, in a wider telecontrol or aquisition network. It is part of the CPU **Serie 4**, in **BLOCK** format, as low as 100x50 mm size.

The **GPC® 114** module can be secured in a plastic mount for connection to **Omega** rails **DIN 46277-1** and **DIN 46277-3**, thereby dispensing with the need of a rack and allowing a less costly mounting direct to the electrical control panel. Thanks to this small size, the **GPC® 184** put into the same plastic rails that contains the peripheral I/O, i.e **ZBx xxx** , forms an unique **BLOCK** element. The **GPC® 184** can also be mounted as a macro CPU module on a peripheral card of the end user, in **Piggy Back** (stack through) mode. The powerfull rom-based **FGDOS** operating system makes easy to take advantage of the on-board resources and allows reduced development time thanks to its support to high level languages like **C**, **PASCAL**, etc. **FGDOS** also lets the User see as **RAM/ROM disks** the memory devices, making possible to use them immediatly and easily by the high level languages disk access instructions. Adding an **82C55**, external to the board, **FGDOS** can manage a **MCI 64** board that drives **PCMCIA RAM cards**, **LCD** or **fluorescent** displays, a matrix keyboard and a parallel printer. **FGDOS** is also capable to program a **FLASH** memory directly on the board. Boars of serie **KDx xxx** exist to be able to access these features immediatly, or, for who needs a well-developed device, operator panels **QTP 24P** and **QTP 16P** exist. These panels have the same look as **QTP 24** and **QTP 16** but don't have on-board intelligence, so they must be driven directly by the **GPC® 184** board, performing a cost reduction.

For getting a quick prototype, cards such as **SPA 03** and **SPA 04** on which it is possible to mount the **GPC® 184** in **Piggy Back** mode, are used. The presence on board of the **ABACO® I/O BUS** connector, allows to drive directly I/O cards as: **ZBR 84**, **ZBR 168**, **ZBR 246, ZBR 324, ZBT 84**, **ZBT 168**, **ZBT 246, ZBT 324** and so on, and through **ABB 03**, **ABB 05** it is possible to manage all the peripheral cards available on **Abaco® BUS**.

- Intelligent Module **Abaco® BLOCK**, **Serie 4**, size 100x50 mm
- Optional container, format **DIN 46277-1 and 3** rails compliant
- CPU **Z180**, with **18,432 MHz** quartz
- Up to **512K** of **EPROM** or **FLASH** and up to **512K** of **RAM**. FGDOS uses memory exceeding 64K as RAM/ROM Disk. The User can reprogram the on-board FLASH memory with his/her program.
- **Real Time Clock** capable to generate **INT**errupts
- **Back Up** for RAM and RTC, through on-board **LITHIUM** battery or external battery
- **Clocked Serial I/O interface**, available to the User, on the I/O connetor
- **2** internal 16 bits wide Programmable Reload **Timer** channels
- 2 **RS232** serial lines, one of which settable as **RS422**, **RS485** or **Current Loop**
- Double **Baud Rate** generator, software programmable
- **Watch Dog** circuitery, hardware manageable
- **Abaco® I/O BUS** da 26 pins expansion connector
- **4** different power saving modes: **Halt,STOP**, **Sleep** and **System Stop**
- **Power Failure** circuitry capable to generate interrupts
- Consumption extermy reduced: only as low as **60 mA** on **5Vdc**
- On-board logic protected against transients by **TransZorb™**
- Wide range of development software available such as **Remote Symbolic Debugger**; **Macro Assembler**; **GET 80**; **C compilers** (**HI TECH C 80, DDS MICRO C 85**); **PASCAL compilers** (**PASCAL 80, EMBEDDED PASCAL**); **FGDOS184** etc.

Here follows a description of the board's functional blocks, with an indication of the operations performed by each one. To easily locate these blocks and verify their connections pleare refer to figure 1.

CPU

GPC® 184 board is designed to employ the **Z180** CPU manifactured by **ZILOG**. This 8 bits CPU is code compatible with Z80 so it features an extended instructions set (170), high speed of execution and data manipulation and efficent vectored interrupts management. Remarkable is the presence of these peripherals inside the CPU:

- Two 16 bits timers, provided with programmable prescaler (PRT);
- Two asynchronous serial lines capable to manage handshake signals (ASCI);
- Two DMA channels for high speed data transfers (DMAC);
- Memory management unit (MMU);
- One synchronous serial line (CSI/O);
- Interrupt controller;
- Wait states generator to access external devices;
- Idle and Stop modes, to reduce power consumption;

For further informations about this component please refer to the manifacturer documentation, or see Appendix B of this manual.

MEMORY DEVICES

On the card can be monted 1024K bytes of memory divided with a maximum of 512K EPROM or FLASH EPROM, 512K static RAM. The **GPC® 184** memory configuration must be chosen considering the application to realize or the specific requirements of the user. Normally the card is equipped with 128K byte of static RAM and all different configurations must be specified from the user, at the moment of the order.

With the on board back up circuit there is the possibility to keep data , also when power supply is failed; in this way the card is always able to maintain parameters, logged data, system status and configuration, etc. without using expensive external UPS. The back up circuit is supplied by a on board lithium battery or an external battery to be connected to a specific connector.

The addressing of memory devices is controlled by a specific control logic, that provides to allocate the devices in the microprocessor address space, this control logic automatically manages the different addressing mode and it satisfies the requests of each **GPC® 184** software tools.

For further information about memory configuration, sockets description and jumpers connection, please refer to "ADDRESSES AND MAPS" and "PERIPHERAL DEVICES SOFTWARE DESCRIPTION" chapters and to "MEMORY SELECTION" paragraph for detailed informations about sockets to use and jumpers configuration.

SERIAL COMMUNICATION

Serial communication is completely software settable both for protocol and for speed (which ranges from 75 to as high as 57,6KBaud with standard clock frequency). These settings are performed programming the ASCI inside the microprocessor and the baude rate generator, for further informations please refer to the manifacturer documentation or to Appendix B of this manual. By hardware it is possible to select, through some on board jumpers,the electric communication protocol. In detail, one line is always buffered as RS 232, while the other line can be buffered in four different electrical protocols: **RS 232**, **current loop**, **RS 485** or **RS 422**; in this last cases also directionality and line activation is programmable.

CLOCK

GPC® 184 is provided with a circuitery that generates the CPU clock frequence (18,432 MHz); this frequence is used also to generate the frequencies needed to the other sections of the board (Timer, serial lines, etc.). If the User needs to run very fast applications the clock frequence can be even doubled by interventing on the proper circuitry (for more informations please contact **grifo®**). We would remark that the CPU <u>clock frequence is always half of the crystal oscillation frequence</u>.

POWER SUPPLY

The card must be powered only with **+5 Vdc through the pin 25 (GND) and pin 26 (+5Vdc) of the CN1 connector**. The power supply circuit generates all the necessary voltages for the card and it is designed for reducing the consumption (the microprocessor power down and idle mode are available) and for increasing the electrical noise immunity. In fact, as low as 60 mA of consumption for the normal working mode, allow the User to supply the board by batteries, solarr panels, small power supplies, etc. An intersting power failure circuitry capable to detect the imminent power black out is installed on the board, so it can start a software intervent by generating an interrupt. Please remember that on board there is a protection circuit aganist voltage peaks by **TransZorb**™.

BOARD CONFIGURATION

Jumper J4 has been introduced expressely to make the board and in particualr the application program confugrable. The possibility to read by software the status of this jumper gives the User the ability to manage many different conditions by an unique program, without having to employ other input singnals (typical applications are: language choice, program parameters definition, operational mode selection, etc.). Some software tools developed for the **GPC® 184** board use jumper J4 to select between the operation modalities RUN and DEBUG, as described in the manuals of the tools themselves.
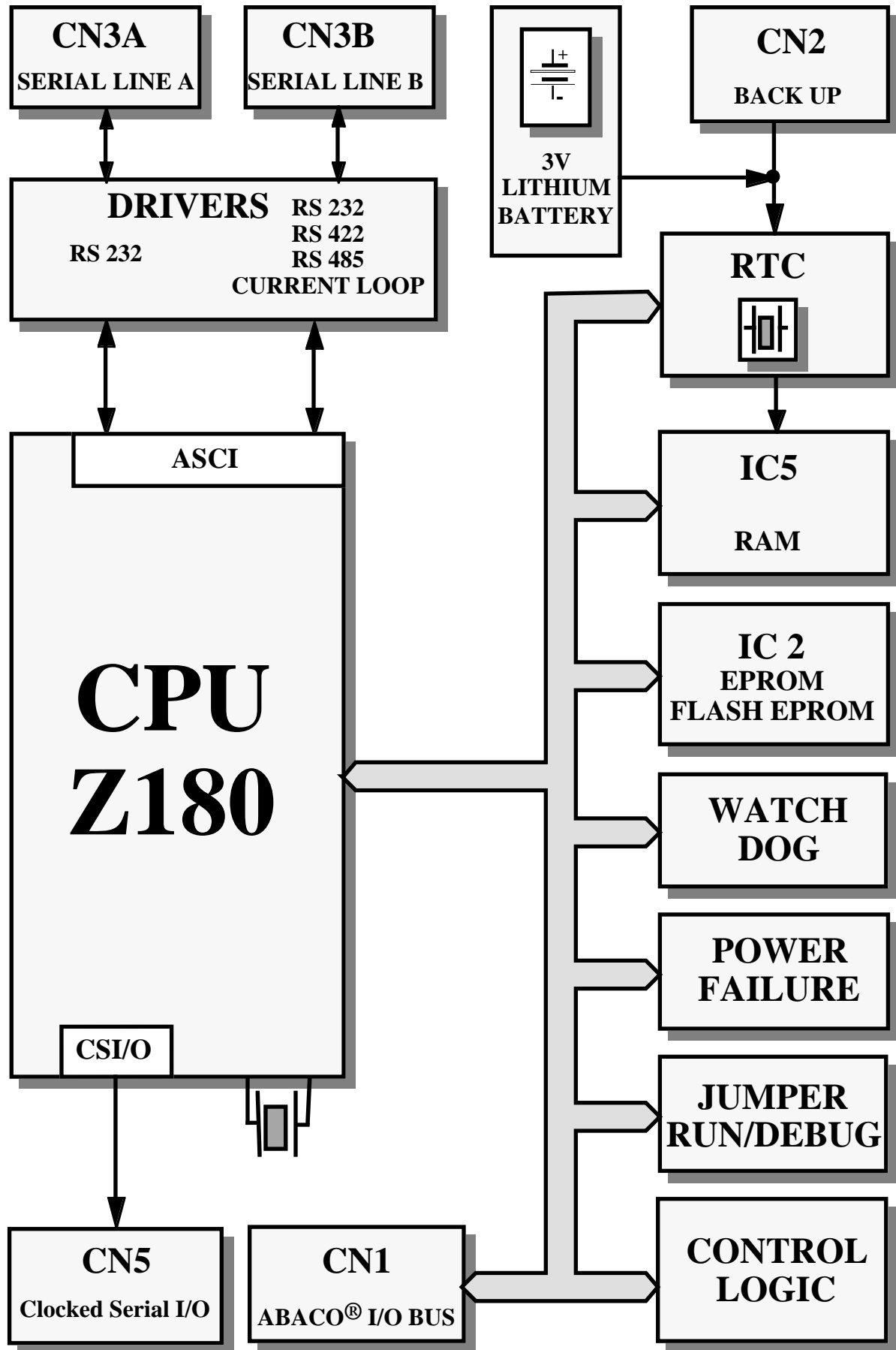
FIGURE 1: BLOCK DIAGRAM

ABACO® I/O BUS

One of the most important features of **GPC® 184** is its possibility to be interfaced to industrial **ABACO® I/O BUS** .Thanks to its standard **ABACO® I/O BUS** connector, the card can be connected to some of the numerous **grifo®** boards,both intelligent and not. For example the user can directly use cards for analog signals acquisition (A/D like **ABC 04** or **ABB 08**), cards for analog signals generation (D/A), cards for digital I/O signals management, cards with timers and counters, cards for temperature controls, etc. also custom boards designed to satisfy specific needs of the end user. Using **ABB 03** or **ABB 05** mother boards it is possible manage all the BUS **ABACO®** single EURO cards. So **GPC® 184** becomes the right component for each industrial automation system, in fact **ABACO® I/O BUS** makes the card easily expandable with the best price/performance ratio.

REAL TIME CLOCK

GPC® 184 board is provided with a complete Real Time Clock device capable to manage hours, minutes, seconds, day of month, month, year and day of week in stand alone mode. The component is supplied by the back up circuitry to warrant data integrity in every working condition and is completely software programmable acting on 16 registers addressable in the CPU I/O addressing space by a specific memory management circuitry.The RTC section can generate interrupts at a software programmable rate, for diverting the CPU from its normal tasks or awakening it from one of its low consumption working modes.

WATCH DOG

GPC® 184 board is provided with a Watch Dog circuitery that, if used, allows to exit from infinite loop or abnormal conditions not managed by the application program. This circuitery is made by an astable section with 1.5 sec of intervent time, is completely software managed (by accessing a register addressed in the CPU addressing space) and gives the board an exterme degree of safety.

RESET CONTACT

P1 reset contact of the **GPC® 184** board allows the user to reset the board and restarting it in a general clearing condition. The main purpose of this contact is to come out of infinite loop conditions, useful especially during debug or to grant a particular initial stat. Please see figure 9 for an easy localization of this contact.

CONTROL LOGIC

A specific control logic is responsable of mapping the registers of the on-board devices and the memory devices.
The logic allocates these devices in the CPU addressing space, for further informations please refer to the paragraph "I/O MAPPING".

TECHNICAL FEATURES

GENERAL FEATURES

Devices:
Two 16 bit timers (PRT)
1 synchronous serial line (CSI/O)
2 DMA channels (DMAC)
1 RS 232 serial line (ASCI1=A)
1 RS 232, RS 422, RS 485, current loop serial line(ASCI0 =B)
1 reset contact
1 astable hardware watch dog
1 real time clock
1 configuration jumper
1 **ABACO®** I/O BUS interface
1 power failure circuitry

Memory:
IC 2:   EPROM from 128K x 8 to 512K x 8
          FLASH EPROM from 128K x 8 to 512K x 8
IC 5:   RAM from 128K x 8 to 512K x 8

CPU:
ZILOG Z180 or HITACHI 64HD180

Crystal (clock) frequency:
18,432 (9,216) MHz

Watch dog intervent time:
from 1,00 sec to 2,25 sec (typical 1,50 sec)

PHYSICAL FEATURES

Size (W x H x D):
100 x 50 x 25 mm   (without container)
110 x 60 x 60 mm   (with DIN rails container)

Weight:
75 g   (without container)
135 g   (with DIN rails container)

Connectors:
CN1:   26 pins, male, vertical, low profile connector
CN2:   2 pins, male, vertical, low profile connector
CN3A: 6 pins, Plug, female
CN3B: 6 pins, Plug, female
CN5:   5+5 pins, male, vertical, strip connector

Temperature range:
from 0 to 50 Centigrad degreeses

Relative humidity:
20% up to 90%   (without condens)

ELECTRIC FEATURES

Power Supply: +5 Vdc

Consumption on 5 Vdc: 60 mA (default configuration)

On board back up battery: 3,0 Vdc; 180 mAh

External back up battery: 3,6÷5 Vdc

Back up current: 1,6 µA (on board battery)

RS 422, RS 485 line termination:

Line termination resistance=	120 Ω
Positive pull up resistance=	3,3 KΩ
Negative pull up resistance=	3,3 KΩ

Power failure intervent threshold: 1,25 Vdc

INSTALLATION

In this chapter there are the information for a right installation and correct use of the card. The user can find the location and functions of each connectors, jumpers and some explanatory diagrams.

CONNECTIONS

The **GPC®184** module has 5 connectors that can be linkeded to other devices or directly to the field, according to system requirements. In this paragraph there are connectors pin out, a short signals description (including the signals direction) and connectors location (see figure 9).

CN2 - BACK UP EXTERNAL BATTERY CONNECTOR

CN2 is a 2 pins, vertical, male connector with 2,54mm pitch. Through CN2 the user can connect an external battery for RAM and RTC back up when the power supply is switched off (for further information please refer to chapter "BACK UP").

+Vbat — — — — — — — | **1   2** | — — — — **GND**
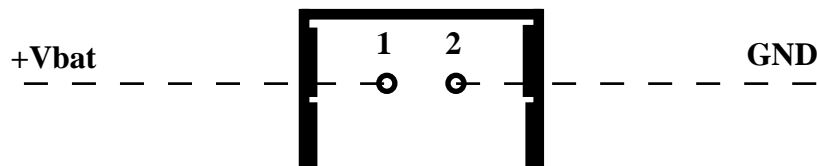
FIGURE 2: CN2 - EXTERNAL BACK UP BATTERY CONNECTOR

Signals description:

+Vbat	=	I	-	Positive pin of external back up battery
GND	=		-	Negative pin of external back up battery

CN1 - ABACO® I/O BUS CONNECTOR

CN1 is a 26 pins, male, vertical, low profile connector with 2,54mm pitch.
Through CN1 the card can be connected to some of the numerous **grifo®** boards, both intelligent and not. All this connector signals are at TTL level.

D0	1 2	**D1**
D2	3 4	**D3**
D4	5 6	**D5**
D6	7 8	**D7**
A0	9 10	**A1**
A2	11 12	**A3**
A4	13 14	**A5**
A6	15 16	**A7**
/WR	17 18	**/RD**
/IORQ	19 20	**/RESET**
/CS1	21 22	**PFI**
/INT BUS	23 24	**/NMI BUS**
GND	25 26	**+5 Vdc**
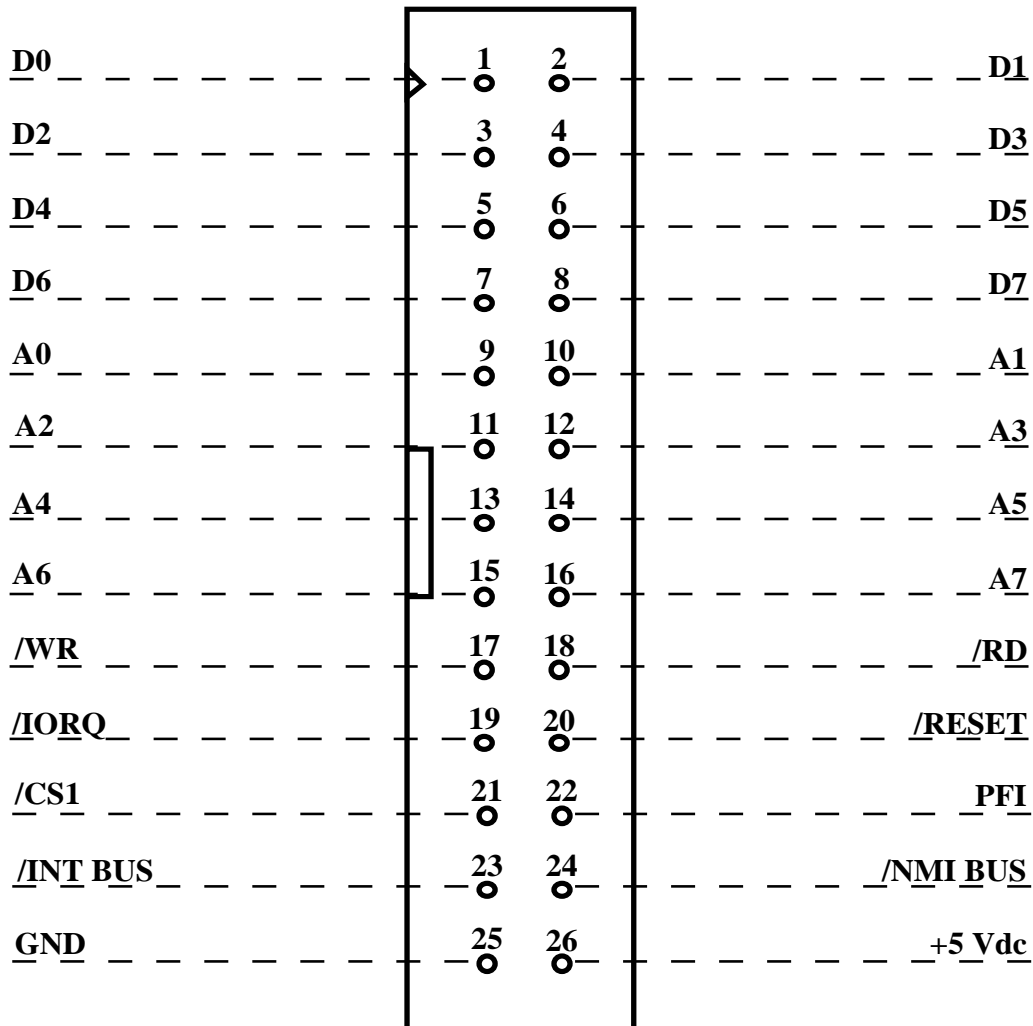
FIGURE 3 CN1 - ABACO® I/O BUS CONNECTOR

Signals description:

A0-A7	=	O	- Address BUS.
D0-D7	=	I/O	- Data BUS.
/INT BUS	=	I	- Interrupt request (open collector type).
/NMI BUS	=	I	- Non maskable interrupt (open collector type).
/IORQ	=	O	- Input output request.
/RD	=	O	- Read cycle status.
/WR	=	O	- Write cycle status.
/RESET	=	O	- Reset.
/CS1	=	O	- Chip select 1: external devices decoded enable
PFI	=	I	- Power Failure input
+5 Vdc	=	I/O	- +5 Vdc power supply.
GND	=		- Ground signal.

FIGURE 4: CARD PHOTO
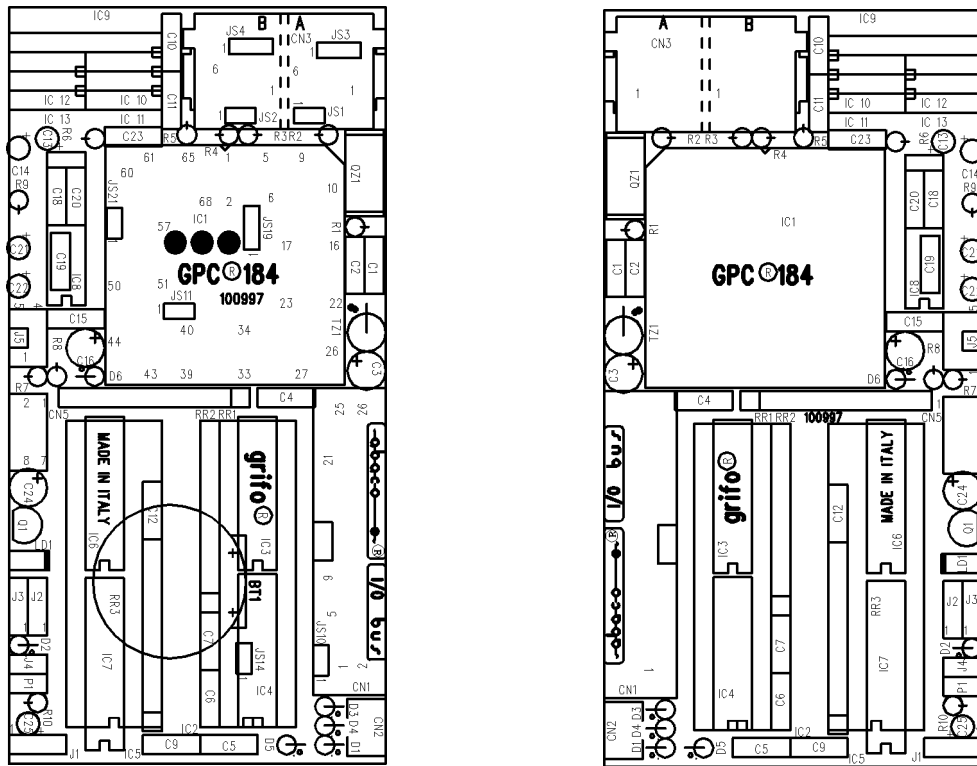
FIGURE 5: COMPONENTS MAPS (SOLDERING SIDE AND COMPONENTS SIDE)

CN3A - SERIAL LINE A CONNECTOR

CN3A is a 6 pins, female PLUG connector for serial communication. Phisically, serial line A of **GPC® 184** board is connected to the ASCI 1 serial line of the CPU.
Placing of the signal has been designed to reduce interference and electrical noise and to simplify connections with other systems, while the electric protocol follows the CCITT normative.
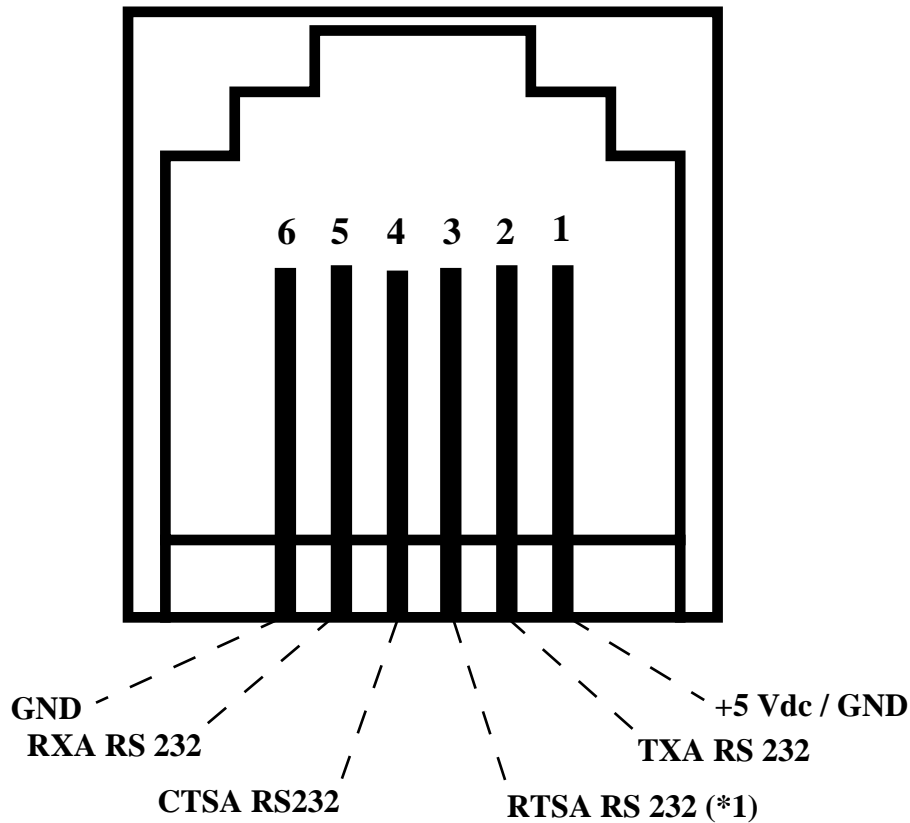
FIGURE 6: CN3A- SERIAL LINE A CONNECTOR

Signals description:

RXA RS 232	=	I	-	Serial line A=ASCI1 RS 232 Receive Data.
TXA RS 232	=	O	-	Serial line A=ASCI1 RS 232 Transmit Data.
CTSA RS 232	=	I	-	Serial line A=ASCI1 RS 232 Clear To Send.
RTSA RS 232	=	O	-	Serial line A=ASCI1 (*1) RS 232 Request To Send.
+5 Vdc/GND	=		-	+5 Vdc power supply or ground signal
GND	=			Ground signal

*1: The output handshake signal RTSA is not software manageable so it is kept continuosly deactived = -10 Vdc. If this configuration is incompatible with the system to be connected, perform the connection without this signal.
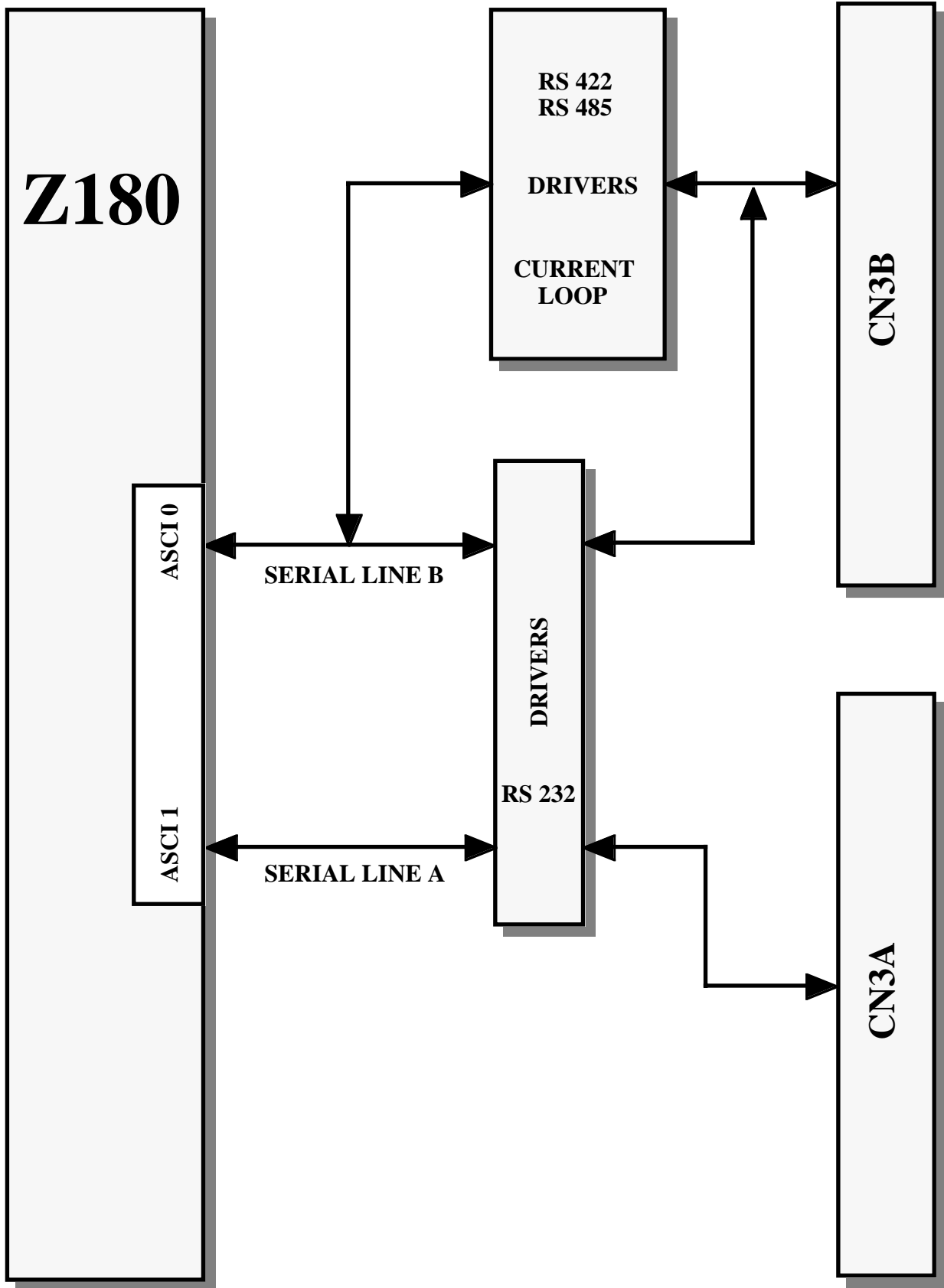
FIGURE 7: SERIAL COMMUNICATION DIAGRAM

CN3B - SERIAL LINE B CONNECTOR

CN3B is a 6 pins, female PLUG connector for serial line B, that can be buffered as RS 232, RS 422, RS 485 or Current Loop. Phisically, serial line B of **GPC® 184** board is connected to the ASCI 0 serial line of the CPU. Placing of the signal has been designed to reduce interference and electrical noise and to simplify connections with other systems, while the electric protocol follows the CCITT normative.

GND   **+5 Vdc / GND**

RXB RS 232 / RXB+ RS 422 /   **TXB RS 232 / TXB+ RS 422 /**
RXTXB+ RS 485 / RXB+ C.L.   **TXB- C.L.**

CTSB RS232 / RXB- RS 422 /   **RTSB RS 232 / TXB- RS 422 /**
RXTXB- RS 485 / RXB- C.L.   **TXB+ C.L.**

FIGURE 8: CN3B- SERIAL LINE B CONNECTOR

Signals description:

RXB RS 232	= I - Serial line B=ASCI 0 RS 232 Receive Data.
TXB RS 232	= O - Serial line B=ASCI 0 RS 232 Transmit Data.
CTSB RS 232	= I - Serial line B=ASCI 0 RS 232 Clear To Send.
RTSB RS 232	= O - Serial line B=ASCI 0 RS 232 Request To Send.
RXB- RS 422	= I - Receive Data Negative: Serial line B=ASCI 0 negative signal for RS 422 serial differential receive.
RXB+ RS 422	= I - Receive Data Positive: Serial line B=ASCI 0 positive signal for RS 422 serial differential receive.
TXB- RS 422	= O - Transmit Data Negative: Serial line B=ASCI 0 negative signal for RS 422 serial differential transmit.
TXB+ RS 422	= O - Transmit Data Positive: Serial line B=ASCI 0 positive signal for RS 422 serial differential transmit.

RXTXB- RS 485	=I/O-	Receive Transmit Data Negative: Serial line B=ASCI 0 negative signal for RS 485 serial differential receive and transmit.
RXTXB+ RS 485	=I/0-	Receive Transmit Data Positive: Serial line B=ASCI 0 positive signal for RS 485 serial differential receive and transmit.
RXB- C.L.	= I -	Receive Data Negative: Serial line B=ASCI 0 negative signal for Current Loop serial bipolar receive.
RXB+ C.L.	= I -	Receive Data Positive: Serial line B=ASCI 0 positive signal for Current Loop serial bipolar receive.
TXB- C.L.	= O -	Transmit Data Negative: Serial line B=ASCI 0 negative signal for Current Loop serial bipolar transmit.
TXB+ C.L.	= O -	Transmit Data Positive: Serial line B=ASCI 0 positive signal for Current Loop serial bipolar transmit.
+5 Vdc/GND	= I -	+5 Vdc or ground signal.
GND	= -	Ground signal.
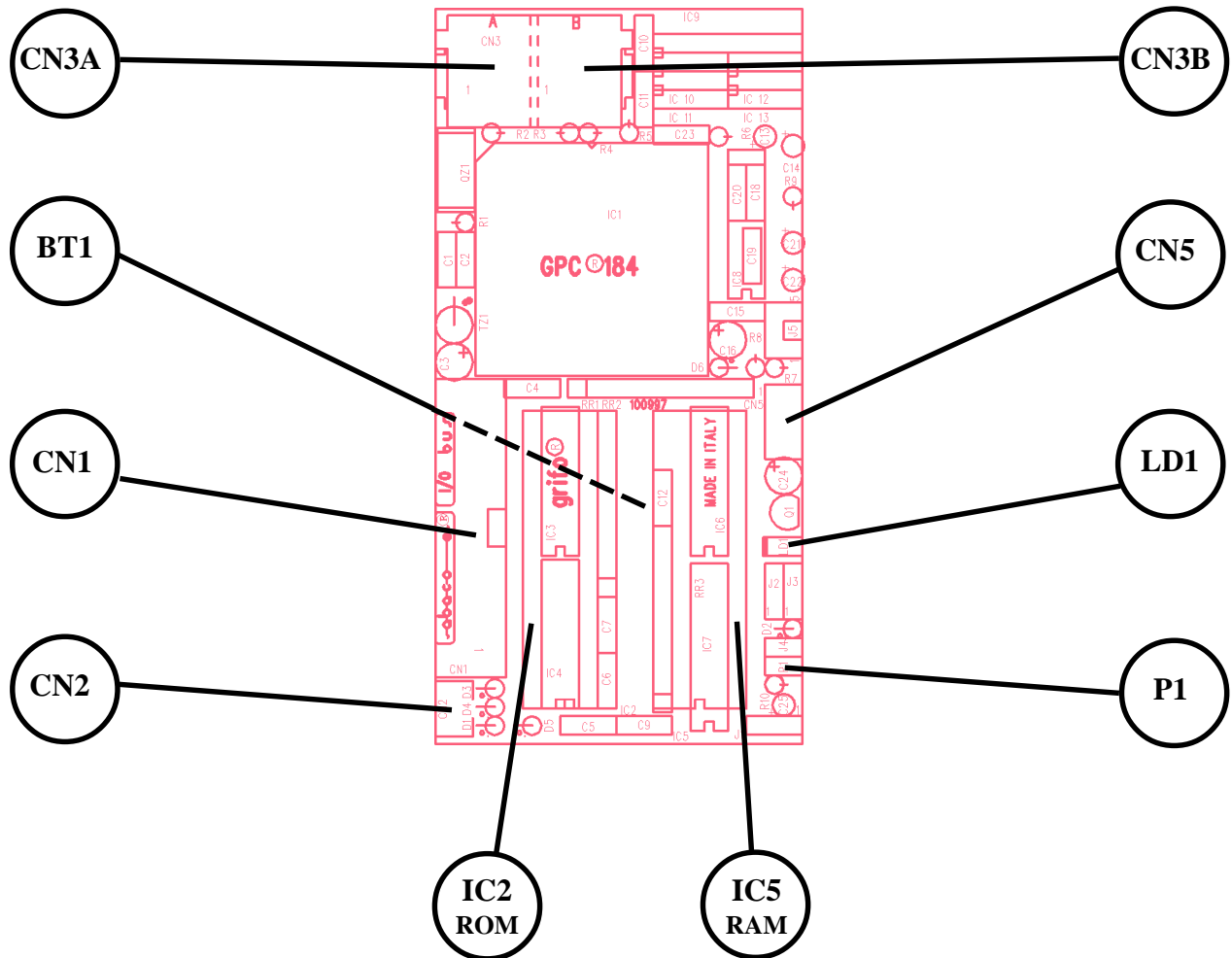
FIGURE 9: LEDS, CONNECTORS, MEMORIES, ETC. LOCATION

CN3A,B GPC® 184

			External System
4	CTSA, CTSB	RTS	
3	RTSA, RTSB	CTS	
5	RXA, RXB	TX	
2	TXA, TXB	RX	
6	GND	GND	
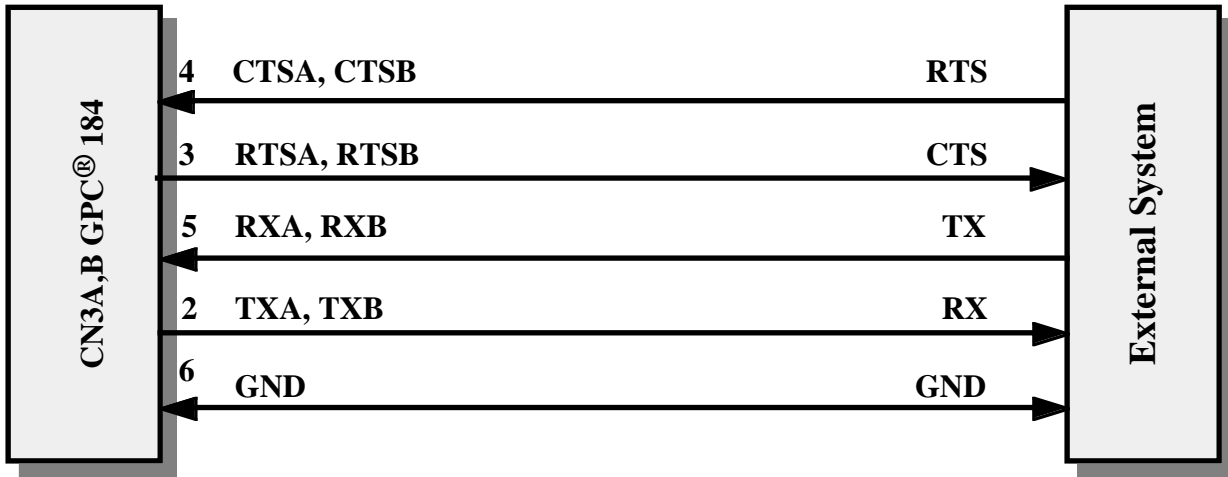
FIGURE 10: RS 232 PIN OUT AND CONNECTION EXAMPLE

CN3B GPC® 184

			External System
	RXB -	TX -	
4	RXB +	TX +	
5	TXB -	RX -	
3	TXB +	RX +	
2	GND	GND	
6			
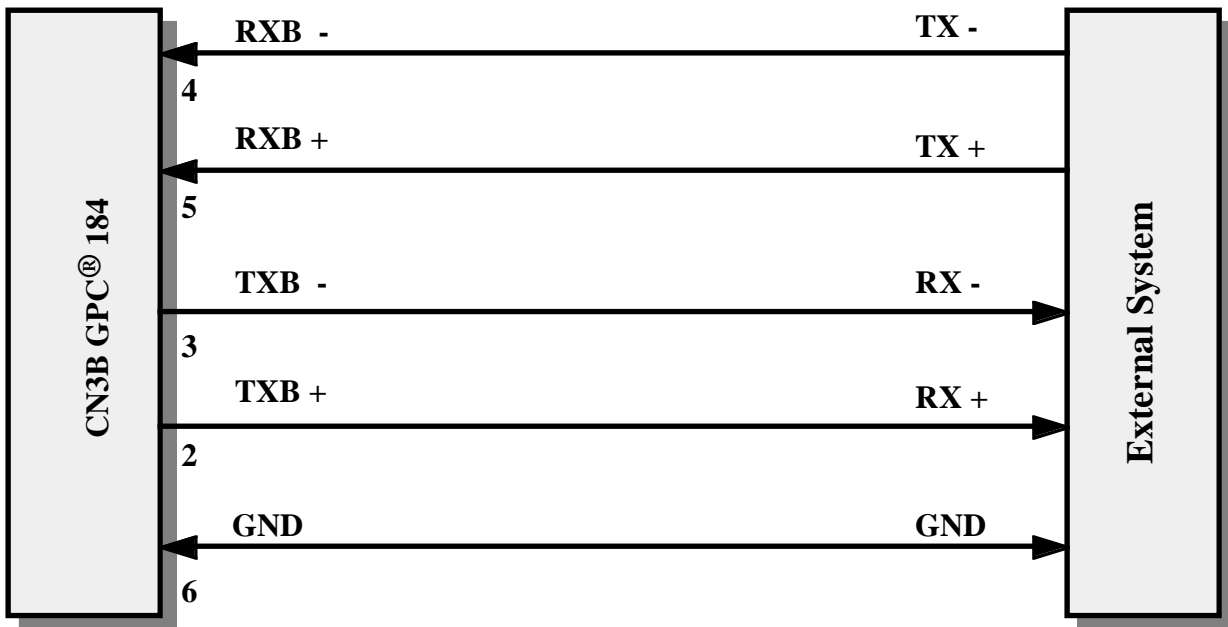
FIGURE 11: RS 422 PIN OUT AND POINT TO POINT CONNECTION EXAMPLE

CN3B GPC® 184

			External System
4	RXTXB -	TX / RX -	
5	RXTXB +	TX / RX +	
6	GND	GND	
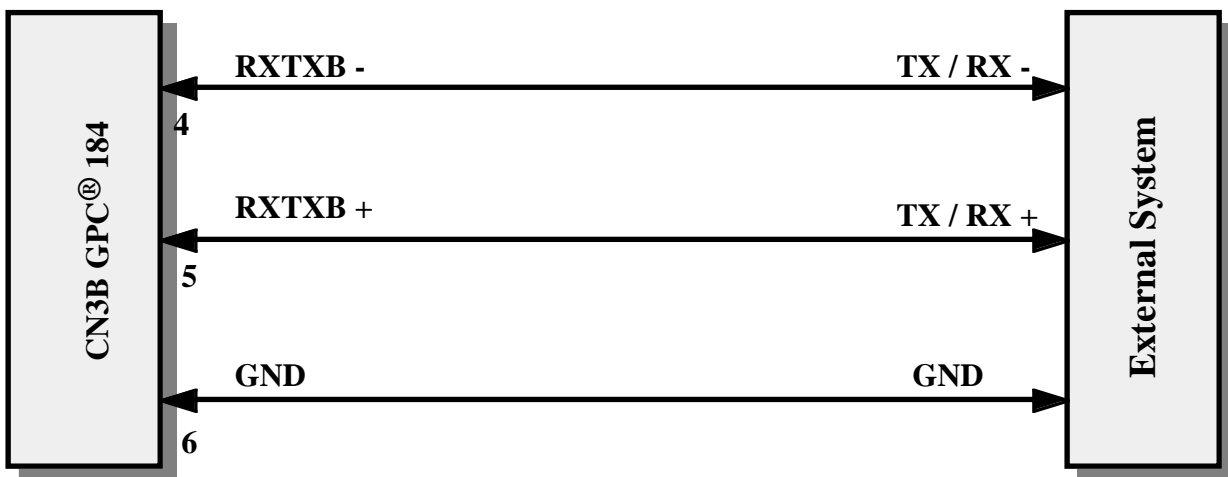
FIGURE 12: RS 485 PIN OUT AND POINT TO POINT CONNECTION EXAMPLE
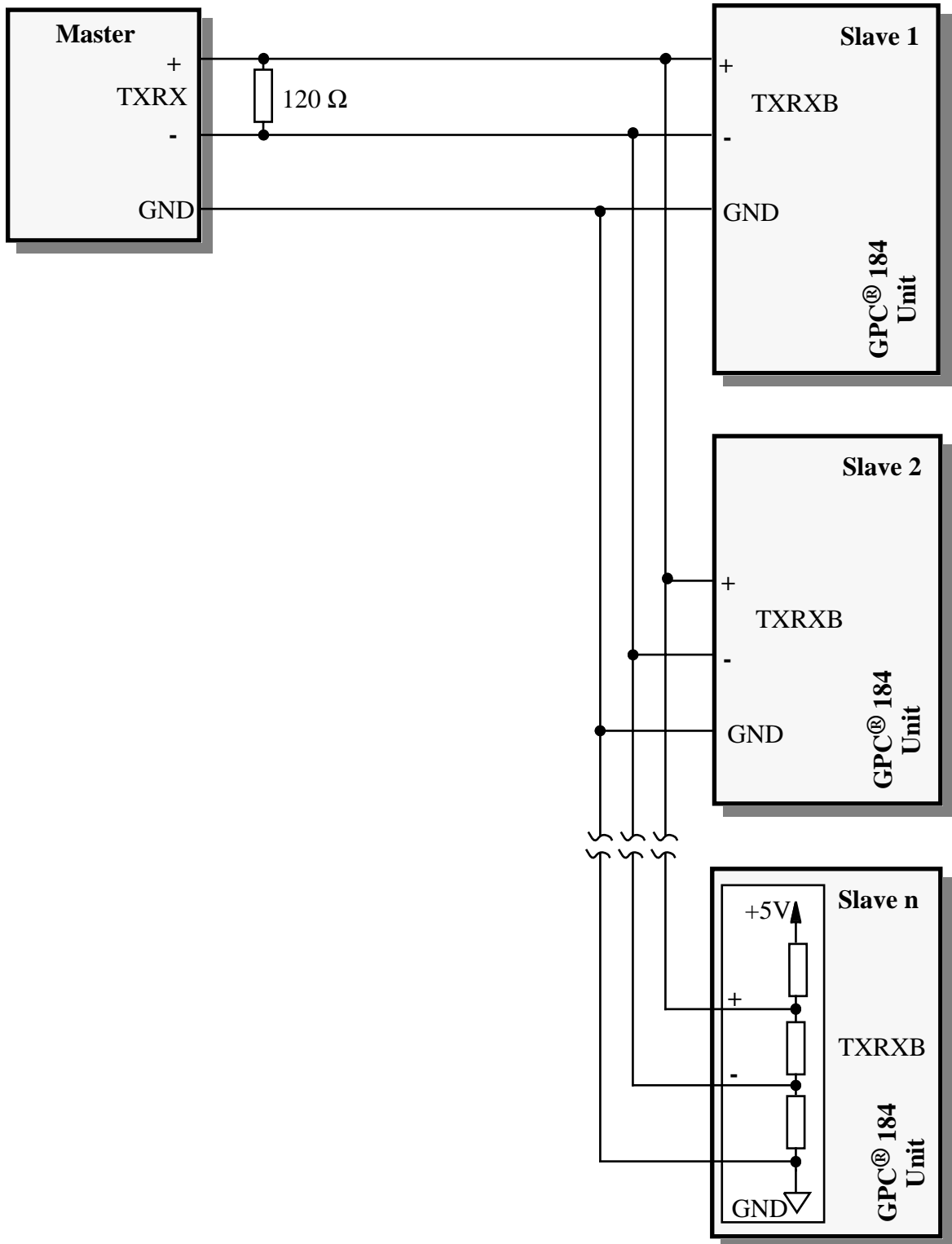
FIGURE 13: RS 485 PIN OUT AND NETWORK CONNECTION EXAMPLE
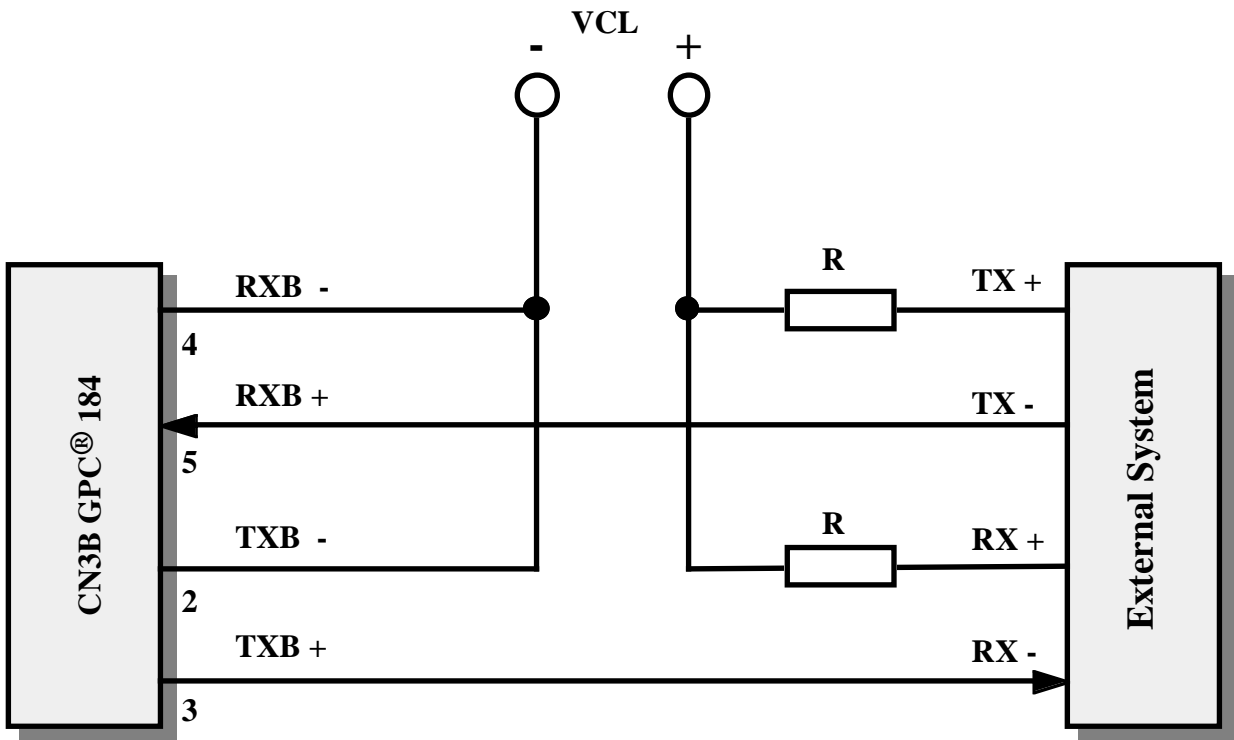
FIGURE 14: 4 WIRES CURRENT LOOP POINT TO POINT CONNECTION EXAMPLE
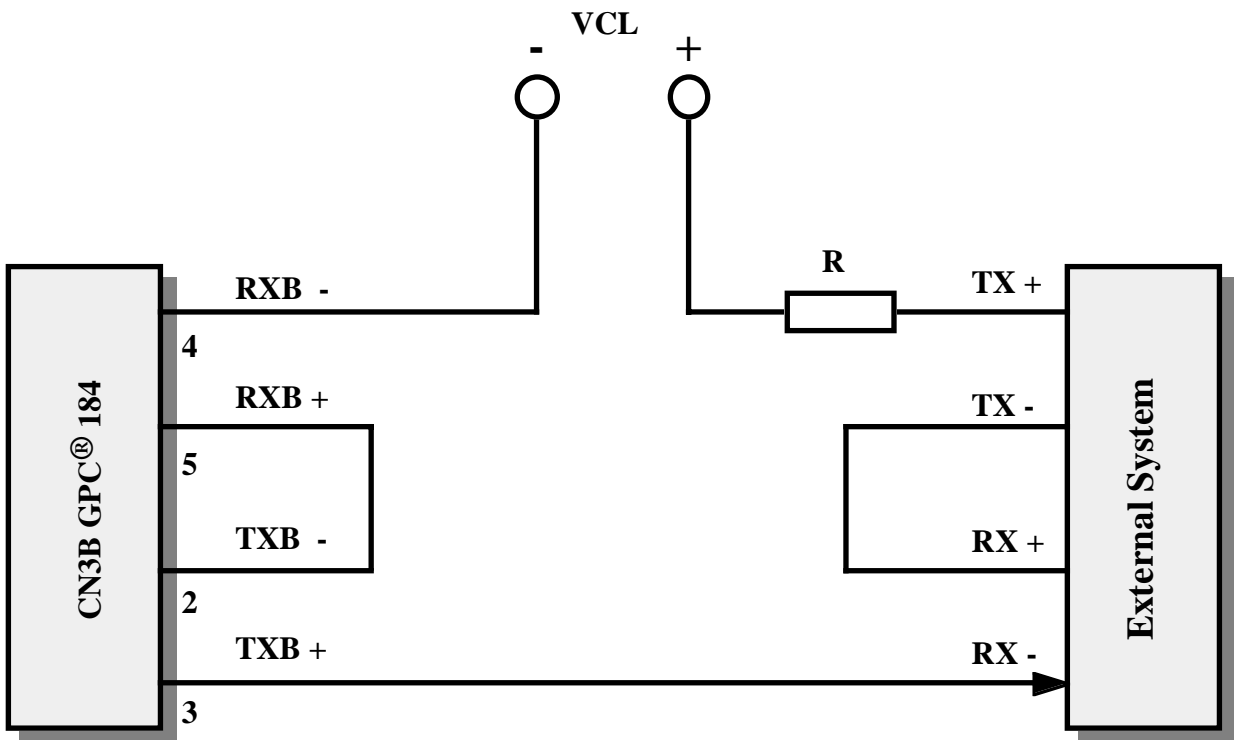
FIGURE 15: 2 WIRES CURRENT LOOP POINT TO POINT CONNECTION EXAMPLE
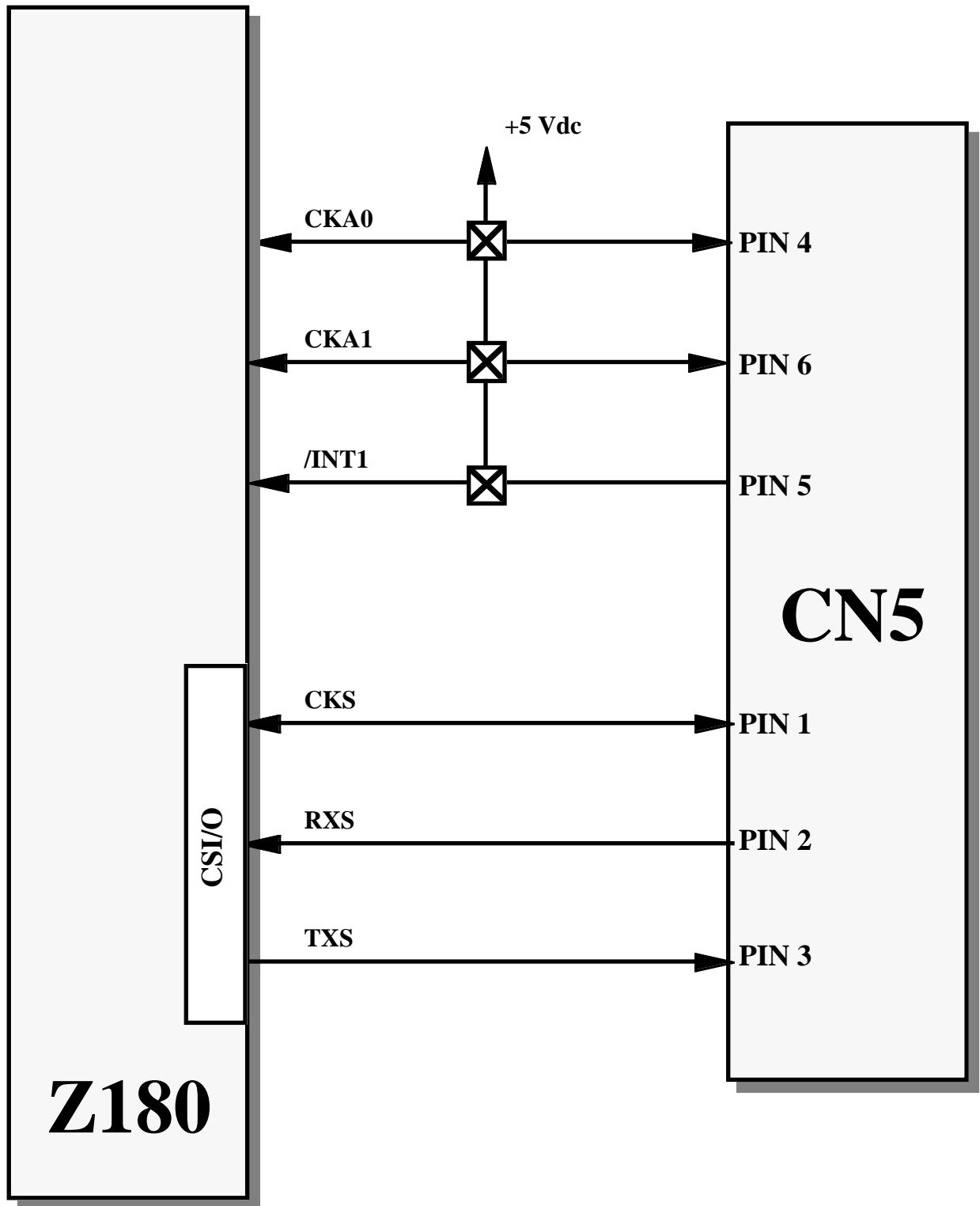
FIGURE 16: CN5 SIGNALS CONNECTION DIAGRAM

CN5 - AUXILIARY SIGNALS CONNECTOR

CN5 is 2.54 mm pitch, 5+5 pins, male, vertical, strip connector. CN5 is the interface for 3 signals of the synchronous serial communication, one /INT 1 interrupt signal, 2 baud rate generator signals and the power supply. All signal are TTL.

CKS		1	2		RXS
TXS		3	4		CKA0
/INT1		5	6		CKA1
GND		7	8		+5Vdc
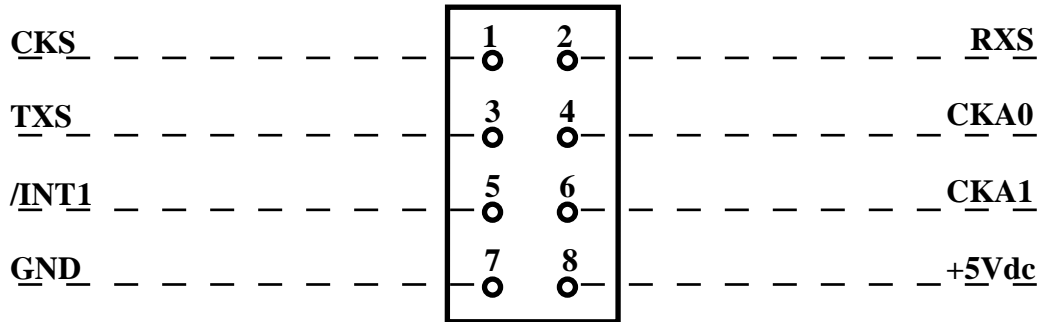
FIGURE 17: CN5 - AUXILIARY SIGNALS CONNECTOR

Signals description:

CKS	=	I/O	- Isochronous serial line clock signal.
RXS	=	I	- Isochronous serial line receive signal.
TXS	=	O	- Isochronous serial line transmit signal.
/INT1	=	I	- Interrupt request /INT1.
CKA0	=	I/O	- ASCI 0 = serial B baud rate generator clock signal.
CKA1	=	I/O	- ASCI 1 = serial A baud rate generator clock signal.
+5 Vdc	=	O	- +5 Vdc power supply.
GND	=		- Ground signal.

I/O CONNECTION

To prevent possible connecting problems between **GPC® 184** and the external systems, the user has to read carefully the information of the previous paragraphs and he must follow these instructions:

- For RS 232,RS 422, RS 485 or Current Loop communication signals the user must follow the standard rules of these protocols.
- For all TTL signals the user must follow the rules of this electric standard. The connected digital signal must be always referred to card digital ground. For TTL signals, the 0 Vdc level corresponds to logic state "0", while 5Vdc level corrisponds to logic state "1".

VISUAL SIGNALATIONS

GPC® 184 board is provided with a LED in order to signal to the User some internal status conditions, as described in the following table:

LED	COLOUR	DESCRIPTION
LD1	Red	Indicates the activation of the Real Time Clock interrupt request signal (/INT2 of the CPU).

FIGURE 18: VISUAL SIGNALATIONS TABLE

The main purpose of this LED is to provide the User a visual indication of the board status, making easier the operations to verify the correct workig of the system. To easily locate the LED on the board please see figure 9, while for a description about the modalities of RTC interrupt generation please refer to the paragraph "REAL TIME CLOCK".

JUMPERS

On **GPC® 184** there are 16 jumpers for card configuration, 9 of them are solder jumpers. Connecting these jumpers, the user can define for example the memory type and size, the peripheral devices functionality and so on. Below there is the jumpers list, location and function.

JUMPERS	N. PIN	FUNCTION
J1	3	It selects IC5 RAM size.
J2	3	Matching with J3, it selects the device type, EPROM or FLASH EPROM, installed on IC2.
J3	3	Matching with J2, it selects the device type, EPROM or FLASH EPROM, installed on IC2.
J4	2	It selects the configuration input (RUN or DEBUG).
J5	5	It selects between RS 422 and RS 485 for serial line B.
JS1	2	Matching with JS2, it connects the termination and forcing circuitry to the RS 485 line or to the RS 422 receive line.
JS2	2	Matching with JS1, it connects the termination and forcing circuitry to the RS 485 line or to the RS 422 receive line.
JS3	3	It selects the type of the connection for pin 1 of CN3A.
JS4	3	It selects the type of the connection for pin 1 of CN3B.
JS10	2	Activates the watch dog circuitry.
JS11	2	It keeps enabled the CPU CTSB handshake.
JS14	2	It connects the on board battery BT1 to the back up circuitry.
JS19	3	It selects which interrupt to connect to the power failure.
JS21	2	It selects the connection of the CTSA handshake.

FIGURE 19: JUMPERS SUMMARIZING TABLE

The following tables describe all the right connections of **GPC® 184** jumpers with their relative functions. To recognize these valid connections, please refer to the board printed diagram (serigraph) or to figure 5 of this manual, where the pins numeration is listed; for recognizing jumpers location, please refer to figures 20, 21. The "*" used in the following tables, denotes the default connection, or on the other hand the connection set up at the end of testing phase, that is the configuration the user receives.
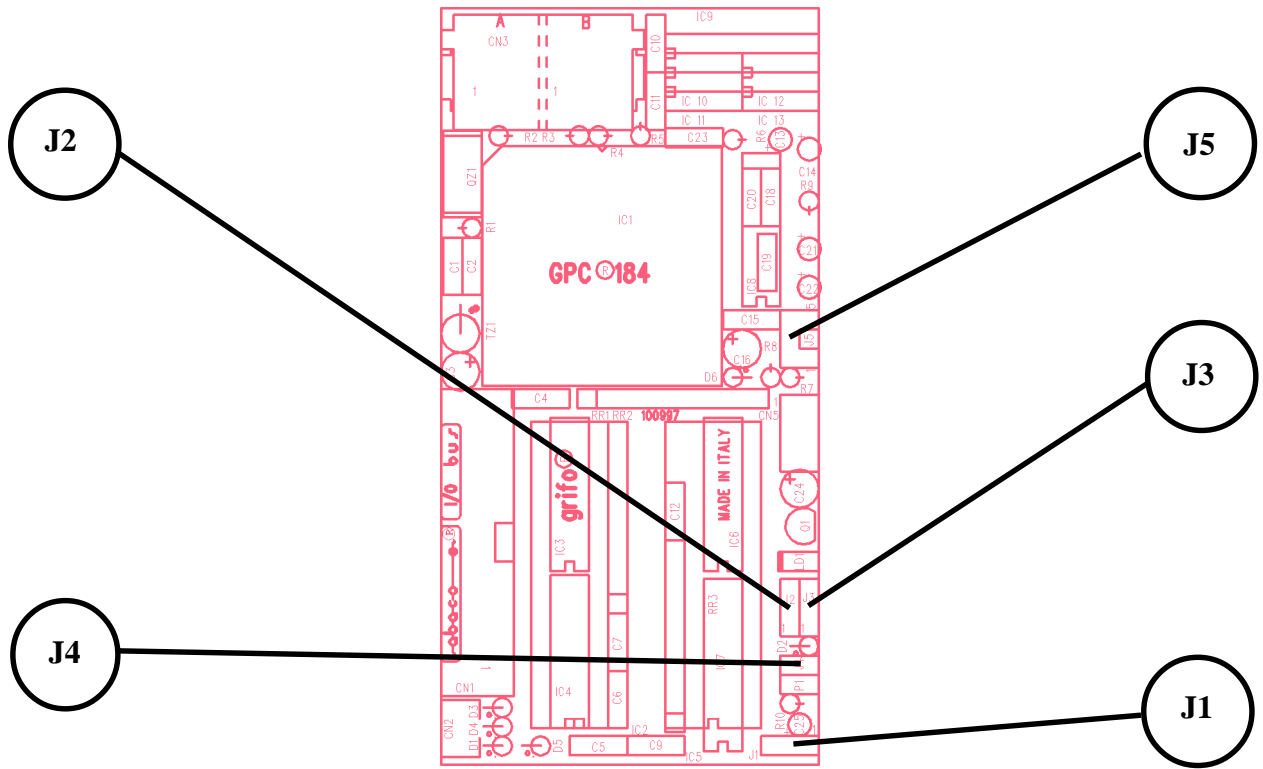
FIGURE 20: JUMPERS LOCATION (COMPONENT SIDE)
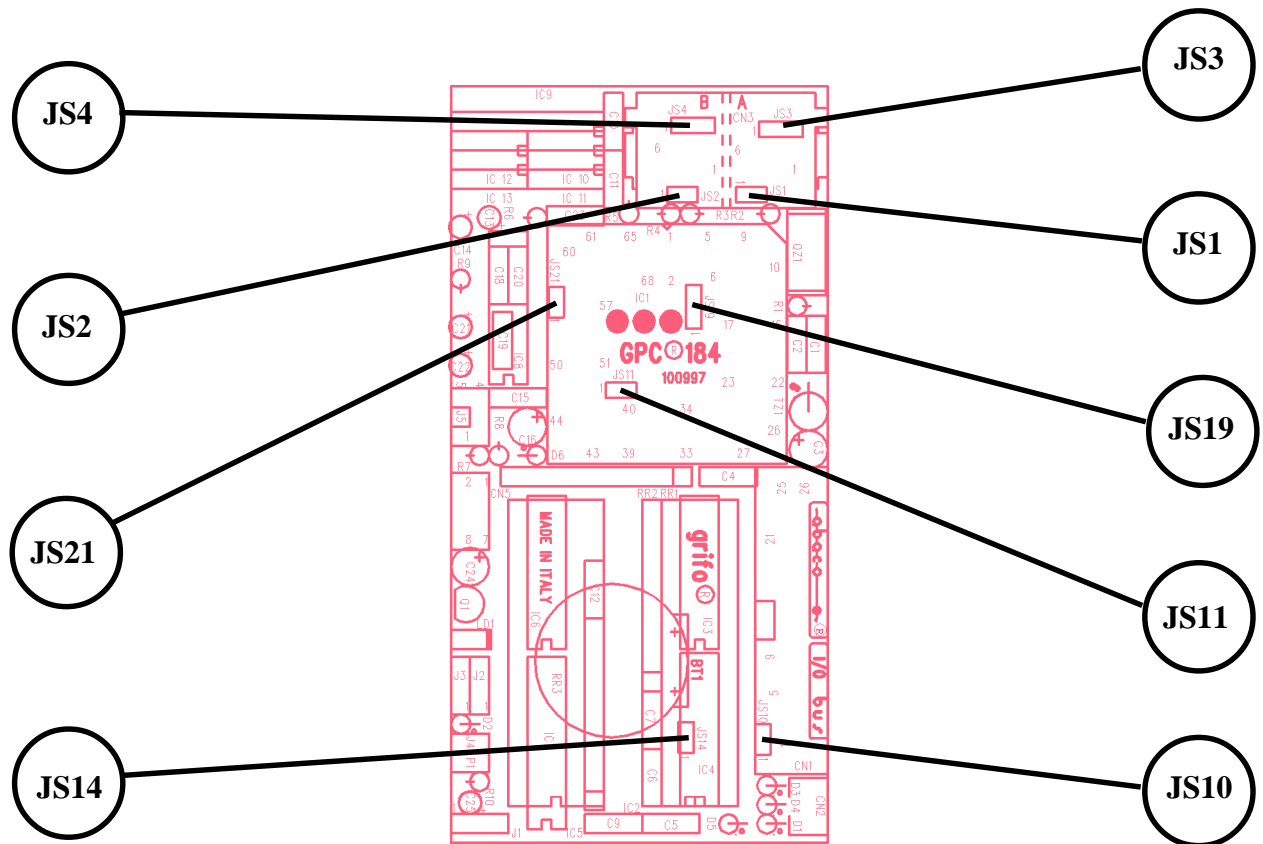
FIGURE 21: JUMPERS LOCATION (SOLDERING SIDE)

2 PINS JUMPERS

JUMPERS	CONNECTION	USE	DEF.
J4	not connected	It connects +5Vcc to the configuration input, selecting RUN mode.	*
	connected	It connects GND to the configuration input, selecting DEBUG mode.	
JS1	not connected	Matching with JS2, it does not connect the forcing and terminating circuitry to the RS 485 line or to the RS 422 receive line.	*
	connected	Matching with JS2, it does connects the forcing and terminating circuitry to the RS 485 line or to the RS 422 receive line.	
JS2	not connected	Matching with JS1, it does not connect the forcing and terminating circuitry to the RS 485 line or to the RS 422 receive line.	*
	connected	Matching with JS1, it does connect the forcing and terminating circuitry to the RS 485 line or to the RS 422 receive line.	
JS10	not connected	Disables the watch dog circuitry.	*
	connected	Enables the watch dog circuitry.	
JS11	not connected	It does not keep enabled the CPU CTS0 (=CTSB) handshake signal.	*
	connected	It keeps enabled the CPU CTS0 (=CTSB) handshake signal.	
JS14	not connected	It does not connect the on-board battery BT1 to the back up circuitry.	*
	connected	It connects the on-board battery BT1 to the back up circuitry.	
JS21	not connected	It does not connect CTS1 (=CTSA) handshake to the CPU.	
	connected	It connects CTS1 (=CTSA) handshake to the CPU.	*

FIGURE 22: 2 PINS JUMPERS TABLE

3 PINS JUMPERS

JUMPERS	CONNECTION	USE	DEF.
J1	position 1-2	It configures IC5 RAM for 128K.	*
	position 2-3	It configures IC5 RAM for 512K.	
J2	position 1-2	It configures IC2 for FLASH EPROM, matching with J3.	
	position 2-3	It configures IC2 for EPROM, matching with J3.	*
J3	position 1-2	It configures IC2 for FLASH EPROM, matching with J2.	
	position 2-3	It configures IC2 for EPROM, matching with J2.	*
JS3	position 1-2	It connects pin 1 of CN3A to GND.	*
	position 2-3	It connects pin 1 of CN3A to +5 Vcc.	
JS4	position 1-2	It connects pin 1 of CN3B to GND.	*
	position 2-3	It connects pin 1 of CN3B to +5 Vcc.	
JS19	Not connected	It does not connect the power failure circuitry.	*
	position 1-2	It connects the power failure circuitry to the CPU /INT0 signal.	
	position 2-3	It connects the power failure circuitry to the CPU /NMI signal.	

FIGURE 23: 3 PINS JUMPERS TABLE

5 PINS JUMPERS

JUMPERS	CONNECTION	USE	DEF.
J5	not connected	It selects the RS 232 protocol for serial line B.	*
	position 1-2 and 3-4	It selects the RS 485 (half duplex 2 wires) for serial line B.	
	position 2-3 and 4-5	It selects the RS 422 (full duplex or half duplex 4 wires) for serial line B.	

FIGURE 24: 5 PINS JUMPERS TABLE

BACK UP

 GPC® 184 ha an on board lithium battery BT1 for the back up of RAM and RTC content when power supply is switched off. Jumper JS14 connects phisically the battery so it can be disconnected to save its duration whenever back-up is not needed. By CN2 connector it is possible to connect an external battery: configuration of jumper JS14 does not affect the working of this battery and it can replace BT1 completely.
Please refer to the paragraph "ELECTRIC FEATURES" to choose the type of the external back up battery, to easily locate see figure 9.

MEMORY SELECTION

On **GPC® 184** can be mounted up to 1024K bytes of memory divided in several configurations, as described in the following table:

IC	DEVICE	SIZE	JUMPERS CONNECTION
2	EPROM	128K Byte	J2, J3 position 2-3
	EPROM	256K Byte	J2, J3 position 2-3
	EPROM	512K Byte	J2, J3 position 2-3
	FLASH EPROM	128K Byte	J2, J3 position 1-2
	FLASH EPROM	512K Byte	J2, J3 position 1-2
5	RAM	128K Byte	J1 position 1-2
	RAM	512K Byte	J1 position 2-3

FIGURE 25: MEMORY SELECTION TABLE

All the above mentioned devices must follow the JEDEC pin out specifications. Fo further informations about the signatures of the component that can be mounted please refer to the manifacturers documentations. To easily locate the memory devices please refer to figure 9.
The default configuration of the **GPC® 184** board memory is only 128K RAM; any different memory configuration can be realized by the User by mounting the opportune devices or can be requested in the ordering phase. Here follow the codes to order the optional memoy configurations:

.512   -> 512K RAM

For further informations about prices and options please contact **grifo**®.

INTERRUPTS

One of the most important **GPC® 184** features is the powerful interrupts management. Here is a short description of how the board's hardware interrupt signals can be managed; a more complete description of the hardware interrupts can be found in the microprocessor data sheets or in Appendix B of this manual.

- **ABACO®** I/O BUS   ->   It generates an /NMI interrupt, by the /NMI BUS signal of CN1 connector.
It generates an /INT0 non vectored interrupt, by the /INT BUS signal of CN1 connector.
- Real Time Clock   ->   It generates an /INT2 vectored interrupt.
- Auxiliary signals   ->   It generates an /INT1 vectored interrupt, by the homonymous CN5 signal.
- Power failure   ->   It generates an /NMI interrupt or an /INT0 non vectored interrupt.
- CPU inside devices   ->   They generate a vectored interrupt. Possible sources of internal interrupt events are: PRT 0, PRT 1, DMA 0, DMA 1, CSI/O, ASCI 0, ASCI 1.

The board features a chained priority structure that manages the case of contemporary interrupts. The addresses of the response procedures for vectored interrupts can be software programmed by the User acing on microprocessor inside registers. So the user program has always the possibility to react promptly to every external event, deciding also the priority of interrupts.

CONFIGURATION INPUTS

GPC® 184 board is provided with one jumper (J4), tipically used for system configuration purposes, that can be software acquired by the user program. The mostly implemented applications for this feature are: working conditions setting, selection of some on-board firmware parameters, etc. The configuration of the jumper generates a signal in complemented logic (0 -> means jumper connected 1 -> means jumper disconnected) that can be read performing a read operation atthe address assigned to the jumper by the on board control logic. Some software tools use this jumper for the selection between the RUN and DEBUG working modalities. For further informations please refer to the paragraph "I/O ADDRESSES", while to easily locate the jumper on the board please refer to figure 20.

SOLDER JUMPERS

The solder jumpers called **JSxx** are connected by a thin copper connection on the solder side. So, if one of their configurations has to be changed, the User must first cut this connection using a sharpened cutter, then make the new connection using a low power soldering tool and some non-corrosive tin.

SERIAL COMMUNICATION SELECTION

The communication serial line A is always buffered in RS 232 while the serial line B can be buffered in RS 232, RS 422, RS 485 or current loop electric standard. By hardware can be selected which one of these electric standard is used, through jumpers connection (as described in the previous tables). By software the serial lines can be programmed to operate with 7, 8, 9 bits per character, parity, between 1 and 2 stop bits at standard or no standard baud rates, through some CPU internal register setting.

Some components necessary for RS 422 and RS 485 communication are not mounted and not tested on the default configuration card, so the first not standard configuration must always be executed by **grifo®** technician; then the user can change himself the configuration, following the below description:

- SERIAL LINE B=ASCI 0 CONFIGURED IN RS 232 (default configuration)

			IC9	=	MAX 202 driver
J5	=	not connected	IC10	=	no component
JS1, JS2	=	not connected	IC11	=	no component
JS11	=	not connected	IC12	=	no component
			IC13	=	no component

- SERIAL LINE B=ASCI 0 CONFIGURED IN CURRENT LOOP (.CLOOP option)

			IC9	=	no component
J5	=	not connected	IC10	=	no component
JS1, JS2	=	not connected	IC11	=	HP 4200 driver
JS11	=	connected	IC12	=	no component
			IC13	=	HP 4100 driver

The current loop serial line is a passive line, so during connection the user must provide an external power supply, as described in figures 14 and 15. The current loop interface allows either point to point or network connection with 4 or 2 wires.

- SERIAL LINE B=ASCI 0 CONFIGURED IN RS 422 (.RS422 option)

			IC9	=	no component
J5	=	position 2-3, 4-5	IC10	=	SN 75176 driver
JS1, JS2	=	(*)	IC11	=	no component
JS11	=	connected	IC12	=	SN 75176 driver
			IC13	=	no component

With /RTSB=/RTS0 signal (managed by software with ASCI 0 registers) the user enables or disables the transmitter driver:

/RTS0 = low level = 0 logic state -> transmitter driver enabled
/RTS0 = high level = 1 logic state -> transmitter driver disabled

allowing either point to point (driver can be mantained always enabled) or network (driver is enabled only when the unit can hold the line) connection.
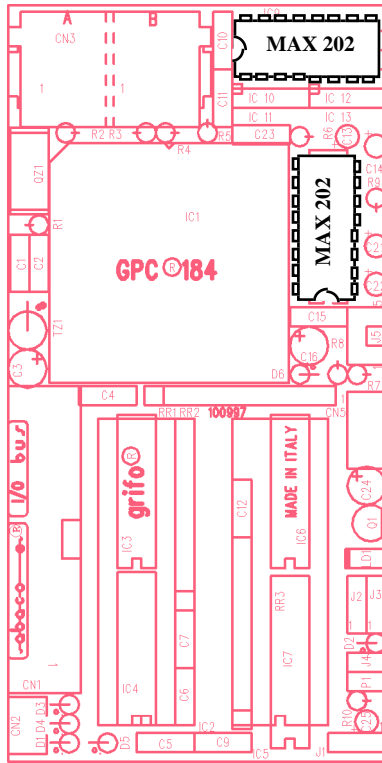
Serial B = ASCI 0 in RS 232
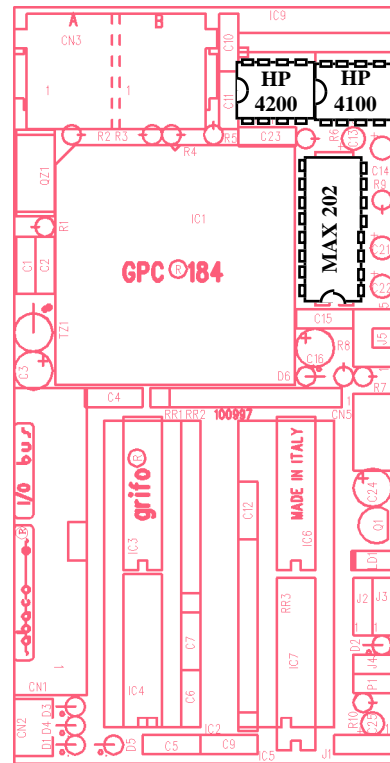
Serial B = ASCI 0 in current loop
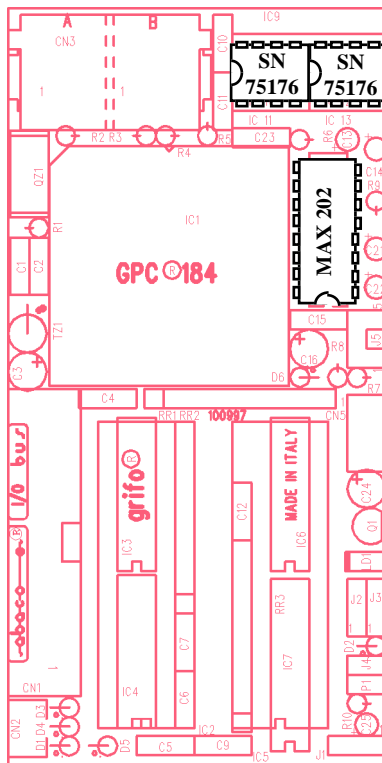
Serial B = ASCI 0 in RS 422
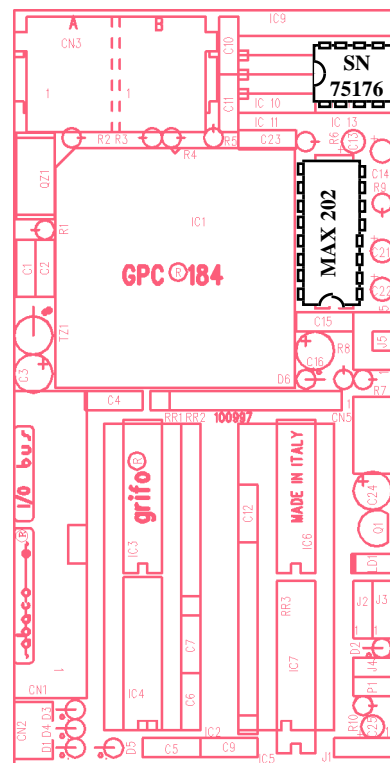
Serial B = ASCI 0 in RS 485

FIGURE 26: SERIAL COMMUNICATION DRIVER LOCATION

- SERIAL LINE B=ASCI 0 CONFIGURED IN RS 485 (.RS485 option)

			IC9	=	no component
J5	=	position 1-2, 3-4	IC10	=	no component
JS1, JS2	=	(*)	IC11	=	no component
JS11	=	connected	IC12	=	SN 75176 driver
			IC13	=	no component

With /RTSB=/RTS0 signal (managed by software with ASCI 0 registers) the user defines the RS 485 line direction:

/RTS0 = low level = 0 logic state -> RS 485 line transmitting
/RTS0 = high level = 1 logic state -> RS 485 line receiving

allowing network connection in a master multi slave system and multi master system. With RS 485 communication line, on CN3B the pins 4 and 5 have the double function of reception and transmission signals. All the transmitted characters are at the same time received when the user select RS 485 on **GPC® 184**; in this way the line conflicts can be immediately recognized by simply testing the received character after each transmission.

(*)   With jumper JS1 and JS2 the RS 422 receiving line or the RS 485 line can be terminated and forced with a suitable resistors circuit. The line termination must be added only at the beginning and at the end of the physical line, connecting both the jumpers. Normally these jumper must be connected in point to point network, or on the farther cards in multipoints network.

After reset or power on phase, the /RTS0 signal is forced to high level that mantain the RS 485 driver receiving and that disables the RS 422 transmitter driver; this condition eliminates any conflict on the communication line.

- SERIAL LINE A=ASCI 1

The output handshake signal RTSA is not software manageable so it is kept continuosly deactived = -10 Vdc. If this condition is incompatible with the system to be connected, perform the connection without this signal.

The JS21 jumper connects the handshake signal CTSA, converted by proper RS 232 driver, to CPU signal /CTS1. This last signal has a double functionality and it can work also as RXS, if the syncronous serial line available on CN5 is used, the JS21 jumper must be disconnected.

For further information about serial communication, please refer to connection examples described in figures 10÷13.

RESET AND WATCH DOG

The watch dog circuit of **GPC® 184** is really efficient and provided of easy software management. In details the most important features of this circuit are:
- astable functionality;
- intervent time of about 1,5 sec;
- hardware enable;
- software retrigger;
With the astable mode when the intervent time elapses, the circuit becomes active, it stay active till the end of reset time (about 200 msec) and after it is deactivated. Jumper JS10 connects the watch dog

circuit to reset circuit so when it is connected the watch dog is enabled and viceversa. The watch dog retrigger operation is described in chapter "WATCH DOG".

After an activation and following deactivation of /RESET signal, the card resumes execution of the program saved on IC2 (at address 0000H) starting from a global reset status of all the on board peripheral devices.

Please remember that the /RESET signal is connected to CN1 connector and that on **GPC® 184** are available other reset sources as the power good circuit and the contact P1. The two pins of P1 can be connected to a normally open contact (i.e. a push button) and when the contact is closed (shortcut of the two pins) the reset circuit is enabled.

POWER FAILURE

Together with the power management circuit of the CPU, it is also available an interesting power failure circuit, that can be connected to two different interruptsignals (/NMI or /INT0).

The power failure circuit checks the voltage connected to PFI pin of CN1 and whenever it reaches the threshold intervent value (**1,25V**), it enables its output and it captures CPU attention if JS19 is connected.

The common use of this circuit is to inform application program of the imminent power supply failure, so as to save the necessary status information. The PFI signal can be connected with advantages to power supply voltage through a dedicated resistors network; this one must provide the threshold intervent voltage with a sufficient advance in confront of /RESET activation. This advance must hold out to the end of interrupt service routine, so the resistors network values must be selected according with used power supply voltage, residue capacitor charge and interrupt service execution time.

SOFTWARE

A wide selection of software development tools can be obtained, allowing use of the module as a system for its own development, both in assembler and in other high level languages; in this way the User can easily develop all the requested application programs in a very short time. Generally all software packages available for the mounted microprocessor, or for the Z80 and Z180 family, can be used, i.e.:

GET 80

It is a complete program with Editor, Communication driver, and Mass Memory management for all Z80 family cards. This program, developed by **grifo**®, allows to operate in the best conditions when **GDOS**, **FGDOS** or **xGDOS MCI** software tools are used; **GET 80** is supplied when one of these tools is ordered and it is personalized with name and general data of the customer. A useful list of pull down menus and the possibility of using mouse, make program use very comfortable. **GET 80** program can be executed both on MS-DOS system and on **MACINTOSH** computers too, through SOFT-PC program. It is supplied on MS-DOS 3"1/2 floppy disk with the documentation on **GDOS 80** manual.

GDOS 184

It is a complete development Tool for **GPC**® **184** card. It is supplied together with **GET 80** program to allow an easy and immediate use of this powerful development system. GDOS is divided in two different structures : the first one works on PC maintaining serial communication with the second one. The second structure is on EPROM, it works on board of the card and it is an efficient operating system that executes many low level functions and, at the same time, it allows high level language use. The combination of the said structures results in a complete machine, in fact the card uses PC resources (like floppy disk, hard disk, printer, keyboard, monitor, etc.) as its own peripheral devices. This resulting "virtual machine" performs operation in a transparent way for the User, so this latter can operate with the same modality of standard PC languages. It is really interesting the compatibility of **GDOS** with all CP/M program and languages; so, if the User has experience, knowledge or developed applications with CP/M, he can use immediately **GDOS**, without any changes.
Moreover, **GDOS** can manage all memory devices exceeding 64K Bytes as RAM disk and ROM disk. The on board RAM devices can directly be used performing data read and write operations with the confortable file formats.
This software tools is supplied on EPROM with MS-DOS **GET 80** floppy disk, some examples, utilities and the operating system documentation.

FGDOS 184

It is really similar to **GDOS**, but it can program and erase the on board **FLASH EPROM** with the application program developed from the User. In this way the external EPROM programmer is not necessary to store definitely the program and it is possible to modify or to add code directly on the installed machine, through a portable PC.
This software tools is supplied on **FLASH EPROM** with **MS-DOS GET 80** floppy disk, some examples, utilities and the operating system documentation.

xGDOS MCI 184

It is a version of **GDOS** or **FGDOS** sofware tools, capable of **PCMCIA** Memory Card management. Using **MCI 64** card, the GDOS operating system manages memory cards as RAM disk or ROM disk. All applications with data acquisition and data logging can be realized with high level languages that manage data on files, with a fast development time and without any software complication.
This software tool is supplied on **EPROM** or **FLASH EPROM** with **MS-DOS GET 80** floppy disk, some examples, utilities and the operating system documentation.

PASCAL 80

It is an efficient and complete **PASCAL Compiler** for **Z80** family cards, with features similar to Release 3.0 of Borland **Turbo PASCAL**. It must work together with any **GDOS** version and it can exceed the 64K memory limits of Z80 family microprocessors through **OVERLAY** modality. More than one application program can be saved in RAM and/or ROM disks and subsequently executed. The terminal emulation of **GET 80** program support the typical full screen PASCAL Editor, including the attributes management.
This program is supplied as **ROM DISK** file in **GDOS EPROM** or **FLASH EPROM** and on MS-DOS floppy disk with some example and manual.

HI TECH C 80

Professional C Cross Compiler of Hi-Tech Software Inc. This Compiler is terribly fast and it generates a small quantity of code. This result is due to advanced techniques in optimizing the generated code based on Artificial Intelligence techniques which allow to get a very compact and very fast code. The package includes: IDE, Compiler, Code optimizer, Assembler, Linker, Remote Debugger and so on. This tool is Full ANSI/ISO Standard and Full Library Source Code. Once the porting of the Remote-Debugger module is done, this tool allows the user the software debugging directly on the hardware that he is experimenting. This type of specilization of the **Remote Debugger** is available from now ant it is supplied with all **grifo®** CPU cards. This software package is on 3" 1/2 diskettes under MS-DOS format along with user manual. This version supports these following CPUs: Z80, Z180, 84C011, 84C11, 84C013, 80C13, 84C015, 84C15, 64180, NCS800, Z181, Z182.

DDS MICRO C 85: low cost ross compiler for C source program. It is a powerful software tool that includes editor, C compiler (integer), assembler, optimizer, linker, library, and remote debugger, in one easy to use integrated development environment. There are also included the library sources and many utilities programs.

NOICE: It is a PC hosted debugger consists of a target specific DOS program, NOICExxx.EXE, and a target resident monitor program. The two programs comunicate via RS 232. NOICE includes: source level debug; a disassembler; a file viewer; memory display and editing; a virtually unlimited number of breakpoints; hardware free single step; definition of symbols; the ability to record and play back files of commands; on line help.

RSD 184

This software tools is a **Remote Symbolic Debugger** with two operating mode. The first one is a monitor debugger modality with software emulation on P.C.; the second is a remote monitor debugger modality that execute code directly on the card. Trough serial communication the User can: down load an HEX file and associated symbol table, debug code in symbolic mode, execute code in step to step mode or in real time mode, set breakpoint, dump and modify memory and registers, etc. RSD software tool supports both **Z80** and **Z180** instrunction sets. Really interesting is the program execution management, in fact many hardware and software breakpoint are supported. **RSD** can be used together with assembler tools, like **ZASM 80**, and C Compiler **CC 80**.
It is supplied on EPROM and on MS-DOS floppy disk with technical manual.

ZASM 80

It is a macro cross assemler that operates on any PC with MS-DOS operating system. It supports both **Z80** and **Z180** instrunction sets. The generated code can be debugged on PC, through software simulation, or directly on target card, through remote modality, using **RSD** software tools. ZASM 80 is compatible with C Compiler **CC 80** of which it assemble the compilation result.
It is supplied on MS-DOS floppy disk with technical manual.

CC 80

It is a complete **C Compiler** with ANSI/ISO standard, provided of floating point procedure, that can generate code for Z80 and Z180 family microprocessors. It works together with cross assembler **ZASM 80** and Symbolic Debugger **RSD**.
It is supplied on MS-DOS floppy disk with technical manual.

EMBEDDED PASCAL Z80 - Z180

Cross compiler for PASCAL source program. It is a powerful software tool that includes editor, PASCAL compiler, assembler, optimizer, library, included in an easy to use integrated development environment for Windows 95 and NT. Many memory models and data types are supported and sources of library are provided too.

DEVICES MAP AND ADDRESSES

INTRODUCTION

In this chapter are reported all informations about card use, related to hardware features of **GPC® 184**. For example the registers addresses, the memory and peripheral devices allocation are described below.

ON BOARD DEVICES ADDRESSES

The on board devices addresses are managed from a control logic, realized with CMOS gates. This control logic allocates memory and peripheral devices with very low power consumption and simple software management.

The control logic has been designed to control the memory and the I/O peripherals addresses in a separate manner. The Z180 microprocessor <u>directly</u> addresses 64K bytes of memory and 256 I/O registers and the control logic provides on board memory and peripheral devices allocattion inside these addresses spaces. The maps management is completely driven by software through the MMU circuit programmation: the used memory can be selected and divided in some size definible segments. About I/O maps the control logic avoids every conflicts problems between CPU internal and external peripherals.

Summarizing the control logic allocates:

- **ABACO®** I/O BUS
- Up to 512K bytes of EPROM or FLASH EPROM on IC 2
- Up to 512K of RAM on IC 5
- Configuration jumper J4
- Real Time Clock
- Watch dog circuit

The addresses of all these devices are described in the following paragraphs and can't be set with different values. If some different specific maps are required, please contact directly **grifo®**.

ABACO® I/O BUS ADDRESSES

The **GPC® 184** control logic defines **ABACO®** I/O BUS addresses and only these addresses must be used to manages correctly the BUS. As described in following "I/O ADDRESSES" table, only the addresses from 80H to FFH are available for **ABACO®** I/O BUS. Any I/O operations at each one of these adrresses enables the /IORQ signal and the other control signals of CN1 connector. In the addresses subrange 80H÷9FH it is also enabled the /CS1 signal, used for external peripheral devices coded selection.

MEMORY ADDRESSES

The maximum 1024K bytes of memory, are allocated on the board as below described:

- Up to 512K bytes of EPROM or FLASH EPROM allocated in memory space.
- Up to 512K bytes of RAM allocated in memory space.

GPC® 184 can directly manage no more than 64K bytes of memory that is the microprocessor logic addressable space. On the board this logic space can be divided in three separated segments: each ones of these segment have software programmable dimension and start address. The CPU internal MMU circuit divides the logical space directly managed by the microprocessor into these 3 segments and it allocates them in the physical memory devices space. The MMU circuit is software programmable with I/O operations to three specific registers in a fast and comfortable manner. So MMU allows software managements of a physical memory space very larger than microprocessor memory space.

The following figure describe available memory configurations; for further informations on MMU use and segments meaning (Common Area 0, Common Area 1 and Bank Area), please refer to appendix B, while for memory devices location and configuration refer to figures 9 and 25.

After power on or reset phase, the MMU circuit allocates all the logical 64K space at the beginning of the physical space, therefore the card starts execution of code saved at address 0000H of EPROM or FLASH EPROM on IC2.

The memory size and type configurations must be selected both according to used software tools and User requests and/or application features. The card configuration for the selected memory device types and sizes on IC2 and IC5 sockets, is performed with some comfortable jumpers, as described in "MEMORY SELECTION" chapter.

Some software tools, i.e. GDOS, self manage the MMU circuit to use all the available memories at high level witout User intervention.
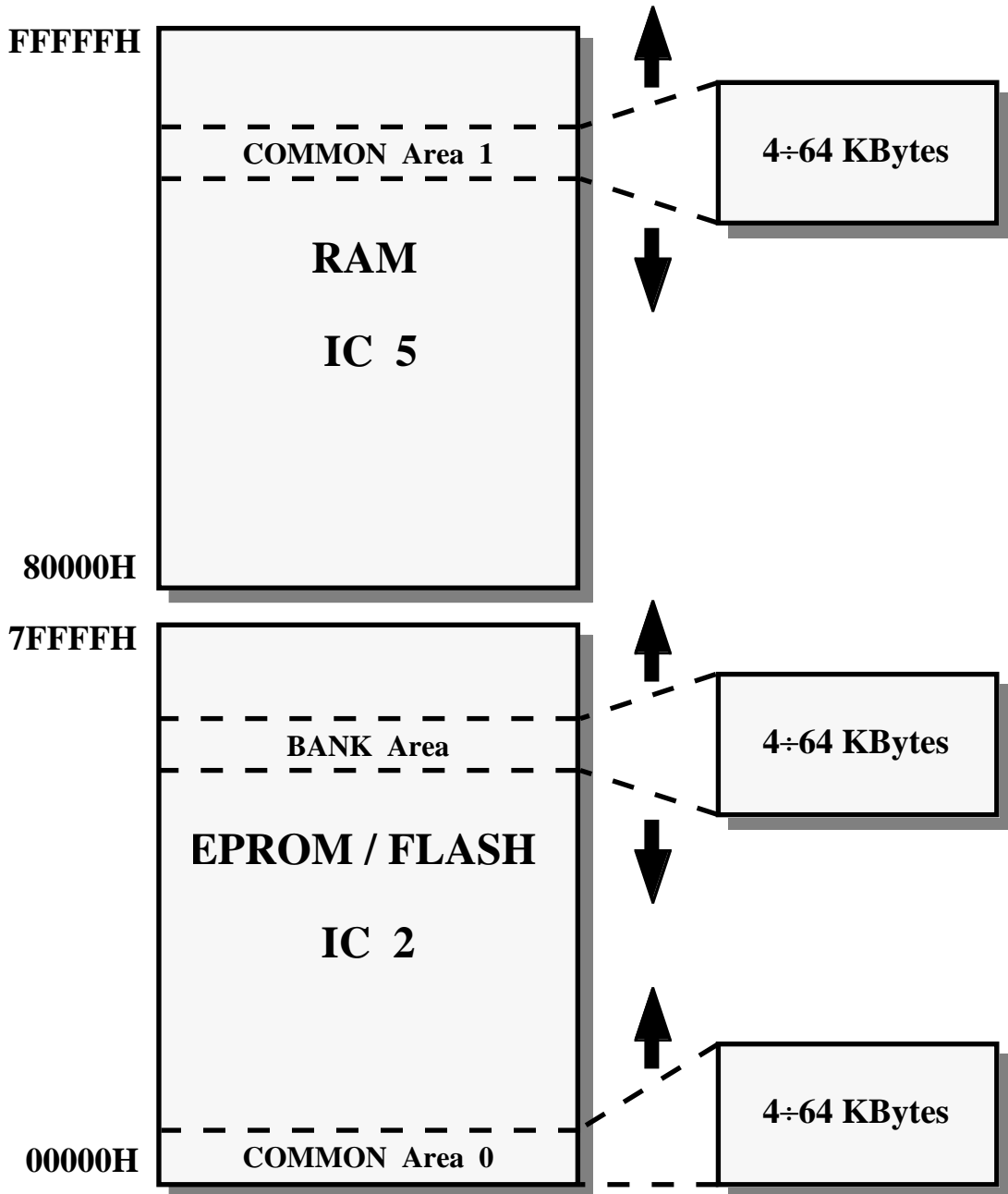
FIGURE 27: MEMORY ALLOCATION

I/O ADDRESSES

The on board control logic manages the allocation of all the peripheral devices registers in the microprocessor I/O space, that is 256 bytes long. Next table shows names, addresses, meanings and directions of peripheral device registers (including the internal microprocessor ones). For a detailed description of the registers function, please refer to next chapter "PERIPHERAL DEVICES SOFTWARE DESCRIPTION".

DEVICES	REG.	ADDRESS	R/W	FUNCTION
ASCI	ASCI	00H÷09H	R/W	Internal microprocessor registers, for asyncronous serial line
CSI/O	CSIO	0AH÷0BH	R/W	Internal microprocessor registers, for Clocked Serial I/O Port management
TIMER	TMR	0CH÷1FH	R/W	Internal microprocessor registers, for Timer/Counter management
DMA	DMA	20H÷32H	R/W	Internal microprocessor registers, for DMA lines management
INTERRUPT	INT	33H÷35H	R/W	Internal microprocessor registers, for interrupts management
REFRESH	RCR	36H÷37H	R/W	Internal microprocessor registers, for Refresh circuit management
MMU	MMU	38H÷3AH	R/W	Internal microprocessor registers, for Memory Management Unit management
I/O	ICR	3BH÷3FH	R/W	Internal microprocessor registers, for I/O control management
REAL TIME CLOCK	SEC1	40H	R/W	Data register for seconds units
	SEC10	41H	R/W	Data register for seconds decines
	MIN1	42H	R/W	Data register for minutes units
	MIN10	43H	R/W	Data register for minutes decines
	HOU1	44H	R/W	Data register for hours units
	HOU10	45H	R/W	Data register for hours decines and AM/PM
	DAY1	46H	R/W	Data register for day units
	DAY10	47H	R/W	Data register for day decines
	MON1	48H	R/W	Data register for month units
	MON10	49H	R/W	Data register for month decines
	YEA1	4AH	R/W	Data register for year units
	YEA10	4BH	R/W	Data register for year decines
	WEE	4CH	R/W	Data register for week day
	REGD	4DH	R/W	Control register D
	REGE	4EH	R/W	Control register E
	REGF	4FH	R/W	Control register F
C. JUMPER	RUNDEB	60÷7FH	R	Register for configuration jumper acquisition
W. DOG	RWD	60÷7FH	R	Register for watch dog retrigger
ABACO ®	/CS1	80H÷9FH	R/W	**ABACO** ® I/O BUS addresses that enable /CS1 signal
I/O BUS	I/OBUS	80H÷FFH	R/W	**ABACO** ® I/O BUS addresses

FIGURE 28: I/O ADDRESSES TABLE

PERIPHERAL DEVICES SOFTWARE DESCRIPTION

In the previous paragraphes are described the external registers addresses, while in this one there is a specific description of registers meaning and function (please refer to I/O addresses table, for the registers names and addresses values). For a more detailed description of the devices, please refer to manufacturing company documentation; for microprocessor internal peripheral devices, not described in this paragraph, refer to appendix B. In the following paragraphs the D7÷D0 indication denotes the eight bits of the combination used in I/O operations.

REAL TIME CLOCK

This peripherial is allocated in 16 consecutives I/O addresses, 3 of which correspond to status registres while the remaining 13 are for datas. Data registers are used both for read operations (of the current time and date) and write operations (to initialize the time and date) just like the status registers which are used in write operations (to program the operative mode) and in read operations (to acquire the RTC status). Here follows a list of the RTC data registers' meanings:

SEC1	- Units of seconds	- 4 least significant bits of SEC1.3÷SEC1.0
SEC10	- Decines of secondi	- 3 least significant bits of SEC10.2÷SEC10.0
MIN1	- Units of minutes	- 4 least significant bits of MIN1.3÷MIN1.0
MIN10	- Decines of minutes	- 3 least significant bits of MIN10.2÷MIN10.0
HOU1	- Units of hours	- 4 least significant bits of HOU1.3÷HOU1.0
HOU10	- Decines of hours	- 2 least significant bits of HOU10.1÷HOU10.0
		The third bit of HOU10.2 indicates AM/PM
DAY1	- Units of day number	- 4 least significant bits of DAY1.3÷DAY1.0
DAY10	- Decines of day number	- 2 least significant bits of DAY10.1÷DAY10.0
MON1	- Units of month	- 4 least significant bits of MON1.3÷MON1.0
MON10	- Decines of month	- 1 least significant bit of MON10.0
YEA1	- Units of year	- 4 least significant bits of YEA1.3÷YEA1.0
YEA10	- Decines of year	- 4 least significant bits of YEA10.3÷YEA10.0
WEE	- Day of the week	- 3 least significant bits of WEE.2÷WEE.0

For this last register the three least significant bits mean:

WEE.2	WEE.1	WEE.0	Day of the week
0	0	0	Sunday
0	0	1	Monday
0	1	0	Tuesday
0	1	1	Wednesday
1	0	0	Thursday
1	0	1	Friday
1	1	0	Saturday

The meaning of the three control registers is:

bit 7 6 5 4 3 2 1 0

REG D = NU NU NU NU 30S IF B H

where:

NU	= Not used.
30S	= If high (1) itallowes a 30 seconds correction of the time. Once set the RTC seconds are reset and the minutes increased, if the previous seconds was equal or greater than 30.
IF	= It manages the RTC interrupt status. When read it shows the current interrupt status (1 active and viceversa), when reset to 0 it disables the RTC interrupt signal if the interrupt mode is selected.
B	= Indictes whether R/W operations can be performed on the registers:
	1 -> operations are not permitted and viceversa.
H	= If high (1) it stores the written time and date.

bit 7 6 5 4 3 2 1 0

REG E = NU NU NU NU T1 T0 I M

where:

NU		= Not used.
T1	T0	= Determin the duration of the internal counters interrupt cycle.
0	0	-> 1/64 second
0	1	-> 1 second
1	0	-> 1 minute
1	1	-> 1 hour
I		= It defines the interrupt operating mode:

	1 -> it selects interrupt mode: when the selected duration elapses the interrupt is enabled and then disabled only with a reset of bit IF of control register D;
	0 -> it selects the standard mode: when the selected duration elapses the interrupt is enabled and then disabled only after 7,8 msec.
M	= It mask the interrupt status:
	1 -> interrupt masked: the RTC interrupt signal is always disabled;
	0 -> interrupt not masked: the RTC interrupt signal reflects interrupt status.

bit 7 6 5 4 3 2 1 0

REG F = NU NU NU NU T 24/12 S R

where:

NU	= Not used.
T	= It determines from which internal counter to take the counting signal:
	1 -> main counter (fast counter for test);
	0 -> 15th counter.
24/12	= It determines the hours counting mode:
	1 -> 0÷23;
	0 -> 1-12 with AM/PM.
S	= If high (1) it stops the clock time counting until the next enabling (0).
R	= If high (1) it resets all the internal counters.

WATCH DOG

Retrigger operation of **GPC® 184** watch dog circuit is performed with a simple read operation at the address of register RWD. This register shares the same address of other on board peripherals, but no conflict are generated in fact retrigger operation is an input operation and the read data has no meaning. To avoid watch dog activation it is necessary to retrigger its circuit at regular time periods and the duration of these periods must be smaller than intervent time. If retrigger doesn't happen as before described and JS14 is connected, when intervention time is elapsed, the card is reset. The default intervention time is about 1.5 sec.

CONFIGURATION JUMPER

The J4 configuration jumper installed on the **GPC® 184** board can be acquired simply by performing a read operation from RUNDEB registers and masking bit D7. The value is in complemented logic, this means that the underlined connected jumper gives a logic value "0" while if the jumper is not connected the logic value read will be "1".
This jumper switches between theRUN (not connected) or the DEBUG (connected) mode, a feature used by some **grifo®** software tools.

CPU INTERNAL PERIPHERALS

The decriptions of the registers that manages the CPU internal peripheral devices (ASCI, CSI/O, TIMER, DMA, INTERRUPT, REFRESH, MMU, I/O) is available in the appendix B. Whenever this informations are still insufficient, please refer to specific documentation of the manufacturing company.

EXTERNAL CARDS

GPC® 184 can be connected to a wide range of block modules and operator interface system produced by **grifo®**, or to many system of other companies. The on board resources can be expanded with a simple connection to the numerous peripheral **grifo®** boards, both intelligent and not, thanks to its standard **ABACO®** I/O BUS connector. Even single EURO cards with BUS **ABACO®** can be connected, by using the proper mother boards.

Hereunder some of these cards are briefly described; ask the detailed information directly to **grifo®**, if required.

QTP G26
Quick Terminal Panel - LCD Graphic, 26 keys

Intelligent user panel equipped with graphic LCD display 240x128 pixel, CFC backlit; optocoupled RS 232 line and additional RS 232, RS 422, RS 485 or current loop serial line. Indipendent optional CAN line controller; serial E2 for set up; RTC and RAM Lithium backed; primary graphic objects; possibility of renaming keys, LEDs and panel name by inserting label with new name into the proper slot; 26 Keys and 16 LEDs with blinking attribute and buzzer manageable by software; built in power supply; reader of magnetic badge, smart card and relay option.

ADC 812
Analog to Digital Converter, 12 bits, multi range

DAS (Data Acquisition System) multi range 8 channels 12 bit A/D conversion lines; track and hold; 6μs conversion time; range ±10, ±5, +10, +5Vdc or 0÷20, 4÷20mA; analog inputs connections through quick terminal screw connectors; **ABACO®** I/O BUS interface; direct mounting for DIN 247277-1 and 3 rails; 4 type dimension.

DAC 212
Digital to Analog Converter 12 bits, multi range

Digital to Analog converter; multi range 2 channels 12 bits ± 10, +10 Vdc output; analog outputs connections through quick terminal screw connectors; **ABACO®** I/O BUS interface; direct mounting for DIN 247277-1 and 3 rails; 4 type dimension.

CAN 14
Control Area Network, 1 channel, galvanically insulated

UART CAN SJA1000; 1 serial channels galvanically insulated; **ABACO®** I/O BUS interface; 4 type dimension; support of CAN 2.0B protocol; transfer rate up to 1M bit/sec; direct mounting for DIN 247277-1 and 3 rails.

ETI 324
Encoder Timer I/O, 3 counters, 24 I/O

Three timers counters driven by 82C54; bidirectional optocoupled encoder input; direction identifier; phases multiplier; 24 digital lines driven by 82C55 on two standard I/O **ABACO®** connectors; **ABACO®** I/O BUS interface; direct mounting for DIN 247277-1 and 3 rails; 4 type dimension.

ABB 05
ABACO® Block BUS 5 slots

5 slots **ABACO®** mother board with power supply. Double power supply built in; 5Vdc 2,5A section for powering the on board logic; second section at 24Vdc 400mA galvanically coupled, for the optocoupled input lines. Auxiliary connector for **ABACO®** I/O BUS. Connection for DIN Ω rails.
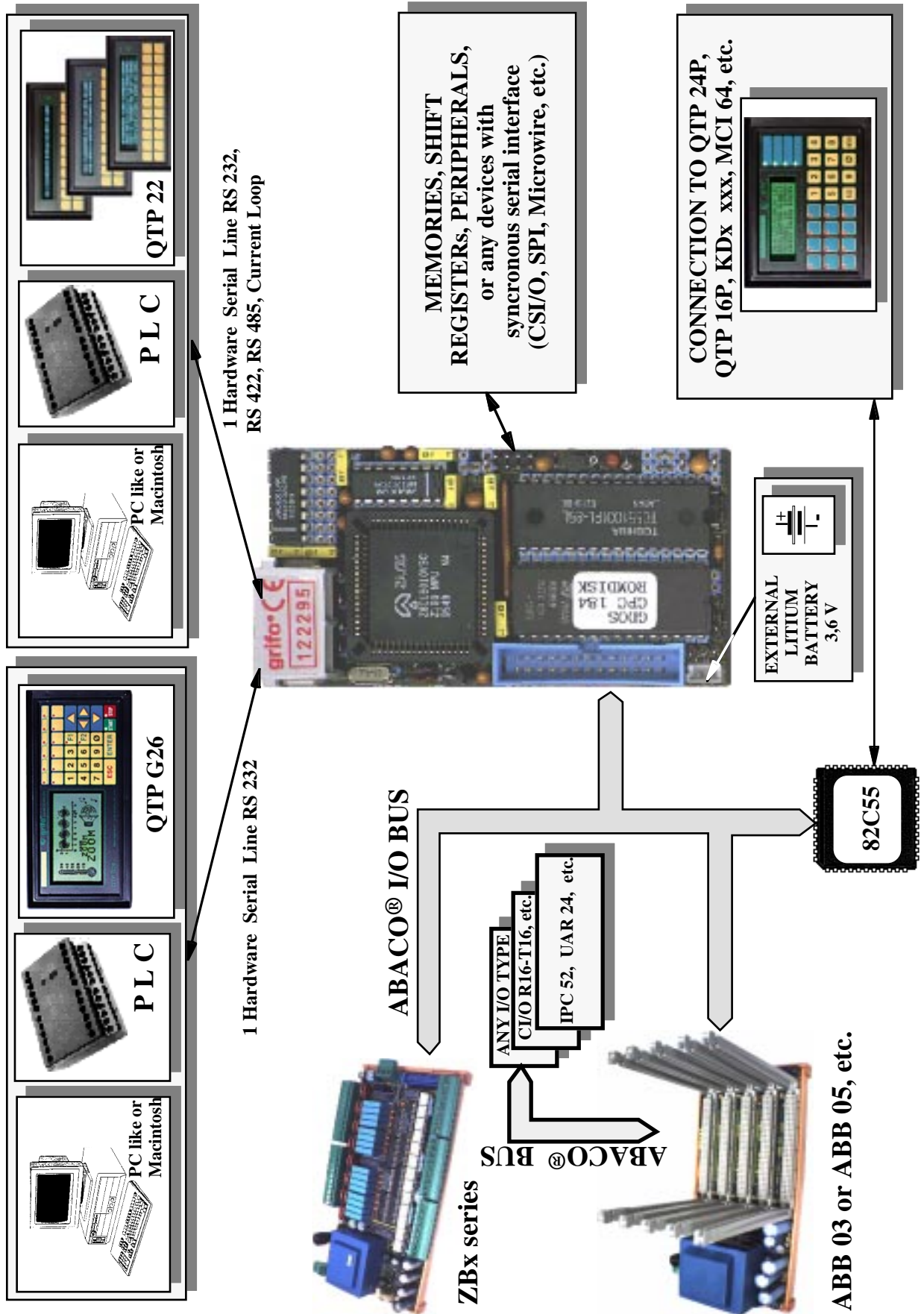
FIGURE 29: AVAILABLE CONNECTIONS DIAGRAM

ABB 03
ABACO® Block BUS 3 slots
3 slots **ABACO®** mother board; 4 TE pitch connectors; **ABACO®** I/O BUS connector; screw terminal for power supply; connection for DIN C type and Ω rails.

ZBT xxx
Zipped BLOCK Transistors xy Input + yz Output
Peripheral cards family having xy optocoupled inputs and yz 3A open collector transistor outputs; plastic container for Ω rails mounting; double power supply, galvanically coupled, for the optocoupled input lines and for the logic plus external card. I/O lines displayed by LEDs; transistors outputs equipped with protection against inductive loads; I/O connections available on easy quick terminal connectors; interface to **ABACO®** I/O BUS. The following models are available: xxx=324 -> 32 In and 24 Out; xxx=246 -> 24 In and 16 Out; xxx=168 -> 16 In and 8 Out; xxx=84 -> 8 In and 4 Out.

IBC 01
Interface Block Comunication
Conversion card for serial communication, 2 RS 232 lines; 1 RS 422-485 line; 1 optical fibre line; selecatble DTE/DCE interface; quick connection for DIN 46277-1 and 3 rails.

FBC xxx
Flat Block Contactxxx pins
This interconnection system "wire to board" allows the connection to many type of flat cable connectors to terminal for external connections. Connection for DIN Ω rails.

BIBLIOGRAPHY

In this chapter there is a complete list of technical books, where the user can find all the necessary documentations on the components mounted on **GPC® 184**.

Data book Manuale TEXAS INSTRUMENTS:	*The TTL Data Book - SN54/74 Families*
Data book Manuale TEXAS INSTRUMENTS:	*RS-422 and RS-485 Interface Circuits*
Data book NEC:	*Memory Products*
Data book HEWLETT PACKARD:	*Optoelectronics Designer's Catalog*
Data book MAXIM:	*New Releases Data Book - Volume 4*
Data book MAXIM:	*Integrated Circuits Data Book*
Data book SEIKO EPSON:	*REAL TIME CLOCK MODULE RTC-72421 Application manual*
Data book ZILOG:	*Z80180 Z180 MPU Technical Manual*
Data book TOSHIBA:	*Mos Memory Products*

For further information and upgrades please refer to specific internet web pages of the manufacturing companies.

APPENDIX A: CARD MECHANICAL MOUNTING

The **GPC® 184** can be physically mounted in two different manner. The first is the piggy back mounting (stack trough mode) that use the two connectors CN1 and CN5 for the interface with a user developed board. This connectors lead out of 7 mm on solder side and the user board must have proper female strip connectors (2,54 mm pitch) where the card can be plugged in, obtaining a single system.

The second mode expect a mounting inside a proper plastic container for a direct mounting on DIN 247277-1 and 3 Ω rails; if the card is used with some other peripheral cards (i.e. **ZBR xxx** or **ZBT xxx**), a single longer container can be used obtaining a single module. The described plastic container code is 414487 type RS/100 by Weidmuller and it can be ordered to **grifo®** as **WM.lll** options, where lll is the required lenght. By selecting this mounting the electric connection between **GPC® 184** and other peripheral cards is performed with a flat cable that must be really short.

In the following figures are described the module dimensions with the connector positions and some immages that illustrate the connection modes.
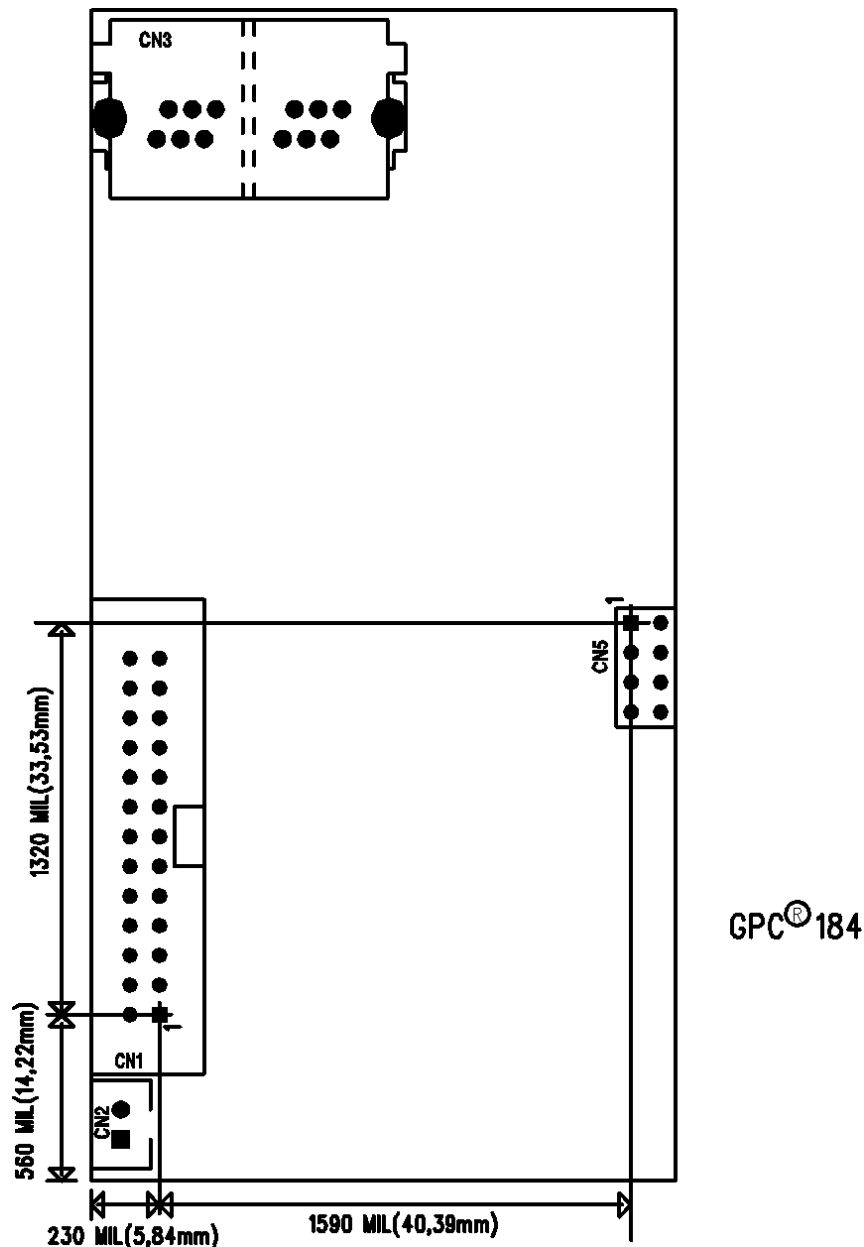

FIGURE A1: MODULE DIMENSION FOR PIGGY BACK MOUNTING
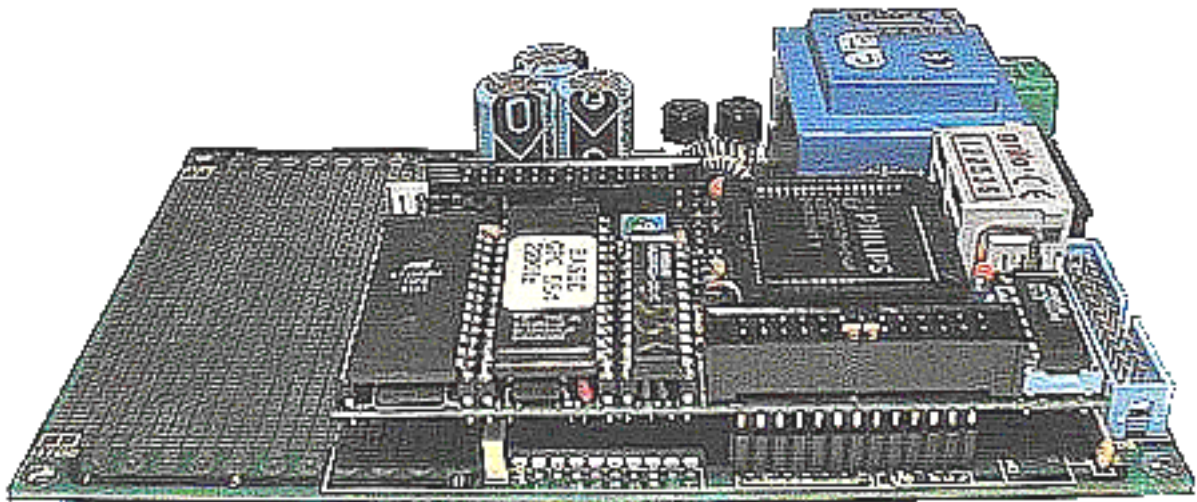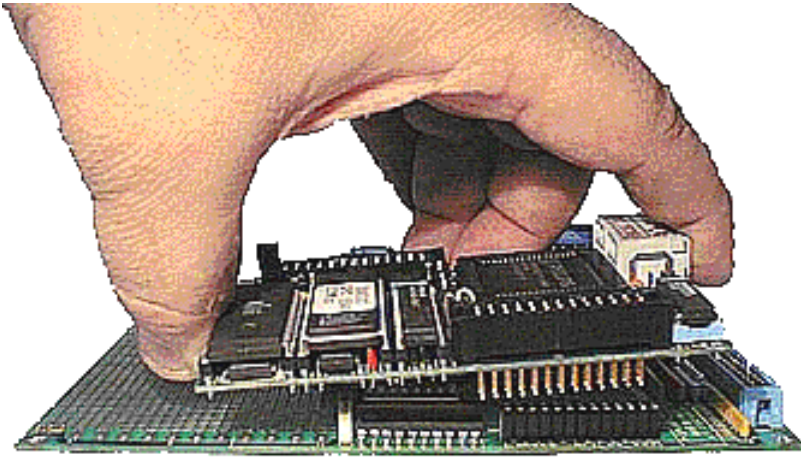
FIGURE A2: PIGGY BACK MOUNTING
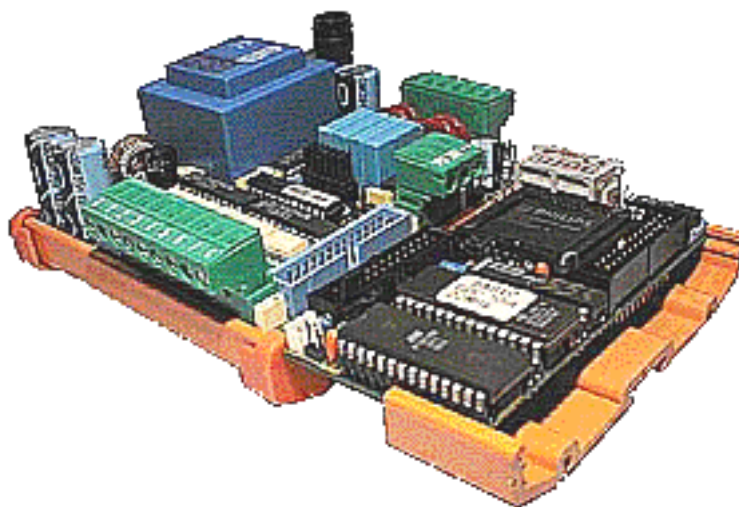
FIGURE A3: WEIDMULLER RAIL MOUNTING

APPENDIX B: ON BOARD DEVICES DESCRIPTION

Z80180/Z8S180/Z8L180
Enhanced Z180 Microprocessor

Notes: All Signals with a preceding front slash, "/" are active Low, for example, B/W (WORD is active Low); /B/W (BYTE is active Low, only). Alternatively, an overslash may be used to signify active Low, for example $\overline{WR}$

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}
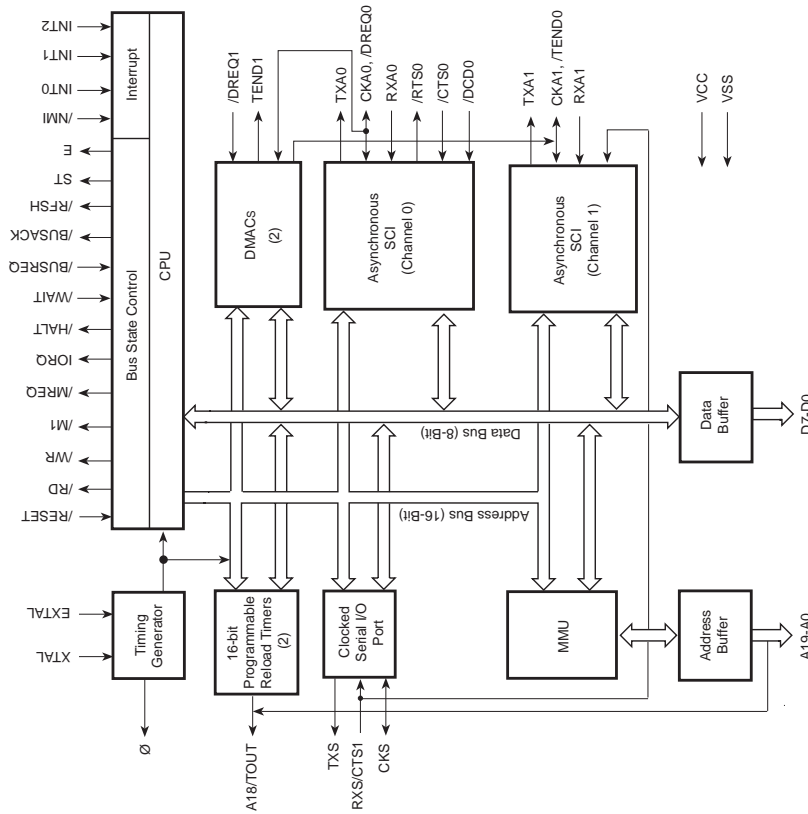
Figure 1. Z80180/Z8S180/Z8L180 Functional Block Diagram

PRELIMINARY PRODUCT SPECIFICATION

Z80180/Z8S180/ Z8L180 SL1919
ENHANCED Z180 MICROPROCESSOR

FEATURES

- Code Compatible with Zilog Z80® CPU
- Extended Instructions
- Two Chain-Linked DMA Channels
- Low Power-Down Modes
- On-Chip Interrupt Controllers
- Three On-Chip Wait-State Generators
- On-Chip Oscillator/Generator
- Expanded MMU Addressing (up to 1 MB)
- Clocked Serial I/O Port

- Two 16-Bit Counter/Timers
- Two Enhanced UARTs (up to 512 Kbps)
- Clock Speeds: 6, 8, 10, 20, 33 MHz
- Operating Range: 5V (3.3V @ 20 MHz)
- Operating Temperature Range: 0°C to +70°C
- -40°C to +85°C Extended Temperature Range
- Three Packaging Styles
  - 68-Pin PLCC
  - 64-Pin DIP
  - 80-Pin QFP

GENERAL DESCRIPTION

The enhanced Z80180/Z8S180/Z8L180™ significantly improves on the previous Z80180 models while still providing full backward compatibility with existing Zilog Z80 devices. The Z80180/Z8S180/Z8L180 now offers faster execution speeds, power saving modes, and EMI noise reduction.

This enhanced Z180 design also incorporates additional feature enhancements to the ASCIs, DMAs, and I_{CC} STANDBY Mode power consumption. With the addition of "ESCC-like" Baud Rate Generators (BRGs), the two ASCIs now have the flexibility and capability to transfer data asynchronously at rates of up to 512 Kbps. In addition, the ASCI receiver has added a 4-byte First In First Out (FIFO) which can be used to buffer incoming data to reduce the incidence of overrun errors. The DMAs have been modified to allow for a "chain-linking" of the two DMA channels when set to take their DMA requests from the same peripherals device. This feature allows for non-stop DMA operation between the two DMA channels, reducing the amount of CPU intervention (Figure 1).

Not only does the Z80180/Z8S180/Z8L180 consume less power during normal operations than the previous mode it has also been designed with three modes intended to further reduce the power consumption. Zilog reduced I_{CC} power consumption during STANDBY Mode to a minimum of 10 µA by stopping the external oscillators and internal clock. The SLEEP mode reduces power by placing the CPU into a "stopped" state, thereby consuming less current while the on-chip I/O device is still operating. The SYSTEM STOP mode places both the CPU and the on-chip peripherals into a "stopped" mode, thereby reducing power consumption even further.

A new clock doubler feature has been implemented in the Z80180/Z8S180/Z8L180 device that allows the programmer to double the internal clock from that of the external clock. This provides a systems cost savings by allowing the use of lower cost, lower frequency crystals instead of the higher cost, and higher speed oscillators.

The Enhanced Z180 is housed in 80-pin QFP, 68-pin PLCC, and 64-pin DIP packages.

HALT and Low-Power Operating Modes. The Z80180/Z8S180/Z8L180 can operate in seven modes with respect to activity and power consumption:

- Normal Operation
- HALT Mode
- IOSTOP Mode
- SLEEP Mode
- SYSTEM STOP Mode
- IDLE Mode
- STANDBY Mode (with or without QUICK RECOVERY)

Normal Operation. The Z80180/Z8S180/Z8L180 processor is fetching and running a program. All enabled functions and portions of the device are active, and the HALT pin is High.

HALT Mode. This mode is entered by the HALT instruction. Thereafter, the Z80180/Z8S180/Z8L180 processor continually fetches the following opcode but does not execute it, and drives the HALT, ST and M1 pins all Low. The oscillator and PHI pin remain active, interrupts and bus granting to external masters, and DRAM refresh can occur and all on-chip I/O devices continue to operate including the DMA channels.

The Z80180/Z8S180/Z8L180 leaves HALT mode in response to a Low on RESET, on to an interrupt from an enabled external request on INT0, INT1, or INT2. In case of an interrupt, the return address will be the instruction following the HALT instruction; at that point the program can either branch back to the HALT instruction to wait for another interrupt, or can examine the new state of the system/application and respond appropriately.
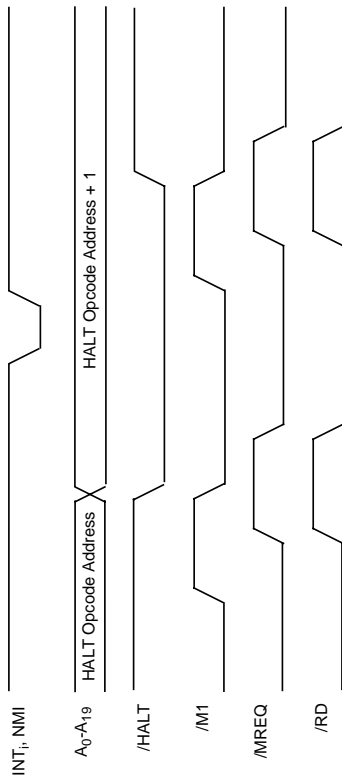

Figure 13. HALT Timing

(Signals: INT_i, NMI / A_0-A_{19} (HALT Opcode Address, HALT Opcode Address + 1) / /HALT / /M1 / /MREQ / /RD)

SLEEP Mode. This mode is entered by keeping the IOSTOP bit (ICR5) bits 3 and 6 of the CPU Control Register (CCR3, CCR6) all zero and executing the SLP instruction. The oscillator and PHI output continue operating, but are blocked from the CPU core and DMA channels to reduce power consumption. DRAM refresh stops but interrupts and granting to external master can occur. Except when the bus is granted to an external master, A19-0 and all control signals except /HALT are maintained High. /HALT is Low. I/O operations continue as before the SLP instruction, except for the DMA channels.

The Z80180/Z8S180/Z8L180 leaves SLEEP mode in response to a low on /RESET, an interrupt request from an on-chip source, an external request on /NMI, or an external request on /INT0, 1, or 2.

If an interrupt source is individually disabled, it cannot bring the Z80180/Z8S180/Z8L180 out of SLEEP mode. If an interrupt source is individually enabled, and the IEF bit is 1 so that interrupts are globally enabled (by an EI instruction), the highest priority active interrupt will occur, with the return address being the instruction after the SLP instruction. If an interrupt source is individually enabled, but the IEF bit is 0 so that interrupts are globally disabled (by a DI instruction), the Z80180/Z8S180/Z8L180 leaves SLEEP mode by simply executing the following instruction(s).

This provides a technique for synchronization with high-speed external events without incurring the latency imposed by an interrupt response sequence. Figure 14 shows the timing for exiting SLEEP mode due to an interrupt request. Note that the Z80180/Z8S180/Z8L180 takes about 1.5 clocks to restart.

Figure 14. SLEEP Timing

(Cycles: SLP 2nd Opcode Fetch Cycle, SLEEP Mode, Opcode Fetch or Interrupt Acknowledge Cycle; T_2 T_3 T_1 T_2 T_S T_S T_S T_1 T_2 T_3. Signals: φ / INT_i, /NMI / A_0-A_{19} (SLP 2nd Opcode Address, FFFFH) / /HALT / M1)

IOSTOP Mode. IOSTOP mode is entered by setting the IOSTOP bit of the I/O Control Register (ICR) to 1. In this case, on-chip I/O (ASCI, CSI/O, PRT) stops operating. However, the CPU continues to operate. Recovery from IOSTOP mode is by resetting the IOSTOP bit in ICR to 0.

SYSTEM STOP Mode. SYSTEM STOP mode is the combination of SLEEP and IOSTOP modes. SYSTEM STOP mode is entered by setting the IOSTOP bit in ICR to 1 followed by execution of the SLP instruction. In this mode, on-chip I/O and CPU stop operating, reducing power consumption, but the PHI output continues to operate. Recovery from SYSTEM STOP mode is the same as recovery from SLEEP mode except that internal I/O sources (disabled by IOSTOP) cannot generate a recovery interrupt.

IDLE Mode. Software can put the Z80180/Z8S180/Z8L180 into this mode by setting the IOSTOP bit (ICR5) to 1, CCR6 to 0, CCR3 to 1 and executing the SLP instruction. The oscillator keeps operating but its output is blocked to all circuitry including the PHI pin. DRAM refresh and all internal devices stop, but external interrupts can occur. Bus granting to external masters can occur if the BREST bit in the CPU control Register (CCR5) was set to 1 before IDLE mode was entered.

The Z80180/Z8S180/Z8L180 leaves IDLE mode in response to a Low on RESET, an external interrupt request on NMI, or an external interrupt request on /INT0, /INT1 or /INT2 that is enabled in the INT/TRAP Control Register. As previously described for SLEEP mode, when the Z80180/Z8S180/Z8L180 leaves IDLE mode due to an NMI, or due to an enabled external interrupt request when the IEF flag is 1 due to an EI instruction, it starts by performing the interrupt with the return address being that of the instruction after the SLP instruction.

If an external interrupt enables the INT/TRAP control register while the IEF1 bit is 0, Z80180/Z8S180/Z8L180 leaves IDLE mode; specifically, the processor restarts by executing the instructions following the SLP instruction.

Zilog

**Z80180/Z8S180/Z8L18i
Enhanced Z180 Microprocesso**

IASCI REGISTER DESCRIPTION

ASCI Transmit Data Register
Ch 1: TDR1

ASCI Transmit Shift Register*
Ch 1: TSR1

ASCI Receive Data FIFO
Ch 1: RDR1

ASCI Receive Shift Register*
Ch 1: RSR1 (8)

ASCI Control Register A
Ch 1: CNTLA1 (8)

ASCI Control Register B
Ch 1: CNTB1 (8)

ASCI Status FIFO
Ch 1

ASCI Status Register
Ch 1: STAT1 (8)

ASCI Extension Control Reg.
Ch 1: ASEXT1 (5)

ASCI Time Constant Low
Ch 1: ASTCIL (8)

ASCI Time Constant High
Ch 1: ASTCIH (8)

TXA_1
RXA_1
$\overline{CTS}_1$

Internal Address/Data Bus

Interrupt Request

ASCI
Control

Baud Rate
Generator 0

Baud Rate
Generator 1

CKA_0
CKA_1
ϕ

ASCI Transmit Data Register
Ch 0: TDR0

ASCI Transmit Shift Register*
Ch 0: TSR0

ASCI Receive Data FIFO
Ch 0: RDR0

ASCI Receive Shift Register*
Ch 0: RSR0 (8)

ASCI Control Register A
Ch 0: CNTLA0 (8)

ASCI Control Register B
Ch 0: CNTB0 (8)

ASCI Status FIFO
Ch 0

ASCI Status Register
Ch 0: STAT0 (8)

ASCI Extension Control Reg.
Ch 0: ASEXT0 (7)

ASCI Time Constant Low
Ch 0: ASTCOL (8)

ASCI Time Constant High
Ch 0: ASTCOH (8)

TXA_0
RXA_0
$\overline{RTS}_0$
$\overline{CTS}_0$
$\overline{DCD}_0$

Note: *Not Program
Accessible.

Figure 32. ASCI Block Diagram

Zilog

**Z80180/Z8S180/Z8L180
Enhanced Z180 Microprocessor**

Figure 15 shows the timing for exiting IDLE mode due to an interrupt request. Note that the Z80180/Z8S180/Z8L180 takes about 9.5 clocks to restart.
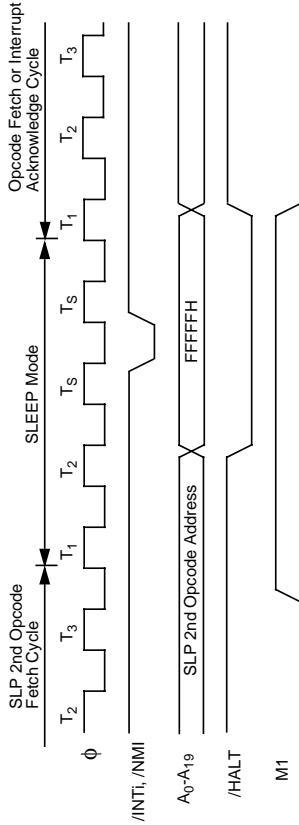
IDLE Mode

Opcode Fetch or Interrupt
Acknowledge Cycle

T_1 T_2 T_3 T_4

ϕ

9.5 Cycle Delay from $\overline{INTi}$ Asserted

$\overline{NMI}$
or
$\overline{INTi}$

A_{19}-A_0 FFFFFH

$\overline{HALT}$

$\overline{M1}$
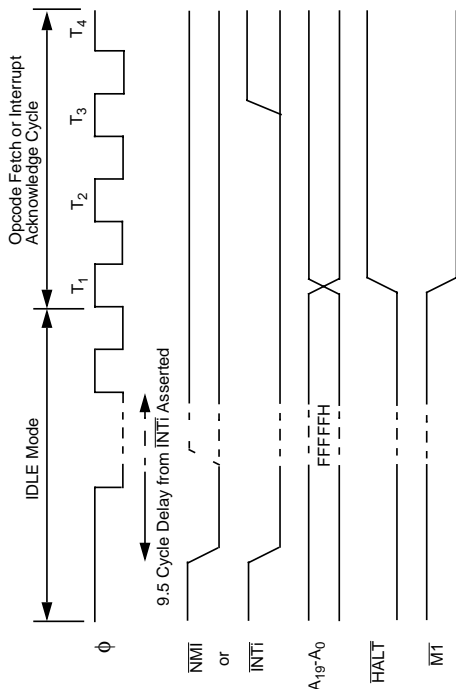
Figure 15. Z80180/Z8S180/Z8L180 IDLE Mode Exit due to External Interrupt

While the Z80180/Z8S180/Z8L180 is in IDLE mode, it will grant the bus to an external master if the BREXT bit (CCR5) is 1. Figure 16 shows the timing for this sequence. Note that the part takes 8 clock cycles longer to respond to the Bus Request than in normal operation.

After the external master negates the Bus Request, the Z80180/Z8S180/Z8L180 disables the PHI clock and remains in IDLE mode.

ASCI CHANNEL CONTROL REGISTER A

ASCI Control Register A 0 (CNTLA0: I/O Address = 00H)

Bit	7	6	5	4	3	2	1	0
	MPE	RE	TE	$\overline{RTS0}$	MPBR/EFR	MOD2	MOD1	MOD0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

ASCI Control Register A 1 (CNTLA1: I/O Address = 01H)

Bit	7	6	5	4	3	2	1	0
	MPE	RE	TE	CKA1D	MPBR/EFR	MOD2	MOD1	MOD0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Figure 33. ASCI Channel Control Register A

MPE: Multi-Processor Mode Enable (bit 7). The ASCI has a multiprocessor communication mode that utilizes an extra data bit for selective communication when a number of processors share a common serial bus. Multiprocessor data format is selected when the MP bit in CNTLB is set to 1. If multiprocessor mode is not selected (MP bit in CNTLB = 0), MPE has no effect. If multiprocessor mode is selected, MPE enables or disables the "wake-up" feature as follows. If MBE is set to 1, only received bytes in which the MPB (multiprocessor bit) = 1 can affect the RDRF and error flags. Effectively, other bytes (with MPB = 0) are "ignored" by the ASCI. If MPE is reset to 0, all bytes, regardless of the state of the MPB data bit, affect the REDR and error flags. MPE is cleared to 0 during RESET.

RE: Receiver Enable (bit 6). When RE is set to 1, the ASCI receiver is enabled. When RE is reset to 0, the transmitter is disables and any transmit operation in progress is interrupted. However, the TDRE flag is not reset and the previous contents of TDRE are held. TE is cleared to 0 in IOSTOP mode during RESET.

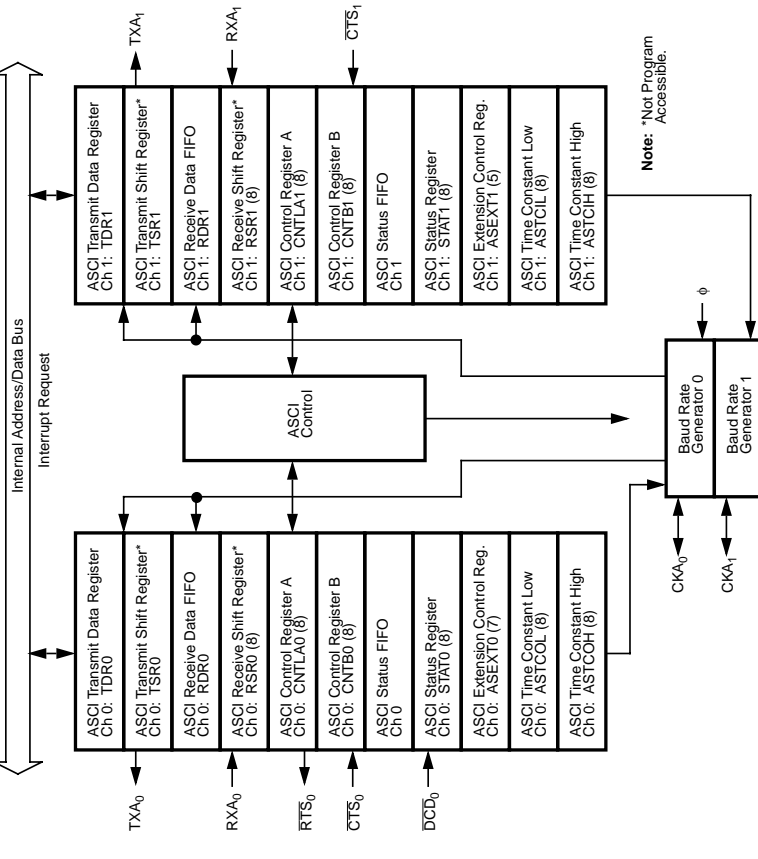**TE: Transmitter Enable (bit 5).** When TE is set to 1, the ASCI receiver is enabled. When TE is reset to 0, the transmitter is disabled and any transmit operation in progress is interrupted. However, the TDRE flag is not reset and the previous contents of TDRE are held. TE is cleared to 0 in IOSTOP mode during RESET.

$\overline{RTS0}$: Request to Send Channel 0 (bit 4 in CNTLA0 only). If bit 4 of the System Configuration Register is 0, the $\overline{RTS0}$/TxS pin has the $\overline{RTS0}$ function. $\overline{RTS0}$ allows the ASCI to control (start/stop) another communication devices transmission (for example, by connecting to that device's CTS input). $\overline{RTS0}$ is essentially a 1 bit output port having no side effects on other ASCI registers or flags.

Bit 4 in CNTLA1 is used.

CKA1D = 1, CKA1/$\overline{TEND}_0$ pin = $\overline{TEND}_0$

CKA1D = 0, CKA1/$\overline{TEND}_0$ pin = CKA1

Cleared to 0 on reset.

MPBR/EFR: Multiprocessor Bit Receive/Error Flag Reset (bit 3). When multiprocessor mode is enabled (MP in CNTLB = 1), MPBR, when read, contains the value of the MPB bit for the last receive operation. When written to 0, the EFR function is selected to reset all error flags (OVRN, FE, PE and BRK in the ASEXT Register) to 0. MPBR/EFR is undefined during RESET.

The following paragraphs explain the various functions of the ASCI registers.

ASCI Transmit Register 0. When the ASCI Transmit Register receives data from the ASCI Transmit Data Register (TDR), the data is shifted out to the TxA pin. When transmission is completed, the next byte (if available) is automatically loaded from TDR into TSR and the next transmission starts. If no data is available for transmission, TSR IDLEs by outputting a continuous High level. This register is not program accessible

ASCI Transmit Data Register 0,1 (TDR0, 1: I/O address = 06H, 07H). Data written to the ASCI Transmit Data Register is transferred to the TSR as soon as TSR is empty. Data can be written while TSR is shifting out the previous byte of data. Thus, the ASCI transmitter is double buffered.

Data can be written into and read from the ASCI Transmit Data Register. If data is read from the ASCI Transmit Data Register, the ASCI data transmit operation will not be affected by this read operation

ASCI Receive Shift Register 0,1 (RSR0,1). This register receives data shifted in on the RxA pin. When full, data is automatically transferred to the ASCI Receive Data Register (RDR) if it is empty. If RSR is not empty when the next incoming data byte is shifted in, an overrun error occurs. This register is not program accessible.

ASCI Receive Data FIFO 0,1 (RDR0, 1: I/O Address = 08H, 09H). The ASCI Receive Data Register is a read-only register. When a complete incoming data byte is assembled in RSR, it is automatically transferred to the 4 character Receive Data First-In First-Out (FIFO) memory. The oldest character in the FIFO (if any) can be read from the Receive Data Register (RDR). The next incoming data byte can be shifted into RSR while the FIFO is full. Thus, the ASCI receiver is well buffered.

ASCI STATUS FIFO

This 4 entry FIFO contains Parity Error, Framing Error, Rx Overrun, and Break status bits associated with each character in the receive data FIFO. The status of the oldest character (if any) can be read from the ASCI status registers as described below

the CKA1 function when bit 0 of the Interrupt Edge registe is 1.

If these bits are not 111 and the BRG mode bit is ASEXT is 0, then these bits specify a power-of-two divider for the PHI clock as shown in Table 9.

Setting or leaving these bits as 111 makes sense for a channel only when its CKA pin is selected for the CKA function. CKAO/CKS has the CKAO function when bit 4 of the System Configuration Register is 0. DCD0/CKA1 has

Table 6. Divide Ratio

SS2	SS1	SS0	Divide Ratio
0	0	0	÷1
0	0	1	÷2
0	1	0	÷4
0	1	1	÷8
1	0	0	÷16
1	0	1	÷32
1	1	0	÷64
1	1	1	External Clock

ASCI STATUS REGISTER 0, 1 (STAT0, 1)

Each channel status register allows interrogation of ASCI communication, error and modem control signal status, and enabling or disabling of ASCI interrupts.

ASCI Status Register 0 (STAT0: I/O Address = 04H)

Bit	7	6	5	4	3	2	1	0
	RDRF	OVRN	PE	FE	RE	DCD̄0	TDRE	TIE
	R	R	R	R	R/W	R	R	R/W

ASCI Status Register 1 (STAT1: I/O Address = 05H)

Bit	7	6	5	4	3	2	1	0
	RDRF	OVRN	PE	FE	RE	CTSIE	TDRE	TIE
	R	R	R	R	R/W	R/W	R	R/W

Figure 35. ASCI Status Registers

RDRF: Receive Data Register Full (bit 7). RDRF is set to 1 when an incoming data byte is loaded into an empty Rx FIFO. Note that if a framing or parity error occurs, RDRF is still set and the receive data (which generated the error) is still loaded into the FIFO. RDRF is cleared to 0 by reading RDR and last character in the FIFO from IOSTOP mode, during RESET and for ASCI0 if the /DCD0 input is auto-enabled and is negated (High).

OVRN: Overrun Error (bit 6). An overrun condition occurs if the receiver has finished assembling a character but the Rx FIFO is full so there is no room for the character. However, this status bit is not set until the last character received before the overrun becomes the oldest byte in the FIFO. This bit is cleared when software writes a 1 to the

EFR bit in the CNTLA register, and also by Reset, ii IOSTOP mode, and for ASCI0 if the /DCD0 pin is auto en abled and is negated (High).

Note that when an overrun occurs, the receiver does nc place the character in the shift register into the FIFO, no any subsequent characters, until the last good characte has come to the top of the FIFO so that OVRN is set, an software then writes a 1 to EFR to clear it.

MOD2, 1, 0: ASCI Data Format Mode 2, 1, 0 (bits 2-0). These bits program the ASCI data format as follows.

MOD2
= 0→7 bit data
= 1→8 bit data

MOD1
= 0→No parity
= 1→Parity enabled

MOD0
= 0→1 stop bit
= 1→2 stop bits

The data formats available based on all combinations c MOD2, MOD1, and MOD0 are shown in Table 5-6.

Table 5. Data Formats

MOD2	MOD1	MOD0	Data Format
0	0	0	Start + 7 bit data + 1 stop
0	0	1	Start + 7 bit data + 2 stop
0	1	0	Start + 7 bit data + parity + 1 sto
0	1	1	Start + 7 bit data + parity + 2 sto
1	0	0	Start + 8 bit data + 1 stop
1	0	1	Start + 8 bit data + 2 stop
1	1	0	Start + 8 bit data + parity + 1 sto
1	1	1	Start + 8 bit data + parity + 2 sto

ASCI CHANNEL CONTROL REGISTER B

ASCI Control Register B 0 (CNTLB0: I/O Address = 02H)
ASCI Control Register B 1 (CNTLB1: I/O Address = 03H)

Bit	7	6	5	4	3	2	1	0
	MPBT	MP	CTS̄/PS	PEO	DR	SS2	SS1	SS0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Figure 34. ASCI Channel Control Register B

MPBT: Multiprocessor Bit Transmit (bit 7). When multiprocessor communication format is selected (MP bit =1), MPBT is used to specify the MPB data bit for transmission. If MPBT = 1, then MPB = 1 is transmitted. If MPBT = 0, then MPB = 0 is transmitted. MPBT state is undefined during and after RESET.

MP: Multiprocessor Mode (bit 6). When MP is set to 1, the data format is configured for multiprocessor mode based on the MOD2 (number of data bits) and MOD0 (number of stop bits) bits in CNTLA. The format is as follows.

Start bit + 7 or 8 data bits + MPB bit + 1 or 2 stop bits

Note that multiprocessor (MP=1) format has no provision for parity. If MP = 0, the data format is based on MOD0, MOD1, MOD2, and may include parity. The MP bit is cleared to 0 during RESET.

CTS/PS: Clear to Send/Prescale (bit 5). When read, /CTS/PS reflects the state of the external /CTS input. If the /CTS input pin is HIGH, /CTS/PS will be read as 1. Note that when the /CTS input pin is HIGH, the TDRE bit is inhibited (i.e. held at 0). For channel 1, the /CTS input is multiplexed with RXS pin (Clocked Serial Receive Data).

Thus, /CTS/PS is only valid when read if the channel CTS1E bit = 1 and the /CTS input pin function is selectec The read data of /CTS/PS is not affected by RESET.

If the SS2-0 bits in this register are not 111, and the BRC mode bit in the ASEXT register is 0, then writing to this b sets the prescale (PS) control as described in the followin "Clock Modes" section. Under those circumstances, a 0 in dicates a divide by 10 prescale function while a 1 indicate: divide by 30. The bit resets to 0.

PEO: Parity Even Odd (bit 4). PEO selects oven or od parity. PEO does not affect the enabling/disabling of parit (MOD1 bit of CNTLA). If PEO is cleared to 0, even parit is selected. If PEO is set to 1, odd parity is selected. PEC is cleared to 0 during RESET.

DR: Divide Ratio (bit 3). If the X1 bit in the ASEXT regis ter is 0, this bit specifies the divider used to obtain bau rate from the data sampling clock. If DR is reset to 0, di vide- by-16 is used, while if DR is set to 1 divide-by-64 i used. DR is cleared to 0 during RESET.

SS2,1,0: Source/Speed Select 2,1,0 (bits 2-0). First, i these bits are 111, as they are after a Reset, the CKA pi

is used as a clock input, and is divided by 1, 16, or 64 depending on the DR bit and the X1 bit in the ASEXT register.

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Address (08H)

Channel 1--

Mnemonics TSR1

Address (09H)

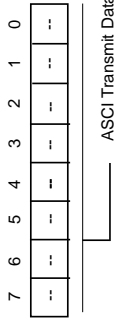| 7	6	5	4	3	2	1	0
--	--	--	--	--	--	--	--

ASCI Transmit Data

Figure 39. ASCI Receive Register Channel 1R

CSI/O CONTROL/STATUS REGISTER

(CNTR: I/O Address = 0AH). CNTR is used to monitor CSI/O status, enable and disable the CSI/O, enable and disable interrupt generation, and select the data cloci speed and source.
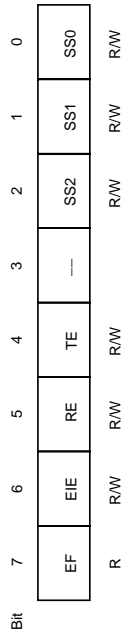
Bit

	7	6	5	4	3	2	1	0
	EF	EIE	RE	TE	—	SS2	SS1	SS0
	R	R/W	R/W	R/W		R/W	R/W	R/W

Figure 40. CSI/O Control Register

EF: End Flag (bit 7). EF is set to 1 by the CSI/O to indicate completion of an 8-bit data transmit or receive operation. If EIE (End Interrupt Enable) bit = 1 when EF is set to 1, a CPU interrupt request is generated. Program access of TRDR only occurs if EF = 1. The CSI/O clears EF to 0 when TRDR is read or written. EF is cleared to 0 during RESET and IOSTOP mode.

EIE: End Interrupt Enable (bit 6). EIE is set to 1 to generate a CPU interrupt request. The interrupt request is inhibited if EIE is reset to 0. EIE is cleared to 0 during RESET.

RE: Receive Enable (bit 5). A CSI/O receive operation is started by setting RE to 1. When RE is set to 1, the data clock is enabled. In internal clock mode, the data clock is output from the CKS pin. In external clock mode, the clock is input on the RXS pin in synchronization with the (internal or external) data clock. After receiving 8 bits of data, the CSI/O automatically clears RE to 0, EF is set to 1, and an interrupt

(if enabled by EIE = 1) is generated. RE and TE are neve both set to 1 at the same time. RE is cleared to 0 durin RESET and ISTOP mode.

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PE: Parity Error (bit 5). A parity error is detected when parity checking is enabled by the MOD1 bit in the CNT1LA register being 1, and a character has been assembled in which the parity does not match the PEO bit in the CNTLB register. However, this status bit is not set until/unless the error character becomes the oldest one in the RxFIFO. PE is cleared when software writes a 1 to the EFR bit in the CNTRLA register, and also by Reset, in IOSTOP mode, and for ASCI0 if the /DCD0 pin is auto-enabled and is negated (High).

FE: Framing Error (bit 4). A framing error is detected when the stop bit of a character is sampled as 0/Space. However, this status bit is not set until/unless the error character becomes the oldest one in the RxFIFO. FE is cleared when software writes a 1 to the EFR bit in the CNTLA register, and also by Reset, in IOSTOP mode, and for ASCIO if the /DCDO pin is auto-enabled and is negated (High).

REI: Receive Interrupt Enable (bit 3). RIE should be set to 1 to enable ASCI receive interrupt requests. When RIE is 1, the Receiver requests an interrupt when a character is received and RDRF is set, but only if neither DMA channel has its Request-routing field set to receive data from this ASCI. That is, if SM1-0 are 11 and SAR17-16 are 10, or DIM1 is 1 and IAR17-16 are 10, then ASCI1 doesn't request an interrupt for RDRF. If RIE is 1, either ASCI requests an interrupt when OVRN, PE or FE is set, and

ASCI0 requests an interrupt when /DCD0 goes High. RIE is cleared to 0 by Reset.

DCD0: Data Carrier Detect (bit 2 STAT0). This bit is se to 1 when the pin is High. It is cleared to 0 on the first rea of STAT0 following the pin's transition from High to Low and during RESET. Bit 6 of the ASEXT0 register is 0 to se lect auto-enabling, and the pin is negated (High). Channe 1 has an external CTS1 input which is multiplexed with thi receive data pin RSX for the CSI/O.

Bit 2 = 0; Select RXS function.

Bit 2 = 1; Select CTS1 function.

TDRE: Transmit Data Register Empty (bit 1). TDRE = indicates that the TDR is empty and the next transmit dat: byte is written to TDR. After the byte is written to TDR TDRE is cleared to 0 until the ASCI transfers the byte from TDR to the TSR and then TDRE is again set to 1. TDRE i set to 1 in IOSTOP mode and during RESET. On ASCIC if the CTS0 pin is auto-enabled in the ASEXT0 register and the pin is High, TDRE is reset to 0.

TIE: Transmit Interrupt Enable (bit 0). TIE should be se to 1 to enable ASCI transmit interrupt requests. If TIE = 1 an interrupt will be requested when TDRE = 1. TIE i cleared to 0 during RESET.
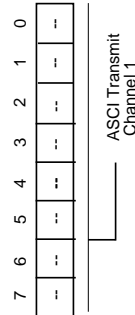
ASCI TRANSMIT DATA REGISTERS

Register addresses 06H and 07H hold the ASCI transmit data for channel 0 and channel 1, respectively.
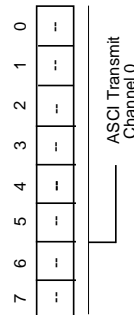
Channel 0

Mnemonics TDR0

Address (06H)

7	6	5	4	3	2	1	0
--	--	--	--	--	--	--	--

ASCI Transmit
Channel 0

Figure 36. ASCI Register

ASCI Receive Register

Register addresses 08H and 09H hold the ASCI receive data for channel 0 and channel 1, respectively.

Channel 0

Address (07H)

7	6	5	4	3	2	1	0
--	--	--	--	--	--	--	--

ASCI Transmit
Channel 1

Figure 37. ASCI Register

Channel 1

Mnemonics TDR1

Mnemonics TSR0 --

Address (08H)

7	6	5	4	3	2	1	0
--	--	--	--	--	--	--	--

ASCI Receive Register Channel 0

Figure 38. ASCI Receive Register Channel 0

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Transmit Enable (bit 4). A CSI/O transmit operation is started by setting TE to 1. When TE is set to 1, the data clock is enabled. When in internal clock mode, the data clock is output from the CKS pin. In external clock mode, the clock is input on the CKS pin. In either case, data is shifted out on the TXS pin synchronous with the (internal or external) data clock. After transmitting 8 bits of data, the CSI/O automatically clears TE to 0, EF is set to 1, and an interrupt (if enabled by EIE = 1) is generated. TE and RE are never both set to 1 at the same time. TE is cleared to 0 during RESET and IOSTOP mode.

SS2, 1, 0: Speed Select 2, 1, 0 (bits 2-0). SS2, SS1 and SS0 select the CSI/O transmit/receive clock source and speed. SS2, SS1 and SS0 are all set to 1 during RESET. Table 10 shows CSI/O Baud Rate Selection.

Table 7. CSI/O Baud Rate Selection

SS2	SS1	SS0	Divide Ratio
0	0	0	÷20
0	0	1	÷40
0	1	0	÷80
0	1	1	÷160
1	0	0	÷320
1	0	1	÷640
1	1	0	÷1280
1	1	1	External Clock Input (less than ÷20.)

After RESET, the CKS pin is configured as an external clock input (SS2, SS1, SS0 = 1). Changing these values causes CKS to become an output pin and the selected clock is output when transmit or receive operations are enabled.

CSI/O Transmit/Receive Data Register
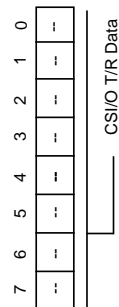**(TRDR: I/O Address = 0BH).**

Bits: 7 6 5 4 3 2 1 0 — CSI/O T/R Data

Figure 41. CSI/O Transmit/Receive Data Register 1R

Timer Reload Register 0L
RLDR0L

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Timer Data Register Channel 0L
TMDR0L
0CH

Bits: 7 6 5 4 3 2 1 0 — ASCI Receive Data

Figure 42. Timer Register Channel 0L

Timer Data Register Channel 0H
TMDR0H
0D H

Bits: 7 6 5 4 3 2 1 0 — Timer Data

Figure 43. Timer Data Register Channel 0H

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0E H

Bits: 7 6 5 4 3 2 1 0 — Timer Reload Data

Figure 44. Timer Reload Register Low

Timer Reload Register 0H
RLDR0H
0F H

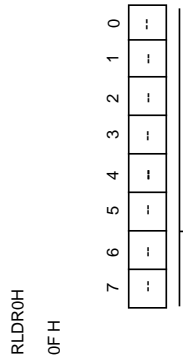Bits: 7 6 5 4 3 2 1 0 — Timer Reload Data

Figure 45. Timer Reload Register Channel

TIMER CONTROL REGISTER (TCR)

TCR monitors both channels (PRT0, PRT1) TMDR status. It also controls enabling and disabling of down counting and interrupts along with controlling output pin A18/TOU for PRT1.
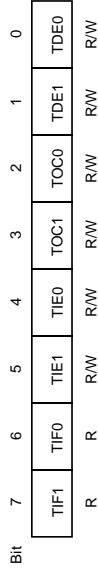
Bit	7	6	5	4	3	2	1	0
	TIF1	TIF0	TIE1	TIE0	TOC1	TOC0	TDE1	TDE0
	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Figure 46. Timer Control Register (TCR: I/O Address = 10H)

TIF1: Timer Interrupt Flag 1 (bit 7). When TMDR1 decrements to 0, TIF1 is set to 1. This generates an interrupt request if enabled by TIE1 = 1. TIF1 is reset to 0 when TCR is read and the higher or lower byte of TMDR1 is read. During RESET, TIF1 is cleared to 0.

TIF0: Timer Interrupt Flag 0 (bit 6). When TMDR0 decrements to 0, TIF0 is set to 1. This generates an interrupt request if enabled by TIE0 = 1. TIF0 is reset to 0 when TCR is read and the higher or lower byte of TMDR0 is read. During RESET, TIF0 is cleared to 0.

TIE1: Timer Interrupt Enable 1 (bit 5). When TIE0 is set to 1, TIF1 = 1 generates a CPU interrupt request. When TIE0 is reset to 0, the interrupt request is inhibited. During RESET, TIE0 is cleared to 0.

TOC1, 0: Timer Output Control (bits 3, 2). TOC1 an TOC0 control the output of PRT1 using the multiplexe TOUT/DREQ pin as shown in Table 11. During RESET TOC1 and TOC0 are cleared to 0. If bit 3 of the IAR1B reg ister is 1, the TOUT function is selected. By programmin TOC1 and TOC0, the TOUT/DREQ pin can be force High, Low, or toggled when TMDR1 decrements to 0.

Table 8. Timer Output Control

TOC1	TOC0	Output
0	0	Inhibited The TOUT/DREQ pin is not affected by the PRT.
0	1	Toggled If bit 3 of IAR1B is 1, the
1	0	TOUT/DREQ pin is toggles or
1	1	set Low or High as indicated.

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Timer Data Register Channel 1L

Mnemonic TMDR1L

Address 14

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
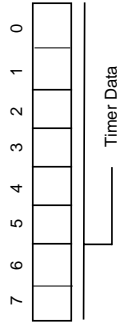
Timer Data

Figure 48. Timer Data Register 1L

Timer Data Register Channel 1H

Mnemonic TMDR1H

Address 15

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
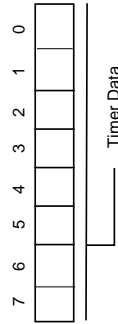
Timer Data

Figure 49. Timer Data Register 1H

Timer Reload Register Channel 1L

Mnemonic RLDR1L

Address 16

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

Reload Data
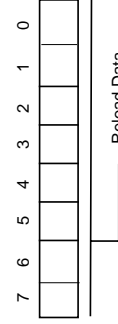
Figure 50. Timer Reload Channel 1L

Timer Reload Register Channel 1L

Mnemonic RLDR1H

Address 17

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

Reload Data
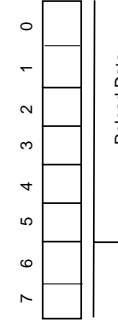
Figure 51. Timer Relaod Register Channel 1L

Free Running Counter (Read Only)

Mnemonic FRC

Address 18

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

Counting Data

Figure 52. Free Running Counter

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TDE1, 0: Timer Down Count Enable (bits 1, 0). TDE1 and TDE0 enable and disable down counting for TMDR1 and TMDR0, respectively. When TDEn (n = 0, 1) is set to 1, down counting is stopped and TMDRn is freely read o written. TDE1 and TDE0 are cleared to 0 during RESE and TMDRn will not decrement until TDEn is set to 1.

DMA DESTINATION ADDRESS REGISTER CHANNEL 0

(DAR0: I/O Address = 23H to 25H) specifies the physical destination address for channel 0 transfers. The register contains 20 bits and can specify up to 1024 KB memory addresses or up to 64 KB I/O addresses. Channel 0 destination can be memory, I/O, or memory mapped I/O. For I/O, the MS bits of this register identify the Request Handshake signal for channel 0.

DMA Destination Address Register Channel 0L

Mnemonic DAR0L

Address 23

Figure 58. DMA Destination Address Register Channel 0L

DMA Destination Address Register Channel 0H

Mnemonic DAR0H

Address 24

Figure 59. DMA Destination Address Register Channel 0H

DMA Destination Address Register Channel 0B

Mnemonic DAR0B

Address 25

Figure 60. DMA Destination Address Register Channel 0B

Note: In the R1 and Z Mask, these DMA registers are expanded from 4 bit to 3 bits in the package version of CP 68

A19*	A18	A17	A16	
X	X	0	0	DMA Transfer Request DREQ0
X	X	0	1	TDR0 (ASCI0)
X	X	1	0	TDR1 (ASCI1)
X	X	1	1	Not Used

DMA SOURCE ADDRESS REGISTER CHANNEL 0

(SAR0: I/O Address = 20H to 22H) specifies the physical source address for channel 0 transfers. The register contains 20 bits and can specify up to 1024 KB memory addresses or up to 64 KB I/O addresses. Channel 0 source can be memory, I/O, or memory mapped I/O. For I/O, the MS bits of this register identify the Request Handshake signal.

DMA Source Address Register, Channel 0L

Mnemonic SAR0L

Address 20

7 6 5 4 3 2 1 0 — DMA Channel 0 Address

Figure 55. DMA Source Address Register 0L

DMA Source Address Register, Channel 0H

Mnemonic SAR0H

Address 21

7 6 5 4 3 2 1 0 — DMA Channel 0 Address

Figure 56. DMA Source Address Register 0H

DMA Source Address Register Channel 0B

Mnemonics SAR0B

Address 22

7 6 5 4 3 2 1 0 — DMA Channel B Address

Figure 57. DMA Source Address Register 0B

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DMA MEMORY ADDRESS REGISTER CHANNEL 1

(MAR1: I/O Address = 28H to 2AH) specifies the physical memory address for channel 1 transfers. This may be destina tion or source memory address. The register contains 20 bits and may specify up to 1024 KB memory address.

DMA Memory Address Register, Channel 1L

Mnemonic MAR1L

Address 28

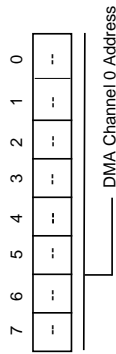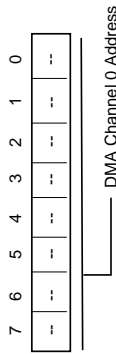**Figure 65. DMA Memory Address Register, Channel 1L**

DMA Memory Address Register, Channel 1H.
Mnemonic MAR1H

Address 29

Figure 66. DMA Memory Address Register, Channel 1H

DMA Memory Address Register, Channel 1B

Mnemonic MAR1B

Address 2A

Figure 67. DMA Memory Address Register, Channel 1B

DMA BYTE COUNT REGISTER CHANNEL 0

(BCRO: I/O Address = 26H to 27H) specifies the number of bytes to be transferred. This register contains 16 bits and ma specify up to 64 KB transfers. When one byte is transferred, the register is decremented by one. If "n" bytes should b transferred, "n" must be stored before the DMA operation.

Note: All DMA Count Register channels are undefined during reset.

DMA Byte Count Register Channel 0L

Mnemonic BCR0L

Address 26

Figure 61. DMA Byte Count Register Channel 0L

DMA Byte Count Register Channel 0H

Mnemonic BCR0H

Address 27

Figure 62. DMA Byte Count Register 0H

DMA Byte Count Register Channel 1L

Mnemonic BCR1L

Address 2E

Figure 63. DMA Byte Count Register 1L

DMA Byte Count Register Channel 0H

Mnemonic BCR1H

Address 2F

Figure 64. DMA Byte Count Register 0H

DMA I/O ADDRESS REGISTER CHANNEL 1

(IAR1: I/O Address = 2BH to 2DH) specifies the I/O address for channel 1 transfers. This may be destination or source I/O address. The register contains 16 bits of I/O address; its most significant byte identifies the Request

Handshake signal and controls the Alternating Channel feature.
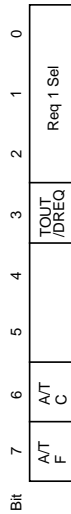
All bits in IAR1B reset to 0.

Bit	7	6	5	4	3	2	1	0
	A/T F	A/T C			TOUT /DREQ		Req 1 Sel	

Figure 68. IAR MS Byte Register (IAR1B: I/O Address 2DH)

DMA I/O Address Register Channel 1L

Mnemonic IAR1L

Address 2B

Figure 69. DMA I/O Address Register Channel 1L

DMA I/O Address Register Channel 1H

Mnemonic IAR1H

Address 2C

Figure 70. DMA I/O Address Register Channel 1H

DMA I/O Address Register Channel 1B

Mnemonic IAR1B

Address 2D

Figure 71. DMA I/O Address Register Channel 1B

DMA STATUS REGISTER (DSTAT)

DSTAT is used to enable and disable DMA transfer and DMA termination interrupts. DSTAT also indicates DMA transfer status, in other words, completed or in progress.
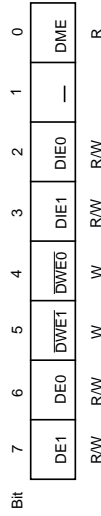
Mnemonic DSTAT

Address 30

Bit	7	6	5	4	3	2	1	0
	DE1	DE0	DWE1	DWE0	DIE1	DIE0	—	DME
	R/W	R/W	W	W	R/W	R/W		R

Figure 72. DMA Status Register (DSTAT: I/O Address = 30H)

DE1: DMA Enable Channel 1 (bit 7). When DE1 = 1 and DME = 1, channel 1 DMA is enabled. When a DMA transfer terminates (BCR1 = 0), DE1 is reset to 0 by the DMAC. When DE1 = 0 and the DMA interrupt is enabled (DIE1 = 1), a DMA interrupt request is made to the CPU.

To perform a software write to DE1, DWE1 should be written with 0 during the same register write access. Writing DE1 to 0 disables channel 1 DMA, but DMA is restartable. Writing DE1 to 1 enables channel 1 DMA and automatically sets DME (DMA Main Enable) to 1. DE1 is cleared to 0 during RESET.

DE0: DMA Enable Channel 0 (bit 6). When DE0 = 1 and DME = 1, channel 0 DMA is enabled. When a DMA transfer terminates (BCR0 = 0), DE0 is reset to 0 by the DMAC. When DE0 = 0 and the DMA interrupt is enabled (DIE0 = 1), a DMA interrupt request is made to the CPU.

To perform a software write to DE0, DWE0 should be written with 0 during the same register write access. Writing DE0 to 0 disables channel 0 DMA. Writing DE0 to 1 enables channel 0 DMA and automatically sets DME (DMA Main Enable) to 1. DE0 is cleared to 0 during RESET.

DWE1: DE1 Bit Write Enable (bit 5). When performing any software write to DE1, DWE1 should be written with 0 during the same access. DWE1 always reads as 1.

DWE0: DE0 Bit Write Enable (bit 4). When performing any software write to DE0, DWE0 should be written with (during the same access. DWE0 always reads as 1.

DIE1: DMA Interrupt Enable Channel 1 (bit 3). Whei DIE1 is set to 1, the termination channel 1 DMA transfe (indicated when DE1 = 0) causes a CPU interrupt reques to be generated. When DIE1 = 0, the channel 0 DMA ter mination interrupt is disabled. DIE0 is cleared to 0 durin(RESET.

DIE0: DMA Interrupt Enable Channel 0 (bit 2). Whei DIE0 is set to 1, the termination channel 0 of DMA transfe (indicated when DE0=0) causes a CPU interrupt request t be generated. When DIE0=0, the channel 0 DMA termina tion interrupt is disabled. DIE0 is cleared to 0 during RE SET.

DME: DMA Main Enable (bit 0). A DMA operation is onl enabled when its DE bit (DE0 for channel 0, DE1 for chan nel 1) and the DME bit is set to 1.

When NMI occurs, DME is reset to 0, thus disabling DM/ activity during the NMI interrupt service routine. To restar DMA, DE- and/or DE1 should be written with 1 (even if th contents are already 1). This automatically sets DME to 1 allowing DMA operations to continue. Note that DME can not be directly written. It is cleared to 0 by NMI or indirect! set to 1 by setting DE0 and/or DE1 to 1. DME is cleared t 0 during RESET.

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Table 12 shows all DMA transfer mode combinations of DM0, DM1, SM0, and SM1. Since I/O to/from I/O transfers are not implemented, 12 combinations are available.
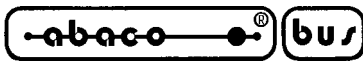
Table 12. Transfer Mode Combinations

DM1	DM0	SM1	SM0	Transfer Mode	Address Increment/Decrement
0	0	0	0	Memory→Memory	SAR0+1, DAR0+1
0	0	0	1	Memory→Memory	SAR0−1, DAR0+1
0	0	1	0	Memory*→Memory	SAR0 fixed, DAR0+1
0	0	1	1	I/O→Memory	SAR0 fixed, DAR0+1
0	1	0	0	Memory→Memory	SAR0+1, DAR0−1
0	1	0	1	Memory→Memory	SAR0−1, DAR0−1
0	1	1	0	Memory*→Memory	SAR0 fixed, DAR0−1
0	1	1	1	I/O→Memory	SAR0 fixed, DAR0−1
1	0	0	0	Memory→Memory*	SAR0+1, DAR0 fixed
1	0	0	1	Memory→Memory*	SAR0−1, DAR0 fixed
1	0	1	0	Reserved	
1	0	1	1	Memory→I/O	SAR0+1, DAR0 fixed
1	1	0	0	Memory I/O	SAR0−1, DAR0 fixed
1	1	0	1	Reserved	
1	1	1	0	Reserved	
1	1	1	1	Reserved	

Note: * Includes memory mapped I/O.

MMOD: Memory Mode Channel 0 (bit). When channel 0 is configured for memory to/from memory transfers there is no Request Handshake signal to control the transfer timing. Instead, two automatic transfer timing modes are selectable: burst (MMOD = 1) and cycle steal (MMOD = 0). For burst memory to/from memory transfers, the DMAC takes control of the bus continuously until the DMA transfer completes (as shown by the byte count register = 0). In cycle steal mode, the CPU is given a cycle for each DMA byte transfer cycle until the transfer is completed.

For channel 0 DMA with I/O source or destination, the se lected Request signal times the transfer and thus MMO is ignored. MMOD is cleared to 0 during RESET.

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DMA MODE REGISTER (DMODE).

DMODE is used to set the addressing and transfer mode for channel 0.

Mnemonic DMODE

Address 31H

Bit	7	6	5	4	3	2	1	0
	—	—	DM1	DM0	SM1	SM0	MMOD	—
			R/W	R/W	R/W	R/W	R/W	R/W

Figure 73. DMA Mode Register (DMODE: I/O Address = 31H)

DM1, DM0: Destination Mode Channel 0 (bits 5,4) specifies whether the destination for channel 0 transfers is memory or I/O, and whether the address should be incremented or decremented for each byte transferred. DM1 and DM0 are cleared to 0 during RESET.

SM1, SM0: Source Mode Channel 0 (bits 3, 2) specifies whether the source for channel 0 transfers is memory or I/O, and whether the address should be incremented or decremented for each byte transferred.

Table 10. Channel 0 Destination

DM1	DM0	Memory I/O	Memory Increment/Decrement
0	0	Memory	+1
0	1	Memory	−1
1	0	Memory	fixed
1	1	I/O	fixed

Table 11. Channel 0 Source

SM1	SM0	Memory I/O	Memory Increment/Decrement
0	0	Memory	+1
0	1	Memory	−1
1	0	Memory	fixed
1	1	I/O	fixed

DMA/WAIT CONTROL REGISTER (DCNTL)

DCNTL controls the insertion of wait states into DMAC (and CPU) accesses of memory or I/O. Also, it defines the Request signal for each channel as level or edge sense.

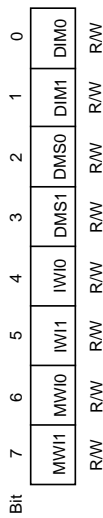| Bit	7	6	5	4	3	2	1	0
	MWI1	MWI0	IWI1	IWI0	DMS1	DMS0	DIM1	DIM0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Figure 74. DMA/WAIT Control Register (DCNTL: I/O Address = 32H)

MWI1, MWI0: Memory Wait Insertion (bits 7-6). Specifies the number of wait states introduced into CPU or DMAC memory access cycles. MWI1 and MWI0 are set to 1 during RESET.

MWI1	MWI0	Wait State
0	0	0
0	1	1
1	0	2
1	1	3

IWI1, IWI0: I/O Wait Insertion (bits 5-4). Specifies the number of wait states introduced into CPU or DMAC I/O access cycles. IWI1 and IWI0 are set to 1 during RESET. See the section on Wait-State Generation for details.

IWI1	IWI0	Wait State
0	0	0
0	1	2
1	0	3
1	1	4

DMS1, DMS0: DMA Request Sense (bits 3-2). DMS1 and DMS0 specify the DMA request sense for channel 1 and channel 1 respectively. When reset to 0, the input is level sense. When set to 1, the input is edge sense. DMS1 and DMS0 are cleared to 0 during RESET.

DMSi	Sense
1	Edge Sense
0	Level Sense

Typically, for an input/source device, the associated DMS bit should be programmed as 0 for level sense because the device has a relatively long time to update its Request signal after the DMA channel reads data from it in the first of the two machine cycles involved in transferring a byte.

An output/destination device has much less time to update its Request signal, after the DMA channel starts a write operation to it, as the second machine cycle of the two cycle involved in transferring a byte. With zero-wait state I/O cycles, which apply only to the ASCIs, it is impossible for a device to update its Request signal in time, and edge sensing must be used.

With one-wait-state I/O cycles (the fastest possible except for the ASCIs), it is unlikely that an output device will be able to update its Request in time, and edge sense is required.

DIM1, DIM0: DMA Channel 1 I/O and Memory Mode (bits 1-0). Specifies the source/destination and address modifier for channel 1 memory to/from I/O transfer modes. DIM1 and DIM0 are cleared to 0 during RESET.

Table 13. Channel 1 Transfer Mode

DIM1	DIM0	Transfer Mode	Address Increment/Decrement
0	0	Memory→I/O	MAR1 +1, IAR1 fixed
0	1	Memory→I/O	MAR1−1, IAR1 fixed
1	0	I/O→Memory	IAR1 fixed, MAR1 + 1
1	1	I/O→Memory	IAR1 fixed, MAR1 −1

INTERRUPT VECTOR LOW REGISTER

Mnemonic: IL

Address 33

Bits 7-5 of IL are used as bits 7-5 of the synthesized interrupt vector during interrupts for the INT1 and INT2 pins and for the DMAs, ASCIs, PRTs, and CSI/O. These three bits are cleared to 0 during Reset (Figure 75).
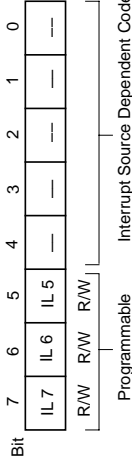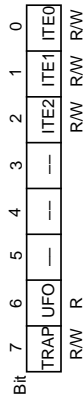
Bit	7	6	5	4	3	2	1	0
	IL7	IL6	IL5	—	—	—	—	—
	R/W	R/W	R/W					

Programmable | Interrupt Source Dependent Code

Figure 75. Interrupt Vector Low Register (IL: I/O Address = 33H)

INT/TRAP CONTROL REGISTER

Mnemonics ITC

Address 34

INT/TRAP Control Register (ITC, I/O Address 34H). This register is used in handling TRAP interrupts and to enable or disable Maskable Interrupt Level 0 and the INT1 and INT2 pins.

Bit	7	6	5	4	3	2	1	0
	TRAP	UFO	—	—	—	ITE2	ITE1	ITE0
	R/W	R				R/W	R/W	R/W

ITE2, 1, 0: Interrupt Enable 2, 1, 0 (bits 2-0). ITE2 and ITE1 enable and disable the external interrupt inputs /INT2 and /INT1, respectively. ITE0 enables and disables interrupts from the on-chip ESCC, CTCs and Bidirectional Centronics controller as well as the external interrupt input /INT0. A 1 in a bit enables the corresponding interrupt level while a 0 disables it. A Reset sets ITE0 to 1 and clears ITE1 and ITE2 to 0.

the starting address of the undefined instruction. This is necessary since the TRAP may occur on either the second or third byte of the Opcode. UFO allows the stacked PC value to be correctly adjusted. If UFO = 0, the first Opcode should be interpreted as the stacked PC-1. If UFO = 1, the first Opcode address is stacked PC-2. UFO is Read-Only.

TRAP Interrupt. The Z80180/Z8S180/Z8L180 generates a non-maskable (not affected by the state of IEF1) TRAP interrupt when an undefined Opcode fetch occurs. This feature can be used to increase software reliability, implement an "extended" instruction set, or both. TRAP may occur during Opcode fetch cycles and also if an undefined

TRAP (bit 7). This bit is set to 1 when an undefined Opcode is fetched. TRAP can be reset under program control by writing it with a 0, however, it cannot be written with 1 under program control. TRAP is reset to 0 during RESET.

UFO: Undefined Fetch Object (bit 6). When a TRAP interrupt occurs, the contents of UFO allow determination of

Figure 77. TRAP Timing-3rd Opcode Undefined

REFRESH CONTROL REGISTER

Mnemonic RCR

Address 36

Figure 78. Refresh Control Register (RCA: I/O Address = 36H)

The RCR specifies the interval and length of refresh cycles, while enabling or disabling the refresh function.

REFE: Refresh Enable (bit 7). REFE = disables the refresh controller while REFE = 1 enables refresh cycle insertion. REFE is set to 1 during RESET.

REFW: Refresh Wait (bit 6). REFW = 0 causes the refresh cycle to be two clocks in duration. REFW = 1 causes the refresh cycle to be three clocks in duration by adding a refresh wait cycle (TRW). REFW is set to 1 during RESET

CYC1, 0: Cycle Interval (bit 1,0). CYC1 and CYC0 specify the interval (in clock cycles) between refresh cycles. In the case of dynamic RAMs requiring 128 refresh cycles every 2 ms (or 256 cycles in every 4 ms), the required refresh intervals is less than or equal to 15.625 us. Thus, the underlined values indicate the best refresh interval depending on CPU clock frequency. CYC0 and CYC1 are cleared to 0 during RESET (see Table 14).

Opcode is fetched during the interrupt acknowledge cycle for $\overline{INT}_0$ when Mode 0 is used.

When a TRAP interrupt occurs, the Z80180/Z8S180/Z8L180 operates as follows:

1. The TRAP bit in the Interrupt TRAP/Control (ITC) register is set to 1.

2. The current PC (Program Counter) value, reflecting the location of the undefined Opcode, is saved on the stack.

3. The Z80180/Z8S180/Z8L180 vectors to logical address 0. Note that if logical address 0000H is mapped to physical address 00000H, the vector is the same as for RESET. In this case, testing the TRAP bit

in ITC will reveal whether the restart at physical address 00000H was caused by RESET or TRAP.

All TRAP interrupts occur after fetching an undefined second Opcode byte following one of the "prefix" Opcode CBH, DDH, EDH, or FDH, or after fetching an undefined third Opcode byte following one of the "double prefix" Opcodes DDCBH or FDCBH.

The state of the Undefined Fetch Object (UFO) bit in ITC allows TRAP software to correctly "adjust" the stacked PC depending on whether the second or third byte of the Opcode generated the TRAP. If UFO=0, the starting address of the invalid instruction is equal to the stacked PC-1. If UFO=1, the starting address of the invalid instruction is equal to the stacked PC-2.
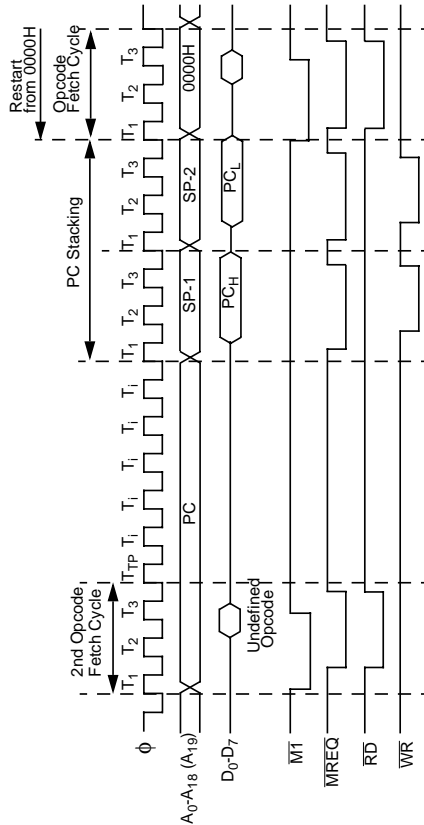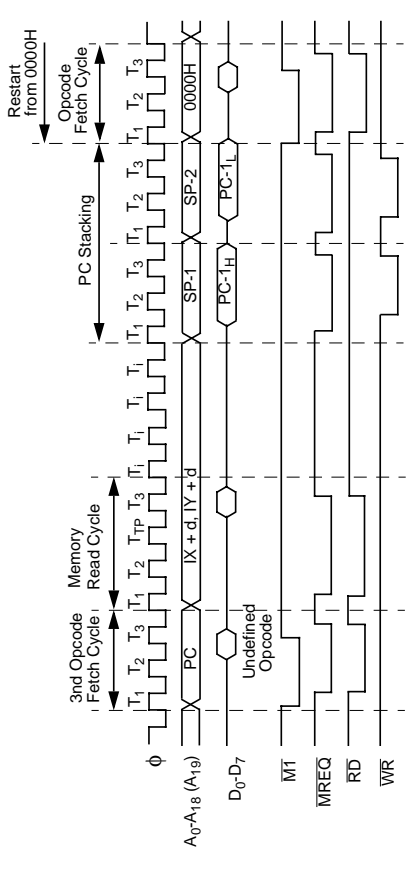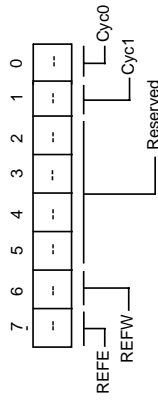
Figure 76. TRAP Timing-2nd Opcode Undefined

Table 14. DRAM Refresh Intervals

CYC1	CYC0	Insertion Interval	Ø:10 MHz	8 MHz	6 MHz	4 MHz	2.5 MHz
					Time Interval		
0	0	10 states	(1.0 µs)*	(1.25 µs)*	1.66 µs	2.5 µs	4.0 µs
0	1	20 states	(2.0 µs)*	(2.5 µs)*	3.3 µs	5.0 µs	8.0 µs
1	0	40 states	(4.0 µs)*	(5.0 µs)*	6.6 µs	10.0 µs	16.0 µs
1	1	80 states	(8.0 µs)*	(10.0 µs)*	13.3 µs	20.0 µs	32.0 µs

Note: *calculated interval

Refresh Control and Reset. After RESET, based on the initialized value of RCR, refresh cycles will occur with an interval of 10 clock cycles and be 3 clock cycles in duration.

Dynamic RAM Refresh Operation

1. Refresh Cycle insertion is stopped when the CPU is in the following states:

   a. During RESET

   b. When the bus is released in response to BUSREQ.

   c. During SLEEP mode.

   d. During WAIT states.

2. Refresh cycles are suppressed when the bus is released in response to BUSREQ. However, the refresh timer continues to operate. Thus, the time at

which the first refresh cycle occurs after th... Z80180/Z8S180/Z8L180 re-acquires the bus depend on the refresh timer and has no timing relationship wit... the bus exchange.

3. Refresh cycles are suppressed during SLEEP mode. If a refresh cycle is requested during SLEEP mode the refresh cycle request is internally "latched" (unt... replaced with the next refresh request). The "latched" refresh cycle is inserted at the end of the first machin... cycle after SLEEP mode is exited. After this initia... cycle, the time at which the next refresh cycle occur... depends on the refresh time and has no relationshi... with the exit from SLEEP mode.

4. The refresh address is incremented by one for eac... successful refresh cycle, not for each refresh. Thus... independent of the number of "missed" refres... requests, each refresh bus cycle will use a refres... address incremented by one from that of the previou... refresh bus cycles.

MMU COMMON BASE REGISTER

Mnemonic CBR

Address 38

MMU Common Base Register (CBR). CBR specifies th... base address (on 4 KB boundaries) used to generate a 20 bit physical address for Common Area 1 accesses. All bit... of CBR are reset to 0 during RESET.
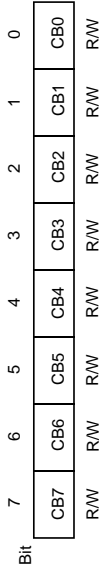
Bit	7	6	5	4	3	2	1	0
	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Figure 79. MMU Common Base Register (BBR: I/O Address = 38H)

MMU BANK BASE REGISTER (BBR).

Mnemonic BBR

Address 39

BBR specifies the base address (on 4 KB boundaries) used to generate a 19-bit physical address for Bank Area accesses. All bits of BBR are reset to 0 during RESET.
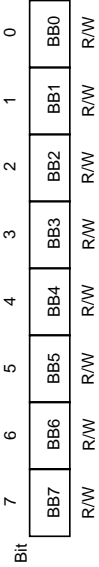
Bit	7	6	5	4	3	2	1	0
	BB7	BB6	BB5	BB4	BB3	BB2	BB1	BB0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Figure 80. MMU Bank Base Register (BBR: I/O Address = 39H)

MMU COMMON/BANK AREA REGISTER (CBAR).

Mnemonic CBAR

Address 3A

CBAR specifies boundaries within the Z80180/Z8S180/Z8L180 64 KB logical address space for up to three areas; Common Area), Bank Area and Common Area 1.

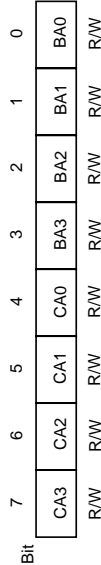MMU Common/Bank Area Register (CBAR: I/O Address = 3 AH)

Bit	7	6	5	4	3	2	1	0
	CA3	CA2	CA1	CA0	BA3	BA2	BA1	BA0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Figure 81. MMU Common/Bank Area Register (CBAR: I/O Address = 3 AH)

CA3-CA0:CA (bits 7-4). CA specifies the start (Low) address (on 4 KB boundaries) for the Common Area 1. This also determines the last address of the Bank Area. All bits of CA are set to 1 during RESET.

BA-BA0 (bits 3-0). BA specifies the start (Low) address (on 4 KB boundaries) for the Bank Area. This also determines the last address of the Common Area 0. All bits of BA are set to 1 during RESET.

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OPERATION MODE CONTROL REGISTER

Mnemonic OMCR

Address 3E

The Z80180/Z8S180/Z8L180 is descended from two different "ancestor" processors, Zilog's original Z80 and the Hitachi 64180. The Operating Mode Control Register (OMCR) can be programmed to select between certain differences between the Z80 and the 64180.
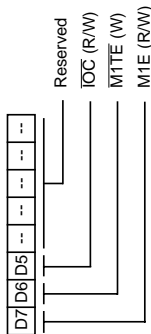
D7	D6	D5	--	--	--	--	--

Reserved
$\overline{IOC}$ (R/W)
M1TE (W)
M1E (R/W)

Figure 82. Operating Control Register (OMCR: I/O Address = 3EH)

Timing diagram signals: φ, A_0-A_{18} (A_{19}), D_0-D_7, $\overline{M1}$, $\overline{MREQ}$, $\overline{RD}$, ST

Sequence values: T_1 T_2 T_3 T_1 ... PC · EDH · PC+1 · 4DH · PC · EDH · PC+1 · 4DH

Figure 83. RETI Instruction Sequence with MIE=0

M1E ($\overline{M1}$ Enable). This bit controls the M1 output and is set to a 1 during reset.

When M1E=1, the $\overline{M1}$ output is asserted Low during the opcode fetch cycle, the $\overline{INT0}$ acknowledge cycle, and the first machine cycle of the $\overline{NMI}$ acknowledge.

On the Z80180/Z8S180/Z8L180, this choice makes the processor fetch an RETI instruction once, and when fetching an RETI from zero-wait-state memory will use three clock machine cycles which are not fully Z80-timing compatible but are compatible with the on-chip CTCs.

When MIE=0, the processor does not drive $\overline{M1}$ Low during instruction fetch cycles, and after fetching an RETI instruction once with normal timing, it goes back and re-fetches the instruction using fully Z80-compatible cycles that include driving M1 Low. This may be needed by some external Z80 peripherals to properly decode the RETI instruction.I/O Control Register (ICR).
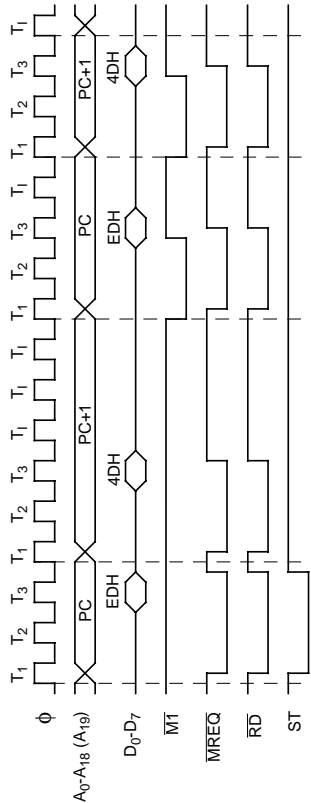
ICR allows relocating of the internal I/O addresses. ICR also controls enabling/disabling of the IOSTOP mode (Figure 84).

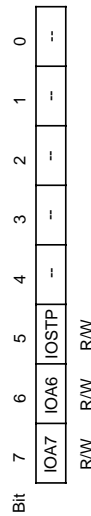| Bit 7	6	5	4	3	2	1	0
IOA7	IOA6	IOSTP	--	--	--	--	--
R/W	R/W	R/W	R/W				

Figure 84. I/O Control Register (ICR: I/O Address = 3FH)

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Enhanced Z180 Microprocessor Zilog

IOA7, 6: I/O Address Relocation (bits 7,6). IOA7 and IOA6 relocate internal I/O as shown in Figure 85. Note that the high-order 8 bits of 16-bit internal I/O address are always 0. IOA7 and IOA6 are cleared to 0 during Reset.
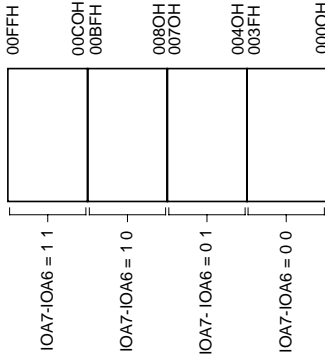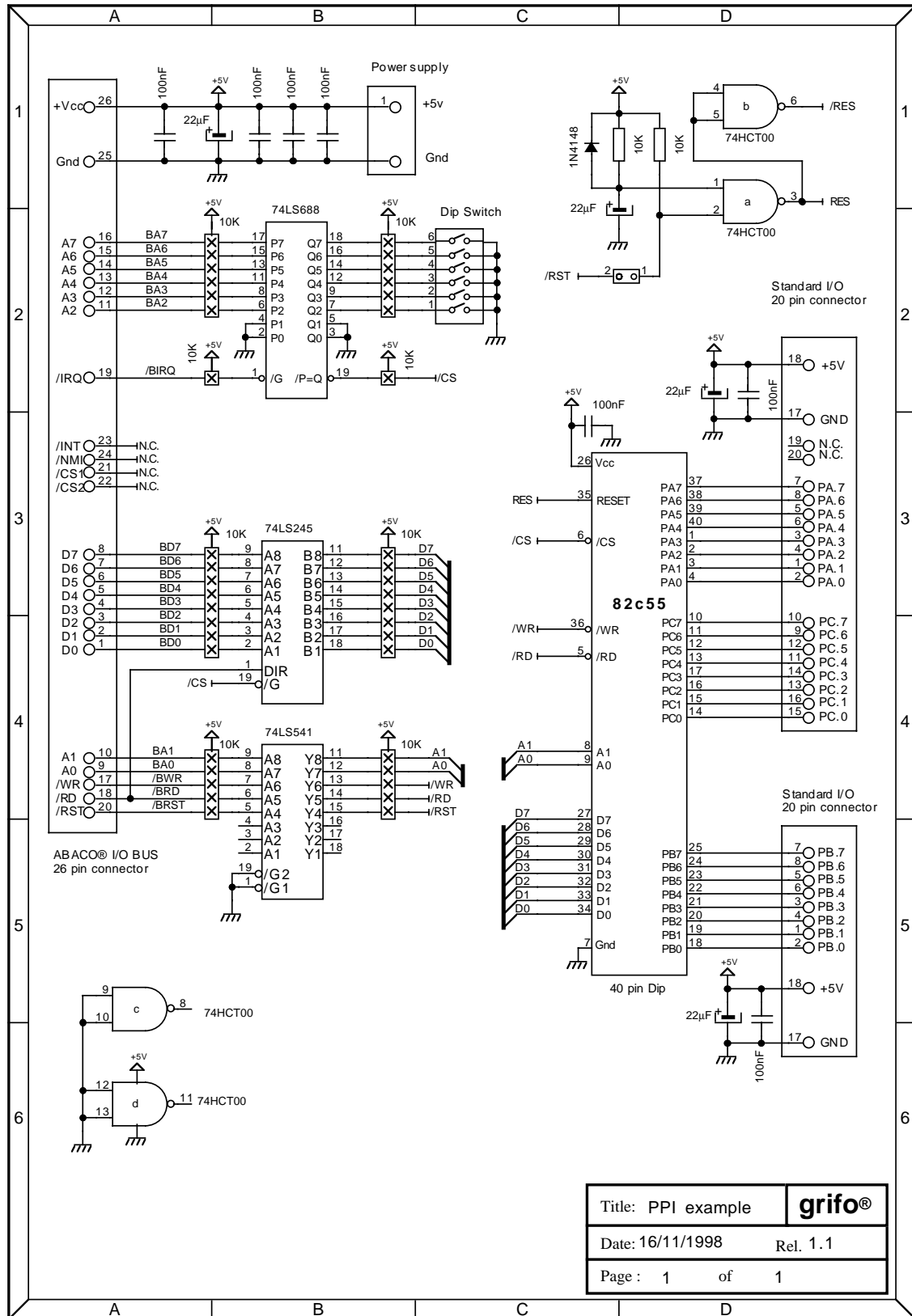
Address relocation map:

00FFH
00C0H
00BFH — IOA7-IOA6 = 1 1
0080H
0070H — IOA7-IOA6 = 1 0
0040H
003FH — IOA7-IOA6 = 0 1
0000H — IOA7-IOA6 = 0 0

Figure 85. I/O Address Relocation

IOSTP. IOSTOP Mode (bit 5). IOSTOP mode is enabled when IOSTP is set to 1. Normal I/O operation resumes when IOSTOP is reprogrammed or Reset to 0
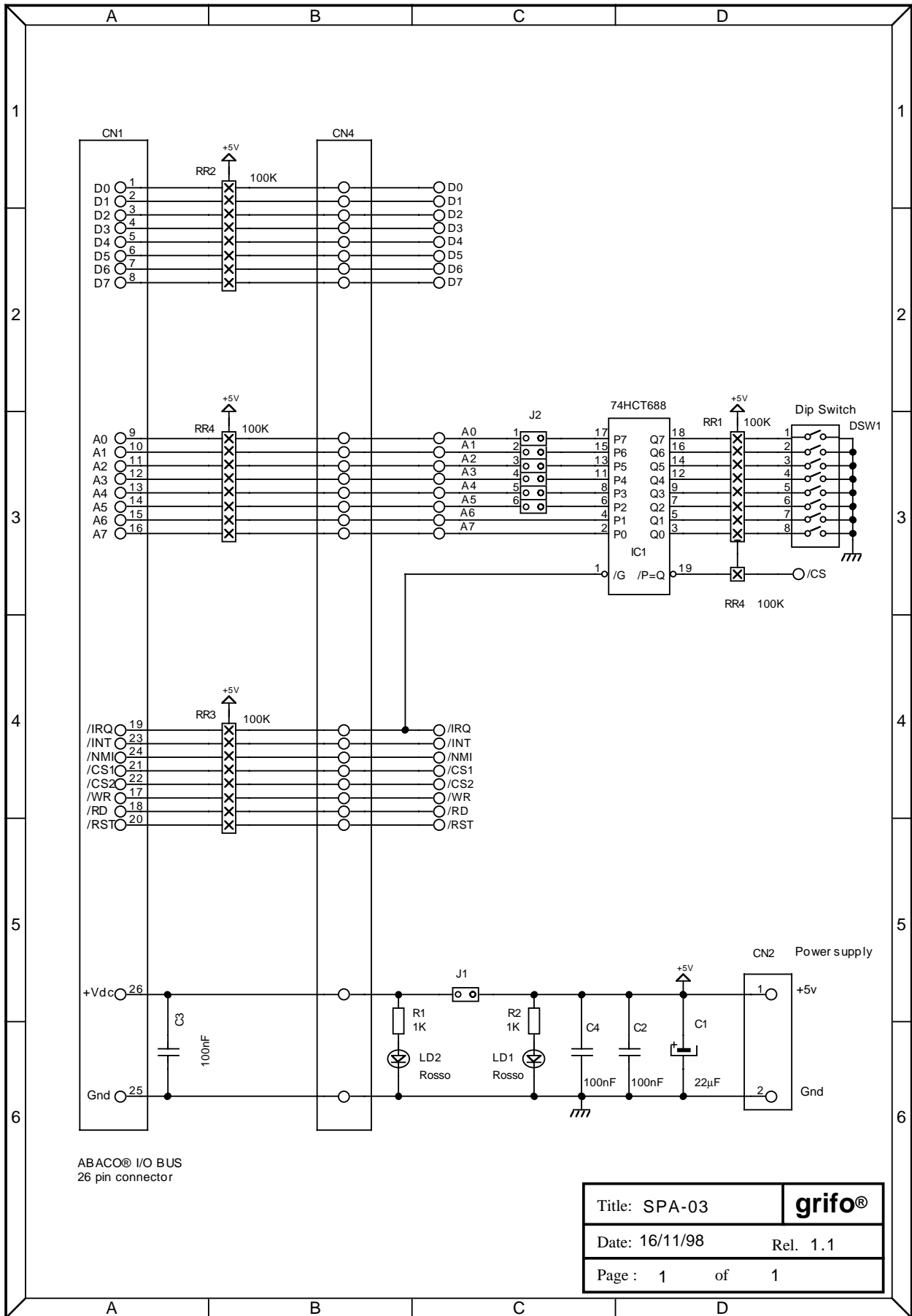
APPENDIX C: ELECTRIC DIAGRAMS

In this appendix are available some electric diagrams of the most frequently used **GPC® 184** interfaces. All these interface can be yourself produced and some of them are standard **grifo®** cards and, if required, they can be directly ordered.

FIGURE C1: PPI EXPANSION ELECTRIC DIAGRAM

FIGURE C2: SPA 03 ELECTRIC DIAGRAM

Standard I/O 20 pin connector

DISPLAY 2x20

DISPLAY 4x20

CN4

RR1

CN1

CN2

PA.7	7	D7	14
PA.6	8	D6	13
PA.5	5	D5	12
PA.4	6	D4	11
PA.3	3	D3	10
PA.2	4	D2	9
PA.1	1	D1	8
PA.0	2	D0	7

+5V RR2

PC.2	13	E	6
PC.1	16	R/W	5
PC.0	15	RS	4
PC.3	14		

Contrast RV1

+5V J1

+5V

R1   R3

+5V	18	2
GND	17	1

C2   C1

R2

Keyboard connector

Matrix Keyboard 4x4

RR2   R7

PC.4	11	R7	4
PC.5	12	R6	3
PC.6	9	R5	3
PC.7	10	R4	2
N.C.	19		
N.C.	20		

D	C	B	A	5
#	9	6	3	
0	8	5	2	
*	7	4	1	

1	**2**	**3**	**A**	5
4	**5**	**6**	**B**	6
7	**8**	**9**	**C**	7
*	**0**	#	**D**	8

1 2 3 4

1 2 3 4 5 6 7 8

DC Power supply

CN3

CN5   +5V   C5

SN7407

1	3	5	7

D0   D1   D2.   D3

PD1

C3 C4

SWITCHING REGOLATOR

A

C6 C9 L1 C8 C7

B

TZ1

OPTIONAL

AC Power supply

Title:	QTP 16P	grifo®
Date: 22-07-1998		Rel. 1.2
Page : 1	of	1

FIGURE C3: QTP 16P ELECTRIC DIAGRAM
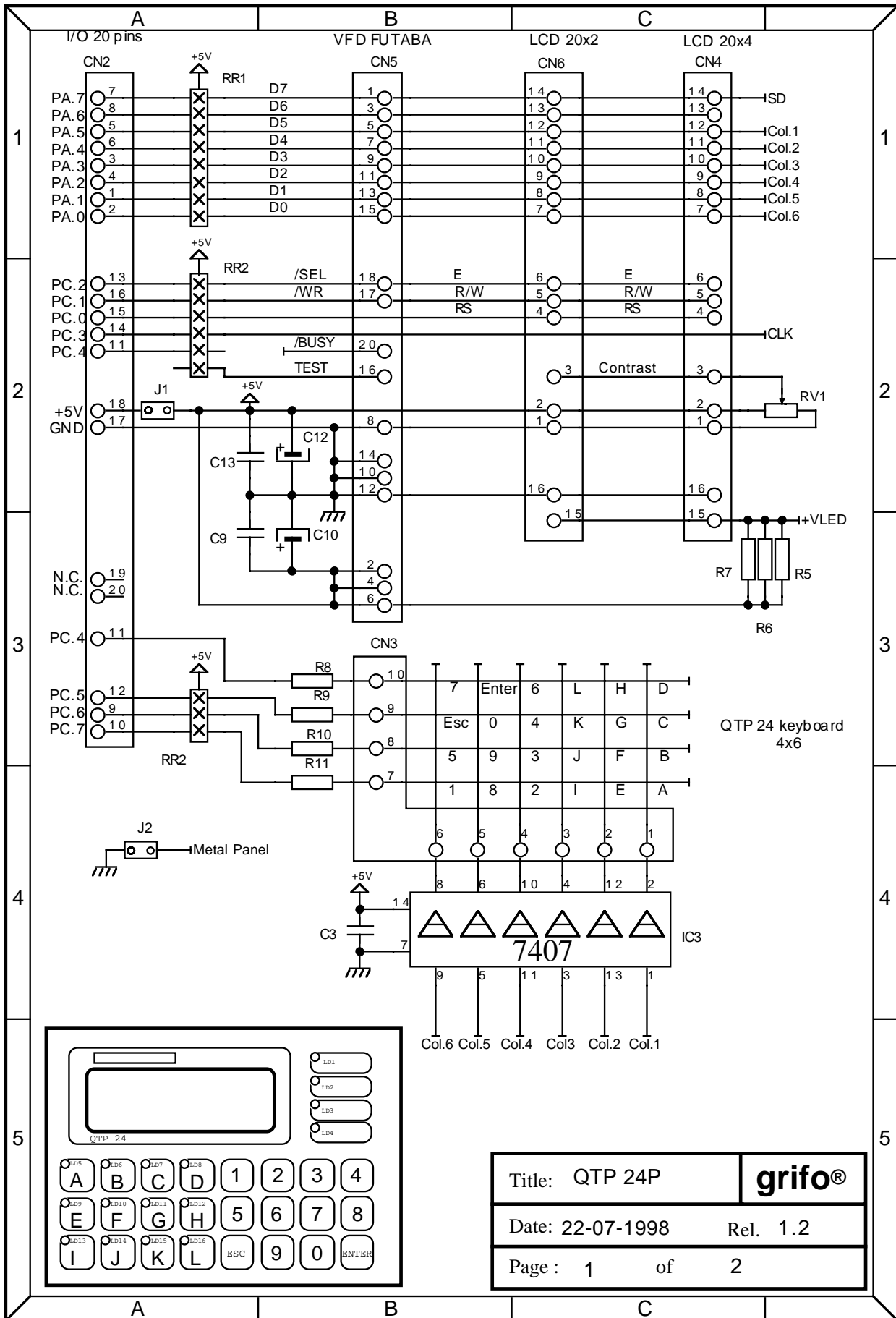
FIGURE C4: QTP 24P ELECTRIC DIAGRAM (1 OF 2)

FIGURE C5: QTP 24P ELECTRIC DIAGRAM (2 OF 2)
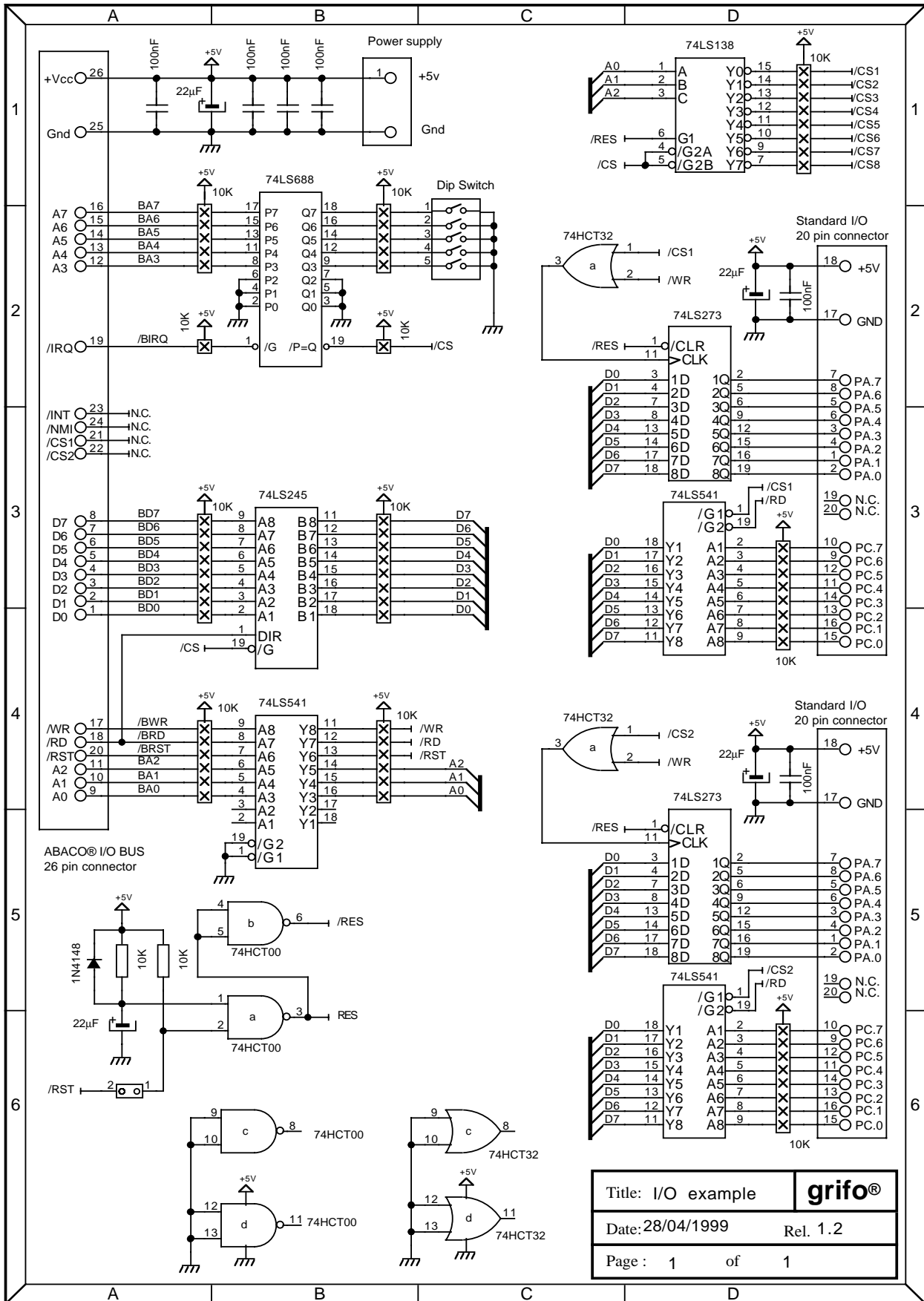
FIGURE C6: ABACO® I/O BUS INPUT OUTPUT ELECTRIC DIAGRAM
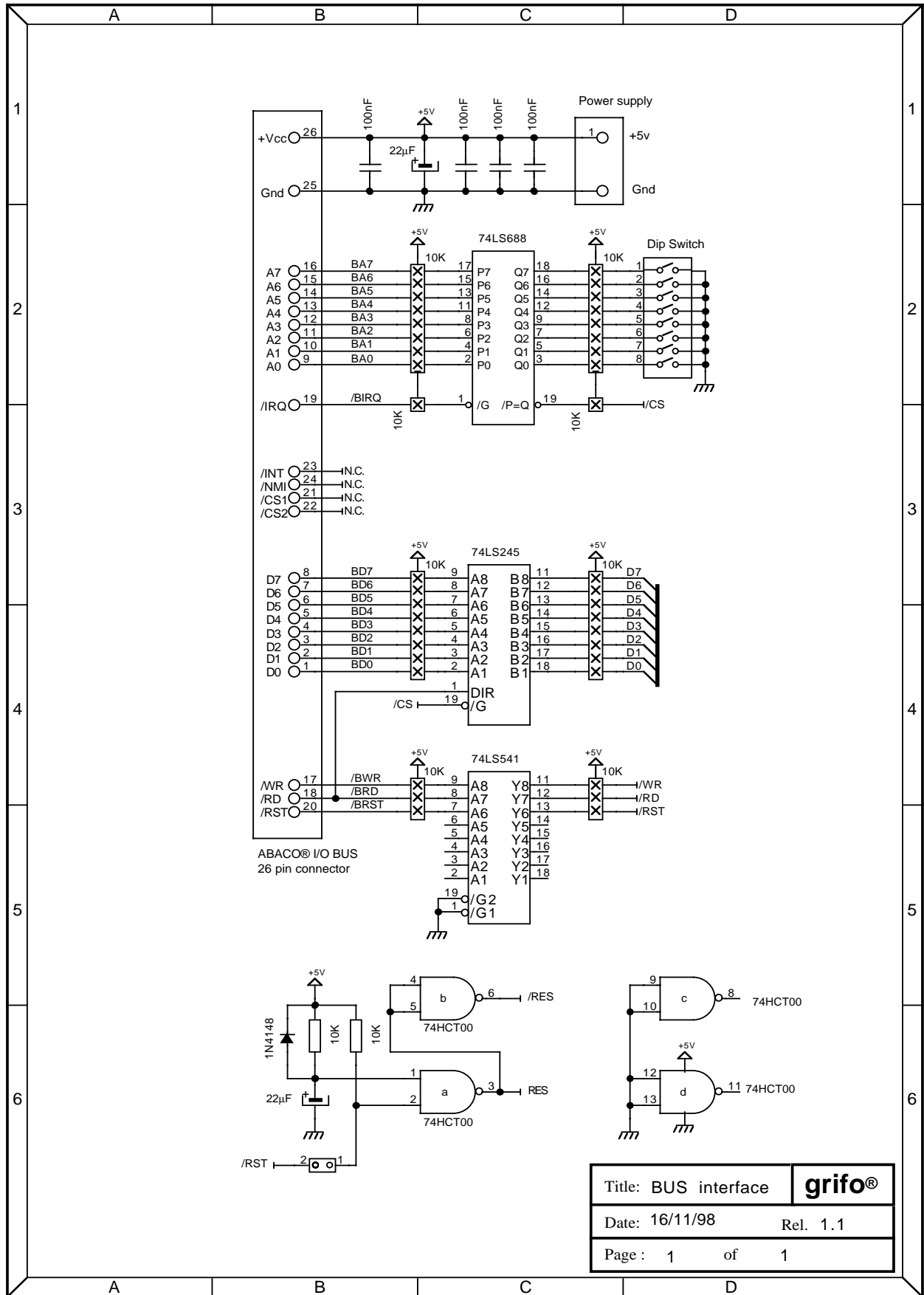
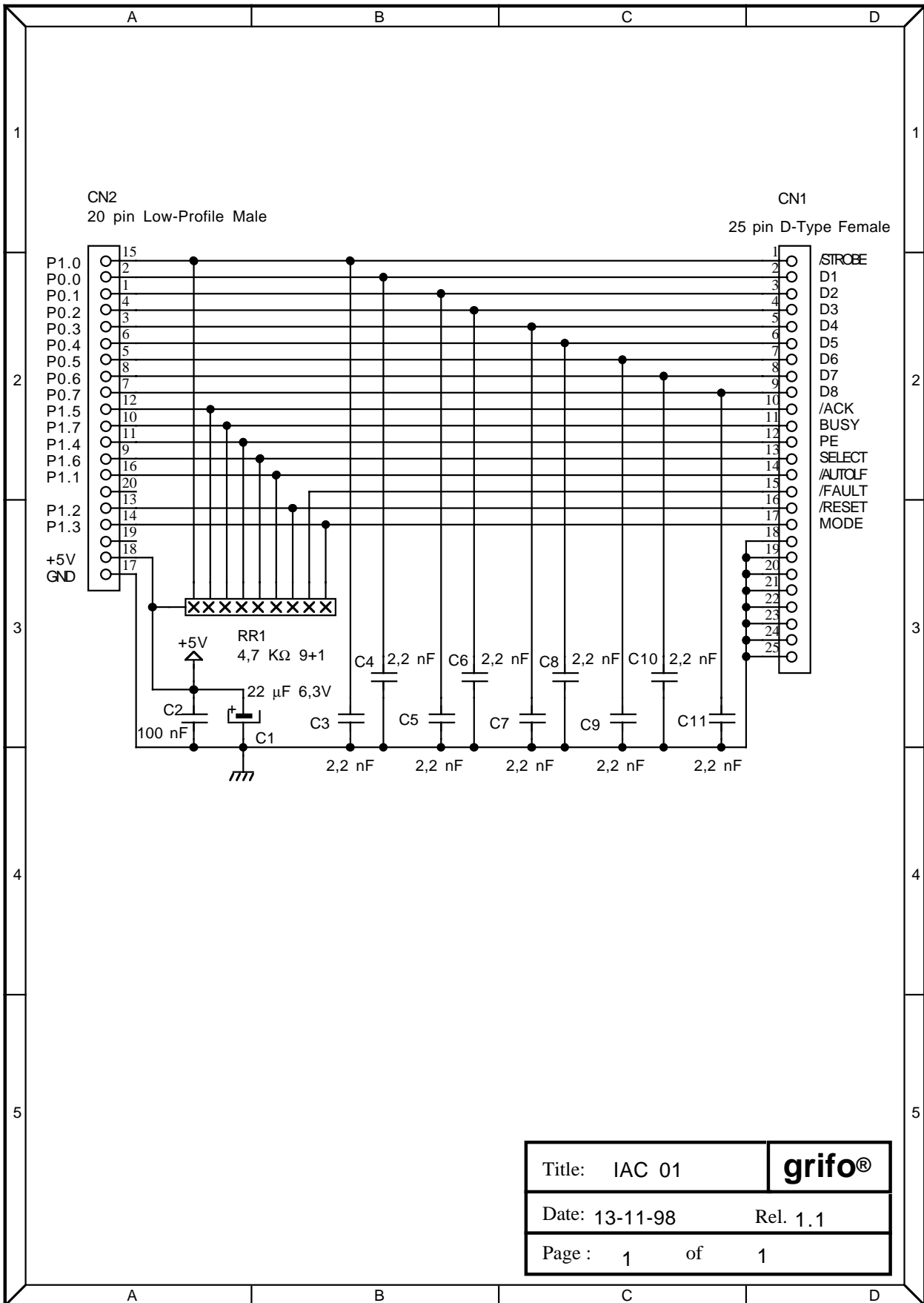**FIGURE C7: BUS INTERFACE ELECTRIC DIAGRAM**

CN2
20 pin Low-Profile Male

CN1
25 pin D-Type Female

P1.0	15
P0.0	2
P0.1	1
P0.2	4
P0.3	3
P0.4	6
P0.5	5
P0.6	8
P0.7	7
P1.5	12
P1.7	10
P1.4	11
P1.6	9
P1.1	16
	20
P1.2	13
P1.3	14
	19
+5V	18
GND	17

CN1:
1 /STROBE
2 D1
3 D2
4 D3
5 D4
6 D5
7 D6
8 D7
9 D8
10 /ACK
11 BUSY
12 PE
13 SELECT
14 /AUTOLF
15 /FAULT
16 /RESET
17 MODE
18
19
20
21
22
23
24
25

RR1
4,7 KΩ 9+1

+5V

22 µF 6,3V

C2
100 nF
C1

C4 2,2 nF   C6 2,2 nF   C8 2,2 nF   C10 2,2 nF

C3   C5   C7   C9   C11
2,2 nF   2,2 nF   2,2 nF   2,2 nF   2,2 nF

Title:	IAC 01	grifo®
Date: 13-11-98		Rel. 1.1
Page : 1	of	1

FIGURE C8: IAC 01 ELECTRIC DIAGRAM

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RS 485   **4**, **7**, **8**, **14**, **16**, **17**, **21**, **24**, **30**
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