GPC® 183
General Purpose Controller Z8S180

TECHNICAL MANUAL

GPC® 183
Edition 5.10
Rel. 02 April 2002
100x149 mm size, Intelligent module of the Abaco® BLOCK series; optional plastic mount for connection to DIN 46277-1 and DIN 46277-3 Ω rails; 22 MHz standard CPU Z8S180; up to 512K of EPROM or FLASH and up to 512K of SRAM; through FGDOS the memory that exceeds 64K is managed as RAM-ROM DISK, it is possible deleting and re-programming the on board FLASH, automatically, with the user program; back up circuitry for SRAM and RTC through internal and external Lithium battery; Real Time Clock capable to generate INT; serial EEPROM up to 8KBytes; 11 lines 12 bits A/D converter with range +2.5 V or 0÷20 mA; 28 TTL I/O lines which are settable by software, 2 status LEDs and active BUZZER; clocked serial I/O interface at user disposal on I/O connector; 1 software readable 3 ways dip switch, and dip for RUN/DEBUG mode; 2 internal channels of Programmable Reload timer of 16bits; 2 serial lines in RS232, one configurable in RS422, RS485 or Current Loop; double Baud Rate generator, settable by software, up to 115.2 KBaund; Watchdog circuitry, hardware switching off, with status LED; 26 pins expansion connector for Abaco® I/O BUS; 2 standard 20 pins Abaco® I/O connectors; 1 standard 20 pins Abaco® A/D connector; Low Power function in Halt, Iostop, Sleep, System Stop, Idle, Standby mode; optional built in wide range power supply, or single external 5Vdc, 235 mA power supply; on board protection against voltage peaks by TransZorb™; wide range of development software such as: Remote Symbolic Debugger, Macro Assembler, GET80, BASIC NSB8, FORTH, C Compilers, HTC 80, Lisp, PASCAL 80, etc.
**IMPORTANT**

Although all the information contained herein have been carefully verified, grifo® assumes no responsibility for errors that might appear in this document, or for damage to things or persons resulting from technical errors, omission and improper use of this manual and of the related software and hardware. 

grifo® reserves the right to change the contents and form of this document, as well as the features and specification of its products at any time, without prior notice, to obtain always the best product.

For specific informations on the components mounted on the card, please refer to the Data Book of the builder or second sources.

**SYMBOLS DESCRIPTION**

In the manual could appear the following symbols:

- !: Attention: Generic danger
- ⚡: Attention: High voltage

**Trade Marks**

GPC®, grifo®: are trade marks of grifo®.

Other Product and Company names listed, are trade marks of their respective companies.
GENERAL INDEX

INTRODUCTION ................................................................................................................... ..... 1
CARD VERSION ................................................................................................................... 1

GENERAL FEATURES ........................................................................................................... 2
  CPU ................................................................................................................................. 3
  BUZZER ........................................................................................................................... 3
  CLOCK ............................................................................................................................ 3
  MEMORY DEVICES ......................................................................................................... 4
  SERIAL COMMUNICATION ............................................................................................. 4
  POWER SUPPLY ............................................................................................................... 4
  ABACO® I/O BUS ........................................................................................................... 6
  I/O LINES ....................................................................................................................... 6
  REAL TIME CLOCK ........................................................................................................ 6
  WATCH DOG .................................................................................................................. 6
  RESET CONTACT .......................................................................................................... 7
  A/D CONVERTER .......................................................................................................... 7
  BOARD CONFIGURATION .............................................................................................. 7
  CONTROL LOGIC .......................................................................................................... 7

TECHNICAL FEATURES ..................................................................................................... 8
  GENERAL FEATURES .................................................................................................. 8
  PHYSICAL FEATURES ................................................................................................... 8
  ELECTRIC FEATURES .................................................................................................... 9

INSTALLATION .................................................................................................................. 10
  CONNECTIONS ............................................................................................................. 10
    CN 2 - POWER SUPPLY CONNECTOR WITH SUPPLY SECTION ................................ 10
    CN3 - PPI 82C55 PORT A AND C I/O CONNECTOR .................................................... 12
    CN4 - BACK UP EXTERNAL BATTERY CONNECTOR ............................................... 13
    CN5 - PPI 82C55 PORT B, TTL INPUTS AND SYNC SERIAL CONNECTOR ............. 14
    CN6 - A/D CONVERTER INPUT CONNECTOR ......................................................... 16
    CN1 - ABACO® I/O BUS CONNECTOR ...................................................................... 18
    CN7B - SERIAL LINE B CONNECTOR ....................................................................... 20
    CN7A - SERIAL LINE A CONNECTOR ....................................................................... 26
  DIGITAL I/O INTERFACES ............................................................................................ 28
  I/O CONNECTION ......................................................................................................... 28
  RESET KEY .................................................................................................................. 29
  TYPE OF ANALOG INPUT SELECTION ...................................................................... 29
  TEST POINT .................................................................................................................. 29
  TRIMMERS AND CALIBRATION .................................................................................. 30
  VISUAL SIGNALATIONS .............................................................................................. 30
  JUMPERS ....................................................................................................................... 31
    5 PINS JUMPERS ...................................................................................................... 31
    2 PINS JUMPERS ...................................................................................................... 32
    3 PINS JUMPERS ...................................................................................................... 32
FIGURES INDEX

FIGURE 1: BLOCK DIAGRAM ................................................................. 5
FIGURE 3: CN2 - POWER SUPPLY CONNECTOR FOR ON BOARD SUPPLY SECTION ......................................................... 10
FIGURE 4: CARD PHOTO ........................................................................ 11
FIGURE 5: CN3 - PPI 82C55 PORT A AND C I/O CONNECTOR ............. 12
FIGURE 6: PORTS A AND C ON CN3 BLOCK DIAGRAM ....................... 13
FIGURE 7: CN4 - EXTERNAL BACK UP BATTERY CONNECTOR .......... 13
FIGURE 8: CN5 - PPI 82C55 PORT B, TTL INPUTS AND SYNCHRONOUS SERIAL LINE CONNECTOR ................... 14
FIGURE 9: PPI 82C55 PORT B, TTL INPUTS AND SYNC SERIAL LINE ON CN5 BLOCK DIAGRAM ................................. 15
FIGURE 10: CN6 - A/D CONVERTER INPUT CONNECTOR .................... 16
FIGURE 11: A/D CONVERTER INPUT BLOCK DIAGRAM ..................... 17
FIGURE 12: CN1 - ABACO® I/O BUS CONNECTOR ............................... 18
FIGURE 13: COMPONENTS MAP (COMPONENTS AND SOLDER SIDE) 19
FIGURE 14: CN7B - SERIAL LINE B CONNECTOR .................................. 20
FIGURE 15: SERIAL COMMUNICATION DIAGRAM .............................. 21
FIGURE 16: RS 232 POINT TO POINT CONNECTION EXAMPLE .......... 22
FIGURE 17: RS 422 POINT TO POINT CONNECTION EXAMPLE .......... 22
FIGURE 18: RS 485 POINT TO POINT CONNECTION EXAMPLE .......... 22
FIGURE 19: RS 485 NETWORK CONNECTION EXAMPLE ....................... 23
FIGURE 20: 4 WIRES CURRENT LOOP POINT TO POINT CONNECTION EXAMPLE ................................................................. 24
FIGURE 21: 2 WIRES CURRENT LOOP POINT TO POINT CONNECTION EXAMPLE ................................................................. 24
FIGURE 22: CURRENT LOOP NETWORK CONNECTION EXAMPLE .......... 25
FIGURE 23: CN7A - SERIAL LINE A CONNECTOR .................................. 26
FIGURE 24: LEDS, DIP SWITCH, CONNECTORS, ETC. LOCATION .......... 27
FIGURE 25: VISUAL SIGNALATIONS TABLE ......................................... 30
FIGURE 26: JUMPERS SUMMARIZING TABLE ....................................... 31
FIGURE 27: 5 PINS JUMPERS LOCATION ............................................. 31
FIGURE 28: 2 PINS JUMPERS TABLE .................................................. 32
FIGURE 29: 3 PINS JUMPERS TABLE .................................................. 32
FIGURE 30: JUMPERS LOCATION .......................................................... 33
FIGURE 31: MEMORY SELECTION TABLE ........................................... 34
FIGURE 32: SERIAL COMMUNICATION DRIVER LOCATION .............. 39
FIGURE 33: I/O ADDRESSING TABLE - PART I ..................................... 44
FIGURE 34: I/O ADDRESSING TABLE - PART II .................................... 45
FIGURE 35: MEMORY ALLOCATION .................................................. 47
FIGURE 36: GPC®183 AVAILABLE CONNECTIONS DIAGRAM .......... 57
FIGURE B1: PPI EXPANSION ELECTRIC DIAGRAM ........................................... C-1
FIGURE B2: SPA 03 ELECTRIC DIAGRAM ........................................... C-2
FIGURE B3: QTP 16P ELECTRIC DIAGRAM ......................................... C-3
FIGURE B4: QTP 24P ELECTRIC DIAGRAM (1 OF 2) ............................... C-4
FIGURE B5: QTP 24P ELECTRIC DIAGRAM (2 OF 2) ............................... C-5
FIGURE B6: ABACO® I/O BUS INPUT OUTPUT ELECTRIC DIAGRAM ................................................................................. C-6
FIGURE B7: BUS INTERFACE ELECTRIC DIAGRAM .......................... C-7
FIGURE B8: IAC 01 ELECTRIC DIAGRAM ............................................ C-8
INTRODUCTION

The use of these devices has turned - IN EXCLUSIVE WAY - to specialized personnel.

The purpose of this handbook is to give the necessary information to the cognizant and sure use of the products. They are the result of a continual and systematic elaboration of data and technical tests saved and validated from the manufacturer, related to the inside modes of certainty and quality of the information.

The reported data are destined- IN EXCLUSIVE WAY- to specialized users, that can interact with the devices in safety conditions for the persons, for the machine and for the enviroment, impersonating an elementary diagnostic of breakdowns and of malfunction conditions by performing simple functional verify operations, in the height respect of the actual safety and health norms.

The informations for the installation, the assemblage, the dismantlement, the handling, the adjustment, the reparation and the contingent accessories, devices etc. installation are destined - and then executable - always and in exclusive way from specialized warned and educated personnel, or directly from the TECHNICAL AUTHORIZED ASSISTANCE, in the height respect of the manufacturer recommendations and the actual safety and health norms.

The devices can't be used outside a box. The user must always insert the cards in a container that respect the actual safety normative. The protection of this container is not threshold to the only atmospheric agents, but specially to mechanic, electric, magnetic, etc. ones.

To be on good terms with the products, is necessary guarantee legibility and conservation of the manual, also for future references. In case of deterioration or more easily for technical updates, consult the AUTHORIZED TECHNICAL ASSISTANCE directly.

To prevent problems during card utilization, it is a good practice to read carefully all the informations of this manual. After this reading, the user can use the general index and the alphabetical index, respectively at the begining and at the end of the manual, to find information in a faster and more easy way.

CARD VERSION

The present handbook is reported to the GPC® 183 card release 300396 and later. The validity of the bring information is subordinate to the number of the card release. The user must always verify the correct correspondence among the two denotations. On the card the release number is present in more points both board printed diagram (serigraph) and printed circuit (for example near battery BT1 on the component side and on the solder side).
General Features

The GPC® 183 is a powerful control Low Cost module capable of operation in stand alone mode or as an intelligent peripheral, and/or remoted, in a wider telecontrol or acquisition network. The GPC® 183 module is secured in a plastic mount for connection to Omega rails DIN 46277-1 and DIN 46277-3, thereby dispensing with the need of rack and allowing a less costly mounting direct to the electrical control panel.

Programming and exploiting the resources of this module is extremely easy thanks to the help of the stout FGDOS romated operative system. This latter supports high level languages such as BASIC PASCAL, C Compilers and so on; it makes available the memory resources as they should be ROM/RAM disk allowing an immediate use of this devices at high level. This module linked to the MCI64 and FGDOS manages PCMCIA cards of RAM cards and, directly, the on board peripherals as A/D converter, serial EEPROM.

In addition to that the GPC® 183 allows a direct management of LCD or Fluorescent displays and matrix keyboard. For an immediate use of this command, KDx x24 boards are available, or if you need a finished object, there are the QTP xxP. These operator panels, offered in the open frame version, bear the same aesthetic as QTP xx, but, as the local intelligence is not furnished, they are driven directly by GPC® 183, allowing a notable cost reduction.

The FGDOS affords truly notable debug facilities, and allows to program directly on board a FLASH with the user program.

The GPC® 183 is equipped with a series of standard Abaco® connectors allowing immediate use of the many BLOCK I/O modules available, or enabling a simple and inexpensive means of connections to equipment interfaces made by the user or by third parties. Abaco® I/O BUS connector allows to drive directly ZBR 324, ZBT 324, ZBR 246, ZBT 246, ZBR 168, and through ABB 03, ABB 05 and so on, it is possible to run all peripheral cards available on ABACO® BUS

- 100x149 mm size, Intelligent module of the Abaco® BLOCK series
- Optional plastic mount for connection to DIN 46277-1 and DIN 46277-3 Ω rails
- 22 MHz standard CPU Z8S180
- Up to 512K of EPROM or FLASH and up to 512K of SRAM. Through FGDOS the memory that exceed 64K is managed as RAM/ROM Disk. It is possible deleting and re-programming the on borad FLASH, automatically, with the user program
- Back up circuitry for SRAM and RTC through internal and external Lithium battery
- Real Time Clock capable to generate INT
- Serial EEPROM up to 8KBytes
- 11 lines 12 bits A/D converter with range +2.5 V; 0÷20 mA
- 28 TTL I/O lines which are settable by software, 2 status LEDs and active BUZZER
- Clocked serial I/O interface at user disposal on I/O connector
- 1 software readable 3 ways dip switch, and dip for RUN/DEBUG mode
- 2 internal channels of Programmable Reload timer of 16bits
- 2 serial lines in RS232, one configurable in RS422, RS485 or Current Loop
- Double Baud Rate generator, settable by software, up to 115.2 KBaupd
- Watch dog circuitry, hardware switching off, with status LED
- 26 pins expansion connector for Abaco® I/O BUS
- 2 standard 20 pins Abaco® I/O connectors
- 1 standard 20 pins Abaco® A/D connector
- Low Power function in Halt, Iostop, Sleep, System Stop, Idle, Standby mode
- Optional Built in wide range power supply, or single external 5Vdc, 235 mA power supply
- On board protection aganist voltage peaks by TransZorb™
- Wide range of development software such as: Remote Symbolic Debugger, Macro Assembler, GET 80, BASIC NSB8, FORTH, C Compilers, HTC 80, Lisp, PASCAL 80, etc.

Here follows a description of the board's functional blocks, with an indication of the operations performed by each one. To easily locate these blocks and verify their connections please refer to figure 1.

**CPU**

GPC® 183 board is designed to employ the Z8S180 CPU manufactured by ZILOG. This 8 bits CPU is code compatible with Z80 and Z180 so it features an extended instructions set (170), high speed of execution and data manipulation and efficient vectored interrupts management. Remarkable is the presence of these peripherals inside the CPU:

- Two 16 bits timers, provided with programmable prescaler (PRT);
- Two asynchronous serial lines capable to manage handshake signals (ASCI);
- Two DMA channels for high speed data transfers (DMAC);
- Memory management unit (MMU);
- One synchronous serial line (CSI/O);
- Interrupt controller;
- Wait states generator to access external devices;
- Five different operating modes, to reduce power consumption;

For further informations about this component please refer to the manufacturer documentation, or see Appendix A of this manual.

**BUZZER**

GPC® 183 board features a capacitive buzzer capable to produce a constant sound, driven by a circuitry that can be software enabled and/or disabled through the control logic, that can be used to generate acoustic alerts, sound feedback, etc.

**CLOCK**

GPC® 183 is provided with a circuitry that generates the CPU clock frequency (22.1184 MHz); this frequency is used also to generate the frequencies needed to the other sections of the board (Timer, serial lines, etc.). If the User needs to run very fast applications the clock frequency can be even doubled by intervening on the proper circuitry (for more informations please contact grifo®). We would remark that the CPU clock frequency is the same of the crystal by programming a CPU register.
MEMORY DEVICES

On the card can be mounted 1032K bytes of memory divided with a maximum of 512KByte EPROM or FLASH EPROM, 512KByte SRAM and 8KByte serial EEPROM. The **GPC® 183** memory configuration must be chosen considering the application to realize or the specific requirements of the user. Normally the card is equipped with 128KByte of static RAM and 8KByte of serial EEPROM; all different configurations must be specified from the user, at the moment of the order. With the on board back up circuit there is the possibility to keep data, also when power supply is failed; in this way the card is always able to maintain parameters, logged data, system status and configuration, etc. without using expensive external UPS. The back up circuit is supplied by a on board lithium battery or an external battery to be connected to a specific connector. The addressing of memory devices is controlled by a specific control logic, that provides to allocate the devices in the microprocessor address space, this control logic automatically manages the different addressing mode and it satisfies the requests of each **GPC® 183** software tools.

For further information about memory configuration, sockets description and jumpers connection, please refer to "ADDRESSES AND MAPS” and "PERIPHERAL DEVICES SOFTWARE DESCRIPTION" chapters and to "MEMORY SELECTION" paragraph for detailed informations about sockets to use and jumpers configuration.

SERIAL COMMUNICATION

Serial communication is completely software settable both for protocol and for speed (which ranges from 50 to as high as 115.2Kbaud with standard clock frequency). These settings are performed programming the ASCI inside the microprocessor and the baud rate generator, for further information please refer to the manifacturer documentation or to Appendix A of this manual. By hardware it is possible to select, through some on board jumpers, the electric communication protocol. In detail, one line is always buffered as RS 232, while the other line can be buffered in four different electrical protocols: **RS 232**, **current loop**, **RS 485** or **RS 422**; in this last cases also directionality and line activation is programmable.

POWER SUPPLY

The unique voltage needed to supply the board (+5 Vdc) can be provided in two ways: directly through pin 25 (GND) and 26 (+5 Vdc) of connector CN1 or through the switching supply sections. The type of supply cannot be changed by the user so it must be specified in the order. On the card the power supply signals are available on all the connectors but when the best power layout is required we suggest to supply power through CN1 and to get it from the other connectors. This explain the direction reported for +5 Vdc signal on each connector of the card. The can be anyway supplied from a connector indicate as output for +5 Vdc but this is severly discouraged so eventual consequences are totally responsibility of the user.

Switching supply section requires an input voltage in the range 8÷24 Vac (12÷34 Vdc) which can be provided through specific standard connectors quick and easy to install, for further information please refer to the paragraph “SUPPLY VOLTAGES”. Power supply circuit is designed to reduce consumption and to increase electrical noise immunity. Please remind that on board there is a protection circuit aganist voltage peaks by **TransZorb™** and that it is a good practise to mantain galvanically isolated from +5 Vdc all the others power voltages of the developed system.
**FIGURE 1: BLOCK DIAGRAM**

- **CPU Z8S180**
- **Drivers**: RS 232, RS 422, RS 485, C. LOOP
- **Serial Lines**: CN7A (Serial Line A), CN7B (Serial Line B)
- **I/O Lines**: CN5 (12 I/O Lines), CN3 (16 I/O Lines)
- **Power Supply**: +5 Vdc, Optional Power Supply
- **Control Logic**: CN1 (ABACO® I/O Bus), CN2 (Power)
- **A/D Lines**: CN6 (11 A/D Lines)
- **Watchdog**: Activity LED, Spot LED, Buzzer
- **RTC**: Real Time Clock
- **EPROMs**: IC10 (EEPROM), IC5 (EPROM)
- **SRAM**: IC4
- **Battery**: CN4 (Back Up)
ABACO® I/O BUS

One of the most important features of GPC® 183 is its possibility to be interfaced to industrial ABACO® I/O BUS. Thanks to its standard ABACO® I/O BUS connector, the card can be connected to some of the numerous grifo® boards, both intelligent and not. For example the user can directly use cards for analog signals acquisition, cards for analog signals generation (D/A), cards for digital I/O signals management, cards with timers and counters, cards for temperature controls, etc. also custom boards designed to satisfy specific needs of the end user.

Using ABB 03 or ABB 05 mother boards it is possible manage all the BUS ABACO® single EURO cards. So GPC® 183 becomes the right component for each industrial automation system, in fact ABACO® I/O BUS makes the card easily expandable with the best price/performance ratio.

I/O LINES

GPC® 323 features three 8 bits parallel ports performing 24 TTL level I/O signals whose directionality is byte-level software settable plus four TTL input lines managed by the control logic. These I/O signals provide the GPC® 183 board more employ possibilities (for example the management of non intelligent peripherals, interfaces, etc.) also in applications where the communication handshake must be completely software managed. The lines are available through two standard I/O ABACO® connectors and can be completely programmed by software programming five registers located in the CPU addressing space.

REAL TIME CLOCK

GPC® 183 board is provided with a complete real time clock device capable to manage hours, minutes, seconds, day of month, month, year and day of week in stand alone mode. The component is supplied by the back up circuitry to warrant data integrity in every working condition and is completely software programmable acting on 16 registers addressable in the CPU I/O addressing space by a specific memory management circuitry. The RTC section can generate interrupts at a software programmable rate, for diverting the CPU from its normal tasks or awakening it from one of its low consumption working modes.

WATCH DOG

GPC® 183 board is provided with a watch dog circuitry that, if used, allows to exit from infinite loop or abnormal conditions not managed by the application program. This circuitry is made by an astable section with 1.5 sec of intervent time, is completely software managed (by accessing a register addressed in the CPU addressing space) and gives the board an extreme degree of safety. Changes of watch dog circuitry intervent time are possible by interventing on its RC net on specific user request; in case of need please contact grifo®.
**RESET CONTACT**

P1 reset contact of the **GPC® 183** board allows the user to reset the board and restarting it in a general clearing condition. The main purpose of this contact is to come out of infinite loop conditions, useful especially during debug or to grant a particular initial stat. Please see figure 9 for an easy localization of this contact.

**A/D CONVERTER**

This peripheral can acquire 11 channels with a maximum resolution of 12 bits. By software it is possible to decide which channels to employ, to start and to stop the acquisition, etc., through a synchronous communication to the device. By means to simplify the management of this device some software packages provide utility procedures that are capable to manage all its parts. The connectable analog signals are variable voltage signals in the range 0÷2.490Vdc (default) or current signals in the range 0÷20 mA (option .8420). This device is optional and must be explicitly requested in the order (code .AD).

**BOARD CONFIGURATION**

A four pins dip switch has been introduced expressly to make the board and in particualr the application program configurable. The possibility to read by software the status of the switches gives the user the ability to manage many different conditions by an unique program, without having to employ other input signals (typical applications are: language choice, program parameters definition, operational mode selection, etc.). **GPC® 183** is also provided with two software managed signalation LEDs to visualize the overall status of the system.

**CONTROL LOGIC**

A specific control logic is responsible of mapping the registers of the on-board devices and the memory devices. The logic allocates these devices in the CPU addressing space, for further informations please refer to the paragraph "I/O MAPPING".
TECHNICAL FEATURES

GENERAL FEATURES

Devices:
24 input/output TTL (PPI)
4 input TTL
two 16 bit timers (PRT)
1 RS 232 serial line (ASCI 1)
1 RS 232, RS 422, RS 485 or current loop serial line (ASCI 0)
11 signals A/D converter
1 local reset key
2 LEDs software manageable
1 watchdog hardware astable
1 real time clock
1 buzzer
1 dip switch featuring 4 dips
1 ABACO® I/O BUS interface
1 power supply section (optional)

Memory:
IC 5: EPROM from 128K x 8 to 512K x 8
FLASH EPROM from 128K x 8 to 512K x 8
IC 4: SRAM from 128K x 8 to 512K x 8
IC 10: serial EEPROM from 256 Bytes up to 8K Bytes

CPU:
ZILOG Z8S180

Crystal (clock) frequency:
22.1184 (22.1184) MHz

A/D resolution:
12 bit

A/D conversion time:
10 µsec

PHYSICAL FEATURES

Size (W x H x D):
100 x 149 x 25 mm (without container)
110 x 160 x 60 mm (with DIN rails container)

Weight:
170 g (without container)
280 g (with DIN rails container)

Connectors:
CN1: 26 pins low profile vertical M
CN2: 2 pins quick release screw terminal M
CN3: 20 pins low profile vertical M
CN4: 2 pins low profile vertical M
CN5: 20 pins low profile vertical M
CN6: 20 pins low profile vertical M
CN7A: 6 pins plug
CN7B: pins plug
Watch dog intervent time: 1.50 sec

Temperature range: from 0 to 50 Centigrad degrees

Relative humidity: 20% up to 90% (without condense)

**ELECTRIC FEATURES**

**Power Supply:**
- +5 Vdc (without supply section)
- 6÷12 Vac (9÷16 Vdc) * (linear supply section)
- 8÷24 Vac (12÷34 Vdc) (switching supply section)

**Consumption on +5 Vdc:**
- 240 mA (default configuration)
- 180 mA (default configuration in low consumption)
- 280 mA (complete configuration)

**Current provided on +5 Vdc for external loads:**
- 720 mA * (without supply section)
- 720 mA * (switching supply section)

**On board back up battery:**
- 3.0 Vdc; 180 mAh

**External back up battery:**
- 3.6÷5 Vdc

**Back up current:**
- 2 μA (on board battery)

**A/D converter input voltage:**
- 0÷2.490 Vdc

**A/D converter input current:**
- 0÷20; 4÷20 mA (with conversion module)

**A/D converter input impedance:**
- 1 KΩ

**RS 422, RS 485 line termination:**
- Line termination resistance= 120 Ω
- Positive pull up resistance= 3.3 KΩ
- Negative pull up resistance= 3.3 KΩ

* Data here reported are referred to a 20 centigrad degreeses environmental temperature (for further informations please refer to the paragraph “SUPPLY VOLTAGES”).
INSTALLATION

In this chapter there are the information for a right installation and correct use of the card. The user can find the location and functions of each connectors, jumpers and some explanatory diagrams.

CONNECTIONS

The GPC®183 module has 7 connectors that can be linkeded to other devices or directly to the field, according to system requirements. In this paragraph there are connectors pin out, a short signals description (including the signals direction), connectors location (please refer to figure 24) and some electrical diagrams that shows the on board circuit of each connector.

CN 2 - POWER SUPPLY CONNECTOR WITH SUPPLY SECTION

CN2 is a 2 pins screw terminal connector. The board supply voltage must be provided through this connector. When using the board without any power supply section, the +5 Vdc must be provided through pin 26 (+Vdc) and pin 25 (GND) of CN1.

![Figure 3: CN2 - Power supply connector for on board supply section](image)

Signals description:

\[
\begin{align*}
8\pm24 \text{ Vac} \ (12\pm34 \text{ Vdc}) & = \text{I- Supply input 8\pm24 \text{ Vac} (12\pm34 \text{ Vdc}) (switching section)} \\
6\pm12 \text{ Vac} \ (9\pm16 \text{ Vdc}) & = \text{or 6\pm12 \text{ Vac} (9\pm16 \text{ Vdc}) (linear section)}
\end{align*}
\]
CN3 - PPI 82C55 PORT A AND C I/O CONNECTOR

CN3 is a 20 pins, male, vertical, low profile connector, 2.54 mm pitch. Through CN3 two parallel 8 bits ports out of three (ports A and C) of programmable peripheral PPI 82C55 are connected to the external world. All this connector’s signals are at TTL level and follow the I/O ABACO® standard.

Signals description:

- **PA.n** = I/O - PPI 82C55 port A n-th digital signal
- **PC.n** = I/O - PPI 82C55 port C n-th digital signal
- **GND** = - Ground signal
- **+5 Vdc** = O - +5 Vdc signal
- **N.C.** = - Not connected

Remarkable is the possibility to connect directly through CN3 a set of interfaces designed to solve several typical problems of industrial automation. We especially would want to remark the simplicity of installation and software management of QTP 24P, KDL x24, KDF 224, etc., that are also supported by high level programming languages. For further informations please refer to the paragraph “OPERATOR INTERFACES”.

Figure 5: CN3 - PPI 82C55 port A and C I/O connector

![Diagram of CN3 - PPI 82C55 port A and C I/O connector]
CN4 - BACK UP EXTERNAL BATTERY CONNECTOR

CN4 is a 2 pins, vertical, male connector with 2.54mm pitch. Through CN4 the user can connect an external battery for SRAM and RTC back up when the power supply is switched off (for further information please refer to chapter "BACK UP").

Signals description:

+Vbat = I - Positive pin of external back up battery
GND = - Negative pin of external back up battery
CN5 - PPI 82C55 PORT B, TTL INPUTS AND SYNC SERIAL LINE CONNECTOR

CN5 is a 20 pins, male, vertical, low profile connector, 2.54 mm pitch. Through CN5 one parallel 8 bits port out of three (port B) of programmable peripheral PPI 82C55, four digital inputs and the synchronous serial line are connected to external world. All this connector's signals are at TTL level and follow the I/O ABACO® standard.

**Figure 8: CN5 - PPI 82C55 port B, TTL inputs and synchronous serial line connector**

Signals description:

- **PB.n**: I/O - PPI 82C55 port B n-th digital signal
- **INn**: I - digital input n-th signal
- **TXS**: O - Synchronous serial line transmission signal
- **RXS**: I - Synchronous serial line reception signal
- **CKS**: I/O - Synchronous serial line clock signal
- **GND**: - Ground signal
- **+5 Vdc**: O - +5 Vdc signal
- **N.C.**: - Not connected
Figure 9: PPI 82C55 port B, TTL inputs and sync serial line on CN5 block diagram
CN6 - A/D CONVERTER INPUT CONNECTOR

CN6 is a 20 pins, male, vertical, low profile connector, 2.54 mm pitch. Through CN6 the 11 A/D converter section input signals interface to the external world. This connector accepts voltage analog signals (0÷2.490 Vdc) or current analog signals (0÷20 mA) and follow the A/D ABACO® standard. Signals are placed in order to reduce interference and electrical noise warranting a good signal transmission and in order to simplify connection with other systems.

FIGURE 10: CN6 - A/D CONVERTER INPUT CONNECTOR

Signals description:

<table>
<thead>
<tr>
<th>ADCn</th>
<th>I</th>
<th>A/D converter n-th channel analog input</th>
</tr>
</thead>
<tbody>
<tr>
<td>GND</td>
<td></td>
<td>Digital ground signal</td>
</tr>
<tr>
<td>AGND</td>
<td></td>
<td>Analog ground signal</td>
</tr>
<tr>
<td>+5 Vdc</td>
<td>O</td>
<td>+5 Vdc signal</td>
</tr>
</tbody>
</table>
**Figure 11: A/D Converter Input Block Diagram**

The diagram illustrates the connection of a VRef. signal to the IC28 TLC 2543, which is an A/D converter. The labels CH0 to CH10 indicate the input channels, and the resistors R34 to R41 are connected to each channel. The circuit diagram shows the block diagram of the A/D converter with specific connections and components labeled accordingly.
CN1 - ABACO® I/O BUS CONNECTOR

CN1 is a 26 pins, male, vertical, low profile connector with 2.54mm pitch. Through CN1 the card can be connected to some of the numerous grifo® boards, both intelligent and not. All this connector signals are at TTL level.

Signals description:

A0-A7 = O - Address BUS.
D0-D7 = I/O - Data BUS.
/INT BUS = I - Interrupt request (open collector type).
/NMI BUS = I - Non maskable interrupt.
/IORQ = O - Input output request.
/RD = O - Read cycle status.
/WR = O - Write cycle status.
/RESET = O - Reset.
/CS1, /CS2 = O - Chip select 1 and 2: external devices decoded enable
PFI = I - Power Failure input
+5 Vdc = I - +5 Vdc power supply.
GND = - Ground signal.
Figure 13: Components map (components and solder side)
CN7B - SERIAL LINE B CONNECTOR

CN7B is a 6 pins, female PLUG connector. On CN7B are available the buffered signals for RS 232, RS 422, RS 485, current loop serial line B that is physically connected to the hardware ASCI 0 of the microprocessor. The electric protocol follows the CCITT normative and all the signals are placed in order to reduce interference and electrical noise and in order to simplify connection with other systems.

Signals description:

**Rx**

- **Rs 232** = I - Serial line B RS 232 Receive Data.
- **Rs 422** = I - Receive Data Negative: Serial line B negative signal for RS 422 serial differential receive.
- **Rs 485** = I/O - Receive Transmit Data Negative: Serial line B negative signal for RS 485 serial differential receive and transmit.
- **C.L.** = I - Receive Data Negative: Serial line B negative signal for Current Loop serial bipolar receive.

**Tx**

- **Rs 232** = O - Serial line B RS 232 Transmit Data.
- **Rs 422** = O - Transmit Data Negative: Serial line B negative signal for RS 422 serial differential transmit.
- **Rs 485** = O - Transmit Data Positive: Serial line B positive signal for RS 485 serial differential receive and transmit.
- **C.L.** = O - Transmit Data Positive: Serial line B positive signal for Current Loop serial bipolar transmit.

**Figure 14: CN7B - Serial Line B Connector**

- RxB RS 232 / TxRx+B+ RS 485 / Rx+B+ RS 422 / Rx+B+ C.L. / Rx-RxB RS 422 / Rx-RxB- C.L. / TxRB- RS 422 / TxR-B- C.L. / CTSB RS 232
- TxR-B RS 232 / TxB+ RS 422 / TxB- C.L. / RTSB RS 232
+5 Vdc = O - +5 Vdc or ground signal.
GND = - Ground signal.

Figure 15: Serial communication diagram
**Figure 16: RS 232 Point to Point Connection Example**

**Figure 17: RS 422 Point to Point Connection Example**

**Figure 18: RS 485 Point to Point Connection Example**
Please remark that in a RS 485 network two forcing resistors must be connected across the net and two termination resistors (120 Ω) must be placed at its extrems, respectevely near the Master unit and the Slave unit at the greatest distance from the Master.

Forcing and terminating circuitry is installed on **GPC® 183** board. It can be enabled or disabled through specific jumers, as explained later.

For further informations please refr to TEXAS INSTRUMENTS Data-Book, "RS 422 and RS 485 Interface Ciciuits", the introduction about RS 422-485.
**Figure 20:** 4 wires current loop point to point connection example

**Figure 21:** 2 wires current loop point to point connection example
Possible passive current loop connections are two: 2 wires and 4 wires. These connections are shown in figures 16-18 where it is possible to see the voltage for VCL and the resistances for current limitation (R). The supply voltage varies in compliance with the number of connected devices and voltage drop on the connection cable.

The choice of the values for these components must be done considering that:

- circulation of a 20 mA current must be guaranteed;
- potential drop on each transmitter is about 2.35 V with a 20 mA current;
- potential drop on each receiver is about 2.52 V with a 20 mA current;
- in case of shortcircuit each transmitter must dissipate at most 125 mW;
- in case of shortcircuit each receiver must dissipate at most 90 mW.

For further info please refer to HEWLETT-PACKARD Data Book, (HCPL 4100 and 4200 devices).
CN7A - SERIAL LINE A CONNECTOR

CN7A is a 6 pins, female PLUG connector for serial communication. Physically, serial line A of GPC® 183 board is connected to the ASCI 1 serial line of the CPU. Placing of the signal has been designed to reduce interference and electrical noise and to simplify connections with other systems, while the electric protocol follows the CCITT normative.

![Diagram of CN7A](image)

**Figure 23: CN7A - Serial line A Connector**

Signals description:

- **RxA RS 232** = I - Serial line A=ASCII RS 232 Receive Data.
- **TxA RS 232** = O - Serial line A=ASCII RS 232 Transmit Data.
- **CTSA RS 232** = I - Serial line A=ASCII RS 232 Clear To Send.
- **RTSA RS 232** = O - Serial line A=ASCII RS 232 Request To Send.
- **+5 Vdc / GND**
- **GND**
  - +5 Vdc power supply or ground signal
  - Ground signal
Figure 24: LEDs, Dip Switch, Connectors, etc. Location
DIGITAL I/O INTERFACES

Through CN3 (ABACO® I/O BUS standard connector) the GPC® 183 card can be connected to all the numerous grifo® boards featuring the same standard pin out. Installation of these modules is very easy; in fact only a 20 pins flat cable (code FLT20+20) that carries also power supply is required, while the software management of these interfaces is as easy and immediate; in fact most of the software packages available for GPC® 183 card are provided with the necessary procedures. These latter are software driver for almost all the languages, and allow to use operator interfaces through the whole power of high level instructions.

Remarkable interfaces are:

- **QTP 16P, QTP 24P, KDL x24, KDF 224, DEB 01**, etc. that solve all the local operator interfacing problems. These modules are provided with all the resources needed to obtain a high level human machine interface (they feature alphanumeric displays, matrix keyboard and visualization LEDs) at a short distance from GPC® 183 card. The available software drivers allow to manage the operator interface resources directly through the high level instructions for console management.

- **IAC 01, DEB 01**: it is an interface for CENTRONICS parallel printer that can be connected with a standard printer cable. About software the developed drivers provide procedures to read and write data at a specified address, for the selected programming language.

- **MCI 64**: it a large mass memory support that can directly manage the PCMCIA memory cards RAM, FLASH, ROM, etc.) in their available sizes. About software the developed drivers provide a complete file system interfacing allowing to access the informations stored in the memory card directly through the high level file management instructions.

- **RBO xx, TBO xx, XBI xx, OBI xx**: these are buffer interfaces for I/O TTL signals. With these modules the TTL input signals are converted in NPN or PNP optoisolated inputs and the TTL output signals are converted in relays or transistor optoisolated outputs. Some of the above mentioned interfaces can be connected directly to CN7.

For more information refer to "EXTERNAL CARDS" chapter and the software tools documentation.

I/O CONNECTION

To prevent possible connecting problems between GPC® 183 and the external systems, the user has to read carefully the information of the previous paragraphs and he must follow these instructions:

- For RS 232, RS 422, RS 485 and current loop communication signals the user must follow the standard rules of these protocols.
- For all TTL signals the user must follow the rules of this electric standard. The connected digital signal must be always referred to card digital ground (GND). For TTL signals, the 0 Vdc level corresponds to logic state "0", while 5Vdc level corresponds to logic state "1".
- The analog inputs (A/D section) must be connected to low impedance signals in the following ranges: 0±2,490 V or 0±20 mA according to selected voltage reference (Vref). Remember that the eleven analog inputs available on CN6 are provided of filter capacitors that ensure an higher stability of the acquired signals, but reduce at the same time the bandwith frequency. For further information please refer to the paragraph “TYPE OF ANALOG INPUT SELECTION”.
RESET KEY

P1 reset key of the GPC® 183 board allows the user to reset the board and restarting it in a general clearing condition. After pressing and releasing P1 the board restarts its execution in EPROM or internal FLASH.

The main purpose of this key is to come out of infinite loop conditions, useful especially during debug and develop phases, or to ensure a particular initial status. Please see figure 24 for an easy localization of this contact.

TYPE OF ANALOG INPUT SELECTION

GPC® 183 board can accept analog voltage and/or current inputs, as described in the previous paragraphs and chapters. The input type selection can be made only for 8 out of 11 input analog channels during the order phase and is performed mounting a specific voltage-current conversion module made by precision resistors (code .8420). In detail:

| R41     | -> | channel 0 |
| R40     | -> | channel 1 |
| R39     | -> | channel 2 |
| R38     | -> | channel 3 |
| R37     | -> | channel 4 |
| R36     | -> | channel 5 |
| R35     | -> | channel 6 |
| R34     | -> | channel 7 |

Should the voltage-current conversion module not to be mounted (default case) the corresponding channel accepts a voltage input signal in the range 0÷2.49 Vdc; otherwise a current input signal is accepted.

The value of the above mentioned resistors is obtained by the following spread:

\[ R = \frac{2.49 \text{ V}}{\text{Imax}} \]

Usually the voltage-current conversion modules are made using 124 Ω precision resistors, corresponding to 4÷20 mA or 0÷20 mA.

To easily locate the voltage-current conversion module please refer to figures 11 and 24.

TEST POINT

The board is provided with a test point called TP1, that allows to read, through a galvanically isolated multimeter, the A/D converter reference voltage which is calibrated in laboratory.

TP1 is made of two contacts:

| pin 1 | -> | Vref |
| pin 2 | -> | GND  |

To easily locate the test point contacts please refer to figure 24, while for further informations about Vref signal please refer to the paragraph “TRIMMER AND CALIBRATION”.

GPC® 183 Rel. 5.10
TRIMMERS AND CALIBRATION

On GPC® 183 is available a trimmer, named RV1, that calibrates the Vref voltage of the optional A/D converter (code .AD) section. The GPC® 183 is subjected to a careful test that verifies and calibrates all the card sections. To easily locate the trimmer, please refer to figure 24. The calibration is executed in laboratory, with a controlled +20°C room temperature, following these steps:

- The A/D voltage reference (Vref) is calibrated through RV1 trimmer, by using a 5 digits precision multimeter, to a value of +2,4900 Vdc, measured on test point TP1.

- The correspondence between the analog input signal and the combination read from A/D is verified. This check is performed with a reference signal connected to A/D inputs and testing that the A/D combination and the theorical combination differ at maximum of the A/D section errors sum.

- The trimmer is blocked with paint.

The analog interfaces use high precision components that are selected during mounting phase to avoid complicate and long calibration procedures. After the calibration, the on board trimmer is blocked with paint to maintain calibration also in presence of mechanic stresses (vibrations, movings, delivery, etc.).

The user must not modify the card calibration, but if thermic drifts, time drifts and so on, make necessary a new calibration, the user must strictly follow the previous described procedure.

VISUAL SIGNALATIONS

GPC® 183 board is provided with six LEDs in order to signal to the User some internal status conditions, as described in the following table:

<table>
<thead>
<tr>
<th>LEDs</th>
<th>COLOUR</th>
<th>PURPOSE</th>
</tr>
</thead>
<tbody>
<tr>
<td>LD1</td>
<td>Green</td>
<td>Software managed activity LED.</td>
</tr>
<tr>
<td>LD2</td>
<td>Red</td>
<td>When lit, indicates the RTC generated interrupt line activation (/INT2 of CPU).</td>
</tr>
<tr>
<td>LD3</td>
<td>Red</td>
<td>When lit, indicates the presence of +5 Vdc power supply.</td>
</tr>
<tr>
<td>LD4</td>
<td>Red</td>
<td>When lit, indicates the CPU /HALT signal activation.</td>
</tr>
<tr>
<td>LD5</td>
<td>Red</td>
<td>When lit, indicates the activation of external watch dog circuitry.</td>
</tr>
<tr>
<td>LD6</td>
<td>Green</td>
<td>Software managed timed activity LED (spot).</td>
</tr>
</tbody>
</table>

The main purpose of this LEDs is to provide the User a visual indication of the board status, making easier the operations to verify the correct working of the system. To easily locate the LEDs on the board please see figure 24.
JUMPERS

On GPC® 183 there are 11 jumpers for card configuration. Connecting these jumpers, the user can define for example the memory type and size, the peripheral devices functionality and so on. Below there is the jumpers list, location and function.

<table>
<thead>
<tr>
<th>JUMPER</th>
<th>N. PINS</th>
<th>PURPOSE</th>
</tr>
</thead>
<tbody>
<tr>
<td>J1</td>
<td>2</td>
<td>Connects pins 26 of CN1 to on board +5 Vdc power supply.</td>
</tr>
<tr>
<td>J2</td>
<td>3</td>
<td>Selects size of memory device on IC4.</td>
</tr>
<tr>
<td>J3</td>
<td>3</td>
<td>Selects kind of memory device on IC5.</td>
</tr>
<tr>
<td>J4</td>
<td>3</td>
<td>Selects kind of memory device on IC5.</td>
</tr>
<tr>
<td>J5</td>
<td>2</td>
<td>Connects on board battery BT1 to back up circuitry.</td>
</tr>
<tr>
<td>J6</td>
<td>2</td>
<td>Connects external watch dog circuitry.</td>
</tr>
<tr>
<td>J7</td>
<td>5</td>
<td>Selects communication type for serial line B between RS 422 and RS 485.</td>
</tr>
<tr>
<td>J8</td>
<td>2</td>
<td>Connects forcing and termination resistors to RS 422, RS 485 reception line.</td>
</tr>
<tr>
<td>J9</td>
<td>2</td>
<td>Connects forcing and termination resistors to RS 422, RS 485 reception line.</td>
</tr>
<tr>
<td>J10</td>
<td>3</td>
<td>Selects the kind of connection for pin 1 of CN7B.</td>
</tr>
<tr>
<td>J11</td>
<td>3</td>
<td>Selects the kind of connection for pin 1 of CN7A.</td>
</tr>
</tbody>
</table>

**FIGURE 26: JUMPERS SUMMARIZING TABLE**

The following tables describe all the right connections of GPC® 183 jumpers with their relative functions. To recognize these valid connections, please refer to the board printed diagram (serigraph) or to figure 13 of this manual, where the pins numeration is listed; for recognizing jumpers location, please refer to figure 30. The "*" used in the following tables, denotes the default connection, or on the other hand the connection set up at the end of testing phase, that is the configuration the user receives.

5 PINS JUMPERS

<table>
<thead>
<tr>
<th>JUMPERS</th>
<th>CONNECTION</th>
<th>PURPOSE</th>
<th>DEF.</th>
</tr>
</thead>
<tbody>
<tr>
<td>J7</td>
<td>position 1-2 and 3-4</td>
<td>Enables RS 485 serial communication (2 wires half duplex) on line B.</td>
<td></td>
</tr>
<tr>
<td>J7</td>
<td>position 2-3 and 4-5</td>
<td>Enables RS 422 serial communication (4 wires full or half duplex) on line B.</td>
<td>*</td>
</tr>
</tbody>
</table>

**FIGURE 27: 5 PINS JUMPERS LOCATION**
### 2 PINS JUMPERS

<table>
<thead>
<tr>
<th>JUMPERS</th>
<th>CONNECTION</th>
<th>PURPOSE</th>
<th>DEF.</th>
</tr>
</thead>
<tbody>
<tr>
<td>J1</td>
<td>not connected</td>
<td>Does not connect pin 26 of CN1 to on board +5 Vdc power supply.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>connected</td>
<td>Connects pin 26 of CN1 to on board +5 Vdc power supply.</td>
<td>*</td>
</tr>
<tr>
<td>J5</td>
<td>not connected</td>
<td>Does not connect on board battery BT1 to backup circuitry.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>connected</td>
<td>Connects on board battery BT1 to backup circuitry.</td>
<td>*</td>
</tr>
<tr>
<td>J6</td>
<td>not connected</td>
<td>Does not connect external watch dog circuitry to reset circuitry.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>connected</td>
<td>Connects external watch dog circuitry to reset circuitry.</td>
<td>*</td>
</tr>
<tr>
<td>J8, J9</td>
<td>not connected</td>
<td>Do not connect forcing and terminating circuitry to RS 422, RS 485 serial line B.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>connected</td>
<td>Connect forcing and terminating circuitry to RS 422, RS 485 serial line B.</td>
<td>*</td>
</tr>
</tbody>
</table>

**Figure 28: 2 pins jumpers table**

### 3 PINS JUMPERS

<table>
<thead>
<tr>
<th>JUMPERS</th>
<th>CONNECTION</th>
<th>PURPOSE</th>
<th>DEF.</th>
</tr>
</thead>
<tbody>
<tr>
<td>J2</td>
<td>position 1-2</td>
<td>Sets IC4 for 128K Byte SRAM.</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>position 2-3</td>
<td>Sets IC4 for 512K Byte SRAM.</td>
<td></td>
</tr>
<tr>
<td>J3</td>
<td>position 1-2</td>
<td>Matching with J4, sets IC5 for EPROM.</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>position 2-3</td>
<td>Matching with J4, sets IC5 for FLASH EPROM.</td>
<td></td>
</tr>
<tr>
<td>J4</td>
<td>position 1-2</td>
<td>Matching with J3, sets IC5 for EPROM.</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>position 2-3</td>
<td>Matching with J3, sets IC5 for FLASH EPROM.</td>
<td></td>
</tr>
<tr>
<td>J10</td>
<td>position 1-2</td>
<td>Connects pin 1 of CN6B to GND.</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>position 2-3</td>
<td>Connects pin 1 of CN6B to +5 Vdc.</td>
<td></td>
</tr>
<tr>
<td>J11</td>
<td>position 1-2</td>
<td>Connects pin 1 of CN6A to GND.</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>position 2-3</td>
<td>Connects pin 1 of CN6A to +5 Vdc.</td>
<td></td>
</tr>
</tbody>
</table>

**Figure 29: 3 pins jumpers table**
FIGURE 30: JUMPERS LOCATION
BACK UP

GPC® 183 has an on board lithium battery BT1 for the back up of SRAM and RTC content when power supply is switched off. Jumper J5 connects physically the battery so it can be disconnected to save its duration whenever back-up is not needed. By CN4 connector it is possible to connect an external battery: configuration of jumper J5 does not affect the working of this battery and it can replace BT1 completely. Please refer to the paragraph “ELECTRIC FEATURES” to choose the type of the external back up battery, to easily locate see figure 24.

MEMORY SELECTION

On GPC® 183 can be mounted up to 1032K bytes of memory divided in several configurations, as described in the following table:

<table>
<thead>
<tr>
<th>IC</th>
<th>DEVICE</th>
<th>SIZE</th>
<th>CONNECTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>EPROM</td>
<td>128K Byte</td>
<td>J3 and J4 in position 1-2</td>
</tr>
<tr>
<td></td>
<td>EPROM</td>
<td>256K Byte</td>
<td>J3 and J4 in position 1-2</td>
</tr>
<tr>
<td></td>
<td>EPROM</td>
<td>512K Byte</td>
<td>J3 and J4 in position 1-2</td>
</tr>
<tr>
<td></td>
<td>FLASH EPROM</td>
<td>128K Byte</td>
<td>J3 and J4 in position 2-3</td>
</tr>
<tr>
<td></td>
<td>FLASH EPROM</td>
<td>512K Byte</td>
<td>J3 and J4 in position 2-3</td>
</tr>
<tr>
<td>4</td>
<td>SRAM</td>
<td>128K Byte</td>
<td>J2 in position 1-2</td>
</tr>
<tr>
<td></td>
<td>SRAM</td>
<td>512K Byte</td>
<td>J2 in position 2-3</td>
</tr>
<tr>
<td>10</td>
<td>EEPROM</td>
<td>256÷8K Byte</td>
<td>-</td>
</tr>
</tbody>
</table>

**Figure 31: Memory selection table**

All the above mentioned devices must follow the JEDEC pin out specifications. For further information about the signatures of the component that can be mounted please refer to the manufacturers documentations. To easily locate the memory devices please refer to figure 24.

The default configuration of the GPC® 183 board memory is only 128K SRAM; any different memory configuration can be realized by the user by mounting the opportune devices or can be requested in the ordering phase. Here follow the codes to order the optional memory configurations:

- **.512** -> 512K SRAM
- **.EE08** -> 8K bit (1024 byte) serial EEPROM
- **.EE16** -> 16K bit (2048 byte) serial EEPROM
- **.EE64** -> 64K bit (8192 byte) serial EEPROM

For further information about prices and options please contact grifo®.
INTERRUPTS

One of the most important GPC® 183 features is the powerful interrupts management. Here is a short description of how the board's hardware interrupt signals can be managed; a more complete description of the hardware interrupts can be found in the microprocessor data sheets or in Appendix A of this manual.

- **ABACO® I/O BUS** -> It generates an /NMI interrupt, by the /NMI BUS signal on CN1.
  It generates an /INT1 vectored interrupt, by /INT BUS signal on CN1.
- **Real Time Clock** -> It generates an /INT2 vectored interrupt.
- **CPU inside devices** -> They generate a vectored interrupt. Possible sources of internal interrupt events are: PRT 0, PRT 1, DMA 0, DMA 1, CSI/O, ASCI 0, ASCI 1.

The board features a chained priority structure that manages the case of contemporary interrupts. The addresses of the response procedures for vectored interrupts can be software programmed by the user acing on microprocessor inside registers. So the user program has always the possibility to react promptly to every external event, deciding also the priority of interrupts.

CONFIGURATION INPUTS

GPC® 183 board is provided with one 4 pins dip switch (DSW1), tipically used for system configuration purposes, that can be software acquired by the user program. The mostly implemented applications for this feature are: working conditions setting, selection of some on-board firmware parameters, etc. The status of switches generates a signal in complemented logic (0 -> switch ON, 1 -> switch OFF) that can be read performing a read operation at the address assigned to the dip switch by the on board control logic. Some software tools use switch 4 for the selection between the RUN and DEBUG working modalities. For further information please refer to the paragraph “I/O ADDRESSES”, while to easily locate the jumper on the board please refer to figure 24.

RESET AND WATCH DOG

The watch dog circuit of GPC® 183 is really efficient and provided of easy software management. In details the most important features of this circuit are:
- astable functionality;
- intervent time of about 1.5 sec;
- hardware enable;
- software retrigger;

With the astable mode when the intervent time elapses, the circuit becomes active, it stay active till the end of reset time then it is deactivated. Jumper J6 connects the watch dog circuit to reset circuit so when it is connected the watch dog is enabled and viceversa. The watch dog retrigger operation is described in chapter "WATCH DOG".

After an activation and following deactivation of /RESET signal, the card resumes execution of the program saved on IC5 (at address 0000H) starting from a global reset status of all the on board peripheral devices.

Please remember that the /RESET signal is connected to CN1 connector and that on GPC® 183 are available other reset sources as the contact P1.
POWER SUPPLY VOLTAGES

GPC® 183 board is provided with an efficient circuitry that solves in an efficient and comfortable way the problem of power supply in any employ condition. Here follows the list of the possible configurations for power supply section:

- **No power supply section (default):**
  The board must be supplied by a +5 Vdc voltage provided directly on the specific pins of CN1 ( +5 Vdc on pin 26, GND on pin 25 ).

- **Linear power supply section (option .ALIM12):**
  The board must be supplied by a 6÷12 Vac alternate voltage, or the corresponding continuous voltage, that must be provided to pins 1 and 2 of CN2.

- **Switching power supply section (option .SW):**
  The board must be supplied by a 8÷24 Vac alternate voltage, or the corresponding continuous voltage (12÷34 Vdc), that must be provided to pin 1 and 2 of CN2.

Regardless the type of supply section chosen, the GPC® 183 board is always provided with an efficient protection circuitry that protects the board against voltage peaks or noise. Please remark that the desired supply section must be explicitly specified in the order; in fact the choice implies a different hardware configuration that must be performed by the grifo® technical personnel.

Jumper J1 connects positive pin (+5 Vdc) of on board supply to ABACO® I/O BUS connector so it must be disconnected only when a board provided with power supply section is connected to a system provided with its own power supply section.

To reduce the CPU consumption IDLE and STOP operating MODEs can be used. These modalities can be selected by programming specific CPU registers and activated executing the HALT instruction, while to restore the normal execution mode interrupt signals must be employed. For further information about this subject please refer to appendix A of this manual or CPU manufacturers documentation.

For further information please refer to paragraph “ELECTRIC FEATURES”.
SERIAL COMMUNICATION SELECTION

The communication serial line A is always buffered in RS 232 while the serial line B can be buffered in RS 232, RS 422, RS 485 or current loop electric standard. By hardware can be selected which one of these electric standard is used, through jumpers connection (as described in the previous tables). By software the serial lines can be programmed to operate with 7, 8 bits per character, parity, 1 or 2 stop bits at standard or no standard baud rates, through some CPU internal register setting.

Some components necessary for RS 422 and RS 485 communication are not mounted and not tested on the default configuration card, so the first not standard configuration must always be executed by grifo® technician; then the user can change himself/herself the configuration, following the below description:

- SERIAL LINE B=ASCI 0 CONFIGURED IN RS 232 (default configuration)
  
  IC27 = MAX 202 driver  
  IC25 = no component  
  IC26 = no component  
  IC29 = no component  
  IC30 = no component

- SERIAL LINE B=ASCI 0 CONFIGURED IN CURRENT LOOP (.CLOOP option)
  
  IC27 = no component  
  IC25 = no component  
  IC26 = HCPL 4100 driver  
  IC29 = no component  
  IC30 = HCPL 4200 driver

The current loop serial line is a passive line, so during connection the user must provide an external power supply, as described in figures 20, 21 and 22. The current loop interface allows either point to point or network connection with 4 or 2 wires.

- SERIAL LINE B=ASCI 0 CONFIGURED IN RS 422 (.RS422 option)
  
  IC27 = no component  
  IC25 = SN 75176 or MAX483  
  IC26 = no component  
  IC29 = SN 75176 or MAX483  
  IC30 = no component

With /RTSB=/RTS0 signal (managed by software with ASCI 0 registers) the user enables or disables the transmitter driver:

/RTS0 = low level = 0 logic state -> transmitter driver enabled
/RTS0 = high level = 1 logic state -> transmitter driver disabled

allowing either point to point (driver can be maintained always enabled) or network (driver is enabled only when the unit can hold the line) connection.
- SERIAL LINE B=ASCI 0 CONFIGURED IN RS 485 (.RS485 option)
  IC27 = no component
  J7 = 1-2, 3-4
  IC25 = SN 75176 or MAX483
  J8, J9 = (*1)
  IC26 = no component
  IC29 = no component
  IC30 = no component

With /RTSB=/RTS0 signal (managed by software with ASCI 0 registers) the user defines the RS 485 line direction:

/RTS0 = low level = 0 logic state -> RS 485 line transmitting
/RTS0 = high level = 1 logic state -> RS 485 line receiving

allowing network connection in a master multi slave system and multi master system. With RS 485 communication line, on CN7B the pins 4 and 5 have the double function of reception and transmission signals. All the transmitted characters are at the same time received when the user selects RS 485 on GPC® 183; in this way the line conflicts can be immediately recognized by simply testing the received character after each transmission.

(*1) With jumper J8 and J9 the RS 422 receiving line or the RS 485 line can be terminated and forced with a suitable resistors circuit. The line termination must be added only at the beginning and at the end of the physical line, connecting both the jumpers. Normally these jumper must be connected in point to point network, or on the farther cards in multipoints network.

After reset or power on phase, the /RTS0 signal is forced to high level that maintain the RS 485 driver receiving and that disables the RS 422 transmitter driver; this condition eliminates any conflict on the communication line.
Serial B = ASCII 0 in RS 232
Serial B = ASCII 0 in current loop

Serial B = ASCII 0 in RS 422
Serial B = ASCII 0 in RS 485

Figure 32: Serial communication driver location
SOFTWARE

A wide selection of software development tools can be obtained, allowing use of the module as a system for its own development, both in assembler and in other high level languages; in this way the User can easily develop all the requested application programs in a very short time. Generally all software packages available for the mounted microprocessor, or for the Z80 and Z180 family, can be used, i.e.:

GET 80
It is a complete program with Editor, Communication driver, and Mass Memory management for all Z80 family cards. This program, developed by grifo®, allows to operate in the best conditions when GDOS, FGDOS or xGDOS MCI software tools are used; GET 80 is supplied when one of these tools is ordered and it is personalized with name and general data of the customer. A useful list of pull down menus and the possibility of using mouse, make program use very comfortable. GET 80 program can be executed both on MS-DOS system and on MACINTOSH computers too, through SOFT-PC program. It is supplied on MS-DOS 3”1/2 floppy disk with the documentation on GDOS 80 manual.

GDOS 183
It is a complete development Tool for GPC® card. It is supplied together with GET 80 program to allow an easy and immediate use of this powerful development system. GDOS is divided in two different structures: the first one works on PC maintaining serial communication with the second one. The second structure is on EPROM, it works on board of the card and it is an efficient operating system that executes many low level functions and, at the same time, it allows high level language use. The combination of the said structures results in a complete machine, in fact the card uses PC resources (like floppy disk, hard disk, printer, keyboard, monitor, etc.) as its own peripheral devices. This resulting “virtual machine” performs operation in a transparent way for the User, so this latter can operate with the same modality of standard PC languages. It is really interesting the compatibility of GDOS with all CP/M program and languages; so, if the User has experience, knowledge or developed applications with CP/M, he can use immediately GDOS, without any changes. Moreover, GDOS can manage all memory devices exceeding 64K Bytes as RAM disk and ROM disk. The on board RAM devices can directly be used performing data read and write operations with the confortable file formats. This software tools is supplied on EPROM with MS-DOS GET 80 floppy disk, some examples, utilities and the operating system documentation.

FGDOS 183
It is really similar to GDOS, but it can program and erase the on board FLASH EPROM with the application program developed from the User. In this way the external EPROM programmer is not necessary to store definitely the program and it is possible to modify or to add code directly on the installed machine, through a portable PC. This software tools is supplied on FLASH EPROM with MS-DOS GET 80 floppy disk, some examples, utilities and the operating system documentation.
xGDOS MCI 183
It is a version of GDOS or FGDOS software tools, capable of PCMCIA Memory Card management. Using MCI 64 card, the GDOS operating system manages memory cards as RAM disk or ROM disk. All applications with data acquisition and data logging can be realized with high level languages that manage data on files, with a fast development time and without any software complication. This software tool is supplied on EPROM or FLASH EPROM with MS-DOS GET 80 floppy disk, some examples, utilities and the operating system documentation.

PASCAL 80
It is an efficient and complete PASCAL Compiler for Z80 family cards, with features similar to Release 3.0 of Borland Turbo PASCAL. It must work together with any GDOS version and it can exceed the 64K memory limits of Z80 family microprocessors through OVERLAY modality. More than one application program can be saved in RAM and/or ROM disks and subsequently executed. The terminal emulation of GET 80 program support the typical full screen PASCAL Editor, including the attributes management. This program is supplied as ROM DISK file in GDOS EPROM or FLASH EPROM and on MS-DOS floppy disk with some example and manual.

HI TECH C 80
Professional C Cross Compiler of Hi-Tech Software Inc. This Compiler is terribly fast and it generates a small quantity of code. This result is due to advanced techniques in optimizing the generated code based on Artificial Intelligence techniques which allow to get a very compact and very fast code. The package includes: IDE, Compiler, Code optimizer, Assembler, Linker, Remote Debugger and so on. This tool is Full ANSI/ISO Standard and Full Library Source Code. Once the porting of the Remote-Debugger module is done, this tool allows the user the software debugging directly on the hardware that he is experimenting. This type of specilization of the Remote Debugger is available from now ant it is supplied with all grifo® CPU cards. This software package is on 3” 1/2 diskettes under MS-DOS format along with user manual. This version supports these following CPUs: Z80, Z180, 84C011, 84C11, 84C013, 80C13, 84C015, 84C15, 64180, NCS800, Z181, Z182.

DDS MICRO C: low cost ross compiler for C source program. It is a powerful software tool that includes editor, C compiler (integer), assembler, optimizer, linker, library, and remote debugger, in one easy to use integrated development environment. There are also included the library sources and many utilities programs.

NOICE: It is a PC hosted debugger consists of a target specific DOS program, NOICExxx.EXE, and a target resident monitor program. The two programs comunicate via RS 232. NOICE includes: source level debug; a disassembler; a file viewer; memory display and editing; a virtually unlimited number of breakpoints; hardware free single step; definition of symbols; the ability to record and play back files of commands; on line help.
RSD 183
This software tool is a **Remote Symbolic Debugger** with two operating modes. The first one is a monitor debugger modality with software emulation on a PC; the second is a remote monitor debugger modality that executes code directly on the card. Through serial communication, the user can: download an HEX file and associated symbol table, debug code in symbolic mode, execute code in step-by-step mode or in real-time mode, set breakpoints, dump and modify memory and registers, etc. RSD software tool supports both **Z80** and **Z180** instruction sets. Really interesting is the program execution management, in fact many hardware and software breakpoints are supported. **RSD** can be used together with assembler tools, like **ZASM 80**, and C Compiler **CC 80**. It is supplied on EPROM and on MS-DOS floppy disk with technical manual.

ZASM 80
It is a macro cross assembler that operates on any PC with MS-DOS operating system. It supports both **Z80** and **Z180** instruction sets. The generated code can be debugged on PC, through software simulation, or directly on target card, through remote modality, using **RSD** software tools. ZASM 80 is compatible with C Compiler **CC 80** of which it assembles the compilation result. It is supplied on MS-DOS floppy disk with technical manual.

CC 80
It is a complete C Compiler with ANSI/ISO standard, provided of floating point procedure, that can generate code for **Z80** and **Z180** family microprocessors. It works together with cross assembler **ZASM 80** and Symbolic Debugger **RSD**. It is supplied on MS-DOS floppy disk with technical manual.

CBZ 80
Complete BASIC compiler, for CPU family Z80 and compatible, capable to generate a very compact and very fast code. It works only matched to any GDOS version. CBZ 80 allows to override the 64 KByte of addressing barriers typical of family Z80. This can be done using the CHAIN technique provided by GDOS matched to the possibility to manage RAM disk and ROM disk provided by several **ABACO** cards. Using it with the powerful editor included in GET80 allows to experiment a powerful work tool to create any application program in an extremely efficient and comfortable way. The program is provided in EPROM with GDOS operating system and in a floppy disk which included also the manual and a set of example programs.
INTRODUCTION

In this chapter are reported all informations about card use, related to hardware features of GPC® 183. For example the registers addresses, the memory and peripheral devices allocation are described below.

ON BOARD DEVICES ADDRESSES

The on board devices addresses are managed from a control logic, realized with CMOS gates. This control logic allocates memory and peripheral devices with very low power consumption and simple software management.

The control logic has been designed to control the memory and the I/O peripherals addresses in a separate manner. The Z8S180 microprocessor directly addresses in total 64K bytes of memory and 256 I/O registers and the control logic provides 1032K Byte on board memory and peripheral devices allocation inside these addresses spaces. The maps management is completely driven by software through the MMU circuit programmation: the used memory can be selected and divided in some size definible segments. About I/O maps the control logic avoids every conflicts problems between CPU internal and external peripherals.

Summarizing the control logic allocates:

- **ABACO® I/O BUS**
  - Up to 512K Byte of EPROM or FLASH EPROM on IC 5
  - Up to 512K Byte of SRAM on IC 4
  - Up to 8K Byte of serial EEPROM on IC 10
  - A/D converter
  - Configuration dip switch DSW1
  - Buzzer
  - Activity LEDs
  - Watch dog circuitery

The addresses of all these devices are described in the following paragraphs and can't be set with different values. If some different specific maps are required, please contact directly grifo®.
**I/O ADDRESSES**

The on board control logic manages the allocation of all the peripheral devices registers in the microprocessor I/O space, that is 256 bytes long. Next table shows names, addresses, meanings and directions of peripheral device registers (including the internal microprocessor ones). For a detailed description of the registers function, please refer to next chapter "PERIPHERAL DEVICES SOFTWARE DESCRIPTION".

<table>
<thead>
<tr>
<th>DEVICES</th>
<th>REG.</th>
<th>ADDRESS</th>
<th>R/W</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>ASCI</td>
<td>ASCI</td>
<td>00H:09H</td>
<td>R/W</td>
<td>Internal microprocessor registers, for asynchronous serial line</td>
</tr>
<tr>
<td>CSI/O</td>
<td>CSIO</td>
<td>0AH:0BH</td>
<td>R/W</td>
<td>Internal microprocessor registers, for Clocked Serial I/O Port management</td>
</tr>
<tr>
<td>TIMER</td>
<td>TMR</td>
<td>0CH:1FH</td>
<td>R/W</td>
<td>Internal microprocessor registers, for Timer/Counter management</td>
</tr>
<tr>
<td>DMA</td>
<td>DMA</td>
<td>20H:32H</td>
<td>R/W</td>
<td>Internal microprocessor registers, for DMA lines management</td>
</tr>
<tr>
<td>INTERRUPT</td>
<td>INT</td>
<td>33H:35H</td>
<td>R/W</td>
<td>Internal microprocessor registers, for interrupts management</td>
</tr>
<tr>
<td>REFRESH</td>
<td>RCR</td>
<td>36H:37H</td>
<td>R/W</td>
<td>Internal microprocessor registers, for Refresh circuit management</td>
</tr>
<tr>
<td>MMU</td>
<td>MMU</td>
<td>38H:3AH</td>
<td>R/W</td>
<td>Internal microprocessor registers, for Memory Management Unit management</td>
</tr>
<tr>
<td>I/O</td>
<td>ICR</td>
<td>3BH:3FH</td>
<td>R/W</td>
<td>Internal microprocessor registers, for I/O control management</td>
</tr>
<tr>
<td>ACT. LED</td>
<td>LD1</td>
<td>40H</td>
<td>R/W</td>
<td>Activity LED LD1 management register.</td>
</tr>
<tr>
<td>BUZZER</td>
<td>BUZ</td>
<td>40H</td>
<td>R/W</td>
<td>Buzzer management register.</td>
</tr>
<tr>
<td>DSW1</td>
<td>DSW1</td>
<td>40H</td>
<td>R</td>
<td>DSW1, LD1, buzzer acquisition register.</td>
</tr>
<tr>
<td>EEPROM</td>
<td>EE</td>
<td>40H</td>
<td>R/W</td>
<td>EEPROM on IC10 management registers.</td>
</tr>
<tr>
<td>RTS1 / CTS1</td>
<td>HAND</td>
<td>40H</td>
<td>R/W</td>
<td>Serial line A handshake management register (/RTS1, /CTS1).</td>
</tr>
<tr>
<td>W. DOG</td>
<td>RWD</td>
<td>44H</td>
<td>W</td>
<td>External watch dog retrigger register.</td>
</tr>
<tr>
<td>LED SPOT</td>
<td>LD6</td>
<td>44H</td>
<td>R</td>
<td>Spot LED LD6 management register.</td>
</tr>
<tr>
<td>INPUT</td>
<td>INP</td>
<td>44H</td>
<td>R</td>
<td>Four input lines acquisition register.</td>
</tr>
</tbody>
</table>

**Figure 33: I/O addressing table - Part I**
<table>
<thead>
<tr>
<th>DISP.</th>
<th>REG.</th>
<th>IND.</th>
<th>R/W</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>RUN / DEBUG</td>
<td>RUNDEB</td>
<td>44H</td>
<td>R</td>
<td>RUN / DEBUG configuration acquisition register.</td>
</tr>
<tr>
<td>PPI 82C55</td>
<td>PDA</td>
<td>48H</td>
<td>R/W</td>
<td>Port A data register.</td>
</tr>
<tr>
<td></td>
<td>PDB</td>
<td>49H</td>
<td>R/W</td>
<td>Port B data register.</td>
</tr>
<tr>
<td></td>
<td>PDC</td>
<td>4AH</td>
<td>R/W</td>
<td>Port C data register.</td>
</tr>
<tr>
<td></td>
<td>CNT</td>
<td>4BH</td>
<td>R/W</td>
<td>Control and command register.</td>
</tr>
<tr>
<td>ABACO® I/O BUS</td>
<td>/CS1</td>
<td>50H-57H</td>
<td>R/W</td>
<td>ABACO® I/O BUS addresses that enable /CS1.</td>
</tr>
<tr>
<td></td>
<td>/CS2</td>
<td>58H-5FH</td>
<td>R/W</td>
<td>ABACO® I/O BUS addresses that enable /CS2.</td>
</tr>
<tr>
<td></td>
<td>I/O BUS</td>
<td>50H-5FH</td>
<td>R/W</td>
<td></td>
</tr>
<tr>
<td>Real Time Clock</td>
<td>SEC1</td>
<td>F0H</td>
<td>R/W</td>
<td>Data register for seconds units.</td>
</tr>
<tr>
<td></td>
<td>SEC10</td>
<td>F1H</td>
<td>R/W</td>
<td>Data register for seconds decines.</td>
</tr>
<tr>
<td></td>
<td>MIN1</td>
<td>F2H</td>
<td>R/W</td>
<td>Data register for minutes units.</td>
</tr>
<tr>
<td></td>
<td>MIN10</td>
<td>F3H</td>
<td>R/W</td>
<td>Data register for minutes decines.</td>
</tr>
<tr>
<td></td>
<td>HOU1</td>
<td>F4H</td>
<td>R/W</td>
<td>Data register for hours units.</td>
</tr>
<tr>
<td></td>
<td>HOU10</td>
<td>F5H</td>
<td>R/W</td>
<td>Data register for hours decines and AM/PM.</td>
</tr>
<tr>
<td></td>
<td>DAY1</td>
<td>F6H</td>
<td>R/W</td>
<td>Data register for day units.</td>
</tr>
<tr>
<td></td>
<td>DAY10</td>
<td>F7H</td>
<td>R/W</td>
<td>Data register for day decines.</td>
</tr>
<tr>
<td></td>
<td>MON1</td>
<td>F8H</td>
<td>R/W</td>
<td>Data register for month units.</td>
</tr>
<tr>
<td></td>
<td>MON10</td>
<td>F9H</td>
<td>R/W</td>
<td>Data register for month decines.</td>
</tr>
<tr>
<td></td>
<td>YEA1</td>
<td>FAH</td>
<td>R/W</td>
<td>Data register for year units.</td>
</tr>
<tr>
<td></td>
<td>YEA10</td>
<td>FBH</td>
<td>R/W</td>
<td>Data register for year decines.</td>
</tr>
<tr>
<td></td>
<td>WEE</td>
<td>FCH</td>
<td>R/W</td>
<td>Data register for week day.</td>
</tr>
<tr>
<td></td>
<td>REGD</td>
<td>FDH</td>
<td>R/W</td>
<td>Control register D.</td>
</tr>
<tr>
<td></td>
<td>REGE</td>
<td>FEH</td>
<td>R/W</td>
<td>Control register E.</td>
</tr>
<tr>
<td></td>
<td>REGF</td>
<td>FFH</td>
<td>R/W</td>
<td>Control register F.</td>
</tr>
</tbody>
</table>

**FIGURE 34: I/O ADDRESSING TABLE - PART II**
ABACO® I/O BUS ADDRESSES

The GPC® 183 control logic defines ABACO® I/O BUS addresses and only these addresses must be used to manage correctly the BUS. As described in following "I/O ADDRESSES" table, only the addresses from 50H to EFH are available for ABACO® I/O BUS. Any I/O operations at each one of these addresses enables the /IORQ signal and the other control signals of CN1 connector. In the addresses subranges 50H÷57H and 58÷5FH the signales /CS1 and /CS2 respectively are enabled. They are used for external peripheral devices coded selection.

MEMORY ADDRESSES

The maximum 1032K bytes of memory, are allocated on the board as below described:

- Up to 512K bytes of EPROM or FLASH EPROM allocated in memory space.
- Up to 512K bytes of SRAM allocated in memory space.
- Up to 8K bytes of serial EEPROM allocated in I/O space.

GPC® 183 can directly manage no more than 64K bytes of memory that is the microprocessor logic addressable space. On the board this logic space can be divided in three separated segments: each ones of these segment have software programmable dimension and start address. The CPU internal MMU circuit divides the logical space directly managed by the microprocessor into these 3 segments and it allocates them in the physical memory devices space. The MMU circuit is software programmable with I/O operations to three specific registers in a fast and comfortable manner. So MMU allows software managements of a physical memory space very larger than microprocessor memory space.

The following figure describes available memory configurations; for further informations on MMU use and segments meaning (Common Area 0, Common Area 1 and Bank Area), please refer to appendix B, while for memory devices location and configuration refer to figures 24 and 31.

After power on or reset phase, the MMU circuit allocates all the logical 64K space at the beginning of the physical space, therefore the card starts execution of code saved at address 0000H of EPROM or FLASH EPROM on IC5.

The memory size and type configurations must be selected both according to used software tools and user requests and/or application features. The card configuration for the selected memory device types and sizes on IC4 and IC5 sockets, is performed with some comfortable jumpers, as described in "MEMORY SELECTION" chapter.

Some software tools, i.e. GDOS, self manage the MMU circuit to use all the available memories at high level witout User intervention.
Figure 35: Memory Allocation
PERIPHERAL DEVICES SOFTWARE DESCRIPTION

In the previous paragraphs are described the external registers addresses, while in this one there is a specific description of registers meaning and function (please refer to I/O addresses table, for the registers names and addresses values). For a more detailed description of the devices, please refer to manufacturing company documentation; for microprocessor internal peripheral devices, not described in this paragraph, refer to appendix A. In the following paragraphs the D7÷D0 indication denotes the eight bits of the combination used in I/O operations.

BUZZER

Buzzer is activated by performing a "write operation" with bit D1=1 at the address of register BUZ; vice versa buzzer is disabled by performing the same operation with bit D1=0. Also, it is possible to read the status of buzzer by performing a read operation from the address of register BUZ and examining bit D1. The remaining 7 bits of register LD4BZ must be defined according to previous setting for avoiding status modifications on other devices, in this case acticity LED LD1, A/D converter, serial EEPROM and handshakes.

BUZ register is reset (all bits to 0) after Reset or power on, maintaining disabled the buzzer circuit.

ACTIVITY LED

Activity LED LD1 is enabled by performing a "write operation" with bit D0=1 at the address of register LD1; vice versa LED is disabled by performing the same operation with bit D0=0. Also, it is possible to read the status of LED by performing a read operation from the address of register LED1 and examining bit D0. The remaining 7 bits of register LD1 must be defined according to previous setting for avoiding status modifications on other devices, in this case buzzer, A/D converter, serial EEPROM and handshakes.

LD1 register is reset (all bits to 0) after Reset or power on, maintaining disabled the activity LED.

EXTERNAL WATCH DOG

Retrigger operation of GPC® 183 external watch dog circuit is performed with a simple write operation at the address of register RWD. This register shares the same address of other on board peripherals, but no conflict are generated in fact retrigger operation is an output operation and the output data has no effect. To avoid external watch dog activation is necessary to retrigger its circuit at regular time periods and the duration of these periods must be smaller than intervention time. If retrigger doesn't happen as before described and J6 is connected, when intervention time is elapsed, the card is reset. Watch dog activation is visualized by LED LD5.
SPOT LED

Spot LED LD6 is enabled by performing a "read operation" from the address of register SPOT. This operation enables the LED for an interval of about 50 msec then the LED turns off automatically. The value READ FROM the SPOT register is meaningless.

The main purpose of this LED is to indicate the working condition of application program without introducing programming difficulties or to signal efficiently the presence of an event that requires a prompt reaction.

DIP SWITCH DSW1 AND RUN/DEBUG

The on board DSW1 dip switch status can be obtained by software, through a simple "read operation" at the DSW1 register address.

The correspondence between register bits and dip switch is as follows:

<table>
<thead>
<tr>
<th>Register Bit</th>
<th>Dip Switch</th>
</tr>
</thead>
<tbody>
<tr>
<td>D6</td>
<td>DSW1.3</td>
</tr>
<tr>
<td>D5</td>
<td>DSW1.2</td>
</tr>
<tr>
<td>D4</td>
<td>DSW1.1</td>
</tr>
</tbody>
</table>

As shown above, only 3 bits in the combination read are affected by dip switches status.

Switch DSW1.4 is the RUN or DEBUG selector, modality specific of some grifo® software packages. Its status can be acquired performing a read operation from the address corresponding to register RUNDEB and examining bit D7. Please remark that, by default, logic level 0 corresponds to RUN mode while logic level 1 corresponds to DEBUG mode.

Reading DSW1 register by software, the user obtains a negated bits combination, in fact "ON" position corresponds to logic level 0 and "OFF" position corresponds to logic level 1.

SERIAL EEPROM

For software management of serial EEPROM module of IC10, please refer to specific manufacturer documentation. This manual reports no software information because management of this component is complex and requires a deep knowledge, anyway the user can use the demo programs supplied with the card. Please remark that first 32 bytes (0÷31) are reserved so they should not be changed. The board control logic allows to realize a serial communication with FC bus standard protocol, through the bits of the specific register EE. The only necessary information is the electric connection:

<table>
<thead>
<tr>
<th>Data Line (SDA)</th>
<th>D2 (input)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock Line (SCL)</td>
<td>D4 (output)</td>
</tr>
</tbody>
</table>

The remaining bits of register EE must be defined according to previous setting for avoiding status modifications on other devices, in this case buzzer, A/D converter, activity LED and handshakes. Please remark that A0, A1 and A2 of this component's slave address are bound to logic 0. Logic 0 means a connection to 0 Vdc and logic 1 means a connection to 5 Vdc.
A/D CONVERTER

For software management of optional A/D converter on IC28, please refer to specific manufacturer documentation. This manual reports no software information because management of this component is complex and requires a deep knowledge, anyway the user can use the demo programs supplied with the card. The board control logic allows to realize a serial communication through the bits of the specific register ADC. The only necessary information is the electric connection:

- D3 (input) -> linea DATA OUT
- D5 (output) -> linea /CS
- D6 (output) -> linea DATA IN
- D7 (output) -> linea I/O CLOCK

The remaining 7 bits of register LD1 must be defined according to previous setting for avoiding status modifications on other devices, in this case buzzer, activity LED, serial EEPROM and handshakes. Logic 0 means a connection to 0 Vdc and logic 1 means a connection to 5 Vdc.

DIGITAL INPUTS

Connector CN5 features 4 digital input TTL signals (please refer to paragraph “CONNECTORS”) that can be acquired by software performing a read operation from the allocation address of register INP. Correspondance between register bits and input signals is:

- D0 -> IN0
- D1 -> IN1
- D2 -> IN2
- D3 -> IN3

As shown above, only the least significant nibble (four bits) repost the four inputs status. Logic 0 means a connection to 0 Vdc and logic 1 means a connection to 5 Vdc.

HANDSHAKE OF SERIAL LINE A

Serial line ASCI 1 of microprocessor is not provided with hardware handshake signals so they are generated by an on board circuitry that can be software managed through the bits of the specific register HAND. Correspondance between register bits and input signals is:

- D7 (input) -> /CTSA
- D2 (output) -> /RTSA

Logic 0 means active logic status of corresponding RS 232 signal and logic 1 means deactive logic status of corresponding RS 232 signal. This circuitry makes GPC® 183 the ideal component for communication management, in fact it is provided with two complete asynchronous serial lines and one synchronous serial line.
PPI 82C55

This external peripheral device is managed through 4 registers: one status register (CNT) and three data registers (PDA, PDB, PDC). The data registers are available both for read operation (to obtain signal status) and for write operation (to set signal status) with the correspondence described in figure 23. The PPI 82C55 can work in three different modes:

MODE 0 = it provides two 8 bits bidirectional ports (A, B) and two 4 bits bidirectional ports (C LOW, C HIGH); output signals are latched and input signals are not latched; no handshake signals are provided.

MODE 1 = it provides two 12 bits ports (A+C LOW and B+C HIGH) where ports A and B are used as 8 I/O lines and port C are used as 4 handshake lines. Both inputs and outputs are latched.

MODE 2 = it provides a 13 bits port (A+C3÷7) where port A is used as 8 I/O lines and the 5 bits of port C are used as handshake, and a 11 bits port (B+C0÷2) where port B is used as 8 I/O lines and the 3 bits of port C are used as handshakes. Both inputs and outputs are latched.

The device is programmed writing an 8 bits word in the status register CNT, with the following bit meaning:

\[ \text{CNT} = SF \ M1 \ M2 \ A \ \text{CH} \ M3 \ B \ \text{CL} \]

where

- \( SF \) = mode Set Flag: if actived (1) the device is enabled for standard I/O operation
- \( M1 \ M2 \) = mode selection:
  - 0 0 = mode 0
  - 0 1 = mode 1
  - 1 X = mode 2
- \( A \) = port A direction: 1=input; 0=output
- \( \text{CH} \) = port C HIGH direction: 1=input; 0=output
- \( M3 \) = mode selection: 1=mode 1; 0=mode 0
- \( B \) = port B direction: 1=input; 0=output
- \( \text{CL} \) = port C LOW direction: 1=input; 0=output

After Reset or power on PPI 82C55 is programmed in mode 0 with all three ports in input; in this way any connection of PPI 82C55 signals can be used without conflict problems.

CPU INTERNAL PERIPHERALS

The descriptions of the registers that manages the CPU internal peripheral devices (ASCI, CSI/O, TIMER, DMA, INTERRUPT, REFRESH, MMU, I/O) is available in the appendix A. Whenever this information are still insufficient, please refer to specific documentation of the manufacturing company.
REAL TIME CLOCK

This peripheral is allocated in 16 consecutive I/O addresses, 3 of which correspond to status registers while the remaining 13 are for data. Data registers are used both for read operations (of the current time and date) and write operations (to initialize the time and date) just like the status registers which are used in write operations (to program the operative mode) and in read operations (to acquire the RTC status). Here follows a list of the RTC data registers’ meanings:

SEC1 - Units of seconds - 4 least significant bits of SEC1.3÷SEC1.0
SEC10 - Decines of secondi - 3 least significant bits of SEC10.2÷SEC10.0
MIN1 - Units of minutes - 4 least significant bits of MIN1.3÷MIN1.0
MIN10 - Decines of minutes - 3 least significant bits of MIN10.2÷MIN10.0
HOU1 - Units of hours - 4 least significant bits of HOU1.3÷HOU1.0

The third bit of HOU10.2 indicates AM/PM
DAY1 - Units of day number - 4 least significant bits of DAY1.3÷DAY1.0
DAY10 - Decines of day number - 2 least significant bits of DAY10.1÷DAY10.0
MON1 - Units of month - 4 least significant bits of MON1.3÷MON1.0
MON10 - Decines of month - 1 least significant bit of MON10.0
YEA1 - Units of year - 4 least significant bits of YEA1.3÷YEA1.0
YEA10 - Decines of year - 4 least significant bits of YEA10.3÷YEA10.0
WEE - Day of the week - 3 least significant bits of WEE.2÷WEE.0

For this last register the three least significant bits mean:

<table>
<thead>
<tr>
<th>WEE.2</th>
<th>WEE.1</th>
<th>WEE.0</th>
<th>Day of the week</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Sunday</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Monday</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Tuesday</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>Wednesday</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Thursday</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>Friday</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>Saturday</td>
</tr>
</tbody>
</table>

The meaning of the three control registers is:

REG D = NU NU NU NU 30S IF B H

where:

NU = Not used.
30S = If high (1) it allows a 30 seconds correction of the time. Once set the RTC seconds are reset and the minutes increased, if the previous seconds was equal or greater than 30.
IF = It manages the RTC interrupt status. When read it shows the current interrupt status (1 active and vice versa), when reset to 0 it disables the RTC interrupt signal if the interrupt mode is selected.
B = Indicates whether R/W operations can be performed on the registers:
   1 -> operations are not permitted and vice versa.
H = If high (1) it stores the written time and date.
### REG E = NU NU NU NU T1 T0 I M

**bit** 7 6 5 4 3 2 1 0

**where:**
- **NU** = Not used.
- **T1** T0 = Determine the duration of the internal counters interrupt cycle.
- 0 0 -> 1/64 second
- 0 1 -> 1 second
- 1 0 -> 1 minute
- 1 1 -> 1 hour
- **I** = It defines the interrupt operating mode:
  - 1 -> it selects interrupt mode: when the selected duration elapses the interrupt is enabled and then disabled only with a reset of bit IF of control register D;
  - 0 -> it selects the standard mode: when the selected duration elapses the interrupt is enabled and then disabled only after 7.8 msec.
- **M** = It mask the interrupt status:
  - 1 -> interrupt masked: the RTC interrupt signal is always disabled;
  - 0 -> interrupt not masked: the RTC interrupt signal reflects interrupt status.

### REG F = NU NU NU NU T 24/12 S R

**bit** 7 6 5 4 3 2 1 0

**where:**
- **NU** = Not used.
- **T** = It determines from which internal counter to take the counting signal:
  - 1 -> main counter (fast counter for test);
  - 0 -> 15th counter.
- **24/12** = It determines the hours counting mode:
  - 1 -> 0÷23;
  - 0 -> 1-12 with AM/PM.
- **S** = If high (1) it stops the clock time counting until the next enabling (0).
- **R** = If high (1) it resets all the internal counters.
EXTERNAL CARDS

GPC® 183 can be connected to a wide range of block modules and operator interface system produced by grifo®, or to many system of other companies. The on board resources can be expanded with a simple connection to the numerous peripheral grifo® boards, both intelligent and not, thanks to its standard ABACO® I/O BUS connector. Even single EURO cards with BUS ABACO® can be connected, by using the proper mother boards. Hereunder some of these cards are briefly described; ask the detailed information directly to grifo®, if required.

ADC 812
Analog to Digital Converter, 12 bits, multi range
DAS (Data Acquisition System) multi range 8 channels 12 bit A/D conversion lines; track and hold; 6µs conversion time; range ±10, ±5, +10, +5Vdc or 0÷20, 4÷20mA; analog inputs connections through quick terminal screw connectors; ABACO® I/O BUS interface; direct mounting for DIN 247277-1 and 3 rails; 4 type dimension.

DAC 212
Digital to Analog Converter 12 bits, multi range
Digital to Analog converter; multi range 2 channels 12 bits ±10, +10 Vdc output; analog outputs connections through quick terminal screw connectors; ABACO® I/O BUS interface; direct mounting for DIN 247277-1 and 3 rails; 4 type dimension.

CAN 14
Control Area Network, 1 channel, galvanically insulated
UART CAN SJA1000; 1 serial channels galvanically insulated; ABACO® I/O BUS interface; 4 type dimension; support of CAN 2.0B protocol; transfer rate up to 1M bit/sec; direct mounting for DIN 247277-1 and 3 rails.

KDL xxx - KDF xxx
Keyboard Display interface - LCD or Fluorescent
Interface with Fluorescent or LCD display, LEDs backlit, 20x2 or 20x4 characters; up to 24 keys matrix keyboard connector. It is directly driven by 16 TTL I/O lines; High level languages supported.

QTP 24 - QTP 24P
Quick Terminal Panel 24 keys with Parallel interface
Intelligent user panel equipped with Fluorescent or LCD display, LEDs backlit, 20x2 or 20x4 characters; RS 232, RS 422, RS 485 or current loop serial line; serial E2 for set up and message. Possibility of re-naming keys, LEDs and panel name by inserting label with new name into the proper slot; 24 Keys and 16 LEDs with blinking attribute and buzzer manageable by software; built in power supply; RTC option, reader of magnetic badge and relay. The QTP 24P is low cost no intelligent (passive) version. It is directly driven from 16 TTL I/O lines; high level languages supported.
QTP 16 - QTP 16P
Quick Terminal Panel 16 keys with Parallel interface
Intelligent user panel equipped with Fluorescent or LCD display, LEDs backlit, 20x2 or 20x4 characters; RS 232, RS 422, RS 485 or current loop serial line; serial E2 for set up and messages; buzzer manageable by software; 4 readable auxiliary opto in lines; power supply 5 Vdc. The QTP 16P is low cost no intelligent (passive) version. It is directly driven from 16 TTL I/O lines.

QTP G28
Quick Terminal Panel - LCD Graphic, 28 keys
LCD display 240x128 pixels, CFC backlit; Optocoupled RS 232 line and additional RS 232/422/485/Current Loop line; CAN line controller; E² for set up; RTC and RAM lithium backed; primary graphic object; possibility of re-naming keys, LEDs and panel name; 28 keys and 16 LEDs with blinking attribute and buzzer manageable by software; Buzzer; built in power supply; reader of magnetic badge and relay option.

OBI N8 - OBI P8
Opto BLOCK Input NPN-PNP
Interface between 8 NPN, PNP optocoupled and displayed input lines, with screw terminal and ABACO® standard I/O 20 pins connector; power supply section; connection for DIN Ω rails.

TBO 01 - TBO 08
Transistor BLOCK Output
Interface for ABACO® standard I/O 20 pins connector; 16 or 8 transistor output lines 45 Vdc 3 A open collector; screw terminal; optocoupled and displayed lines; connection for DIN 247277-1 and 3 rails.

XBI R4 - XBI T4
miXed BLOCK Input-Output
Interface for ABACO® standard I/O 20 pins connector; 4 Relays 3A with MOV or 4 optocoupled Transistors 3A open collectors; 4 input lines optocoupled; screw terminal; connection for DIN Ctype and Ω rails.

FBC xxx
Flat Block Contactxxx pins
This interconnection system "wire to board" allows the connection to many type of flat cable connectors to terminal for external connections. Connection for DIN Ω rails.

IBC 01
Interface Block Communication
Conversion card for serial communication, 2 RS 232 lines; 1 RS 422-485 line; 1 optical fibre line; selectable DTE/DCE interface; quick connection for DIN 46277-1 and 3 rails.

DEB 01
Didactis Experimental Board
Supporting card for 16 TTL I/O lines use. It includes: 16 keys, 16 LEDs, 4 digits, 16 keys matrix keyboard, Centronics printer interface, LCD display and fluorescent display interface, GPC® 68 I/O connector, field connection with screw terminal.
MCI 64
Memory Cards Interfaces 64 MBytes
Interfacing card for managing 68 pins PCMCIA memory cards, it is directly driven from any ABACO® I/O standard connector; High level languages GDOS supported.

ZBR xxx
Zipped BLOCK Relays xx Input + xx Output
Peripheral cards family, relays outputs, equipped with housing for Ω rails mounting. Double power supply built in; 5Vdc section for powering the on board logic and an external CPU cards; second section, galvanically coupled, for the optocoupled input lines. All I/O lines are displayed by LEDs. Relays contacts are 3A and are MOV protected. All I/O connections are availables on quick terminal connectors. 1 connector interface to ABACO® I/O BUS. The ZBR serie represent the ideal complement for cards 3 and 4 type. The ZBR cards can be directly driven, through the PC parallel port, by using the PCC A26 low cost interface card. ZBR 324 -> 32 opto in, 24 relays; ZBR 246 -> 24 opto in, 16 relays; ZBR 168 -> 16 opto in, 8 relays; ZBR 84 -> 8 opto in, 4 relays.

ZBT xxx
Zipped BLOCK Transistors xx Input + xx Output
Peripheral cards family having optocoupled outputs and 3A transistor in open collector. Cards are equipped with housing for Ω rails mounting. Double power supply built in; 5Vdc section for powering the on board logic and an external CPU cards; second section, galvanically coupled, for the optocoupled input lines. All I/O lines are displayed by LEDs. All output transistors are equipped with protection against inductive loads. All I/O connections are availables on quick terminal connectors. Connector interface to ABACO® I/O BUS. The ZBT serie represent the ideal complement for cards 3 and 4 type. The ZBT cards can be directly driven, through the PC parallel port, by using the PCC A26 low cost interface card. ZBT 324 -> 32 opto in, 24 transistors; ZBT 246 -> 24 opto in, 16 transistors; ZBT 168 -> 16 opto in, 8 transistors; ZBT 84 -> 8 opto in, 4 transistors.

ABB 03
ABACO® Block BUS 3 slots
3 slots ABACO® mother board; 4 TE pitch connectors; ABACO® I/O BUS connector; screw terminal for power supply; connection for DIN C type and Ω rails.

ABB 05
ABACO® Block BUS 5 slots
5 slots ABACO® mother board with power supply. Double power supply built in; 5Vdc 2.5A section for powering the on board logic; second section at 24Vdc 400mA galvanically coupled, for the optocoupled input lines. Auxiliary connector for ABACO® I/O BUS. Connection for DIN Ω rails.

IPC 52
Intelligent Peripheral Controller, 24 analogic input
This intelligent peripheral card acquires 24 independent analogical input lines: 8 PT 100 or PT 1000 sensors, 8 J,K,S,T thermocouples, 8 analog input ±2Vdc or 4÷20mA; 16 bits + sign A/D section; 0.1 °C resolution; 32K RAM for local data logging; buzzer; 16 TTL I/O lines; 5 or 8 conversion per second; facility of networking up to 127 IPC 52 cards using serial line, BUS interfacing or through RS 232, RS 422, RS 485 or current loop line. Only 5Vdc power supply.
Figure 36: GPC® 183 AVAILABLE CONNECTIONS DIAGRAM

**OPTIONS FOR POWER SUPPLY**
- +5 Vdc
- 12÷34 Vdc
- 8÷24 Vac (Switching)

**DIRECT CONNECTION TO QTP 24P**

**DIGITAL TTL INPUT/OUTPUT**
- to XBI-01, OBI-01, RBO-08 etc....

**CURRENT to VOLTAGE CONVERTER**
- 8 A-V modules

**CURRENT to VOLTAGE CONVERTER**
- +2,490 V
  - or CURRENT
  - 0÷20 mA, 4÷20 mA

**SOFTWARE or HARDWARE SERIAL LINE RS-232**

**CURRENT TO VOLTAGE**
- 12 Bit ANALOG INPUT
- VOLTAGE
- +2,490 V

**EXTERNAL LITHIUM BATTERY**
- 3.6 V to RAM Back up

**1 RS 232 OR RS 422, 485, CURRENT LOOP**

**ABACO® BUS**
- ABACO® I/O BUS
- ABACO® I/O BUS
- ZBx series
- Any I/O type
- CI/O R16-T16, etc.
- IPC52, UAR 24, etc.
- ABB 03 or ABB 05, etc.

**DIRECT CONNECTION TO QTP 24P**

**1 SOFTWARE or HARDWARE SERIAL LINE RS-232**

**PC like or Macintosh**

**PLC**
- PC like or Macintosh
- PLC

**QTP 24**
- QTP 24
- etc..............
In this chapter there is a complete list of technical books, where the user can find all the necessary documentations on the components mounted on GPC® 183.

Data book Manual TEXAS INSTRUMENTS: *The TTL Data Book - SN54/74 Families*
Data book Manual TEXAS INSTRUMENTS: *RS-422 and RS-485 Interface Circuits*
Manual TEXAS INSTRUMENTS: *Linear Circuits Data Book - Volume 1 and 3*

Data book NEC: *Memory Products*
Manual NEC: *Microprocessors and Peripherals - Volume 3*

Manual SGS-THOMSON: *Programmable logic manual - GAL products*

Data book HEWLETT PACKARD: *Optoelectronics Designer's Catalog*

Data book MAXIM: *New Releases Data Book - Volume 4*
Data book MAXIM: *Integrated Circuits Data Book*

Manual HEWLETT PACKARD: *Optoelectronics Designer’s Catalog*

Manual MAXIM: *New Releases Data Book - Volume 4*
Manual MAXIM: *New Releases Data Book - Volume 5*

Manual XICOR: *Data Book*

Data book SEIKO EPSON: *REAL TIME CLOCK MODULE RTC-72421 Application manual*

Manual NATIONAL SEMICONDUCTOR: *Linear Databook - Volume 1*
Data book ZILOG: *Z80S180/Z8L180 Enhanced Z180 Microprocessor*

Data book TOSHIBA: *Mos Memory Products*

For further information and upgrades please refer to specific internet web pages of the manufacturing companies.
**PRELIMINARY PRODUCT SPECIFICATION**

**Z80180/Z8S180/Z8L180 SL1919**

**ENHANCED Z180 MICROPROCESSOR**

**FEATURES**
- Code Compatible with Zilog Z80® CPU
- Extended Instructions
- Two Chain-Linked DMA Channels
- Low Power-Down Modes
- On-Chip Interrupt Controllers
- Three On-Chip Wait-State Generators
- On-Chip Oscillator/Generator
- Expanded MMU Addressing (up to 1 MB)
- Clocked Serial I/O Port
- Two 16-Bit Counter/Timers
- Two Enhanced UARTs (up to 512 kbps)
- Clock Speeds: 6, 8, 10, 20, 33 MHz
- Operating Range: 5V (3.3V@ 20 MHz)
- Operating Temperature Range: 0°C to +70°C
- -40°C to +85°C Extended Temperature Range
- Three Packaging Styles
  - 68-Pin PLCC
  - 64-Pin DIP
  - 80-Pin QFP

**GENERAL DESCRIPTION**

The enhanced Z80180/Z8S180/Z8L180™ significantly improves on the previous Z80180 models while still providing full backward compatibility with existing Zilog Z80 devices. The Z80180/Z8S180/Z8L180 now offers faster execution speeds, power saving modes, and EMI noise reduction.

This enhanced Z80 design also incorporates additional feature enhancements to the ASCIs, DMAs, and Icc STANDBY Mode power consumption. With the addition of "ESCC-like" Baud Rate Generators (BRGs), the two ASCIs now have the flexibility and capability to transfer data asynchronously at rates of up to 512 kbps. In addition, the ASCI receiver has added a 4-byte First-In First-Out (FIFO) which can be used to buffer incoming data to reduce the incidence of overrun errors. The DMAs have been modified to allow for a "chain-linking" of the two DMA channels when set to take their DMA requests from the same peripherals device. This feature allows for non-stop DMA operation between the two DMA channels, reducing the amount of CPU intervention (Figure 1).

Not only does the Z80180/Z8S180/Z8L180 consume less power during normal operations than the previous model, it has also been designed with three modes intended to further reduce the power consumption. Zilog reduced Icc power consumption during STANDBY Mode to a minimum of 10 µA by stopping the external oscillators and internal clock. The SLEEP mode reduces power by placing the CPU into a "stopped" state, thereby consuming less current while the on-chip I/O device is still operating. The SYSTEM STOP mode places both the CPU and the on-chip peripherals into a "stopped" mode, thereby reducing power consumption even further.

A new clock doubler feature has been implemented in the Z80180/Z8S180/Z8L180 device that allows the programmer to double the internal clock from that of the external clock. This provides a systems cost savings by allowing the use of lower cost, lower frequency crystals instead of the higher cost, and higher speed oscillators.

The Enhanced Z180 is housed in 80-pin QFP, 68-pin PLCC, and 64-pin DIP packages.
HALT and Low-Power Operating Modes. The Z80180/Z8S180/Z8L180 can operate in seven modes with respect to activity and power consumption:

- **Normal Operation**
- **HALT Mode**
- **IOSTOP Mode**
- **SYSTEM STOP Mode**
- **IDLE Mode**
- **STANDBY Mode (with or without QUICK RECOVERY)**

### Normal Operation
The Z80180/Z8S180/Z8L180 processor is fetching and running a program. All enabled functions and portions of the device are active, and the HALT pin is High.

### HALT Mode
This mode is entered by the HALT instruction. The Z80180/Z8S180/Z8L180 processor continually fetches the following opcode but does not execute it, and drives the HALT, ST and M1 pins all Low. The oscillator and PHI pin remain active, interrupts and bus granting to external masters, and DRAM refresh can occur and all on-chip I/O devices continue to operate including the DMA channels.

### IOSTOP Mode
IOSTOP mode is entered by setting the IOSTOP bit of the I/O Control Register (ICR) to 1. In this case, on-chip I/O (ASCI, CSI/O, PRT) stops operating. Recovery from IOSTOP mode is by resetting the IOSTOP bit to 0.

### SYSTEM STOP Mode
SYSTEM STOP mode is the combination of SLEEP and IOSTOP modes. SYSTEM STOP mode is entered by setting the IOSTOP bit in ICR to 1 followed by execution of the SLP instruction. In this mode, on-chip I/O and CPU stop operating, reducing power consumption, but the PHI output continues to operate. Recovery from SYSTEM STOP mode is the same as recovery from SLEEP mode except that internal I/O sources (disabled by IOSTOP) cannot generate a recovery interrupt.

### IDLE Mode
Software can put the Z80180/Z8S180/Z8L180 into this mode by setting the IOSTOP bit of the I/O Control Register (ICR) to 1. In this case, on-chip I/O (ASCI, CSI/O, PRT) stops operating. Recovery from IDLE mode is by setting the IOSTOP bit to 0.

### SLEEP Mode
SLEEP mode is by simply executing the following instruction(s).

This provides a technique for synchronization with high-speed external events without incurring the latency imposed by an interrupt response sequence. Figure 14 shows the timing for exiting SLEEP mode due to an interrupt request. Note that the Z80180/Z8S180/Z8L180 takes about 1.5 clocks to restart.

---

**Figure 13. HALT Timing**

**Figure 14. SLEEP Timing**

---

If an interrupt source is individually disabled, it cannot bring the Z80180/Z8S180/Z8L180 out of SLEEP mode. If an interrupt source is individually enabled, and the IEF bit is 0 so that interrupts are globally disabled (by a DI instruction), the Z80180/Z8S180/Z8L180 leaves SLEEP mode by simply executing the following instruction(s).

---

If an interrupt source is individually disabled, it cannot bring the Z80180/Z8S180/Z8L180 out of SLEEP mode. If an interrupt source is individually enabled, and the IEF bit is 0 so that interrupts are globally disabled (by a DI instruction), the Z80180/Z8S180/Z8L180 leaves SLEEP mode by simply executing the following instruction(s).

This provides a technique for synchronization with high-speed external events without incurring the latency imposed by an interrupt response sequence. Figure 14 shows the timing for exiting SLEEP mode due to an interrupt request. Note that the Z80180/Z8S180/Z8L180 takes about 1.5 clocks to restart.
Figure 15 shows the timing for exiting IDLE mode due to an interrupt request. Note that the Z80180/Z8S180/Z8L180 takes about 9.5 clocks to restart.

While the Z80180/Z8S180/Z8L180 is in IDLE mode, it will grant the bus to an external master if the BREXT bit (CCR5) is 1. Figure 16 shows the timing for this sequence. Note that the part takes 8 clock-cycles longer to respond to the Bus Request than in normal operation.

After the external master negates the Bus Request, the Z80180/Z8S180/Z8L180 disables the PHI clock and remains in IDLE mode.

STANDBY Mode (With or Without QUICK RECOVERY).
Software can put the Z80180/Z8S180/Z8L180 into this mode by setting the IOSTOP bit (ICR5) to 1 and CCR6 to 1, and executing the SLP instruction. This mode stops the on-chip oscillator and thus draws the least power of any mode, less than 10µA.

As with IDLE mode, the Z80180/Z8S180/Z8L180 will leave STANDBY mode in response to a Low on RESET or on NMI, or a Low on INT0 that is enabled by a 1 in the corresponding bit in the INT/TRAP Control Register, and will grant the bus to an external master if the BREXT bit in the CPU Control Register (CCR5) is 1. But the time required for all of these operations is greatly increased by the need to restart the on-chip oscillator and ensure that it has stabilized to square-wave operation.

When an external clock is connected to the EXTAL pin rather than a crystal to the XTAL and EXTAL pins, and the external clock runs continuously, there is little need to use STANDBY mode because there is no time required to restart the oscillator, and other modes restart faster. However, if external logic stops the clock during STANDBY mode (for example, by decoding HALT Low and M1 High for several clock cycles), then STANDBY mode can be useful to allow the external clock source to stabilize after it is re-enabled.

When external logic drives RESET Low to being a Z80180/Z8S180/Z8L180 out of STANDBY mode, and a crystal is used or an external clock source has been stopped, the external logic must hold RESET Low until the on-chip oscillator or external clock source has restarted and stabilized.

The clock stability requirements of the Z80180/Z8S180/Z8L180 are much less in the divide-by-two mode that's selected by a Reset sequence and thereafter controlled by the Clock Divide bit in the CPU Control Register (CCR7). Because of this, software should:

a. Program CCR7 to 0 to select divide-by-two mode, before the SLP instruction that enters STANDBY mode, and.

b. After a Reset, interrupt, or in-line restart after the SLP 01 instruction, delay programming CCR7 back to 1 to set divide-by-one mode, as long as possible to allow additional clock stabilization time.

If software sets CCR6 to 1 before the SLP instruction places the MPU in STANDBY mode, the value in the CCR3 bit determines how long the Z80180/Z8S180/Z8L180 will wait for oscillator reset and stabilization when it leaves STANDBY mode due to an external interrupt request. If CCR3 is 0, the Z80180/Z8S180/Z8L180 waits 217 (131,072) clock cycles, while if CCR3 is 1, it waits only 64 clock cycles. The latter is called QUICK RECOVERY mode. The same delay applies to granting the bus to an external master.
As described previously for SLEEP and IDLE modes, when a Z80180/Z8S180/Z8L180 leaves STANDBY mode due to the NMI flag Low, or when it leaves STANDBY mode due to an enabled INTO interrupt before the end of the clock stabilization delay, the Z80180/Z8S180/Z8L180 takes either 64 or 217 (131,072) clock cycles to restart, depending on the CCR3 bit. When D6 and D3 are both 1, setting IOSTOP (ICR5) and executing a SLP instruction puts the part into QUICK RECOVERY STANDBY mode, in which the on-chip oscillator is stopped, and the part allows only 64 clock cycles for the oscillator to stabilize when it’s restarted. The latter section, HALT and Low Power Modes, describes the subject more fully.

Figure 17. Z80180/Z8S180/Z8L180 STANDBY Mode Exit due to External Interrupt

While the Z80180/Z8S180/Z8L180 is in STANDBY mode, it will grant the bus to an external master if the BREXT bit (CCR5) is 1. Figure 18 shows the timing of this sequence. Note that the part takes 64 or 217 (131,072) clock cycles to grant the bus depending on the CCR3 bit. The latter (non-Quick-Recovery) case may be prohibitive for many “demand driven” external masters. If so, QUICK RECOVERY or IDLE mode can be used.

Figure 18. Z80180/Z8S180/Z8L180 STANDBY Mode Exit due to External Interrupt

While the Z80180/Z8S180/Z8L180 external master during STANDBY mode, when the BREXT bit in the CPU Control Register (CCR5) is 1.

As described previously for SLEEP and IDLE modes, when a Z80180/Z8S180/Z8L180 leaves STANDBY mode due to the NMI flag Low, or when it leaves STANDBY mode due to an enabled INTO interrupt before the end of the clock stabilization delay, the Z80180/Z8S180/Z8L180 takes either 64 or 217 (131,072) clock cycles to restart, depending on the CCR3 bit.
Z80180/Z8S180/Z8L180
Enhanced Z180 Microprocessor
Zilog

Bit 12 LNIO. This bit controls the drive capability of certain external I/O pins of the Z8S180/Z8L180. When this bit is set to 1, the output drive capability of the following pins is reduced to 33% of the original drive capability:
- RTSO/TxS
- DCA1
- DCA0
- TXA0
- TXA1
- TOUT

Bit 0 LNAD/DATA. This bit controls the drive capability of the Address/Data bus output drivers. If this bit is set to 1, the output drive capability of the Address and Data bus output is reduced to 33% of its original drive capability:
- BUSACK
- RD
- WR
- M1
- MREQ
- IORD
- RFSH
- HALT

Bit 1 LNCPUCTL. This bit controls the drive capability of the CPU Control pins. When this bit is set to 1, the output drive capability of the following pins is reduced to 33% of the original drive capability:
- /BUSACK
- /RD
- /WR
- /M1
- /MREQ
- /IORQ
- /RFSH
- /HALT

Clocking Serial I/O (CSI/O). The CSI/O channel provides a half-duplex serial transmitter and receiver. This channel can be used for simple high-speed data connection to another microprocessor or microcomputer. TRDR is used for both CSI/O transmission and reception. Thus, the system design must ensure that the constraints of half-duplex operation are met. (Transmit and Receive operation cannot occur simultaneously.) For example, if a CSI/O transmission is attempted while the CSI/O is receiving data, a CSI/O will not work. Also note that TRDR is not buffered. Therefore, attempting to perform a CSI/O transmit while the previous transmit data is still being shifted out causes the shift data to be immediately updated, thereby corrupting the transmit operation in progress. Similarly, reading TRDR while a transmit or receive is in progress should be avoided.

Figure 7. CSI/O Block Diagram

Internal Address/Data Bus

CSI/O Transmit/Receive Data Register: TRDR (8)

CSI/O Control Register: CNTR (8)

Figure 8. Operating Control Register (OMCR: I/O Address = 3EH)

Operation Modes
Z80® versus 64180 Compatibility. The Z80180/Z8S180/Z8L180 is descended from two different “ancestor” processors, Zilog’s original Z80 and the Hitachi’s 64180. The Operating Mode Control Register (OMCR), shown in Figure 8, can be programmed to select between certain Z80 and 64180 differences.

M1E (M1 Enable). This bit controls the M1 output and is set to a 1 during reset.

When M1E=1, the M1 output is asserted Low during the opcode fetch cycle, the INT0 acknowledge cycle, and the first machine cycle of the NMI acknowledge. On the Z80180/Z8S180/Z8L180, this choice makes the processor fetch an RETI instruction once, and when fetching an RETI from zero-wait-state memory will use three clock machine cycles, which are not fully Z80-timing compatible but are compatible with the on-chip CTCs.

When M1E=0, the processor does not drive M1 Low during instruction fetch cycles, and after fetching an RETI instruction once with normal timing, it goes back and re-fetches the instruction using fully Z80-compatible cycles that include driving M1 Low. This may be needed by some external Z80 peripherals to properly decode the RETI instruction. Figure 9 and Table 4 show the RETI sequence when M1E=0.
IASCI REGISTER DESCRIPTION

The following paragraphs explain the various functions of the ASCI registers.

ASCI Transmit Register 0. When the ASCI Transmit Register receives data from the ASCI Transmit Data Register (TDR), the data is shifted out to the TxA pin. When transmission is completed, the next byte (if available) is automatically loaded from TDR into TSR and the next transmission starts. If no data is available for transmission, TSR IDLEs by outputting a continuous High level. This register is not program accessible.

ASCI Transmit Data Register 0,1 (TDR0, 1: I/O address = 06H, 07H). Data written to the ASCI Transmit Data Register is transferred to the TSR as soon as TSR is empty. Data can be written while TSR is shifting out the previous byte of data. Thus, the ASCI transmitter is double buffered.

Data can be written into and read from the ASCI Transmit Data Register. If data is read from the ASCI Transmit Data Register, the ASCI data transmit operation will not be affected by this read operation.

ASCI Receive Shift Register 0,1 (RSR0,1). This register receives data shifted in on the RxA pin. When full, data is automatically transferred to the ASCI Receive Data Register (RDR) if it is empty. If RSR is not empty when the new incoming data byte is shifted in, an overrun error occurs. This register is not program accessible.

ASCI Receive Data FIFO 0,1 (RDR0, 1: I/O Address = 08H, 09H). The ASCI Receive Data Register is a read-only register. When a complete incoming data byte is assembled in RSR, it is automatically transferred to the 4 character Receive Data First-In-First-Out (FIFO) memory. The oldest character in the FIFO (if any) can be read from the Receive Data Register (RDR). The next incoming data byte can be shifted into RSR while the FIFO is full. Thus, the ASCI receiver is well buffered.

ASCI STATUS FIFO

This 4 entry FIFO contains Parity Error, Framing Error, Rx Overrun, and Break status bits associated with each character in the receive data FIFO. The status of the oldest character (if any) can be read from the ASCI status registers as described below.

Note: Not Program Accessible.
Table 5. Data Formats

<table>
<thead>
<tr>
<th>Bit</th>
<th>Function</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>MPE</td>
<td>Multiprocessor Mode Enable (bit 7)</td>
</tr>
<tr>
<td>6</td>
<td>RE</td>
<td>Receiver Enable (bit 6)</td>
</tr>
<tr>
<td>5</td>
<td>TE</td>
<td>Transmitter Enable (bit 5)</td>
</tr>
<tr>
<td>4</td>
<td>MPBR/EFR</td>
<td>Multiprocessor Bit Receive/Error Flag Receive (bit 4)</td>
</tr>
<tr>
<td>3</td>
<td>PEO</td>
<td>Parity Even Odd (bit 3)</td>
</tr>
<tr>
<td>2</td>
<td>MPEBR/EFR</td>
<td>Multiprocessor Bit Transmit/Error Flag Transmit (bit 2)</td>
</tr>
<tr>
<td>1</td>
<td>MOD2</td>
<td>Number of data bits</td>
</tr>
<tr>
<td>0</td>
<td>MOD0</td>
<td>Number of stop bits</td>
</tr>
</tbody>
</table>

MOD2 = 0→7 bit data = 1→8 bit data

MOD0 = 0→No parity = 1→Parity enabled

MOD1 = 0→1 stop bit, = 1→2 stop bits

MOD2, MOD1, and MOD0 are shown in Table 5-6.

Table 5. Data Formats

<table>
<thead>
<tr>
<th>MOD2</th>
<th>MOD1</th>
<th>MOD0</th>
<th>Data Format</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Start + 7 bit data + 1 stop</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Start + 7 bit data + 2 stop</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Start + 7 bit data + parity + 1 stop</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>Start + 7 bit data + parity + 2 stop</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>Start + 8 bit data + 1 stop</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>Start + 8 bit data + parity + 1 stop</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>Start + 8 bit data + parity + 2 stop</td>
</tr>
</tbody>
</table>

Z80180/Z8S180/Z8L180

Enhanced Z180 Microprocessor

Zilog

ASCI CHANNEL CONTROL REGISTER A

ASCI Control Register A 0 (CNTLA0: I/O Address = 00H)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Function</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>MPE</td>
<td>Multiprocessor Mode Enable (bit 7)</td>
</tr>
<tr>
<td>6</td>
<td>RE</td>
<td>Receiver Enable (bit 6)</td>
</tr>
<tr>
<td>5</td>
<td>TE</td>
<td>Transmitter Enable (bit 5)</td>
</tr>
<tr>
<td>4</td>
<td>MPBR/EFR</td>
<td>Multiprocessor Bit Receive/Error Flag Receive (bit 4)</td>
</tr>
<tr>
<td>3</td>
<td>PEO</td>
<td>Parity Even Odd (bit 3)</td>
</tr>
<tr>
<td>2</td>
<td>MPEBR/EFR</td>
<td>Multiprocessor Bit Transmit/Error Flag Transmit (bit 2)</td>
</tr>
<tr>
<td>1</td>
<td>MOD2</td>
<td>Number of data bits</td>
</tr>
<tr>
<td>0</td>
<td>MOD0</td>
<td>Number of stop bits</td>
</tr>
</tbody>
</table>

Z80180/Z8S180/Z8L180

Enhanced Z180 Microprocessor

Zilog

ASCI CHANNEL CONTROL REGISTER B

ASCI Control Register B 0 (CNTLB0: I/O Address = 02H)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Function</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>MPBT</td>
<td>Multiprocessor Bit Transmit (bit 7)</td>
</tr>
<tr>
<td>6</td>
<td>MP</td>
<td>Multiprocessor Mode (bit 6)</td>
</tr>
<tr>
<td>5</td>
<td>CTS/PS</td>
<td>Clear to Send/Prescale (bit 5)</td>
</tr>
<tr>
<td>4</td>
<td>PE</td>
<td>Parity Even Odd (bit 4)</td>
</tr>
<tr>
<td>3</td>
<td>DR</td>
<td>Divide Ratio (bit 3)</td>
</tr>
<tr>
<td>2</td>
<td>SS2</td>
<td>Source/Sink Select (bits 2-0)</td>
</tr>
<tr>
<td>1</td>
<td>SS1</td>
<td>Source/Sink Select (bits 2-0)</td>
</tr>
<tr>
<td>0</td>
<td>SS0</td>
<td>Source/Sink Select (bits 2-0)</td>
</tr>
</tbody>
</table>

Preliminary 1-40

Page A-7
Zilog

Table 6. Divide Ratio

<table>
<thead>
<tr>
<th>SS2</th>
<th>SS1</th>
<th>SS0</th>
<th>Divide Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>4</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>8</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>16</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>32</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>64</td>
</tr>
</tbody>
</table>

ASCI Status Register 0, 1 (STAT0, 1)

Channel status register allows interrogation of ASCI communication, error and modem control signal status, and enabling or disabling of ASCI interrupts.

**ASCI Status Register 0 (STAT0: I/O Address = 04H)**

- RDRF: Receive Data Register Full (bit 7). RDRF is set to 1 when an incoming data byte is loaded into an empty Rx FIFO. Note that if a framing or parity error occurs, RDRF is still set and the receive data (which generated the error) is still loaded into the FIFO. RDRF is cleared to 0 by reading RDRF and last character in the FIFO from IOSTOP mode, during RESET and for ASCI0 if the /DCD0 pin is auto-enabled and is negated (High).
- OVRN: Overrun Error (bit 6). An overrun condition occurs if the receiver has finished assembling a character but the Rx FIFO is full so there is no room for the character. However, this status bit is not set until the last character received before the overrun becomes the oldest byte in the FIFO. This bit is cleared when software writes a 1 to the EFR bit in the CNTLA register, and also by Reset, IOSTOP mode, and for ASCI0 if the /DCD0 pin is auto-enabled and is negated (High).

**ASCI Status Register 1 (STAT1: I/O Address = 05H)**

- TDRE: Transmit Data Register Empty (bit 1). TDRE is set to 1 when the Transmit Data Register (TDR) is empty. TDRE is cleared to 0 by reading TDRE and last character in the TDR from IOSTOP mode, during RESET and for ASCI0 if the /DCD0 pin is auto-enabled and is negated (High).
- RDRF: Receive Data Register Full (bit 7). RDRF is set to 1 when an incoming data byte is loaded into an empty Rx FIFO. Note that if a framing or parity error occurs, RDRF is still set and the receive data (which generated the error) is still loaded into the FIFO. RDRF is cleared to 0 by reading RDRF and last character in the FIFO from IOSTOP mode, during RESET and for ASCI0 if the /DCD0 pin is auto-enabled and is negated (High).

ASCI 180/180A/Z8L/180 Enhanced Z180 Microprocessor

**ASCI Transmit Data Registers**

Register addresses 06H and 07H hold the ASCI transmit data for channel 0 and channel 1, respectively.

- Channel 0
  - Mnemonics TDR0
  - Address (06H)

- Channel 1
  - Mnemonics TDR1
  - Address (07H)

**ASCI Receive Register**

Register addresses 08H and 09H hold the ASCI receive data for channel 0 and channel 1, respectively.

- Channel 0
  - Mnemonics TSR0

- Channel 1
  - Mnemonics TSI0
CSI/O CONTROL/STATUS REGISTER

(MN: I/O Address = 0AH). CNTR is used to monitor CSI/O status, enable and disable the CSI/O, and select the data clock speed and source.

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>EF</td>
<td>EIE</td>
<td>RE</td>
<td>TE</td>
<td>—</td>
<td>SS2</td>
<td>SS1</td>
<td>SS0</td>
</tr>
<tr>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
</tr>
</tbody>
</table>

EF: End Flag (bit 7). EF is set to 1 by the CSI/O to indicate completion of an 8-bit data transmit or receive operation. If enabled by EIE = 1, EF is cleared to 0 during RESET and IOSTOP mode.

EIE: End Interrupt Enable (bit 6). If enabled by EIE = 1, an interrupt is generated when EF is set to 1 or during RESET and IOSTOP mode.

RE: Receive Enable (bit 5). When RE is set to 1, the data clock is enabled. In internal clock mode, the data clock is output from the CKS pin. In external clock mode, the clock is input on the CKS pin. If enabled by EIE = 1, RE is cleared to 0 during RESET and IOSTOP mode.

SS2, SS1, SS0: Speed Select 2, 1, 0 (bits 2-0). SS2, SS1, and SS0 select the CSI/O transmit/receive clock source and speed. SS2, SS1, and SS0 are all set to 1 during RESET.

Table 7. CSI/O Baud Rate Selection

<table>
<thead>
<tr>
<th>SS2</th>
<th>SS1</th>
<th>SS0</th>
<th>Divide Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>&lt;20</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>&lt;40</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>&lt;80</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>&lt;160</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>&lt;320</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>&lt;640</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>&lt;1280</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>External Clock Input (less than &lt;20)</td>
</tr>
</tbody>
</table>

After RESET, the CKS pin is configured as an external clock input (SS2, SS1, SS0 = 1). Changing these values causes CKS to become an output pin and the selected clock is output when transmit or receive operations are enabled.

CSI/O Transmit/Receive Data Register

(TRDR: I/O Address = 0BH).

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Timer Data Register Channel 0L

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Timer Data Register Channel 0H

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Timer Reload Register 0L

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Timer Reload Data

Figure 44. Timer Reload Register Low

Figure 45. Timer Reload Register Channel

Figure 46. Timer Control Register (TCR: I/O Address = 10H)

<table>
<thead>
<tr>
<th>Bit</th>
<th>TIF1</th>
<th>TIFO</th>
<th>TIE1</th>
<th>TIE0</th>
<th>TOC1</th>
<th>TOC0</th>
<th>TOE1</th>
<th>TOE0</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>R</td>
<td>R</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
</tr>
<tr>
<td>6</td>
<td>R</td>
<td>R</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
</tr>
<tr>
<td>5</td>
<td>R</td>
<td>R</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
</tr>
<tr>
<td>4</td>
<td>R</td>
<td>R</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
</tr>
<tr>
<td>3</td>
<td>R</td>
<td>R</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
</tr>
<tr>
<td>2</td>
<td>R</td>
<td>R</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
</tr>
<tr>
<td>1</td>
<td>R</td>
<td>R</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
</tr>
<tr>
<td>0</td>
<td>R</td>
<td>R</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
</tr>
</tbody>
</table>

Table 8. Timer Output Control

<table>
<thead>
<tr>
<th>TOC1</th>
<th>TOC0</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Inhibited</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>TOT/DREQ pin is toggled</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>The TOT/DREQ pin is not affected by the PRT.</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>set Low or High as indicated.</td>
</tr>
</tbody>
</table>

DCD0 dis (bit 6, ASCI0 only). If this bit is 0, then the DCD0 pin "auto-enables" the ASCI0 receiver, such that when the pin is negated/high, the Receiver is held in a RESET state. The state of the DCD0 pin has no effect on receiver operation. In either state of this bit, software can read the state of the DCD0 pin in the STAT0 register, and the receiver will interrupt on a rising edge of DCD0.

CTS0 dis (bit 5, ASCI0 only). If this bit is 0, then the CTS0 pin "auto-enables" the ASCI0 transmitter, in that when the pin is negated/high, the TDR bit in the STAT0 register is forced to 0. If this bit is 1, the state of the CTS0 pin has no effect on the transmitter. Regardless of the state of this bit, software can read the state of the CTS0 pin in the CNTLB0 register.

Table 8. Timer Output Control

<table>
<thead>
<tr>
<th>TOC1</th>
<th>TOC0</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Inhibited</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>TOT/DREQ pin is toggled</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>The TOT/DREQ pin is not affected by the PRT.</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>set Low or High as indicated.</td>
</tr>
</tbody>
</table>

BRG Mode (bit 3). If the SS2-0 bits in the CNTLB register are not 111, and this bit is 0, then the Baud Rate Generator divides PHI by 10 or 30, depending on the BRG Mode. The duration of the Break is under software control (one of the PRTs or CTCs can be used to time it). This bit resets to 0, in which state TXA carries the serial output of the transmitter.
Timer Data Register Channel 1L
Mnemonic TMDR1L
Address 14

Fig. 48. Timer Data Register 1L

7 6 5 4 3 2 1 0

Timer Data

Fig. 51. Timer Reload Register Channel 1L

7 6 5 4 3 2 1 0

Reload Data

Free Running Counter (Read Only)
Mnemonic FRC
Address 18

Fig. 52. Free Running Counter

7 6 5 4 3 2 1 0

Counting Data

Timer Reload Register Channel 1L
Mnemonic RLDR1L
Address 17

Fig. 49. Timer Data Register 1H

7 6 5 4 3 2 1 0

Reset Data

Fig. 50. Timer Reload Channel 1L

7 6 5 4 3 2 1 0

Reload Data

ASCI TIME CONSTANT REGISTERS

If the SS2-0 bits of the CNTLA register are not 111, and the
BRG Mode bit in the ASEXT register is 1, the ASCI divides
the PHI clock by twice (the 16-bit value in these registers,
plus two), to obtain the clock that is presented to the trans-
mitter and receiver for division by 1, 16, or 64 and that can
be output on the CKAI pin.
DMA SOURCE ADDRESS REGISTER CHANNEL 0

(SAR0: I/O Address = 20H to 22H) specifies the physical source address for channel 0 transfers. The register contains 20 bits and can specify up to 1024 KB memory addresses or up to 64 KB I/O addresses. Channel 0 source can be memory, I/O, or memory mapped I/O. For I/O, the MS bits of this register identify the Request Handshake signal.

DMA Source Address Register, Channel 0L

Address 20

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Table 9. Low Noise Option

<table>
<thead>
<tr>
<th>Low Noise Option</th>
<th>ADDR 1E</th>
<th>ADDR 1E, bit 6=1</th>
<th>ADDR 1E, bit 6=0</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADDR 1E, bit 6=1</td>
<td>20 MHz @ 4.5V, 100°C</td>
<td>33 MHz @ 4.5V, 100°C</td>
<td></td>
</tr>
<tr>
<td>ADDR 1E, bit 6=0</td>
<td>10 MHz @ 3.0V, 100°C</td>
<td>20 MHz @ 3.0V, 100°C</td>
<td></td>
</tr>
</tbody>
</table>

Low Noise

Bit 6: Low Noise Crystal Option. Setting this bit to 1 will enable the low noise option for the EXTAL and XTAL pins. This option reduces the gain, in addition to reduction the output drive capability to 30% of its original drive capability. The Low Noise Crystal Option is recommended in the use of crystals for PCMCIA applications where the crystal may be driven too hard by the oscillator. Setting this bit to 0 will select for normal operation of the EXTAL and XTAL pins. The default for this bit is 0.

Note: Operating restrictions for device operation are listed below. If low noise option is required, and normal device operation is needed, use the clock multiplier feature.

Figure 54. Clock Multiplier Register

Figure 55. DMA Source Address Register 0L

Figure 56. DMA Source Address Register 0H

Figure 57. DMA Source Address Register 0B

Note: Operating restrictions for device operation are listed below. If low noise option is required, and normal device operation is needed, use the clock multiplier feature.
DMA DESTINATION ADDRESS REGISTER CHANNEL 0

(DAR0: I/O Address = 23H to 25H) specifies the physical destination address for channel 0 transfers. The register contains 20 bits and can specify up to 1024 KB memory addresses or up to 64 KB I/O addresses. Channel 0 destination can be memory, I/O, or memory mapped I/O. For I/O, the MS bits of this register identify the Request Handshake signal for channel 0.

DMA Destination Address Register Channel 0L
Mnemonic DAR0L
Address 23

DMA Destination Address Register Channel 0B
Mnemonic DAR0B
Address 25

Note: In the R1 and Z Mask, these DMA registers are expanded from 4 bit to 3 bits in the package version of CP-68.

DMA DESTINATION ADDRESS REGISTER CHANNEL 0H

Mnemonic DAR0H
Address 24

DMA BYTE COUNT REGISTER CHANNEL 0

(BCR0: I/O Address = 26H to 27H) specifies the number of bytes to be transferred. This register contains 16 bits and may specify up to 64 KB transfers. When one byte is transferred, the register is decremented by one. If "n" bytes should be transferred, "n" must be stored before the DMA operation.

Note: All DMA Count Register channels are undefined during reset.

DMA Byte Count Register Channel 0L
Mnemonic BCR0L
Address 26

DMA Byte Count Register Channel 0H
Mnemonic BCR0H
Address 27

DMA Byte Count Register Channel 1L
Mnemonic BCR1L
Address 2E

DMA Byte Count Register Channel 1H
Mnemonic BCR1H
Address 2F
DMA MEMORY ADDRESS REGISTER CHANNEL 1

MAR1: I/O Address = 28H to 2AH specifies the physical memory address for channel 1 transfers. This may be destination or source memory address. The register contains 20 bits and may specify up to 1024 KB memory address.

DMA Memory Address Register, Channel 1L
Mnemonic MAR1L
Address 28

DMA Memory Address Register, Channel 1H
Mnemonic MAR1H
Address 29

DMA Memory Address Register, Channel 1B
Mnemonic MAR1B
Address 2A

Figure 66. DMA Memory Address Register, Channel 1H

DMA I/O ADDRESS REGISTER CHANNEL 1

IAR1: I/O Address = 2BH to 2DH specifies the I/O address for channel 1 transfers. This may be destination or source I/O address. The register contains 16 bits of I/O address; its most significant byte identifies the Request Handshake signal and controls the Alternating Channel feature.

All bits in IAR1B reset to 0.

DMA I/O Address Register Channel 1L
Mnemonic IAR1L
Address 2B

DMA I/O Address Register Channel 1H
Mnemonic IAR1H
Address 2C

DMA I/O Address Register Channel 1B
Mnemonic IAR1B
Address 2D

Figure 69. DMA I/O Address Register Channel 1L

Figure 70. DMA I/O Address Register Channel 1H
DMA STATUS REGISTER (DSTAT)

DSTAT is used to enable and disable DMA transfer and DMA termination interrupts. DSTAT also indicates DMA transfer status, in other words, completed or in progress.

<table>
<thead>
<tr>
<th>Bit</th>
<th>DE1</th>
<th>DE0</th>
<th>DWE1</th>
<th>DIE1</th>
<th>DIE0</th>
<th>DME</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**DE1**: DMA Enable Channel 1 (bit 7). When DE1 = 1 and DME = 1, channel 1 DMA is enabled. When a DMA transfer terminates (BCR1 = 0), DE1 is reset to 0 by the DMAC. When DE1 = 0 and the DMA interrupt is enabled (DE1 = 1), a DMA interrupt request is made to the CPU.

To perform a software write to DE1, DWE1 should be written with 0 during the same register write access. Writing DE1 to 1 enables channel 1 DMA and automatically sets DME (DMA Main Enable) to 1. DE1 is cleared to 0 during RESET.

**DE0**: DMA Enable Channel 0 (bit 6). When DE0 = 1 and DME = 1, channel 0 DMA is enabled. When a DMA transfer terminates (BCR0 = 0), DE0 is reset to 0 by the DMAC. When DE0 = 0 and the DMA interrupt is enabled (DE0 = 1), a DMA interrupt request is made to the CPU.

To perform a software write to DE0, DWE0 should be written with 0 during the same register write access. Writing DE0 to 0 disables channel 0 DMA. Writing DE0 to 1 enables channel 0 DMA and automatically sets DME (DMA Main Enable) to 1. DE0 is cleared to 0 during RESET.

**DWE1**: DE1 Bit Write Enable (bit 5). When performing any software write to DE1, DWE1 should be written with 0 during the same access. DWE1 always reads as 1.

**DWE0**: DE0 Bit Write Enable (bit 4). When performing any software write to DE0, DWE0 should be written with 0 during the same access. DWE0 always reads as 1.

**DIE1**: DMA Interrupt Enable Channel 1 (bit 3). When DIE1 is set to 1, the termination DMA transfer (indicated when DE1 = 0) causes a CPU interrupt request to be generated. When DIE1 = 0, the channel 0 DMA termination interrupt is disabled. DIE1 is cleared to 0 during RESET.

**DIE0**: DMA Interrupt Enable Channel 0 (bit 2). When DIE0 is set to 1, the termination channel 0 of DMA transfer (indicated when DE0 = 0) causes a CPU interrupt request to be generated. When DIE0 = 0, the channel 0 DMA termination interrupt is disabled. DIE0 is cleared to 0 during RESET.

**DME**: DMA Main Enable (bit 0). A DMA operation is only enabled when its DE bit (DE0 for channel 0, DE1 for channel 1) and the DME bit is set to 1.

When NMI occurs, DME is reset to 0, thus disabling DMA activity during the NMI interrupt service routine. To restart DMA, DE and/or DE1 should be written with 1 (even if contents are already 1). This automatically sets DME to allowing DMA operations to continue. Note that DME cannot be directly written, it is cleared to 0 by TBR or indirectly set to 1 by setting DE0 and/or DE1 to 1. DME is cleared to 0 during RESET.

**DMA MODE REGISTER (DMODE)**

DMODE is used to set the addressing and transfer mode for channel 0.

<table>
<thead>
<tr>
<th>Bit</th>
<th>DM1</th>
<th>DM0</th>
<th>SM1</th>
<th>SM0</th>
<th>MMOD</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**DM1**, DM0: Destination Mode Channel 0 (bits 5, 4) specifies whether the destination for channel 0 transfers is memory or I/O, and whether the address should be incremented or decremented for each byte transferred. DM1 and DM0 are cleared to 0 during RESSET.

**SM1**, SM0: Source Mode Channel 0 (bits 3, 2) specifies whether the source for channel 0 transfers is memory or I/O, and whether the address should be incremented or decremented for each byte transferred.

### Table 10. Channel 0 Destination

<table>
<thead>
<tr>
<th>DM1</th>
<th>DM0</th>
<th>Memory</th>
<th>Memory Increment/Decrement</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Memory</td>
<td>+1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Memory</td>
<td>–1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Memory</td>
<td>fixed</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>I/O</td>
<td>fixed</td>
</tr>
</tbody>
</table>

### Table 11. Channel 0 Source

<table>
<thead>
<tr>
<th>SM1</th>
<th>SM0</th>
<th>Memory</th>
<th>Memory Increment/Decrement</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Memory</td>
<td>+1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Memory</td>
<td>–1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Memory</td>
<td>fixed</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>I/O</td>
<td>fixed</td>
</tr>
</tbody>
</table>
Table 12. Transfer Mode Combinations

<table>
<thead>
<tr>
<th>DM1</th>
<th>DM0</th>
<th>SM1</th>
<th>SM0</th>
<th>Transfer Mode</th>
<th>Increment/Decrement</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Memory→Memory</td>
<td>SAR0+1, DAR0+1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Memory→Memory</td>
<td>SAR0+1, DAR0+1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Memory*→Memory</td>
<td>SAR0 fixed, DAR0+1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Memory→Memory</td>
<td>SAR0+1, DAR0-1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>Memory→Memory</td>
<td>SAR0-1, DAR0-1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>I/O→Memory</td>
<td>SAR0 fixed, DAR0-1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Memory→Memory*</td>
<td>SAR0+1, DAR0 fixed</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Memory→Memory*</td>
<td>SAR0-1, DAR0 fixed</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Memory→I/O</td>
<td>SAR0+1, DAR0 fixed</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>Reserved</td>
<td></td>
</tr>
</tbody>
</table>

Note: * Includes memory mapped I/O.

MMOD: Memory Mode Channel 0 (bit). When channel 0 is configured for memory to/from memory transfers, there is no Request Handshake signal to control the transfer timing. Instead, two automatic transfer timing modes are selectable: burst (MMOD = 1) and cycle steal (MMOD = 0). For burst memory to/from memory transfers, the DMA takes control of the bus continuously until the DMA transfer completes (as shown by the byte count register = 0). In cycle steal mode, the CPU is given a cycle for each DMA byte transfer cycle until the transfer is completed.

For channel 0 DMA with I/O source or destination, the selected Request signal times the transfer and thus MMOD is ignored. MMOD is cleared to 0 during RESET.

Typically, an input/output device, the associated DM bit should be programmed as 0 for level sense because the device has a relatively long time to update its Request signal after the DMA channel reads data from it in the first of the two machine cycles involved in transferring a byte. An output/destination device has much less time to update its Request signal after the DMA channel starts a write operation to it, as the second machine cycle of the two cycle involved in transferring a byte. With zero wait state I/O devices, which apply only to the ASCIs, it is impossible for the device to update its Request signal in time, and edge sensing must be used.
With one-wait-state I/O cycles (the fastest possible except for the ASCIs), it is unlikely that an output device will be able to update its Request in time, and an edge sense is required.

**DIM1, DIM0: DMA Channel 1 I/O and Memory Mode (bits 1-0)**. Specifies the source/destination and address modifier for channel 1 memory to/from I/O transfer modes.

**Interrupt Vector Low Register**

Mnemonic: IL

Address 33

Bits 7-5 of IL are used as bits 7-5 of the synthesized interrupt vector during interrupts for the INT1 and INT2 pins and for the DMAs, ASCIs, PRTs, and C/SI/O. These three bits are cleared to 0 during Reset (Figure 75).

**Table 13. Channel 1 Transfer Mode**

<table>
<thead>
<tr>
<th>Address</th>
<th>DIM1</th>
<th>DIM0</th>
<th>Transfer Mode</th>
<th>Increment/Decrement</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0</td>
<td>Memory→I/O</td>
<td>MAR1=I, IAR1 fixed</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0 1</td>
<td>Memory→I/O</td>
<td>MAR1 fixed, MAR1=I</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 0</td>
<td>I/O→Memory</td>
<td>IAR1 fixed, MAR1=I</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 1</td>
<td>I/O→Memory</td>
<td>IAR1 fixed, MAR1 fixed</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Interrupt Source Dependent Code**

- **IL 7**: Trap
- **IL 6**: Trap
- **IL 5**: Programmed
- **IL 4**: Interrupt Source Dependent Code
- **IL 3-0**: Trap

When a TRAP interrupt occurs, the Z80180/Z8S180/Z8L180 operates as follows:

1. The TRAP bit in the Interrupt TRAP Control (ITC) register is set to 1.
2. The current PC (Program Counter) value, reflecting the location of the undefined Opcode, is saved on the stack.
3. The Z80180/Z8S180/Z8L180 vectors to logical address 0. Note that if logical address 0000H is mapped to physical address 00000H, the vector is the same as for RESET. In this case, testing the TRAP bit in ITC will reveal whether the restart at physical address 00000H was caused by RESET or TRAP.

All TRAP interrupts occur after fetching an undefined second and third Opcode by following one of the "prefix" OpCodes CBH, DDH, EDH, or FDH, or after fetching an undefined third Opcode by following one of the "double prefix" OpCodes DDCBH or FDCBH.

The state of the Undefined Fetch Object (UFO) bit in IT allows the TRAP software to correctly “adjust” the stacked PC depending on whether the second or third byte of the Opcode can generate the TRAP. If UFO=0, the starting address of the invalid instruction is equal to the stacked PC-1. UFO=1, the starting address of the invalid instruction is equal to the stacked PC-2.
Zilog®

ITALIAN TECHNOLOGY

Z80180/Z8S180/Z8L180 Enhanced 2160 Microprocessor

REFRESH CONTROL REGISTER

Mnemonic: RCR
Address: 36

REFE: Refresh Enable (bit 7). If REF = 1, refresh is enabled. If REF = 0, refresh is disabled.

REFW: Refresh Wait (bit 6). If REFW = 0, refresh is in effect for 2 clock cycles. If REFW = 1, refresh is in effect for 3 clock cycles.

CYC1, CYC0: Cycle Interval (bit 1, 0). CYC1 and CYC0 specify the interval in clock cycles between refresh cycles.

The refresh function is disabled during RESET. After RESET, based on the initialized value of RCR, refresh cycles will occur with an interval of 10 clock cycles and be 3 clock cycles in duration.

Table 14. DRAM Refresh Intervals

<table>
<thead>
<tr>
<th>CYC1</th>
<th>CYC0</th>
<th>Insertion Time Interval</th>
<th>Ø: 10 MHz</th>
<th>8 MHz</th>
<th>6 MHz</th>
<th>4 MHz</th>
<th>2.5 MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>10 states (10.0 s)</td>
<td>1.06 Ø</td>
<td>1.25 Ø</td>
<td>1.66 Ø</td>
<td>2.5 Ø</td>
<td>4.0 Ø</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>20 states (20.0 s)</td>
<td>2.0 Ø</td>
<td>2.5 Ø</td>
<td>3.3 Ø</td>
<td>5.0 Ø</td>
<td>8.0 Ø</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>40 states (40.0 s)</td>
<td>4.0 Ø</td>
<td>5.0 Ø</td>
<td>6.6 Ø</td>
<td>10.0 Ø</td>
<td>16.0 Ø</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>80 states (80.0 s)</td>
<td>8.0 Ø</td>
<td>10.0 Ø</td>
<td>13.3 Ø</td>
<td>20.0 Ø</td>
<td>32.0 Ø</td>
</tr>
</tbody>
</table>

Note: *calculated interval

Refresh Control and Reset. After RESET, based on the initialized value of RCR, refresh cycles will occur with an interval of 10 clock cycles and be 3 clock cycles in duration.

Dynamic RAM Refresh Operation

1. Refresh Cycle insertion is stopped when the CPU is in the following states:
   a. During RESET
   b. When the bus is released in response to BUSREQ
   c. During SLEEP mode
   d. During WAIT states.

2. Refresh cycles are suppressed when the bus is released in response to BUSREQ. However, the refresh timer continues to operate. Thus, the time at which the first refresh cycle occurs after Z80180/Z8S180/Z8L180 re-acquires the bus depends on the refresh timer and has no timing relationship with the bus exchange.

3. Refresh cycles are suppressed during SLEEP mode if a refresh cycle is requested during SLEEP mode. The refresh cycle request is internally "latched" (untimed with the next refresh request). The "latched" refresh cycle is inserted at the end of the first mach cycle after SLEEP mode is exited. After this initial cycle, the time at which the next refresh cycle occurs depends on the refresh time and has no relationship with the exit from SLEEP mode.

4. The refresh address is incremented by one for each successful refresh cycle, not for each refresh. Thus independent of the number of "missed" refresh requests, each refresh bus cycle will use a refresh address incremented by one from that of the previous refresh bus cycles.

MMU COMMON BASE REGISTER

Mnemonic: CBR
Address: 38

Reserved

Figure 79. MMU Common Base Register (BBR: I/O Address = 38H)
MMU BANK BASE REGISTER (BBR).

Mnemonic BBR
Address 39

<table>
<thead>
<tr>
<th>Bit</th>
<th>BB7</th>
<th>BB6</th>
<th>BB5</th>
<th>BB4</th>
<th>BB3</th>
<th>BB2</th>
<th>BB1</th>
<th>BB0</th>
</tr>
</thead>
<tbody>
<tr>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
</tr>
</tbody>
</table>

**Figure 80. MMU Bank Base Register (BBR: I/O Address = 39H)**

MMU COMMON/BANK AREA REGISTER (CBAR).

Mnemonic CBAR
Address 3A

<table>
<thead>
<tr>
<th>MMU Common/Bank Area Register (CBAR: I/O Address = 3 AH)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit</td>
</tr>
<tr>
<td>-----</td>
</tr>
<tr>
<td>R/W</td>
</tr>
</tbody>
</table>

**Figure 81. MMU Common/Bank Area Register (CBAR: I/O Address = 3 AH)**

OPERATION MODE CONTROL REGISTER

Mnemonic OMCR
Address 3E

The Z80180/Z8S180/Z8L180 is descended from two different “ancestor” processors, Zilog’s original Z80 and the Hitachi 64180. The Operation Mode Control Register (OMCR) can be programmed to select between certain differences between the Z80 and the 64180.

**Figure 82. Operating Control Register (OMCR: I/O Address = 3EH)**

**Figure 83. RETI Instruction Sequence with MIE=0**

I/O Control Register (ICR).

ICR allows relocating of the internal I/O addresses. ICR also controls enabling/disabling of the IOSTOP mode (Figure 84).
IOA7, 6: I/O Address Relocation (bits 7,6). IOA7 and IOA6 relocate internal I/O as shown in Figure 85. Note that the high-order 8 bits of 16-bit internal I/O address are always 0. IOA7 and IOA6 are cleared to 0 during Reset.

IOSTOP Mode (bit 5). IOSTOP mode is enabled when IOSTOP is set to 1. Normal I/O operation resumes when IOSTOP is reprogrammed or Reset to 0.

<table>
<thead>
<tr>
<th>IOA7:IOA6</th>
<th>000OH</th>
<th>003FH</th>
<th>0040H</th>
<th>0041H</th>
<th>0042H</th>
<th>0043H</th>
<th>0070H</th>
<th>0071H</th>
</tr>
</thead>
<tbody>
<tr>
<td>11</td>
<td>00FFH</td>
<td>00COH</td>
<td>00BFH</td>
<td>008OH</td>
<td>007OH</td>
<td>004OH</td>
<td>003FH</td>
<td>0000H</td>
</tr>
</tbody>
</table>

Figure 85. I/O Address Relocation
APPENDIX B: ELECTRIC DIAGRAMS

In this appendix are available some electric diagrams of the most frequently used GPC® 183 interfaces. All these interfaces can be yourself produced and some of them are standard grifo® cards and, if required, they can be directly ordered.
**Figure B2: SPA 03 Electric Diagram**

- **Title:** SPA-03
- **Date:** 16/11/98
- **Rel.:** 1.1
- **Page:** 1 of 1
Figure B4: QTP 24P Electric Diagram (1 of 2)
FIGURE B5: QTP 24P ELECTRIC DIAGRAM (2 OF 2)
FIGURE B6: ABACO® I/O BUS INPUT OUTPUT ELECTRIC DIAGRAM
FIGURE B7: BUS INTERFACE ELECTRIC DIAGRAM
Figure B8: IAC 01 electric diagram
APPENDIX C: ALPHABETICAL INDEX

A
A/D ABACO® 16
A/D CONVERSION TIME 8
A/D CONVERTER 7, 8, 43, 50
   A/D RESOLUTION 8
   ANALOG INPUTS 28
   INPUT CONNECTOR 16
   INPUT CURRENT 9
   INPUT IMPEDANCE 9
   INPUT VOLTAGE 9
   VOLTAGE-CURRENT CONVERSION 29
ABACO® BUS 54
ABACO® I/O BUS 6, 18, 35, 36, 43, 54
ABB 03 6
ABB 05 6
ADDRESSES 43
   ABACO® I/O BUS ADDRESSES 46
   I/O ADDRESSES 44
   MEMORY ADDRESSES 46
ASC1 3, 4, 8, 20, 26, 37, 50

B
BACK UP 34
BACK UP BATTERY 13
   CURRENT 9
   EXTERNAL 9
   ON BOARD 9
BIBLIOGRAPHY 58
BT1 34
BUZZER 3, 43, 48

C
CARD VERSION 1
CLOCK 3, 8
CONNECTIONS 10
CONNECTORS 8
   CN1 18
   CN2 10
   CN3 12
   CN4 13
   CN5 14
   CN6 16
   CN7A 26
   CN7B 20
CONSUMPTION ON +5 VDC  9
CONTROL LOGIC  7
CPU INTERNAL PERIPHERALS  51
CSI/O  3
CURRENT LOOP  4, 24, 28
CURRENT PROVIDED ON +5 VDC  9

D
DEBUG  35
DIP SWITCH  49
DMAC  3
DSW1  43, 49

E
EPROM  4, 8, 32, 34, 43
EXTERNAL CARDS  54

F
FGDOS 183  40
FLASH EPROM  4, 8, 32, 34, 43

G
GET 80  40

H
HANDSHAKE OF SERIAL LINE A  50

I
I/O ABACO®  12, 14
I/O CONNECTION  28
I/O SIGNALS  6
IDLE MODE  36
INPUTS  35
INPUTS  50
INTERFACES  28
INTERRUPTS  35
INTRODUCTION  1

J
JUMPERS  31
  2 PINS JUMPERS  32
  3 PINS JUMPERS  32
  5 PINS JUMPERS  31
<table>
<thead>
<tr>
<th>Section</th>
<th>Pages</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>30, 43</td>
</tr>
<tr>
<td>ACTIVITY</td>
<td>48</td>
</tr>
<tr>
<td>SPOT LED</td>
<td>49</td>
</tr>
<tr>
<td>M</td>
<td>34</td>
</tr>
<tr>
<td>MEMORY SELECTION</td>
<td>34</td>
</tr>
<tr>
<td>MMU</td>
<td>3</td>
</tr>
<tr>
<td>O</td>
<td>28</td>
</tr>
<tr>
<td>OPERATOR INTERFACES</td>
<td>28</td>
</tr>
<tr>
<td>P</td>
<td>35</td>
</tr>
<tr>
<td>PI</td>
<td>35</td>
</tr>
<tr>
<td>PHOTO</td>
<td>11</td>
</tr>
<tr>
<td>POWER SUPPLY</td>
<td>4, 9, 10, 32, 36</td>
</tr>
<tr>
<td>LINEAR</td>
<td>10, 36</td>
</tr>
<tr>
<td>SWITCHING</td>
<td>10, 36</td>
</tr>
<tr>
<td>PPI</td>
<td>8</td>
</tr>
<tr>
<td>PPI 82C55</td>
<td>12, 14, 51</td>
</tr>
<tr>
<td>PRT</td>
<td>3, 8</td>
</tr>
<tr>
<td>Q</td>
<td>28</td>
</tr>
<tr>
<td>QTP 16P</td>
<td>28</td>
</tr>
<tr>
<td>QTP 24P</td>
<td>28</td>
</tr>
<tr>
<td>R</td>
<td>6, 13</td>
</tr>
<tr>
<td>REAL TIME CLOCK</td>
<td>6, 13</td>
</tr>
<tr>
<td>RELATIVE HUMIDITY</td>
<td>9</td>
</tr>
<tr>
<td>RESET</td>
<td>35</td>
</tr>
<tr>
<td>RESET CONTACT</td>
<td>7</td>
</tr>
<tr>
<td>RESET KEY</td>
<td>29</td>
</tr>
<tr>
<td>RS 232</td>
<td>4, 22, 26, 28</td>
</tr>
<tr>
<td>RS 422</td>
<td>4, 22, 28, 31</td>
</tr>
<tr>
<td>RS 422, RS 485 LINE TERMINATION</td>
<td>9, 23, 32, 38</td>
</tr>
<tr>
<td>RS 485</td>
<td>4, 22, 28, 31</td>
</tr>
<tr>
<td>RTC</td>
<td>34, 35, 52</td>
</tr>
<tr>
<td>RUN</td>
<td>35</td>
</tr>
<tr>
<td>RV1</td>
<td>30</td>
</tr>
<tr>
<td>S</td>
<td>4</td>
</tr>
<tr>
<td>SERIAL COMMUNICATION</td>
<td>4</td>
</tr>
<tr>
<td>SERIAL EEPROM</td>
<td>4, 8, 34, 43, 49</td>
</tr>
<tr>
<td>SERIAL LINE</td>
<td></td>
</tr>
</tbody>
</table>
SYNCHRONOUS  14
SERIAL LINE A  26
SERIAL LINE B
  CONNECTOR  20
  CURRENT LOOP  24, 37
  RS 232  22, 37
  RS 422  22, 31, 37
  RS 485  22, 31, 38
SIZE  8
SOFTWARE DESCRIPTION  48
SRAM  4, 8, 13, 34, 43
STOP MODE  36

T
  TEMPERATURE RANGE  9
  TEST POINT  29
  TP1  29, 30
  TRANSZORB™  4
  TTL  28
  TTL INPUTS  14
  TTL LINES  12

V
  VISUAL SIGNALATIONS  30

W
  WATCH DOG  6, 32, 35, 43, 48
    INTERVENT TIME  9
  WEIGHT  8

Z
  Z8S180  3, 8