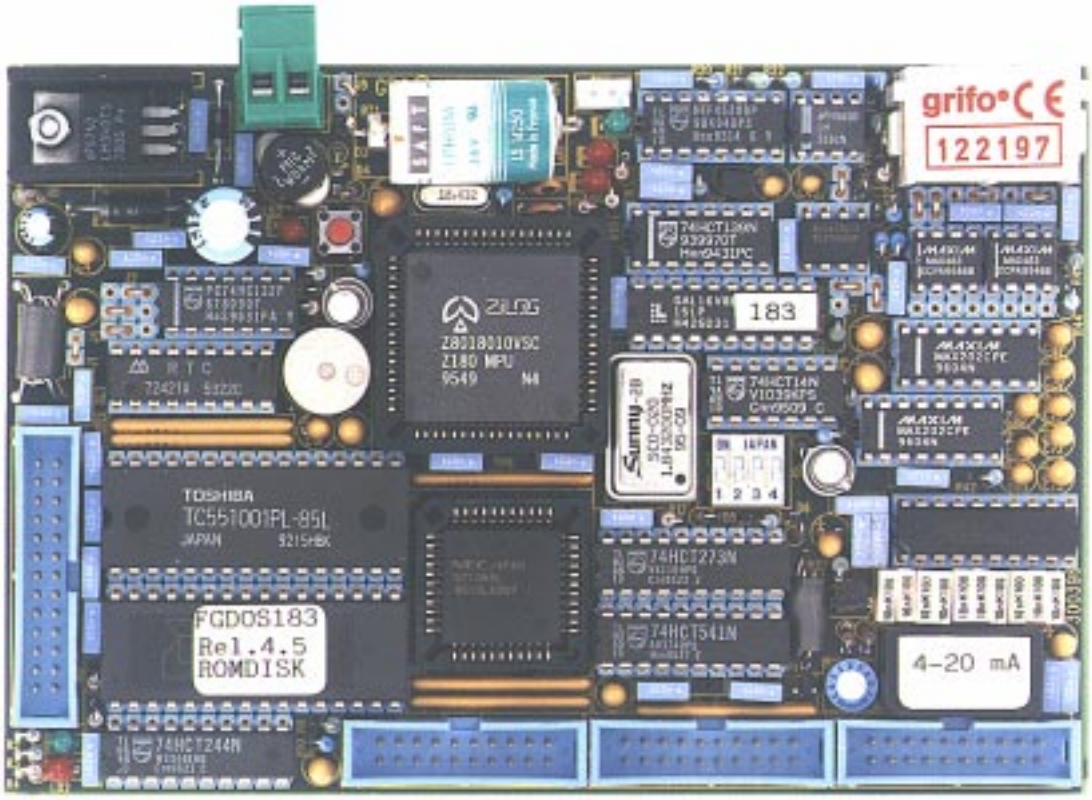
GPC® 183

General Purpose Controller Z8S180

TECHNICAL MANUAL



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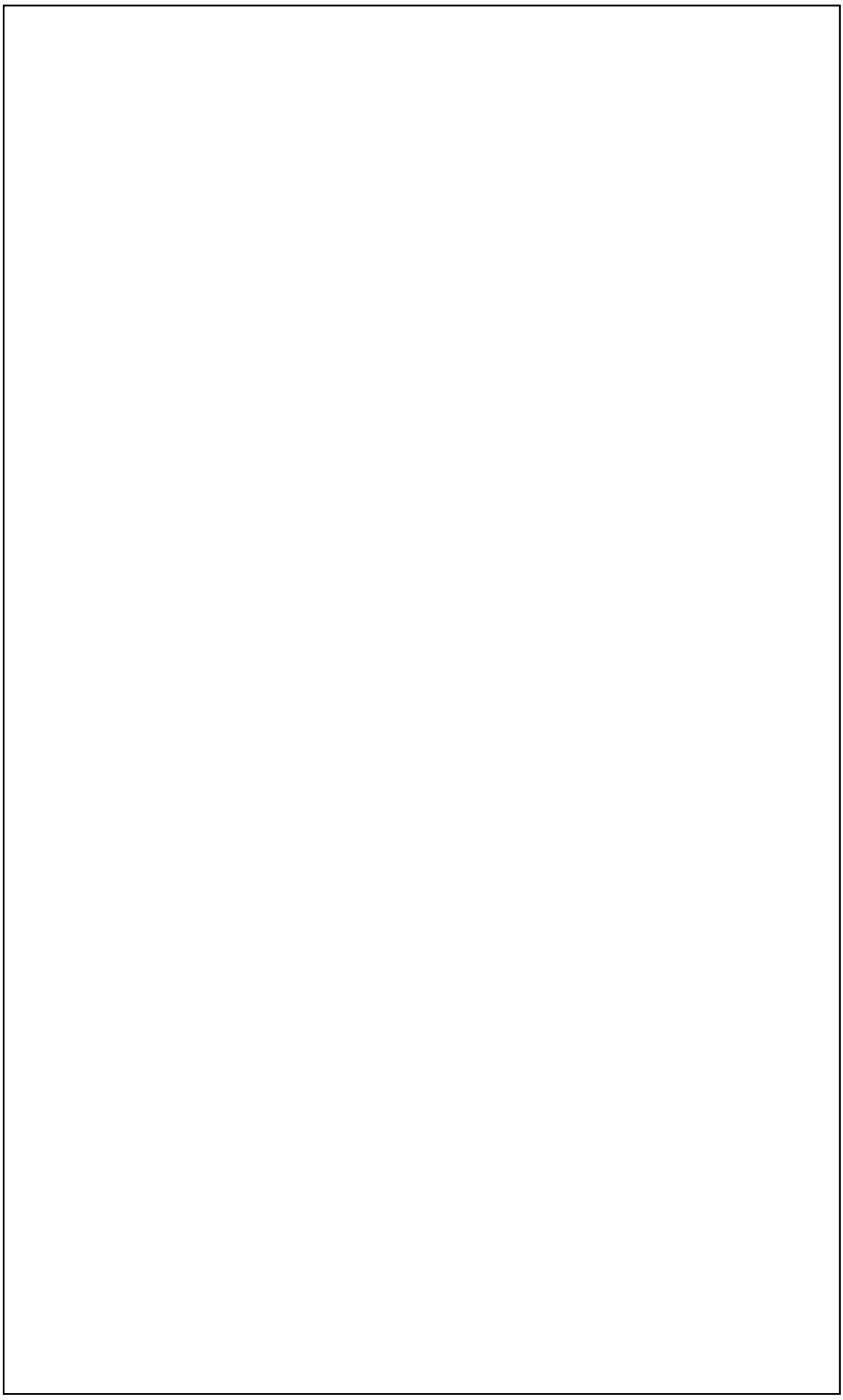
GPC® 183 Edition 5.10 *Rel. 02 April 2002*



GPC® 183

General Purpose Controller Z8S180

TECHNICAL MANUAL

100x149 mm size, Intelligent module of the **Abaco® BLOCK** series; optional plastic mount for connection to **DIN 46277-1** and **DIN 46277-3** Ω rails; **22 MHz standard CPU Z8S180**; **up to 512K of EPROM** or **FLASH** and up to **512K of SRAM**; through **FGDOS** the memory that exceeds 64K is managed as RAM/ROM Disk, it is possible deleting and re-programming the on borad FLASH, automatically, with the user program; **back up** circuitery for **SRAM** and **RTC** through internal and external **Lithium** battery; **Real Time Clock** capable to generate INT; serial **EEPROM** up to 8KBytes; 11 lines **12 bits A/D** converter with range +2.5 V or 0÷20 mA; **28 TTL I/O** lines which are settable by software, **2** status **LEDs** and active **BUZZER**; clocked serial I/O interface at user disposal on I/O connector; 1 software readable 3 ways **dip switch**, and dip for RUN/DEBUG mode; 2 internal channels of Programmable Reload timer of 16bits; 2 serial lines in **RS232**, one configurable in **RS422**,**RS485** or **Current Loop**; double Baud Rate generator,settable by software, up to 115.2 KBaud; **Watch dog** circuitery, hardware switching off, with status LED; 26 pins expansion connector for **Abaco® I/O BUS**; 2 standard 20 pins **Abaco® I/O** connectors; 1 standard 20 pins **Abaco® A/D** connector; Low Power function in **Halt**, **Iostop**, **Sleep**, **System Stop**, **Idle**, **Standby** mode; optional built in wide range power supply, or single external **5Vdc**, **235 mA** power supply; on board protection aganist voltage peaks by **TransZorb™**; wide range of developement software such as: **Remote Symbolic Debugger**, **Macro Assembler**, **GET 80**, **BASIC NSB8**, **FORTH**, **C Compilers**, **HTC 80**, **Lisp**, **PASCAL 80, etc.**

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IMPORTANT

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grifo® reserves the right to change the contents and form of this document, as well as the features and specification of its products at any time, without prior notice, to obtain always the best product.
For specific informations on the components mounted on the card, please refer to the Data Book of the builder or second sources.

SYMBOLS DESCRIPTION

In the manual could appear the following symbols:

Attention: Generic danger

Attention: High voltage

Trade Marks

abaco®, **GPC®**, **grifo®** : are trade marks of **grifo®**.
Other Product and Company names listed, are trade marks of their respective companies.

GENERAL INDEX

FIGURES INDEX

INTRODUCTION

The use of these devices has turned - IN EXCLUSIVE WAY - to specialized personnel.

The purpose of this handbook is to give the necessary information to the cognizant and sure use of the products. They are the result of a continual and systematic elaboration of data and technical tests saved and validated from the manufacturer, related to the inside modes of certainty and quality of the information.

The reported data are destined- IN EXCLUSIVE WAY- to specialized users, that can interact with the devices in safety conditions for the persons, for the machine and for the enviroment, impersonating an elementary diagnostic of breakdowns and of malfunction conditions by performing simple functional verify operations , in the height respect of the actual safety and health norms.

The informations for the installation, the assemblage, the dismantlement, the handling, the adjustment, the reparation and the contingent accessories, devices etc. installation are destined - and then executable - always and in exclusive way from specialized warned and educated personnel, or directly from the TECHNICAL AUTHORIZED ASSISTANCE, in the height respect of the manufacturer recommendations and the actual safety and health norms.

The devices can't be used outside a box. The user must always insert the cards in a container that rispect the actual safety normative. The protection of this container is not threshold to the only atmospheric agents, but specially to mechanic, electric, magnetic, etc. ones.

To be on good terms with the products, is necessary guarantee legibility and conservation of the manual, also for future references. In case of deterioration or more easily for technical updates, consult the AUTHORIZED TECHNICAL ASSISTANCE directly.

To prevent problems during card utilization, it is a good practice to read carefully all the informations of this manual. After this reading, the user can use the general index and the alphabetical index, respectly at the begining and at the end of the manual, to find information in a faster and more easy way.

CARD VERSION

The present handbook is reported to the **GPC® 183** card release **300396** and later. The validity of the bring information is subordinate to the number of the card release. The user must always verify the correct correspondence among the two denotations. On the card the release number is present in more points both board printed diagram (serigraph) and printed circuit (for example near battery BT1 on the component side and on the solder side).

GENERAL FEATURES

The **GPC® 183** is a powerful control **Low Cost** module capable of operationg in stand alone mode or as an intelligent peripheral, and/or remoted, in a wider telecontrol or aquisition network. The **GPC® 183** module is secured in a plastic mount for connection to **Omega** rails **DIN 46277-1** and **DIN 46277-3**, thereby dispensing with the need of rack and allowing a less costly mounting direct to the electrical control panel.
Programming and exploiting the resources of this module is extremely easy thanks to the help of the stout **FGDOS** romated operative system. This latter supports high level languages such as BASIC PASCAL, C Compilers and so on; it makes available the memory resources as they should be **ROM/ RAM disk** allowing an immediate use of this devices at high level. This module linked **to the MCI64** and **FGDOS** manages **PCMCIA** cards of **RAM cards** and, directly, the on board peripherals as **A/D converter**, **serial EEPROM**. In addition to that the **GPC® 183** allows a direct management of **LCD** or **Fluorescent displays** and matrix keyboard**.** For an immediate use of this command, **KDx x24** boards are available, or if you need a finished object, there are the **QTP xxP.**These operator panels, offered in the open frame version, bear the same aesthetic as **QTP xx**, but, as the local intelligence is not furnished, they are driven directly by **GPC® 183**, allowing a notable cost reduction.The FGDOS affords truly notable debug facilities, and allows to program directly on board a **FLASH** with the user program.
The **GPC®183** is equipped with a series of standard **Abaco®**connectors allowing immediate use of the many **BLOCK I/O** modules available, or enabling a simple and inexpensive means of connections to equipment interfaces made by the user or by third parties. **Abaco® I/O BUS** connector allows to drive directly **ZBR 324**, **ZBT 324**, **ZBR 246**, **ZBT 246**, **ZBR 168**, and through **ABB 03, ABB 05** and so on, it is possible to run all peripheral cards available on **ABACO® BUS**

- 100x149 mm size, Intelligent module of the **Abaco® BLOCK** series
- Optional plastic mount for connection to **DIN 46277-1** and **DIN 46277-3** Ω rails
- **22 MHz standard CPU Z8S180**
- **Up to 512K of EPROM** or **FLASH** and up to **512K of SRAM.** Through **FGDOS** the memory that exceed 64K is managed as RAM/ROM Disk. It is possible deleting and re-programming the on borad FLASH, automatically, with the user program
- **Back up** circuitery for **SRAM** and **RTC** through internal and external **Lithium** battery
- **Real Time Clock** capable to generate INT
- Serial **EEPROM** up to 8KBytes
- 11 lines **12 bits A/D** converter with range +2.5 V; 0÷20 mA
- **28 TTL I/O** lines which are settable by software, **2** status **LEDs** and active **BUZZER**
- Clocked serial I/O interface at user disposal on I/O connector
- 1 software readable 3 ways **dip switch**, and dip for RUN/DEBUG mode
- 2 internal channels of Programmable Reload timer of 16bits
- 2 serial lines in **RS232**, one configurable in **RS422**,**RS485** or **Current Loop**
- Double Baud Rate generator,settable by software, up to 115.2 KBaud
- **Watch dog** circuitery, hardware switching off, with status LED
- 26 pins expansion connector for **Abaco®_I/O BUS**
- 2 standard 20 pins **Abaco® I/O** connectors
- 1 standard 20 pins **Abaco® A/D** connector
- Low Power function in **Halt**, **Iostop**, **Sleep**, **System Stop**, **Idle**, **Standby** mode
- Optional Built in wide range power supply, or single external **5Vdc**, **235 mA** power supply
- On board protection aganist voltage peaks by **TransZorb™**

- Wide range of developement software such as: **Remote Symbolic Debugger**, **Macro Assembler**, **GET 80**, **BASIC NSB8**, **FORTH**, **C Compilers**, **HTC 80**, **Lisp**, **PASCAL 80, etc.**

Here follows a description of the board's functional blocks, with an indication of the operations performed by each one. To easily locate these blocks and verify their connections pleare refer to figure 1.

CPU

GPC® 183 board is designed to employ the **Z8S180** CPU manifactured by **ZILOG**. This 8 bits CPU is code compatible with Z80 and Z180 so it features an extended instructions set (170), high speed of execution and data manipulation and efficent vectored interrupts management. Remarkable is the presence of these peripherals inside the CPU:

- Two 16 bits timers, provided with programmable prescaler (PRT);
- Two asynchronous serial lines capable to manage handshake signals (ASCI);
- Two DMA channels for high speed data transfers (DMAC);
- Memory management unit (MMU);
- One synchronous serial line (CSI/O);
- Interrupt controller;
- Wait states generator to access external devices;
- Five different operating modes, to reduce power consumption;

For further informations about this component please refer to the manifacturer documentation, or see Appendix A of this manual.

BUZZER

GPC® 183 board features a capacitive buzzer capable to produce a constant sound, driven by a circuitry that can be software enabled and/or disabled through the cotrol logic, that can be used to generate acoustic alerts, sound feedback, etc.

CLOCK

GPC® 183 is provided with a circuitery that generates the CPU clock frequence (22.1184 MHz); this frequence is used also to generate the frequencies needed to the other sections of the board (Timer, serial lines, etc.). If the User needs to run very fast applications the clock frequence can be even doubled by interventing on the proper circuitry (for more informations please contact **grifo®**). We would remark that the CPU clock frequence is the same of the crystal by programming a CPU register.

MEMORY DEVICES

On the card can be monted 1032K bytes of memory divided with a maximum of 512KByte EPROM or FLASH EPROM, 512KByte SRAM and 8KByte serial EEPROM. The **GPC® 183** memory configuration must be chosen considering the application to realize or the specific requirements of the user. Normally the card is equipped with 128KByte of static RAM and 8KByte of serial EEPROM; all different configurations must be specified from the user, at the moment of the order. With the on board back up circuit there is the possibility to keep data , also when power supply is failed; in this way the card is always able to maintain parameters, logged data, system status and configuration, etc. without using expensive external UPS. The back up circuit is supplied by a on board lithium battery or an external battery to be connected to a specific connector.
The addressing of memory devices is controlled by a specific control logic, that provides to allocate the devices in the microprocessor address space, this control logic automatically manages the different addressing mode and it satisfies the requests of each **GPC® 183** software tools.
For further information about memory configuration, sockets description and jumpers connection, please refer to "ADDRESSES AND MAPS" and "PERIPHERAL DEVICES SOFTWARE DESCRIPTION" chapters and to "MEMORY SELECTION" paragraph for detailed informations about sockets to use and jumpers configuration.

SERIAL COMMUNICATION

Serial communication is completely software settable both for protocol and for speed (which ranges from 50 to as high as 115.2KBaud with standard clock frequency). These settings are performed programming the ASCI inside the microprocessor and the baude rate generator, for further information please refer to the manifacturer documentation or to Appendix A of this manual. By hardware it is possible to select, through some on board jumpers,the electric communication protocol. In detail, one line is always buffered as RS 232, while the other line can be buffered in four different electrical protocols: **RS 232**, **current loop**, **RS 485** or **RS 422**; in this last cases also directionality and line activation is programmable.

POWER SUPPLY

The unique voltage needed to supply the board (+5 Vdc) can be provided in two ways: directly through pin 25 (GND) and 26 (+5 Vdc) of connector CN1 or through the switching supply sections. The type of supply cannot be changed by the user so it must be specified in the order.
On the card the power supply signals are available on all the connectors but when the best power layout is required we suggest to supply power through CN1 and to get it from the other connectors. This explain the direction reported for +5 Vdc signal on each connector of the card. The can be anyway supplied from a connector indicate as output for +5 Vdc but this is severly discouraged so eventual consequences are totally responsability of the user.
Switching supply section requires an input voltage in the range **8÷24 Vac** (12÷34 Vdc) which can be provided through specific standard connectors quick and easy to install, for further information please refer to the paragraph “SUPPLY VOLTAGES”.
Power supply circuit is designed to reduce consumption and to increase electrical noise immunity. Please remind that on board there is a protection circuit aganist voltage peaks by **TransZorb**™ and that it is a good practise to mantain galvanically isolated from +5 Vdc all the others power voltages of the developed system.

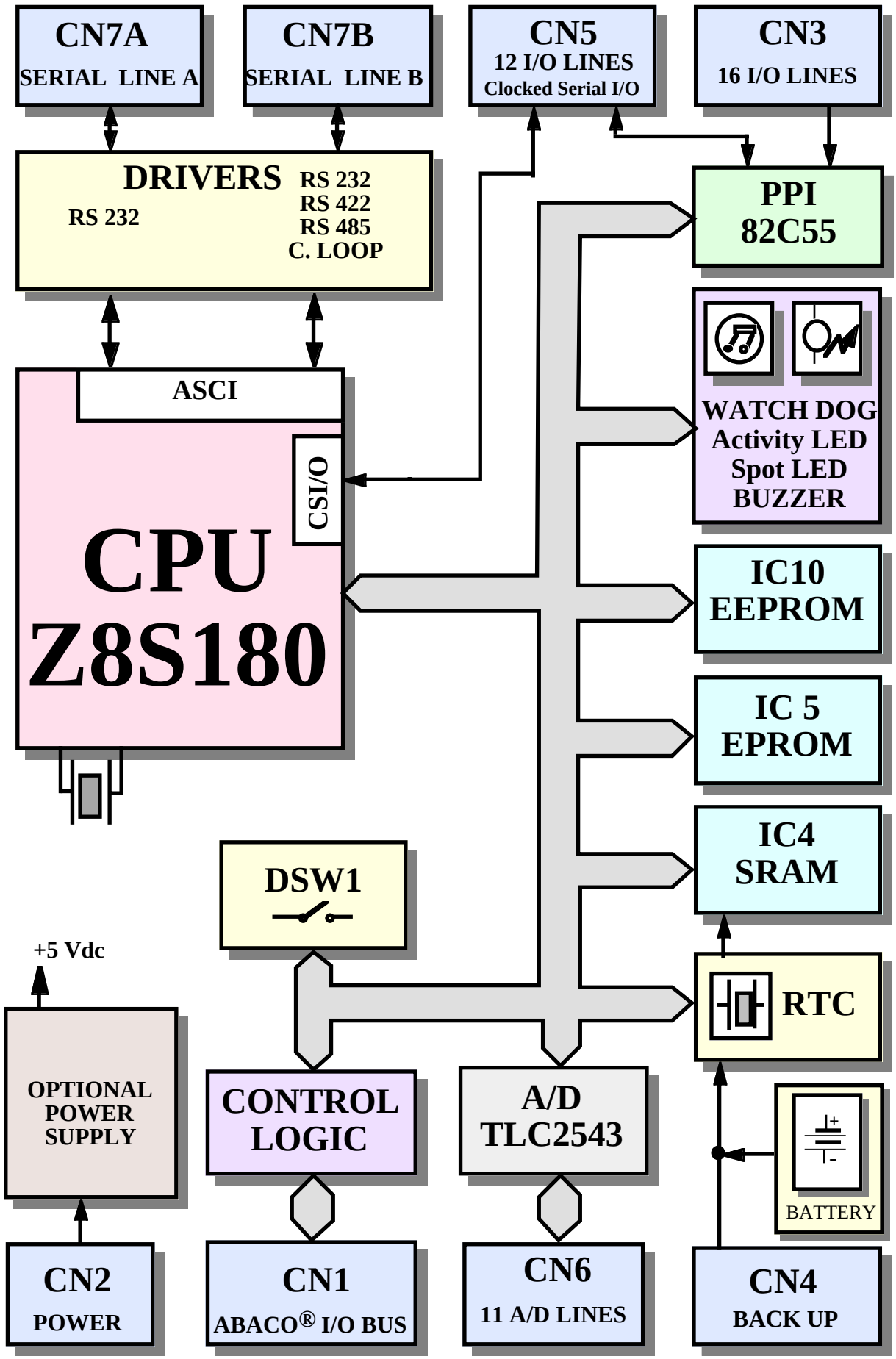


FIGURE 1: BLOCK DIAGRAM

ABACO® I/O BUS

One of the most important features of **GPC® 183** is its possibility to be interfaced to industrial **ABACO® I/O BUS** .Thanks to its standard **ABACO® I/O BUS** connector, the card can be connected to some of the numerous **grifo®** boards,both intelligent and not. For example the user can directly use cards for analog signals acquisition, cards for analog signals generation (D/A), cards for digital I/O signals management, cards with timers and counters, cards for temperature controls, etc. also custom boards designed to satisfy specific needs of the end user.
Using **ABB 03** or **ABB 05** mother boards it is possible manage all the BUS **ABACO®** single EURO cards. So **GPC® 183** becomes the right component for each industrial automation system, in fact **ABACO® I/O BUS** makes the card easily expandable with the best price/performance ratio.

I/O LINES

GPC® 323 features three 8 bits parallel ports performing 24 TTL level I/O signals whose directionality is byte-level software settable plus four TTL input lines managed by the control logic. These I/O signals provide the **GPC® 183** board more employ possibilities (for example the management of non intelligent peripherals, interfaces, etc.) also in applications where the communcation handshake must be completely software managed. The lines are available through two standard I/O **ABACO®** connectors and can be completely programmed by software programming five registers located in the CPU addressing space.

REAL TIME CLOCK

GPC® 183 board is provided with a complete real time clock device capable to manage hours, minutes, seconds, day of month, month, year and day of week in stand alone mode. The component is supplied by the back up circuitry to warrant data integrity in every working condition and is completely software programmable acting on 16 registers addressable in the CPU I/O addressing space by a specific memory management circuitry.The RTC section can generate interrupts at a software programmable rate, for diverting the CPU from its normal tasks or awakening it from one of its low consumption working modes.

WATCH DOG

GPC® 183 board is provided with a watch dog circuitery that, if used, allows to exit from infinite loop or abnormal conditions not managed by the application program. This circuitery is made by an astable section with 1.5 sec of intervent time, is completely software managed (by accessing a register addressed in the CPU addressing space) and gives the board an exterme degree of safety.
Changes of watch dog circuitery intervent time are possible by interventing on its RC net on specific user request; in case of need please contact **grifo®**.

RESET CONTACT

P1 reset contact of the **GPC® 183** board allows the user to reset the board and restarting it in a general clearing condition. The main purpose of this contact is to come out of infinite loop conditions, useful especially during debug or to grant a particular initial stat. Please see figure 9 for an easy localization of this contact.

A/D CONVERTER

This peripheral can acquire 11 channels with a maximun resolution of 12 bits.
By software it is possible to decide which channels to employ, to start and to stop the acquisition, etc., through a synchronous communication to the device. By means to simplify the management of this device some software packages provide utility procedures that are capable to manage all its parts. The connectable analog signals are variable voltage signals in the range 0÷2.490Vdc (default) or current signals in the range 0÷20 mA (option **.8420**). This device is optional and must be explicitally requested in the order (code **.AD**).

BOARD CONFIGURATION

A four pins dip switch has been introduced expressely to make the board and in particualr the application program confugrable. The possibility to read by software the status of the switches gives the user the ability to manage many different conditions by an unique program, without having to employ other input singnals (typical applications are: language choice, program parameters definition, operational mode selection, etc.). **GPC® 183** is also provided with two software managed signalation LEDs to visualize the overall status of the system.

CONTROL LOGIC

A specific control logic is responsable of mapping the registers of the on-board devices and the memory devices.
The logic allocates these devices in the CPU addressing space, for further informations please refer to the paragraph "I/O MAPPING".

TECHNICAL FEATURES

GENERAL FEATURES

Devices:

24 input/output TTL (PPI)
4 input TTL
two 16 bit timers (PRT)
1 RS 232 serial line (ASCI 1)
1 RS 232, RS 422, RS 485 or current loop serial line (ASCI 0)
11 signals A/D converter
1 local reset key
2 LEDs software manageable
1 watch dog hardware astable
1 real time clock
1 buzzer
1 dip switch featuring 4 dips
1 **ABACO®** I/O BUS interface
1 power supply section (optional)

Memory:

IC 5:	EPROM from 128K x 8 to 512K x 8
	FLASH EPROM from 128K x 8 to 512K x 8
IC 4:	SRAM from 128K x 8 to 512K x 8
IC 10:	serial EEPROM from 256 Bytes up to 8K Bytes

CPU: ZILOG Z8S180

Crystal (clock) frequency: 22.1184 (22.1184) MHz

A/D resolution: 12 bit

A/D conversion time: 10 µsec

PHYSICAL FEATURES

Size (W x H x D):

100 x 149 x 25 mm	(without container)
110 x 160 x 60 mm	(with DIN rails container)

Weight:

170 g	(without container)
280 g	(with DIN rails container)

Connectors:

CN1:	26 pins low profile vertical M
CN2:	2 pins quick release screw terminal M
CN3:	20 pins low profile vertical M
CN4:	2 pins low profile vertical M
CN5:	20 pins low profile vertical M
CN6:	20 pins low profile vertical M
CN7A:	6 pins plug
CN7B:	pins plug

Watch dog intervent time:	1.50 sec
Temperature range:	from 0 to 50 Centigrad degreeses
Relative humidity:	20% up to 90% (without condense)

ELECTRIC FEATURES

Power Supply:	+5 Vdc		(without supply section)
	6÷12 Vac	(9÷16 Vdc) *	(linear supply section)
	8÷24 Vac	(12÷34 Vdc)	(switching supply section)
Consumption on +5 Vdc:	240 mA (default configuration) 180 mA (default configuration in low consumption) 280 mA (complete configuration)		
Current provided on +5 Vdc for external loads:	720 mA *		(without supply section)
	720 mA *		(switching supply section)
On board back up battery:	3.0 Vdc; 180 mAh		
External back up battery:	3.6÷5 Vdc		
Back up current:	2 µA (on board battery)		
A/D converter input voltage:	0÷2.490 Vdc		
A/D converter input current:	0÷20; 4÷20 mA		(with conversion module)
A/D converter input impedance:	1 K Ω		
RS 422, RS 485 line termination:	Line termination resistance=		120 Ω
	Positive pull up resistance=		3.3 KΩ
	Negative pull up resistance=		3.3 KΩ

* Data here reported are referred to a 20 centigrad degreeeses environmental temperature (for further informations please refer to the paragraph “SUPPLY VOLTAGES”).

INSTALLATION

In this chapter there are the information for a right installation and correct use of the card. The user can find the location and functions of each connectors, jumpers and some explanatory diagrams.

CONNECTIONS

The **GPC®183** module has 7 connectors that can be linkeded to other devices or directly to the field, according to system requirements. In this paragraph there are connectors pin out, a short signals description (including the signals direction), connectors location (please refer to figure 24) and some electrical diagrams that shows the on board circuit of each connector.

CN 2 - POWER SUPPLY CONNECTOR WITH SUPPLY SECTION

CN2 is a 2 pins screw terminal connector. The board supply voltage must be provided through this connector. When using the board without any power supply section, the +5 Vdc must be provided through pin 26 (+Vdc) and pin 25 (GND) of CN1.

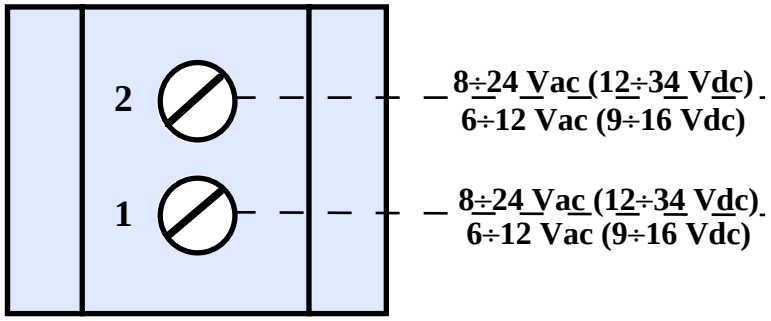


FIGURE 3: CN2 - POWER SUPPLY CONNECTOR FOR ON BOARD SUPPLY SECTION

Signals description:

8÷24 Vac (12÷34 Vdc) = I- Supply input 8÷24 Vac (12÷34 Vdc) (switching section)
6÷12 Vac (9÷16 Vdc) or 6÷12 Vac (9÷16 Vdc) (linear section)

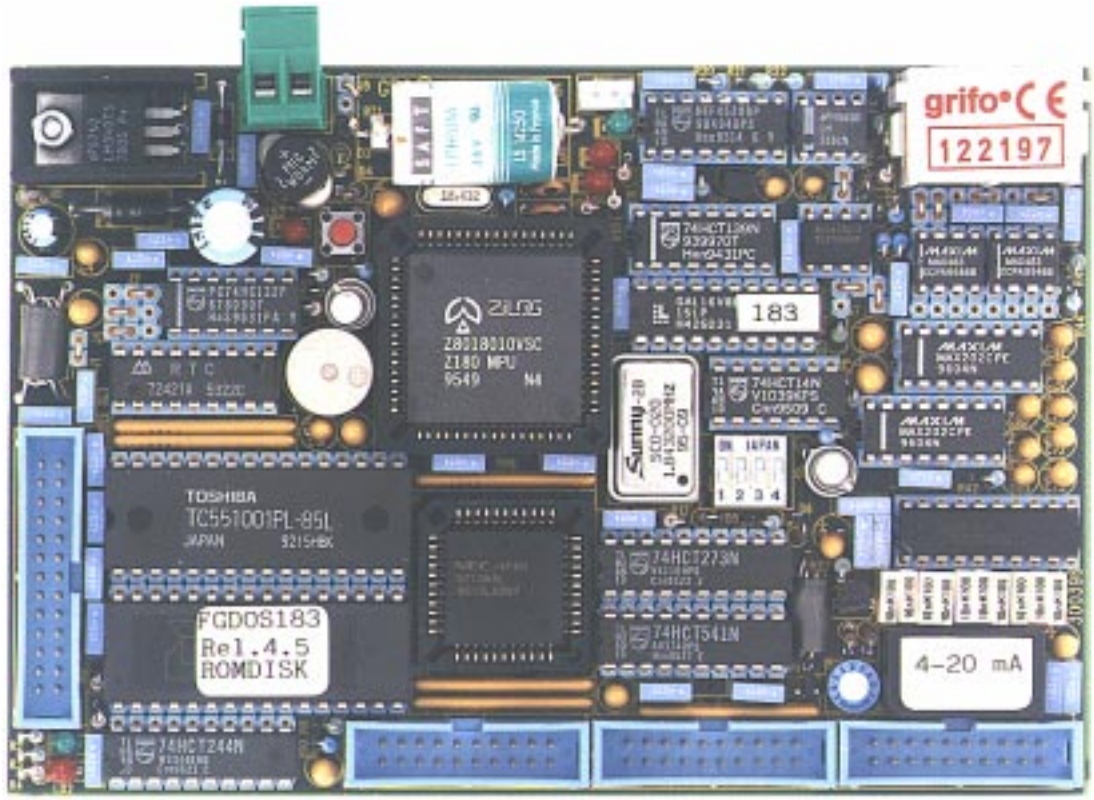


FIGURE 4: CARD PHOTO

CN3 - PPI 82C55 PORT A AND C I/O CONNECTOR

CN3 is a 20 pins, male, vertical, low profile connector, 2.54 mm pitch.Through CN3 two parallel 8 bits ports out of three (ports A and C) of programmable peripheral PPI 82C55 are conected to external world. All this connector's signals are at TTL level and follow the **I/O ABACO®** standard.

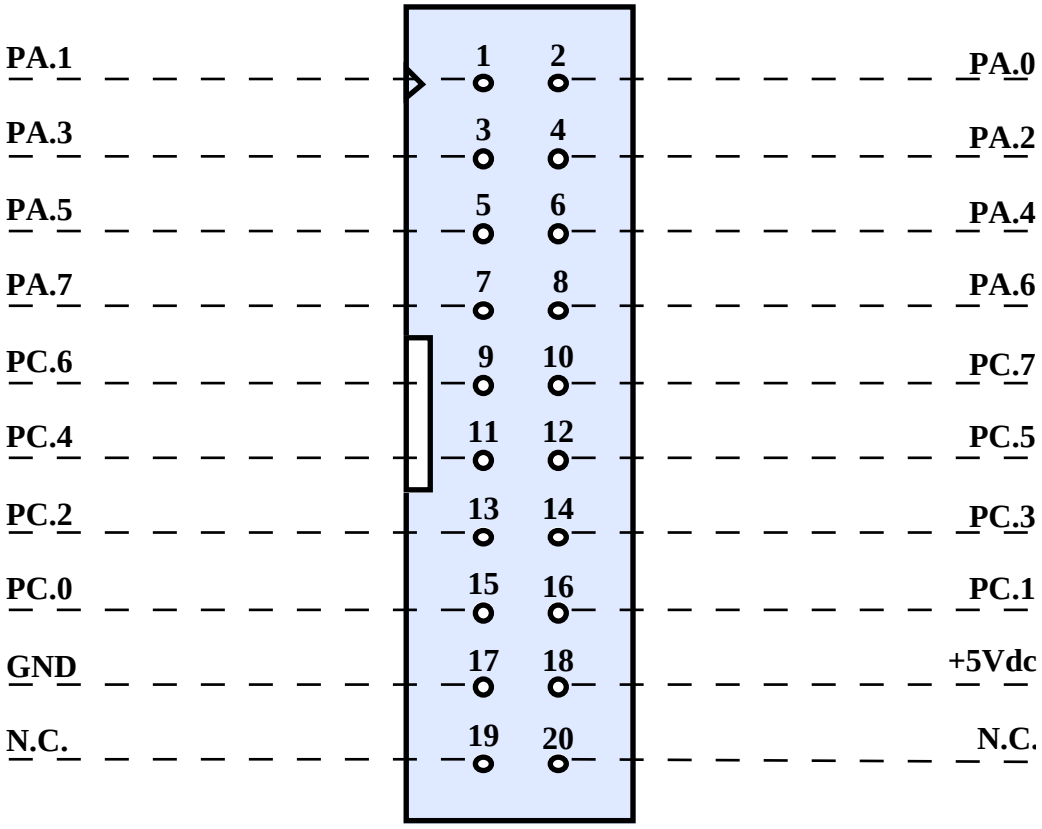


FIGURE 5: CN3 - PPI 82C55 PORT A AND C I/O CONNECTOR

Signals description:

PA.n	=	I/O	-	PPI 82C55 port A n-th digital signal
PC.n	=	I/O	-	PPI 82C55 port C n-th digital signal
GND	=		-	Ground signal
+5 Vdc	=	O	-	+5 Vdc signal
N.C.	=		-	Not connected

Remarkable is the possibility to connect directly through CN3 a set of interfaces designed to solve several typical problems of industrial automation. We especially would want to remark the simplicity of installation and software management of **QTP 24P**, **KDL x24**, **KDF 224**, etc., that are also supported by high level programming languages. For further informations please refer to the paragraph “OPERATOR INTERFACES”.

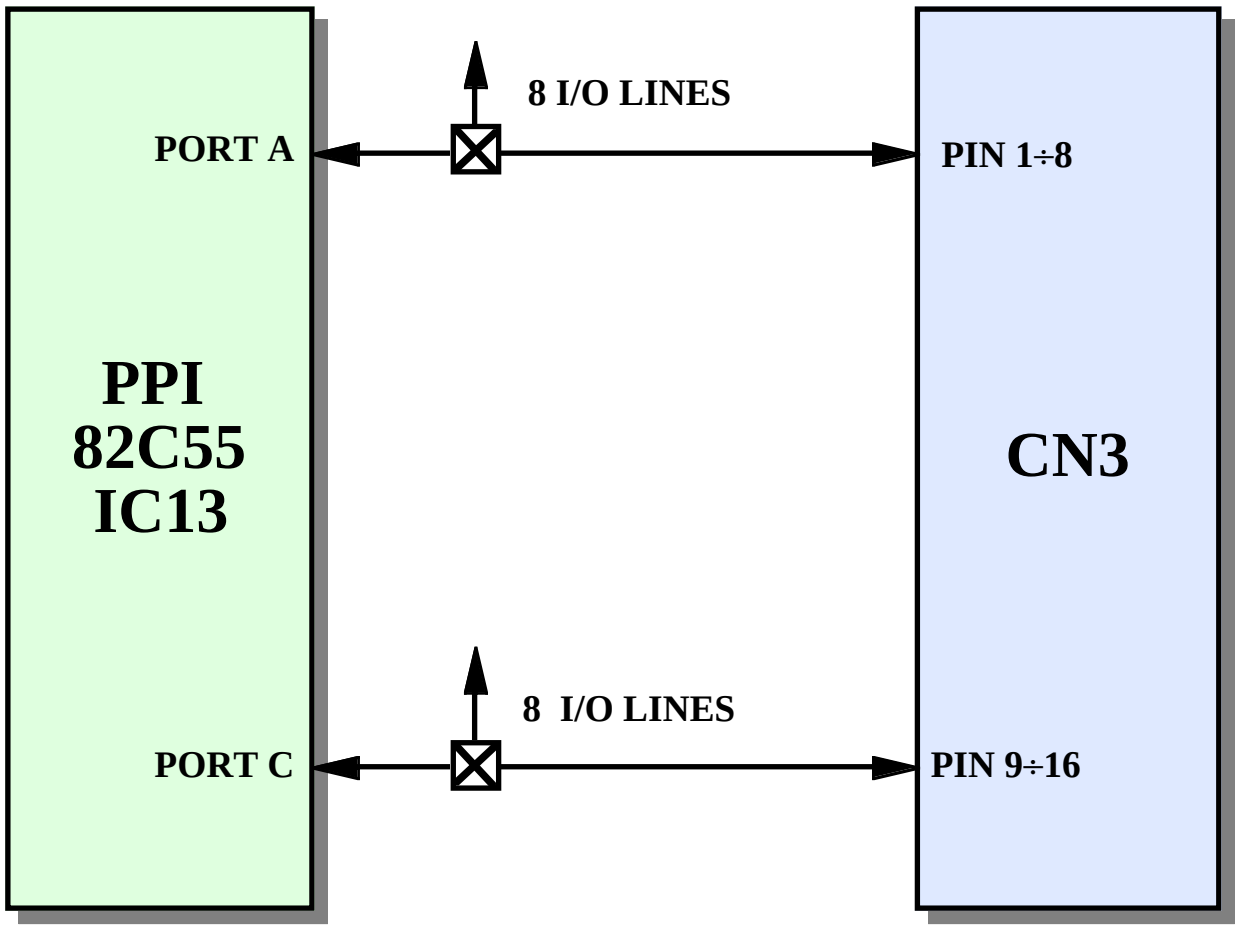


FIGURE 6: PORTS A AND C ON CN3 BLOCK DIAGRAM

CN4 - BACK UP EXTERNAL BATTERY CONNECTOR

CN4 is a 2 pins, vertical, male connector with 2.54mm pitch. Through CN4 the user can connect an external battery for SRAM and RTC back up when the power supply is switched off (for further information please refer to chapter "BACK UP").

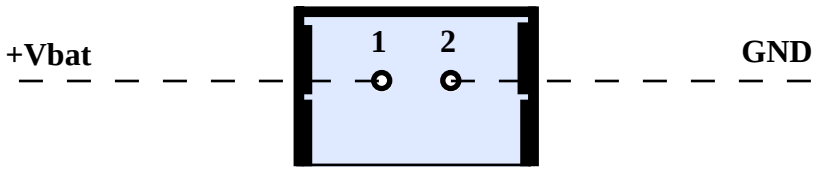


FIGURE 7: CN4 - EXTERNAL BACK UP BATTERY CONNECTOR

Signals description:

+Vbat	=	I	-	Positive pin of external back up battery
GND	=		-	Negative pin of external back up battery

CN5 - PPI 82C55 PORT B, TTL INPUTS AND SYNC SERIAL LINE CONNECTOR

CN5 is a 20 pins, male, vertical, low profile connector, 2.54 mm pitch.Through CN5 one parallel 8 bits port out of three (port B) of programmable peripheral PPI 82C55, four digital inputs and the synchronous serial line are conected to external world. All this connector's signals are at TTL level and follow the **I/O ABACO®** standard.

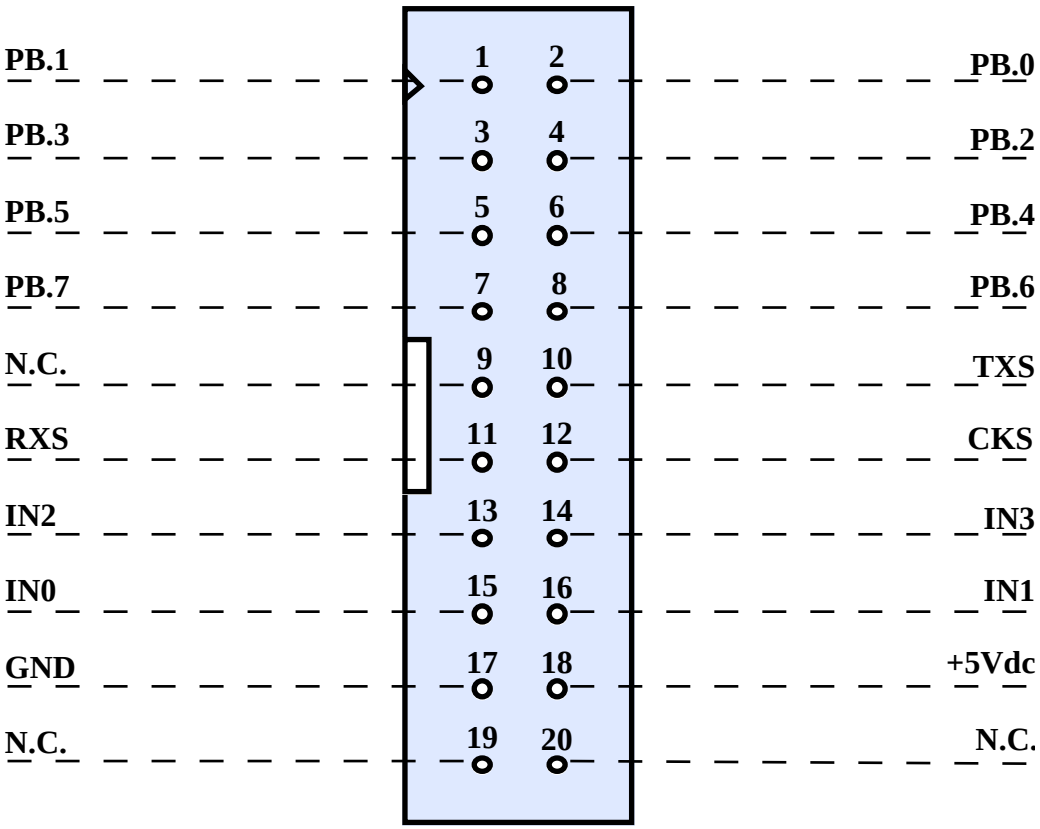


FIGURE 8: CN5 - PPI 82C55 PORT B, TTL INPUTS AND SYNCRONOUS SERIAL LINE CONNECTOR

Signals description:

PB.n	=	I/O	-	PPI 82C55 port B n-th digital signal
INn	=	I	-	digital input n-th signal
TXS	=	O	-	Synchronous serial line transmission signal
RXS	=	I	-	Synchronous serial line reception signal
CKS	=	I/O	-	Synchronous serial line clock signal
GND	=		-	Ground signal
+5 Vdc	=	O	-	+5 Vdc signal
N.C.	=		-	Not connected

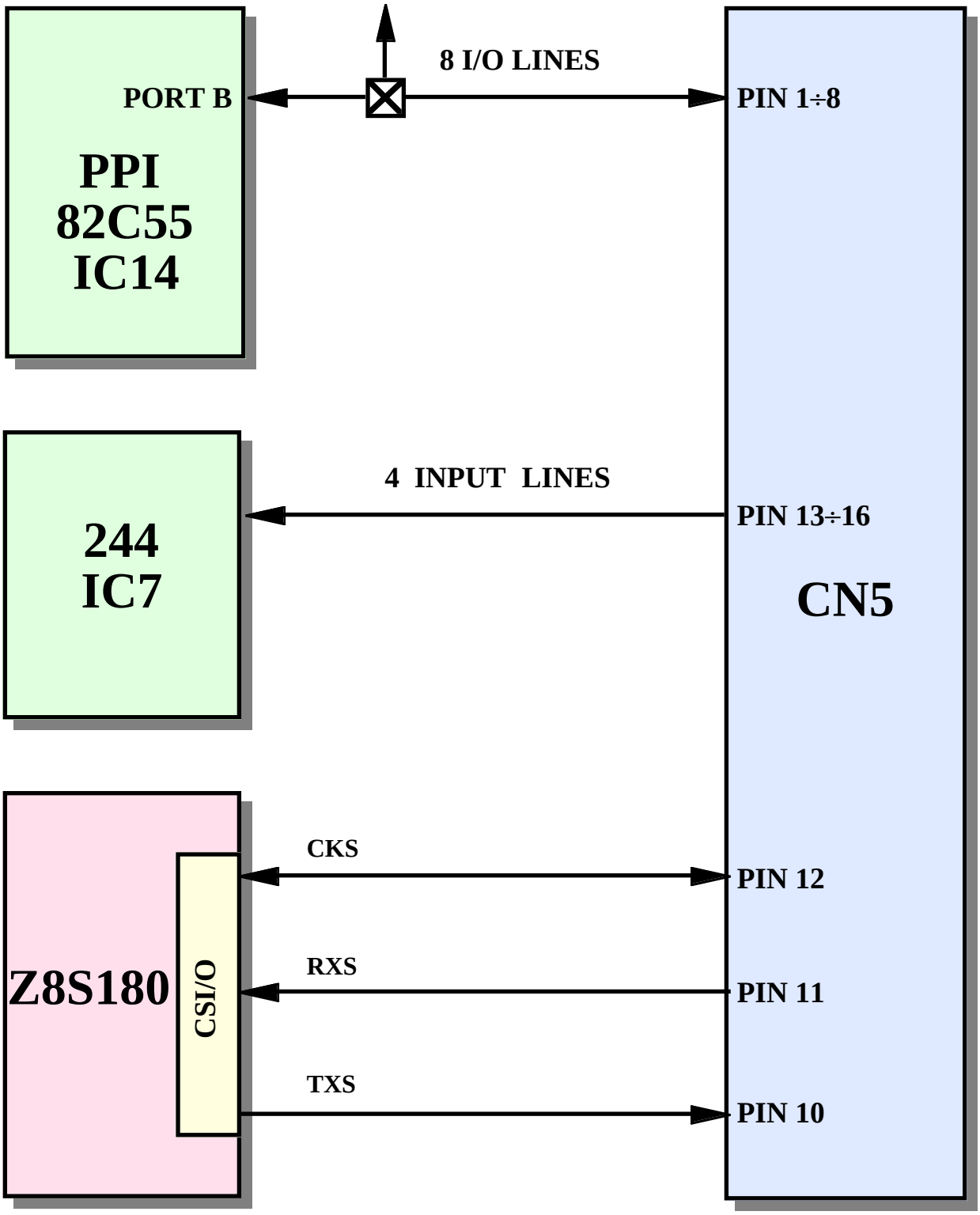


FIGURE 9: PPI 82C55 PORT B, TTL INPUTS AND SYNC SERIAL LINE ON CN5 BLOCK DIAGRAM

CN6 - A/D CONVERTER INPUT CONNECTOR

CN6 is a 20 pins, male, vertical, low profile connector, 2.54 mm pitch. Through CN6 the 11 A/D converter section input signals interface to the external world.
This connector accepts voltage analog signals (0÷2.490 Vdc) or current analog signals (0÷20 mA) and follow the **A/D ABACO®** standard.
Signals are placed in order to reduce interference and electricale nois warranting a good signal transmission and in order to simplify connection with other systems.

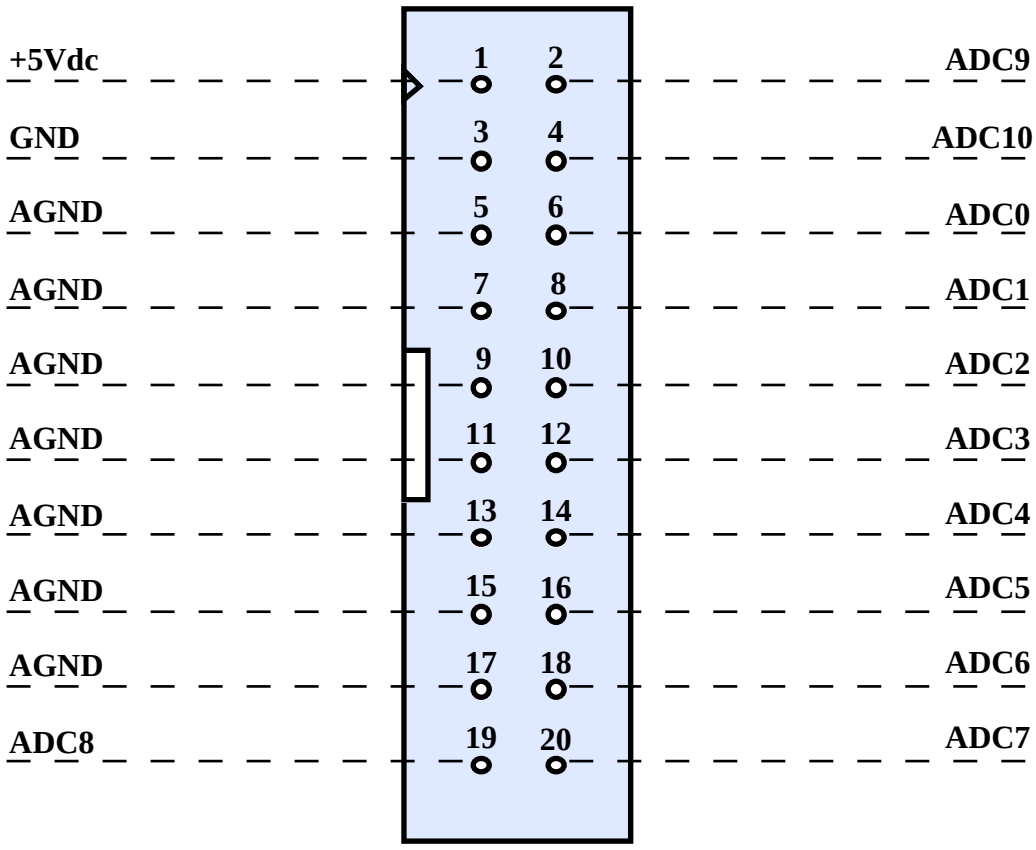


FIGURE 10: CN6 - A/D CONVERTER INPUT CONNECTOR

Signals description:

ADCn	=	I	-	A/D converter n-th channel analog input
GND	=		-	Digital ground signal
AGND	=		-	Analog ground signal
+5 Vdc	=	O	-	+5 Vdc signal

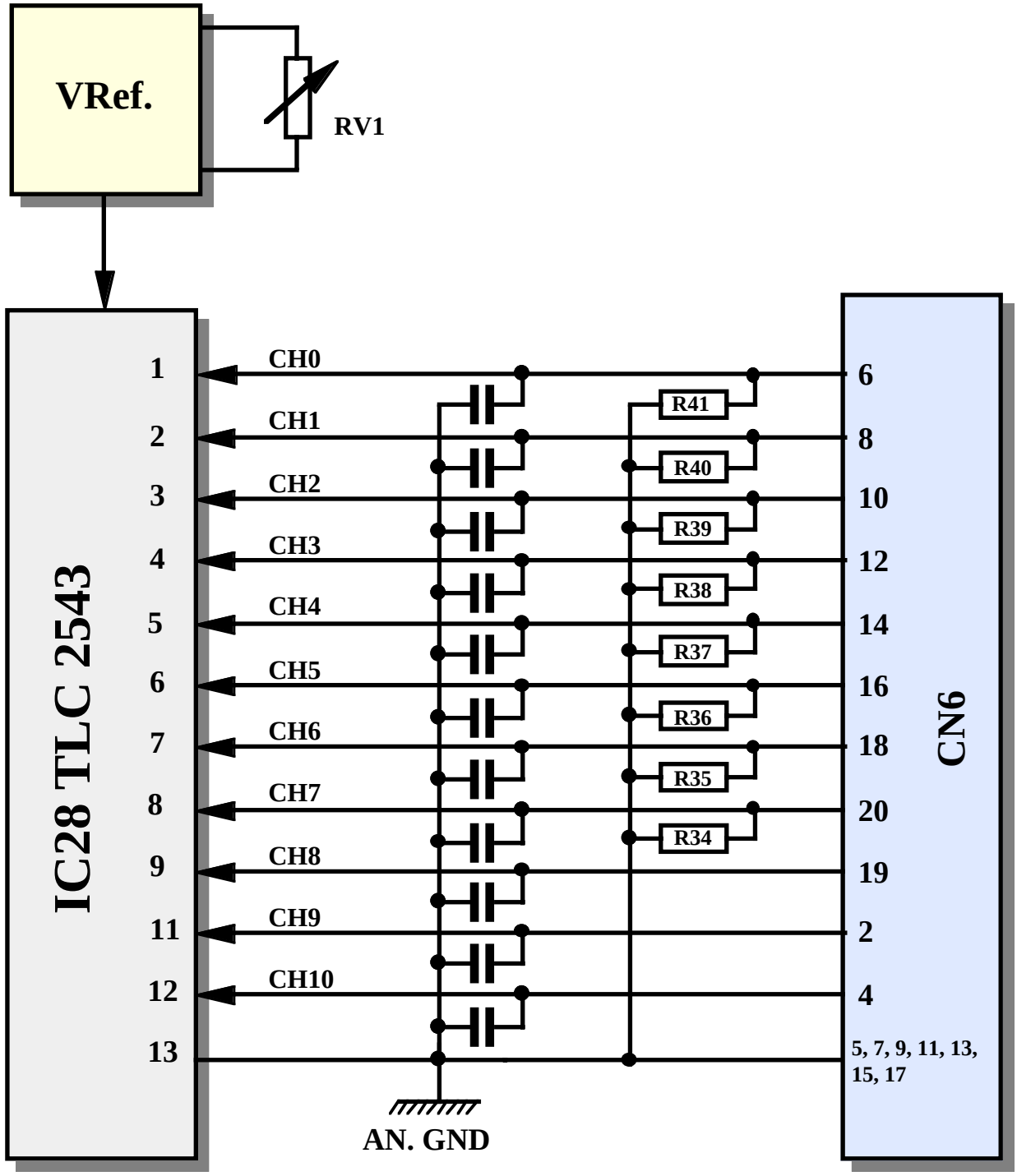


FIGURE 11: A/D CONVERTER INPUT BLOCK DIAGRAM

CN1 - ABACO® I/O BUS CONNECTOR

CN1 is a 26 pins, male, vertical, low profile connector with 2.54mm pitch.
Through CN1 the card can be connected to some of the numerous **grifo®** boards,both intelligent and not. All this connector signals are at TTL level.

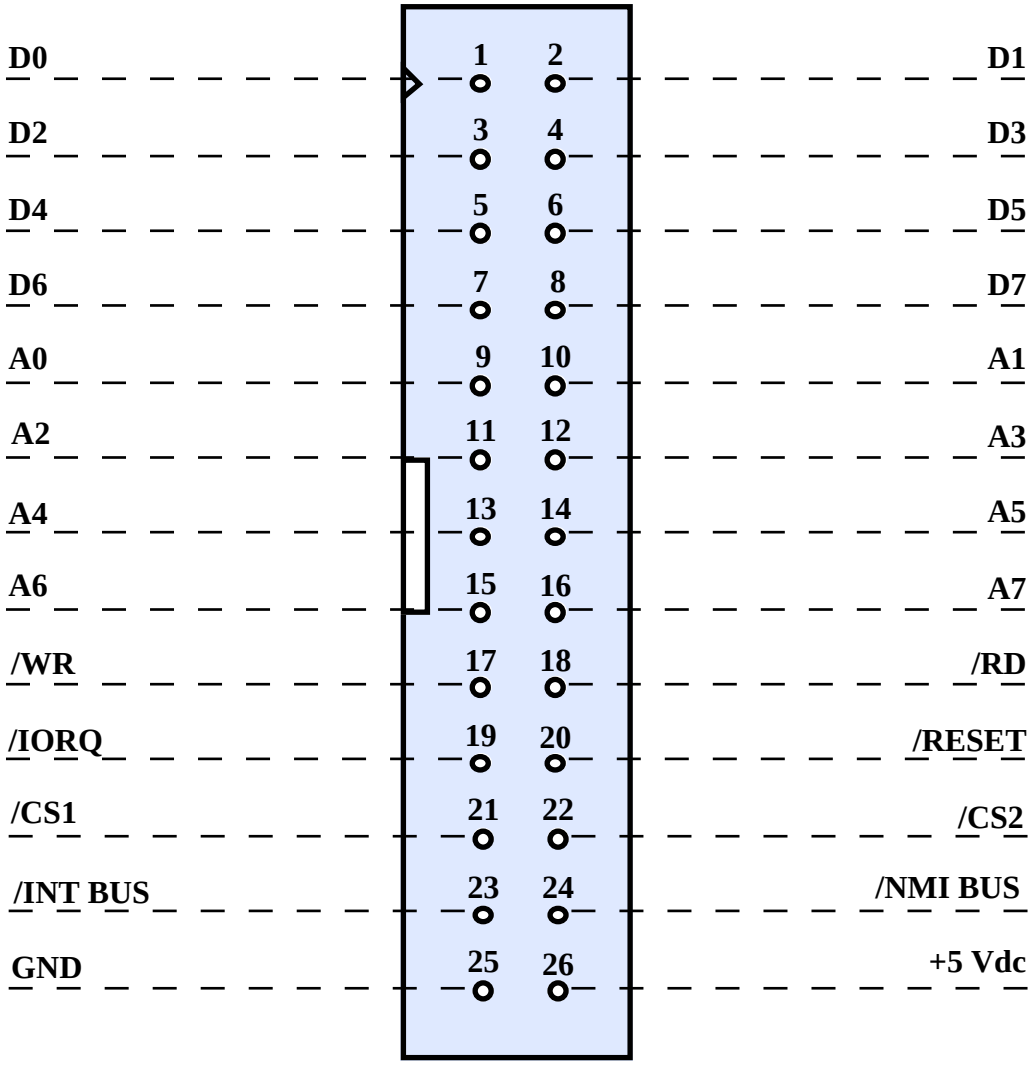


FIGURE 12: CN1 - ABACO® I/O BUS CONNECTOR

Signals description:

A0-A7	=	O	- Address BUS.
D0-D7	=	I/O	- Data BUS.
/INT BUS	=	I	- Interrupt request (open collector type).
/NMI BUS	=	I	- Non maskable interrupt.
/IORQ	=	O	- Input output request.
/RD	=	O	- Read cycle status.
/WR	=	O	- Write cycle status.
/RESET	=	O	- Reset.
/CS1, /CS1	=	O	- Chip select 1 and 2: external devices decoded enable
PFI	=	I	- Power Failure input
+5 Vdc	=	I	- +5 Vdc power supply.
GND	=		- Ground signal.

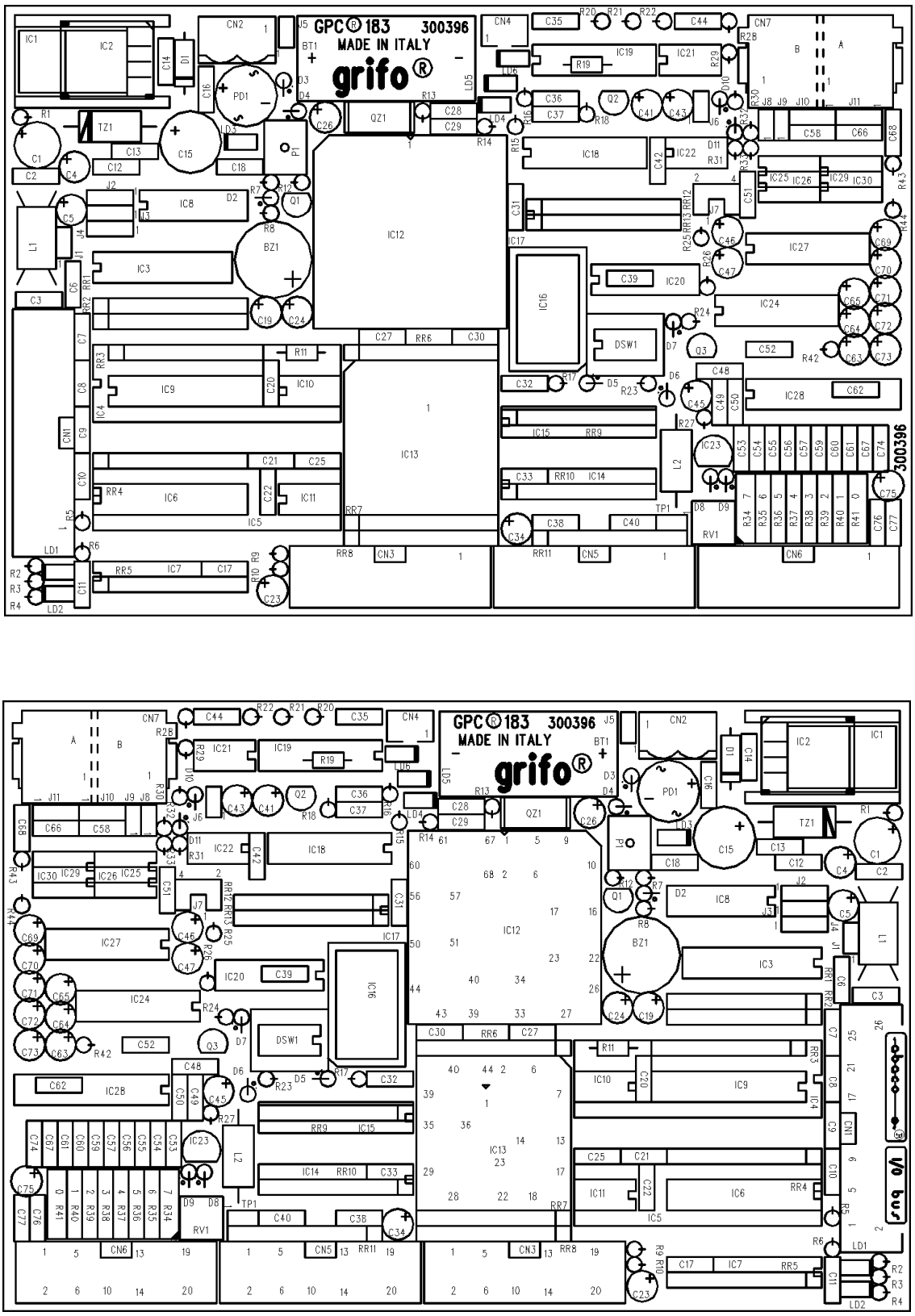


FIGURE 13: COMPONENTS MAP (COMPONENTS AND SOLDER SIDE)

CN7B - SERIAL LINE B CONNECTOR

CN7B is a 6 pins, female PLUG connector.
On CN7B are available the buffered signals for RS 232, RS 422, RS 485, current loop serial line B that is phisically connected to the hardware ASCI 0 of the microprocessor. The electric protocol follows the CCITT normative and all the signals are placed in order to reduce interference and electrical noise and in order to simplify connection with other systems.

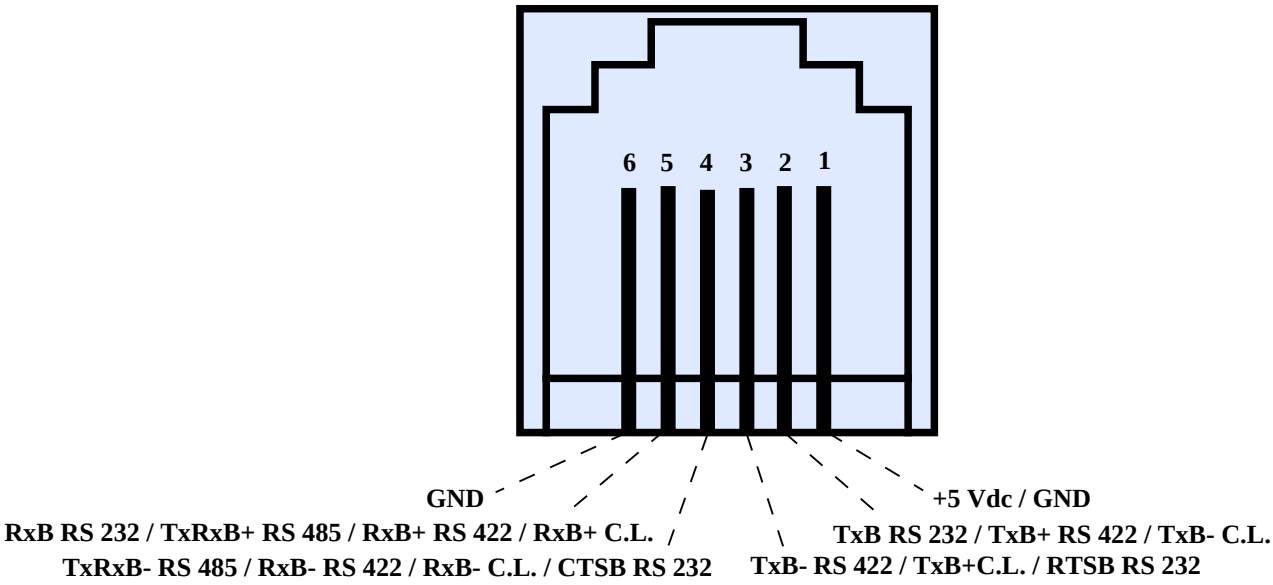


FIGURE 14: CN7B - SERIAL LINE B CONNECTOR

Signals description:

RxB RS 232 = I - Serial line B RS 232 Receive Data.
TxB RS 232 = O - Serial line B RS 232 Transmit Data.
RxB- RS 422 = I - Receive Data Negative: Serial line B negative signal for RS 422 serial differential receive.
RxB+ RS 422 = I - Receive Data Positive: Serial line B positive signal for RS 422 serial differential receive.
TxB- RS 422 = O - Transmit Data Negative: Serial line B negative signal for RS 422 serial differential transmit.
TxB+ RS 422 = O - Transmit Data Positive: Serial line B positive signal for RS 422 serial differential transmit.
RxTxB- RS 485 =I/O- Receive Transmit Data Negative: Serial line B negative signal for RS 485 serial differential receive and transmit.
RxTxB+ RS 485 =I/O- Receive Transmit Data Positive: Serial line B positive signal for RS 485 serial differential receive and transmit.
RXB- C.L. = I - Receive Data Negative: Serial line B negative signal for Current Loop serial bipolar receive.
RXB+ C.L. = I - Receive Data Positive: Serial line B positive signal for Current Loop serial bipolar receive.
TXB- C.L. = O - Transmit Data Negative: Serial line B negative signal for Current Loop serial bipolar transmit.
TXB+ C.L. = O - Transmit Data Positive: Serial line B positive signal for Current Loop serial bipolar transmit.

+5 Vdc = O - +5 Vdc or ground signal.
GND = - Ground signal.

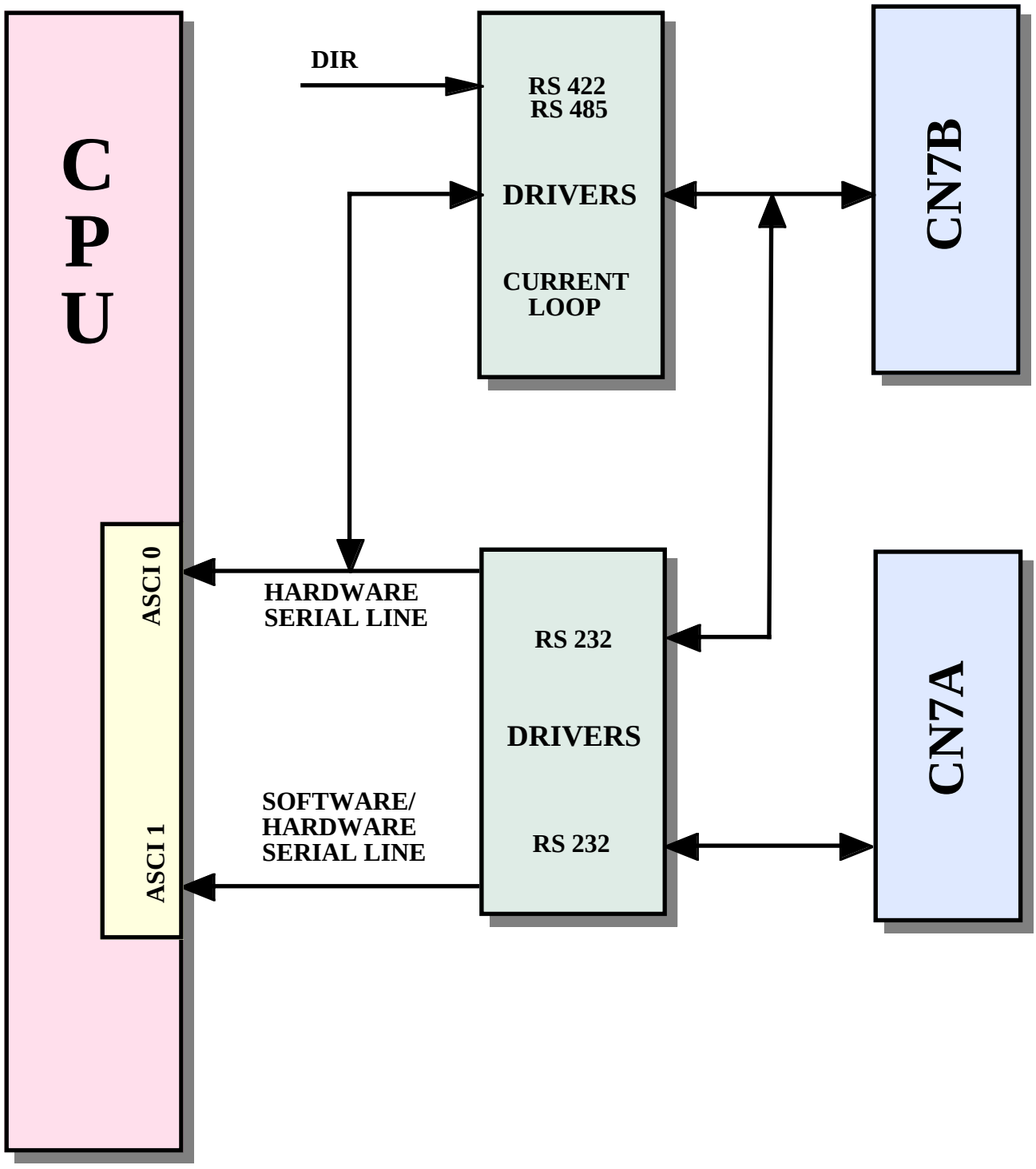


FIGURE 15: SERIAL COMMUNICATION DIAGRAM

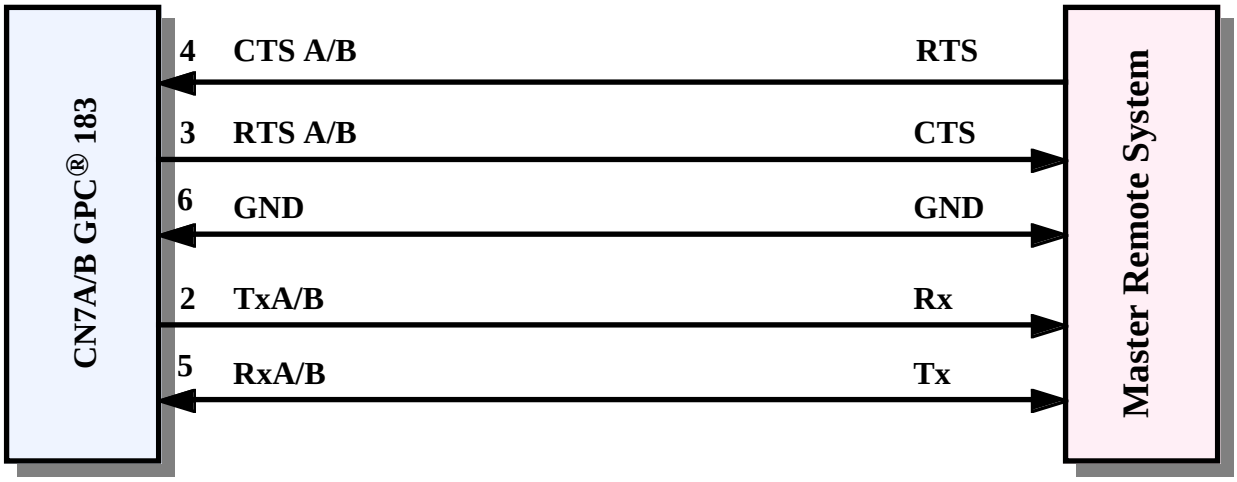


FIGURE 16: RS 232 POINT TO POINT CONNECTION EXAMPLE

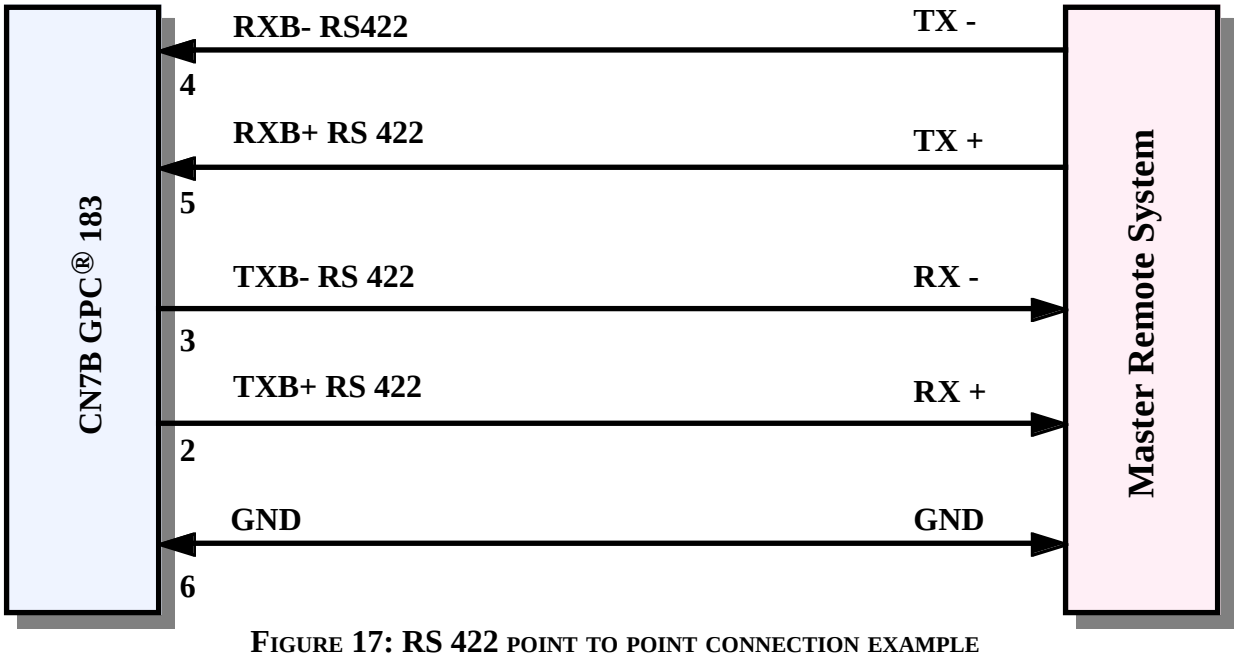


FIGURE 17: RS 422 POINT TO POINT CONNECTION EXAMPLE

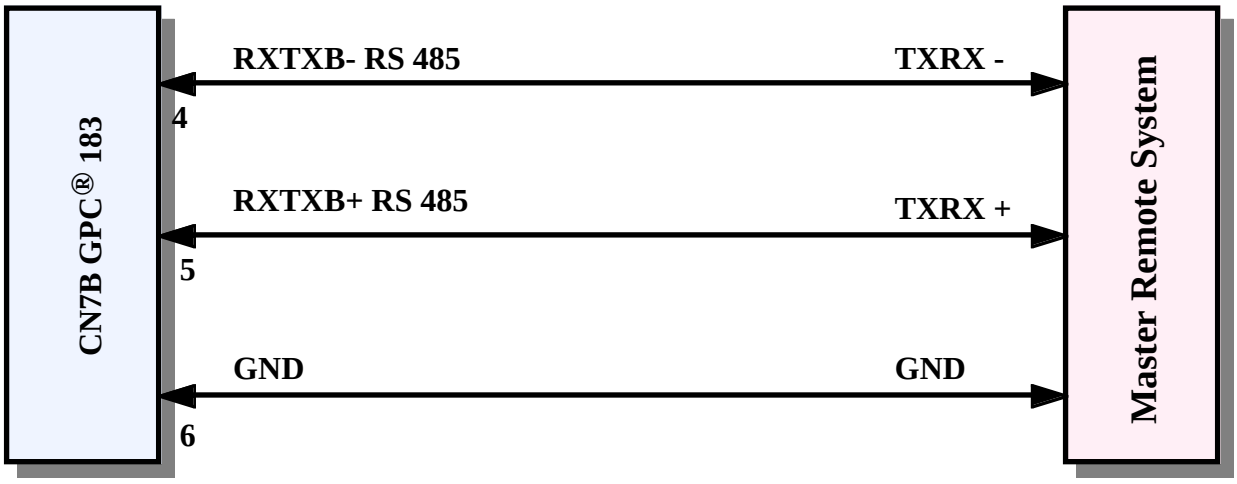


FIGURE 18: RS 485 POINT TO POINT CONNECTION EXAMPLE

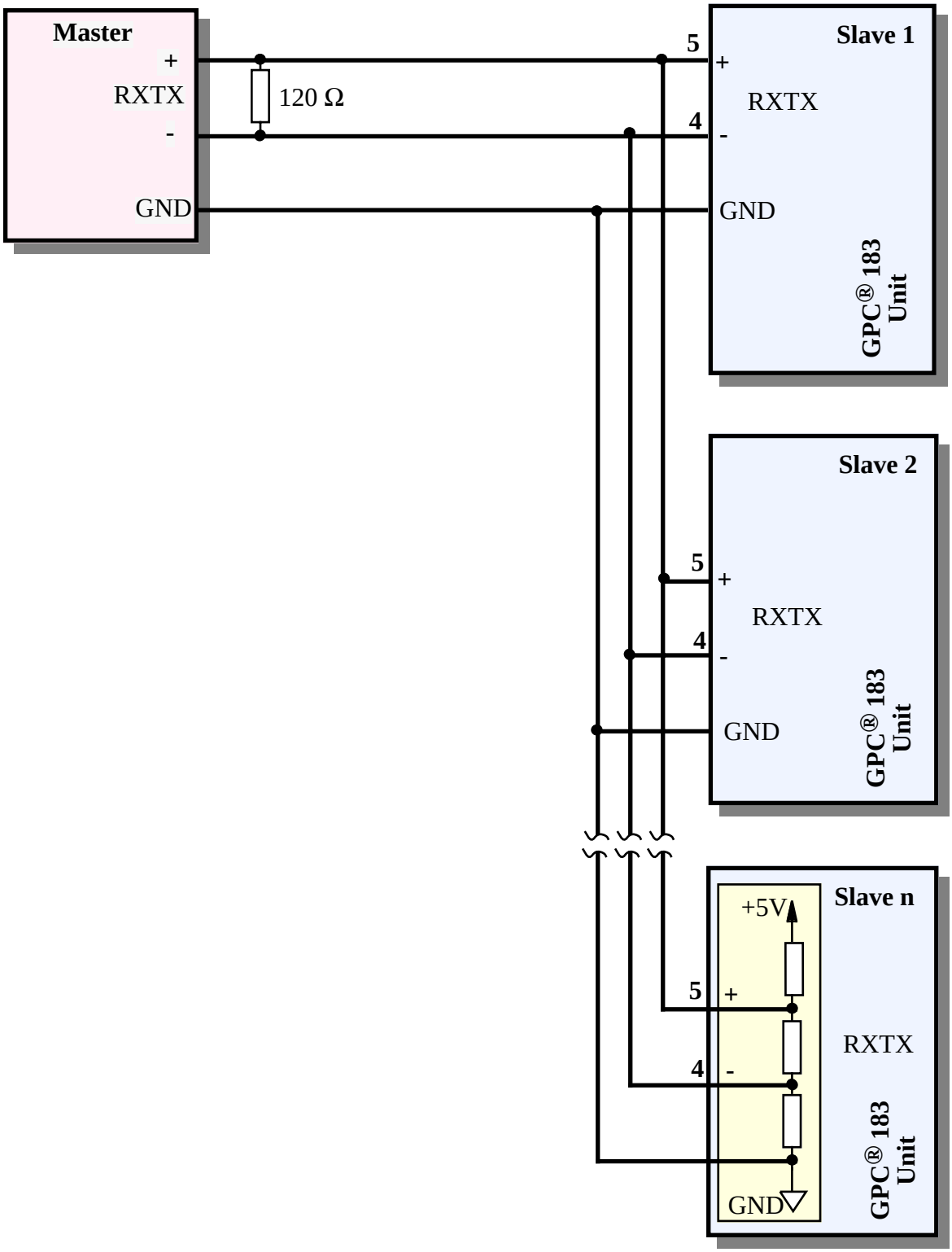


FIGURE 19: RS 485 NETWORK CONNECTION EXAMPLE

Please remark that in a RS 485 network two forcing resistors must be connected across the net and two termination resistors (120 Ω)must be placed at its extrems, respectevely near the Master unit and the Slave unit at the greatest distance from the Master.
Forcing and terminating circuitry is installed on **GPC® 183** board. It can be enabled or disabled through specific jumers, as explained later.
For further informations please refr to TEXAS INSTRUMENTS Data-Book , "*RS 422 and RS 485 Interface Cicuits*", the introduction about RS 422-485.

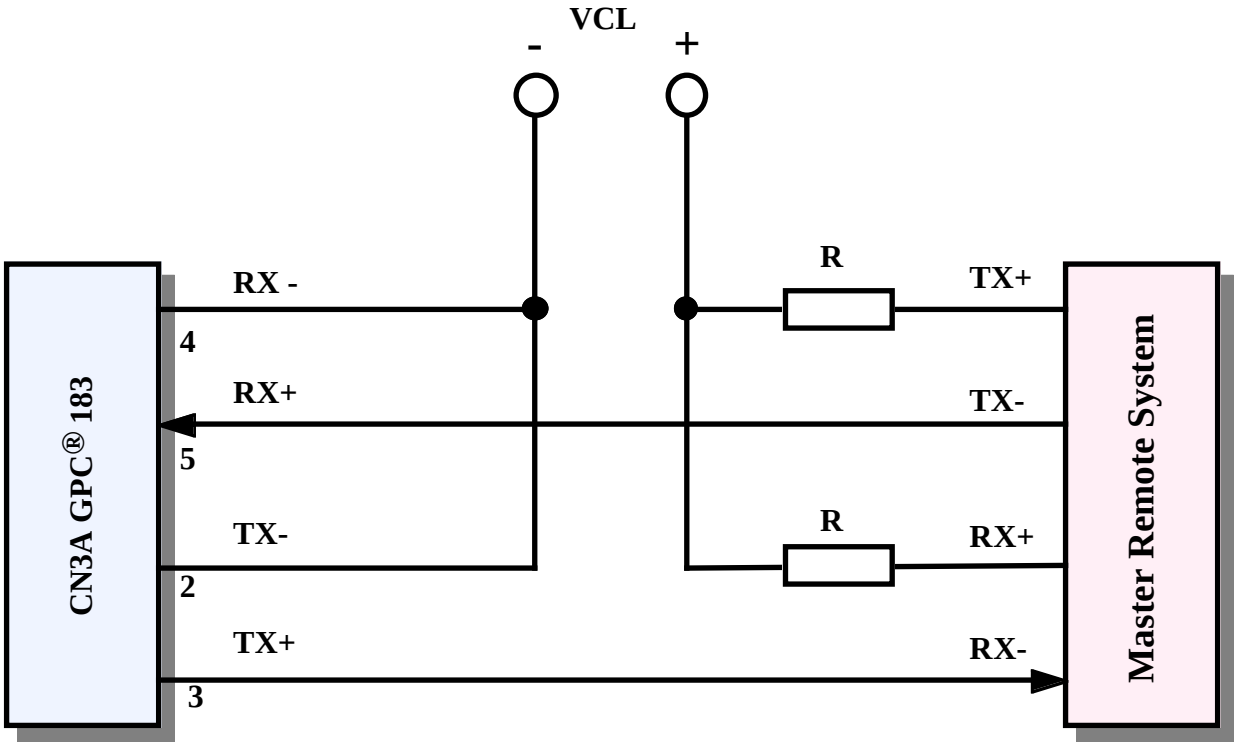


FIGURE 20: 4 WIRES CURRENT LOOP POINT TO POINT CONNECTION EXAMPLE

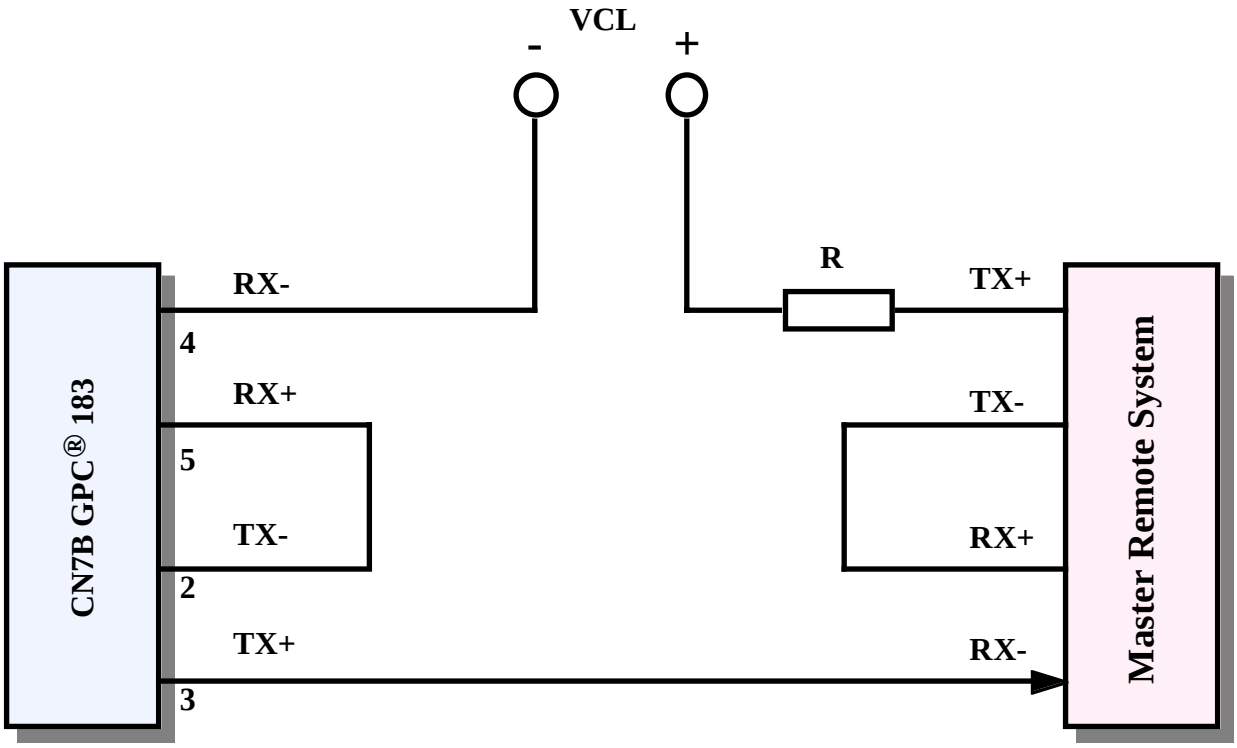


FIGURE 21: 2 WIRES CURRENT LOOP POINT TO POINT CONNECTION EXAMPLE

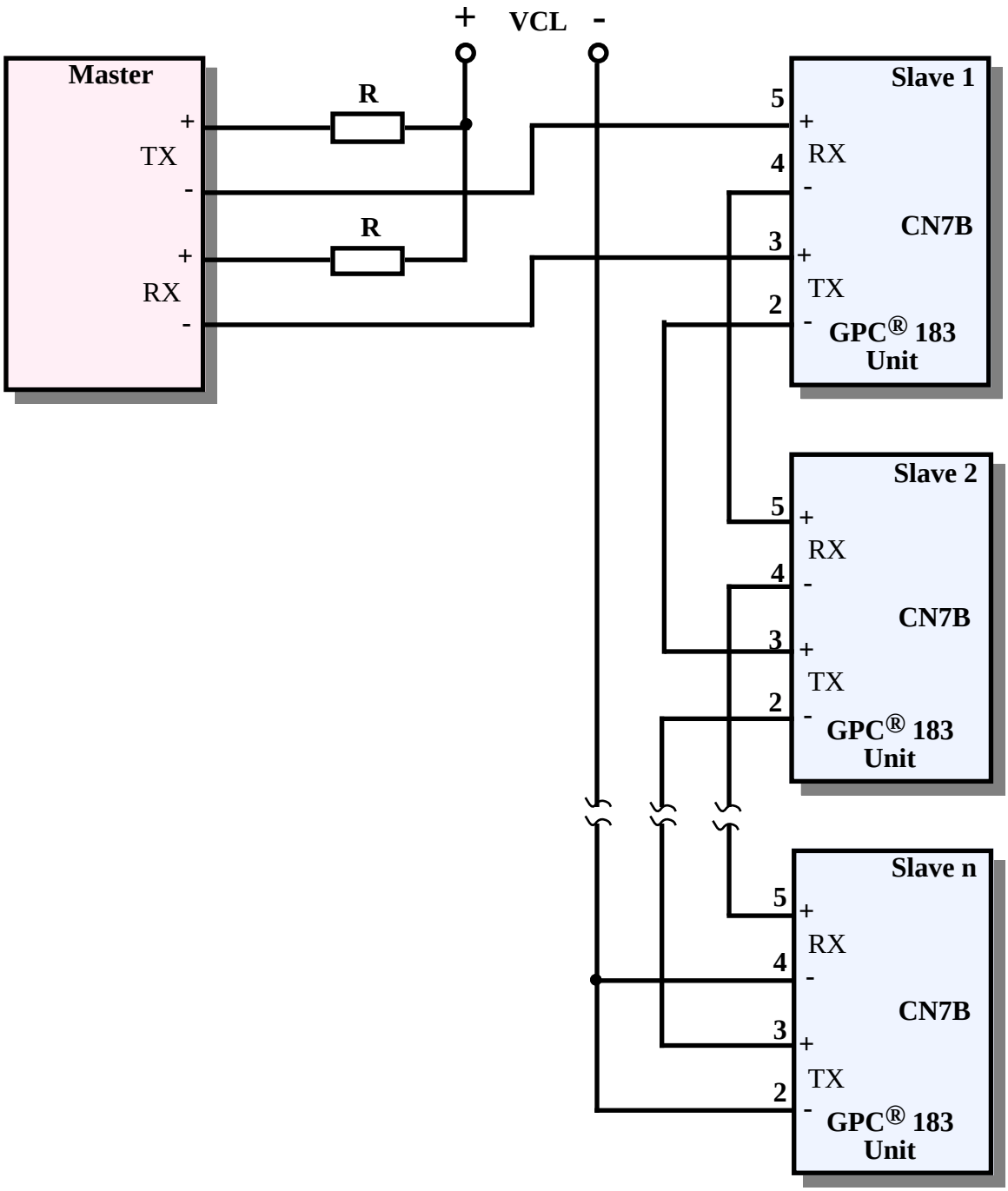


FIGURE 22: CURRENT LOOP NETWORK CONNECTION EXAMPLE

Possible passive current loop connections are two: 2 wires and 4 wires. These connections are shown in figures 16÷18 where it is possible to see the voltage for **VCL** and the resistances for current limitation (**R**). The supply voltage varies in compliance with the number of connected devices and voltage drop on the connection cable.
The choice of the values for these components must be done cosidering that:
- circulation of a **20 mA** current must be guaranteed;
- potential drop on each transmitter is about **2.35 V** with a 20 mA current;
- potential drop on each receiver is about **2.52 V** cwith a 20 mA current;
- in case of shortciruit each transmitter must dissipate at most **125 mW**;
- in case of shortciruit each receiver must dissipate at most **90 mW**.

For further info please refer to HEWLETT-PACKARD Data Book, (**HCPL 4100** and **4200** devices).

CN7A - SERIAL LINE A CONNECTOR

CN7A is a 6 pins, female PLUG connector for serial communication. Phisically, serial line A of **GPC® 183** board is connected to the ASCI 1 serial line of the CPU.
Placing of the signal has been designed to reduce interference and electrical noise and to simplify connections with other systems, while the electric protocol follows the CCITT normative.

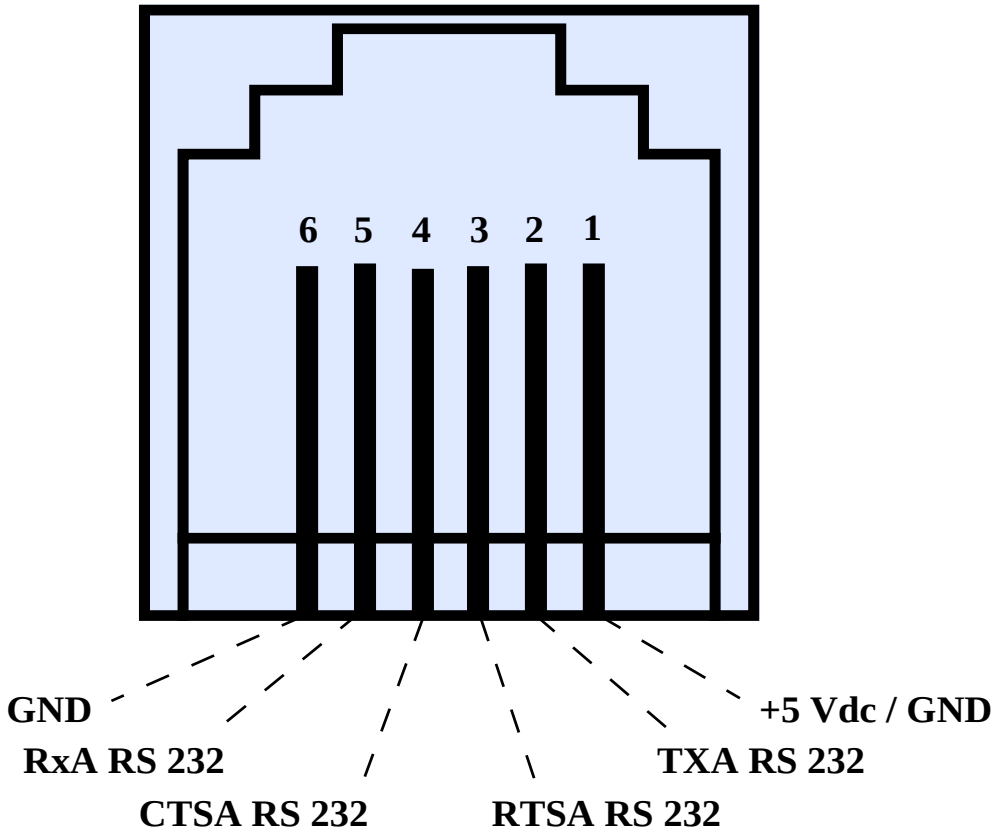


FIGURE 23: CN7A- SERIAL LINE A CONNECTOR

Signals description:

RxA RS 232	=	I	-	Serial line A=ASCI1 RS 232 Receive Data.
TxA RS 232	=	O	-	Serial line A=ASCI1 RS 232 Transmit Data.
CTSA RS 232	=	I	-	Serial line A=ASCI1 RS 232 Clear To Send.
RTSA RS 232	=	O	-	Serial line A=ASCI1 RS 232 Request To Send.
+5 Vdc/GND	=		-	+5 Vdc power supply or ground signal
GND	=			Ground signal

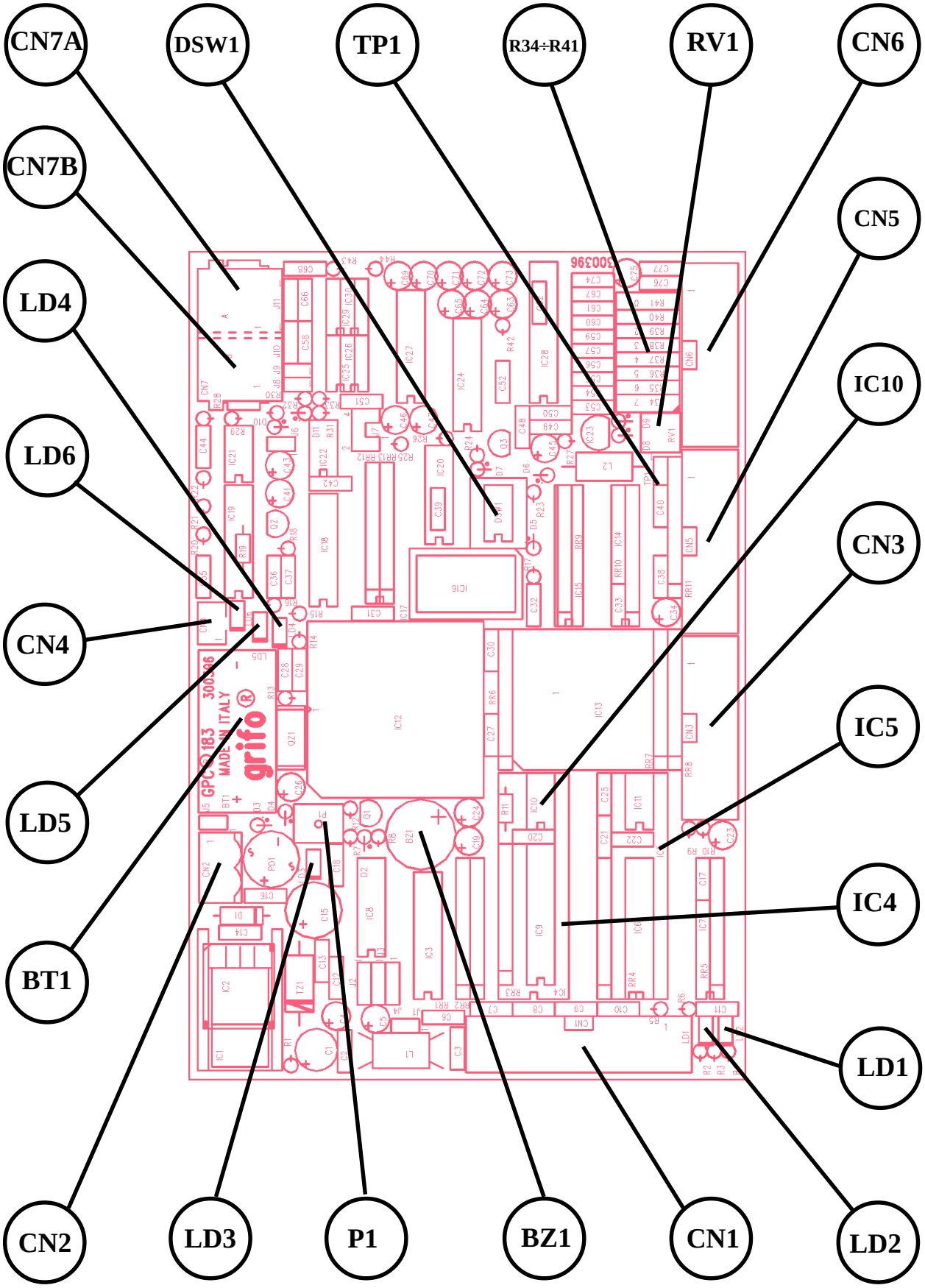


FIGURE 24: LEDS, DIP SWITCH, CONNECTORS, ETC. LOCATION

DIGITAL I/O INTERFACES

Through CN3 (**ABACO**® I/O BUS standard connector) the **GPC® 183** card can be connected to all the numerous **grifo®** boards featuring the same standard pin out. Installation of these modules is very easy; in fact only a 20 pins flat cable (code FLT20+20) that carries also power supply is required, while the software management of these interfaces is as easy and immediate; in fact most of the software packages available for **GPC® 183** card are provided with the necessary procedures. These latter are software driver for almost all the languages, and allow to use operator interfaces through the whole power of high level instructions.
Remarkable interfaces are:

- **QTP 16P, QTP 24P**, **KDL x24**, **KDF 224**, **DEB 01**, etc. that solve all the local operator interfacing problems. These modules are provided with all the resources needed to obtain a high level human machine interface (they feature alphanumeric displays, matrix keyboard and visualization LEDs) at a short distance from **GPC® 183** card. The available software drivers allow to manage the operator interface resources directly through the high level instructions for console management.

- **IAC 01**, **DEB 01**: it is an interface for CENTRONICS parallel printer that can be connected with a standard printer cable. About software the developed drivers provide procedures to read and write data at a specified address, for the selected programming language.

- **MCI 64**: it a large mass memory support that can directly manage the PCMCIA memory cards RAM, FLASH, ROM, etc.) in their available sizes. About software the developed drivers provide a complete file system interfacing allowing to access the informations stored in the memory card directly through the high level file management instructions.

- **RBO xx**, **TBO xx**, **XBI xx**, **OBI xx**: these are buffer interfaces for I/O TTL signals. With these modules the TTL input signals are converted in NPN or PNP optoisolated inputs and the TTL output signals are converted in relays or transistor optoisolated outputs. Some of the above mentioned interfaces can be connected directly to CN7.

For more information refer to "EXTERNAL CARDS" chapter and the software tools documentation.

I/O CONNECTION

To prevent possible connecting problems between **GPC® 183** and the external systems, the user has to read carefully the information of the previous paragraphs and he must follow these instrunctions:

- For RS 232, RS 422, RS 485 and current loop communication signals the user must follow the standard rules of these protocols.
- For all TTL signals the user must follow the rules of this electric standard. The connected digital signal must be always referred to card digital ground (GND). For TTL signals, the 0 Vdc level corresponds to logic state "0", while 5Vdc level corrisponds to logic state "1".
- The analog inputs (A/D section) must be connected to low impedance signals in the following ranges: 0÷2,490 V or 0÷20 mA according to selected voltage reference (Vref). Remember that the eleven analog inputs available on CN6 are provided of filter capacitors that ensure an higher stability of the acquired signals, but reduce at the same time the bandwith frequency. For further information please refer to the paragraph “TYPE OF ANALOG INPUT SELECTION”.

RESET KEY

P1 reset key of the **GPC® 183** board allows the user to reset the board and restarting it in a general clearing condition. After pressing and releasing P1 the board restarts its execution in EPROM or internal FLASH.
The main purpose of this key is to come out of infinite loop conditions, useful especially during debug and develop phases, or to ensure a particular initial status. Please see figure 24 for an easy localization of this contact.

TYPE OF ANALOG INPUT SELECTION

GPC® 183 board can accept analog voltage and/or current inputs, as described in the previous paragraphs and chapters. The input type selection can be made only for 8 out of 11 input analog channels during the order phase and is performed mounting a specific voltage-current conversion module made by precision resistors (code **.8420**). In detail:

R41	->	channel 0
R40	->	channel 1
R39	->	channel 2
R38	->	channel 3
R37	->	channel 4
R36	->	channel 5
R35	->	channel 6
R34	->	channel 7

Should the voltage-current conversion module not to be mounted (default case) the corresponding channel accepts a voltage input signal in the range 0÷2.49 Vdc; otherwise a current input signal is accepted.
The value of the above mentioned resistors is obtained by the following spread;

R = 2.49 V / Imax

Usually the voltage-current conversion modules are made using 124 Ω precision resistors, corresponding to 4÷20 mA or 0÷20 mA.
To easily locate the voltage-current conversion module please refer to figures 11 and 24.

TEST POINT

The board is provided with a test point called TP1, that allows to read, through a galvanically isolated multimeter, the A/D converter reference voltage which is calibrated in laboratory.
TP1 is made of two contacts:

pin 1	->	Vref
pin 2	->	GND

To easily locate the test point contacts please refer to figure 24, while for further informations about Vref signal please refer to the paragraph “TRIMMER AND CALIBRATION”.

TRIMMERS AND CALIBRATION

On **GPC® 183** is available a trimmer, named **RV1**, that calibrates the Vref voltage of the optional A/D converter (code **.AD**) section. The **GPC® 183** is subjected to a careful test that verifies and calibrates all the card sections. To easily locate the trimmer, please refer to figure 24. The calibration is executed in laboratory, with a conntrolled +20 C° room temperature, following these steps:

-The A/D voltage reference (Vref) is calibrated through RV1 trimmer, by using a 5 digits precision multimeter, to a value of +2,4900 Vdc, measured on test point TP1.

- The corrispondance between the analog input signal and the combination read from A/D is verified. This check is performed with a reference signal connected to A/D inputs and testing that the A/D combination and the theoric combination differ at maximum of the A/D section errors sum.

- The trimmer is blocked with paint.

The analog interfaces use high precision components that are selected during mounting phase to avoid complicate and long calibration procedures. After the calibration, the on board trimmer is blocked with paint to mantain calibration also in presence of mechanic stresses (vibrations, movings, delivery, etc.).
The user must not modify the card calibration, but if thermic drifts,time drifts and so on, make necessary a new calibration, the user must strictly follow the previous described procedure.

VISUAL SIGNALATIONS

GPC® 183 board is provided with six LEDs in order to signal to the User some internal status conditions, as described in the following table:

LEDs	COLOUR	PURPOSE
LD1	Green	Software managed activity LED.
LD2	Red	When lit, indicates the RTC generated interrupt line activation (/INT2 of CPU).
LD3	Red	When lit, indicates the presence of +5 Vdc power supply.
LD4	Red	When lit, indicates the CPU /HALT signal activation.
LD5	Red	When lit, indicates the activation of external watch dog circuitery.
LD6	Green	Software managed timed activity LED (spot).

FIGURE 25: VISUAL SIGNALATIONS TABLE

The main purpose of this LEDs is to provide the User a visual indication of the board status, making easier the operations to verify the correct workig of the system. To easily locate the LEDs on the board please see figure 24.

JUMPERS

On **GPC® 183** there are 11 jumpers for card configuration. Connecting these jumpers, the user can define for example the memory type and size, the peripheral devices functionality and so on. Below there is the jumpers list, location and function.

JUMPER	N. PINS	PURPOSE
J1	2	Connects pins 26 of CN1 to on board +5 Vdc power supply.
J2	3	Selects size of memory device on IC4.
J3	3	Selects kind of memory device on IC5.
J4	3	Selects kind of memory device on IC5.
J5	2	Connects on board battery BT1 to back up circuitery.
J6	2	Connects external watch dog circuitery.
J7	5	Selects communication type for serial line B between RS 422 and RS 485.
J8	2	Connects forcing and termination resistors to RS 422, RS 485 reception line.
J9	2	Connects forcing and termination resistors to RS 422, RS 485 reception line.
J10	3	Selects the kind of connection for pin 1 of CN7B.
J11	3	Selects the kind of connection for pin 1 of CN7A.

FIGURE 26: JUMPERS SUMMARIZING TABLE

The following tables describe all the right connections of **GPC® 183** jumpers with their relative functions. To recognize these valid connections, please refer to the board printed diagram (serigraph) or to figure 13 of this manual, where the pins numeration is listed; for recognizing jumpers location, please refer to figure 30. The "*" used in the following tables, denotes the default connection, or on the other hand the connection set up at the end of testing phase, that is the configuration the user receives.

5 PINS JUMPERS

JUMPERS	CONNECTION	PURPOSE	DEF.
J7	position 1-2 and 3-4	Enables RS 485 serial communication (2 wires half duplex) on line B.	
	position 2-3 and 4-5	Enables RS 422 serial communication (4 wires full or half duplex) on line B.	*

FIGURE 27: 5 PINS JUMPERS LOCATION

2 PINS JUMPERS

JUMPERS	CONNECTION	PURPOSE	DEF.
J1	not connected	Does not connect pin 26 of CN1 to on board +5 Vdc power supply.	
	connected	Connects pin 26 of CN1 to on board +5 Vdc power supply.	*
J5	not connected	Does not connect on board battery BT1 to back up circuitery.	*
	connected	Connects on board battery BT1 to back up circuitery.	
J6	not connected	Does not connect external watch dog circuitery to reset circuitery.	*
	connected	Connect external watch dog circuitery to reset circuitery.	
J8, J9	not connected	Do not connect forcing and terminating circuitery to RS 422, RS 485 serial line B.	*
	connected	Connect forcing and terminating circuitery to RS 422, RS 485 serial line B.	

FIGURE 28: 2 PINS JUMPERS TABLE

3 PINS JUMPERS

JUMPERS	CONNECTION	PURPOSE	DEF.
J2	position 1-2	Sets IC4 for 128K Byte SRAM.	*
	position 2-3	Sets IC4 for 512K Byte SRAM.	
J3	position 1-2	Matching with J4, sets IC5 for EPROM.	*
	position 2-3	Matching with J4, sets IC5 for FLASH EPROM.	
J4	position 1-2	Matching with J3, sets IC5 for EPROM.	*
	position 2-3	Matching with J3, sets IC5 for FLASH EPROM.	
J10	position 1-2	Connects pin 1 of CN6B to GND.	*
	position 2-3	Connects pin 1 of CN6B to +5 Vdc.	
J11	position 1-2	Connects pin 1 of CN6A to GND.	*
	position 2-3	Connects pin 1 of CN6A to +5 Vdc.	

FIGURE 29: 3 PINS JUMPERS TABLE

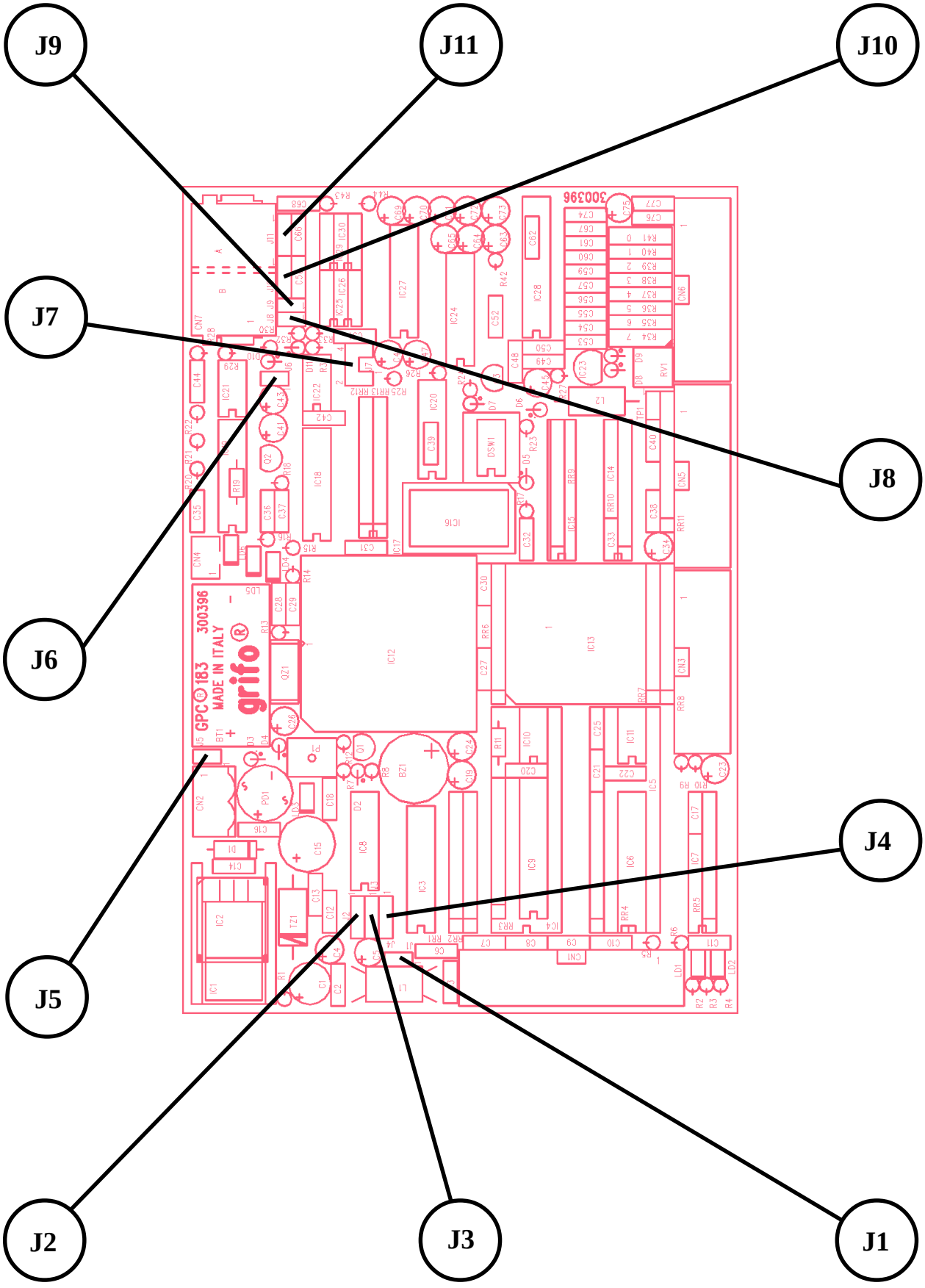


FIGURE 30: JUMPERS LOCATION

BACK UP

GPC® 183 has an on board lithium battery BT1 for the back up of SRAM and RTC content when power supply is switched off. Jumper J5 connects phisically the battery so it can be disconnected to save its duration whenever back-up is not needed. By CN4 connector it is possible to connect an external battery: configuration of jumper J5 does not affect the working of this battery and it can replace BT1 completely.
Please refer to the paragraph "ELECTRIC FEATURES" to choose the type of the external back up battery, to easily locate see figure 24.

MEMORY SELECTION

On **GPC® 183** can be mounted up to 1032K bytes of memory divided in several configurations, as described in the following table:

IC	DEVICE	SIZE	CONNECTION
5	EPROM	128K Byte	J3 and J4 in position 1-2
	EPROM	256K Byte	J3 and J4 in position 1-2
	EPROM	512K Byte	J3 and J4 in position 1-2
	FLASH EPROM	128K Byte	J3 and J4 in position 2-3
	FLASH EPROM	512K Byte	J3 and J4 in position 2-3
4	SRAM	128K Byte	J2 in position 1-2
	SRAM	512K Byte	J2 in position 2-3
10	EEPROM	256÷8K Byte	-

FIGURE 31: MEMORY SELECTION TABLE

All the above mentioned devices must follow the JEDEC pin out specifications. For further information about the signatures of the component that can be mounted please refer to the manifacturers documentations. To easily locate the memory devices please refer to figure 24.
The default configuration of the **GPC® 183** board memory is only 128K SRAM; any different memory configuration can be realized by the user by mounting the opportune devices or can be requested in the ordering phase. Here follow the codes to order the optional memoy configurations:

.512	->	512K SRAM
.EE08	->	8K bit (1024 byte) serial EEPROM
.EE16	->	16K bit (2048 byte) serial EEPROM
.EE64	->	64K bit (8192 byte) serial EEPROM

For further information about prices and options please contact **grifo®**.

INTERRUPTS

One of the most important **GPC® 183** features is the powerful interrupts management. Here is a short description of how the board's hardware interrupt signals can be managed; a more complete description of the hardware interrupts can be found in the microprocessor data sheets or in Appendix A of this manual.

- **ABACO®** I/O BUS	->	It generates an /NMI interrupt, by the /NMI BUS signal on CN1. It generates an /INT1 vectored interrupt, by /INT BUS signal on CN1.
- Real Time Clock	->	It generates an /INT2 vectored interrupt.
- CPU inside devices	->	They generate a vectored interrupt. Possible sources of internal interrupt events are: PRT 0, PRT 1, DMA 0, DMA 1, CSI/O, ASCI 0, ASCI 1.

The board features a chained priority structure that manages the case of contemporary interrupts. The addresses of the response procedures for vectored interrupts can be software programmed by the user acing on microprocessor inside registers. So the user program has always the possibility to react promptly to every external event, deciding also the priority of interrupts.

CONFIGURATION INPUTS

GPC® 183 board is provided with one 4 pins dip switch (DSW1), tipically used for system configuration purposes, that can be software acquired by the user program. The mostly implemented applications for this feature are: working conditions setting, selection of some on-board firmware parameters, etc. The status of switches generates a signal in complemented logic (0 -> switch ON, 1 -> switch OFF) that can be read performing a read operation atthe address assigned to the dip switch by the on board control logic. Some software tools use switch 4 for the selection between the RUN and DEBUG working modalities. For further information please refer to the paragraph “I/O ADDRESSES”, while to easily locate the jumper on the board please refer to figure 24.

RESET AND WATCH DOG

The watch dog circuit of **GPC® 183** is really efficient and provided of easy software management. In details the most important features of this circuit are:
- astable functionality;
- intervent time of about 1.5 sec;
- hardware enable;
- software retrigger;

With the astable mode when the intervent time elapses, the circuit becomes active, it stay active till the end of reset time then it is deactivated. Jumper J6 connects the watch dog circuit to reset circuit so when it is connected the watch dog is enabled and viceversa. The watch dog retrigger operation is described in chapter "WATCH DOG".
After an activation and following deactivation of /RESET signal, the card resumes execution of the program saved on IC5 (at address 0000H) starting from a global reset status of all the on board peripheral devices.
Please remember that the /RESET signal is connected to CN1 connector and that on **GPC® 183** are available other reset sources as the contact P1.

POWER SUPPLY VOLTAGES

GPC® 183 board is provided with and efficent circuitry that solves in an efficent and comfortable way the problem of power supply in any employ condition. Here follows the list of the possible configurations for power supply section:

- *No power supply section (default):*
  The board must be supplied by a +5 Vdc voltage provided directly on the specific pins of CN1 (**+5 Vdc** on pin 26, **GND** on pin 25).

- *Linear power supply section (option **.ALIM12**)*:
  The board must be supplied by a 6÷12 Vac altenate voltage, or the corresponding continuous voltage, that must be provided to pins 1 and 2 of CN2.

- *Switching power supply section (option **.SW**)*:
  The board must be supplied by a 8÷24 Vac alternate voltage, or the corresponding continuous voltage (12÷34 Vdc), that must be provided to pin 1 and 2 of CN2.

Regardless the type of supply section chosen, the **GPC® 183** board is always provided with an efficent protection circuitry that protects the board against voltage peaks or noise. Please remark that the desired supply section must be explicitally specified in the order; in fact the choice implies a different hardware configuration that must be performed by the **grifo®** technical pesonnel.
Jumper J1 connects positive pin (+5 Vdc) of on board supply to **ABACO®** I/O BUS connector so it must be disconnected only when a board provided with power supply section is connected to a system provided with its own power supply section.
To reduce the CPU consumption IDLE and STOP operating MODEs can be used. These modalities can be selected by programming specific CPU registers and activated executing the HALT instruction, while to restore the normal execution mode interrupt signals must be employed. For further information about this subject please refer to appendix A of this manual or CPU manufacturers documentation.
For further information please refer to paragraph “ELECTRIC FEATURES”.

SERIAL COMMUNICATION SELECTION

The communication serial line A is always buffered in RS 232 while the serial line B can be buffered in RS 232, RS 422, RS 485 or current loop electric standard. By hardware can be selected which one of these electric standard is used, through jumpers connection (as described in the previous tables). By software the serial lines can be programmed to operate with 7, 8 bits per character, parity, 1 or 2 stop bits at standard or no standard baud rates, through some CPU internal register setting.
Some components necessary for RS 422 and RS 485 communication are not mounted and not tested on the default configuration card, so the first not standard configuration must always be executed by **grifo®** technician; then the user can change himself/herself the configuration, following the below description:

- SERIAL LINE B=ASCI 0 CONFIGURED IN RS 232 (default configuration)

			IC27	=	MAX 202 driver
J7	=	not connected	IC25	=	no component
J8, J9	=	not connected	IC26	=	no component
			IC29	=	no component
			IC30	=	no component

- SERIAL LINE B=ASCI 0 CONFIGURED IN CURRENT LOOP (**.CLOOP** option)

			IC27	=	no component
J7	=	not connected	IC25	=	no component
J8, J9	=	not connected	IC26	=	HCPL 4100 driver
			IC29	=	no component
			IC30	=	HCPL 4200 driver

The current loop serial line is a passive line, so during connection the user must provide an external power supply, as described in figures 20, 21 and 22. The current loop interface allows either point to point or network connection with 4 or 2 wires.

- SERIAL LINE B=ASCI 0 CONFIGURED IN RS 422 (**.RS422** option)

			IC27	=	no component
J7	=	2-3, 4-5	IC25	=	SN 75176 or MAX483
J8, J9	=	(*1)	IC26	=	no component
			IC29	=	SN 75176 or MAX483
			IC30	=	no component

With /RTSB=/RTS0 signal (managed by software with ASCI 0 registers) the user enables or disables the transmitter driver:

/RTS0 = low level = 0 logic state -> transmitter driver enabled
/RTS0 = high level = 1 logic state -> transmitter driver disabled

allowing either point to point (driver can be mantained always enabled) or network (driver is enabled only when the unit can hold the line) connection.

- SERIAL LINE B=ASCI 0 CONFIGURED IN RS 485 (.RS485 option)

			IC27	=	no component
J7	=	1-2, 3-4	IC25	=	SN 75176 or MAX483
J8, J9	=	(*1)	IC26	=	no component
			IC29	=	no component
			IC30	=	no component

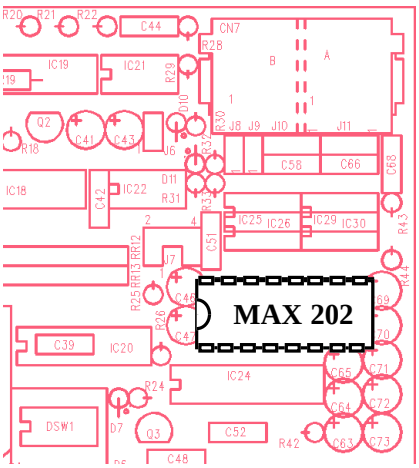
With /RTSB=/RTS0 signal (managed by software with ASCI 0 registers) the user defines the RS 485 line direction:

/RTS0 = low level	= 0 logic state	->	RS 485 line transmitting
/RTS0 = high level	= 1 logic state	->	RS 485 line receiving

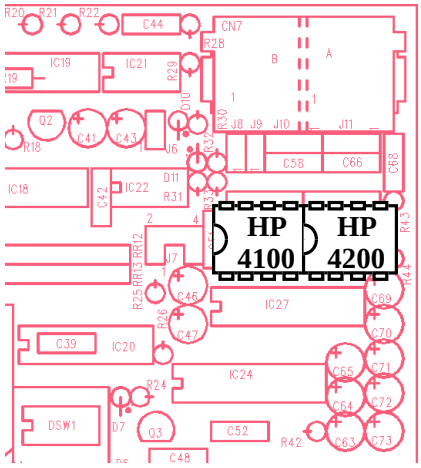
allowing network connection in a master multi slave system and multi master system. With RS 485 communication line, on CN7B the pins 4 and 5 have the double function of reception and transmission signals. All the transmitted characters are at the same time received when the user select RS 485 on **GPC® 183**; in this way the line conflicts can be immediately recognized by simply testing the received character after each transmission.

(*1) With jumper J8 and J9 the RS 422 receiving line or the RS 485 line can be terminated and forced with a suitable resistors circuit. The line termination must be added only at the beginning and at the end of the physical line, connecting both the jumpers. Normally these jumper must be connected in point to point network, or on the farther cards in multipoints network.

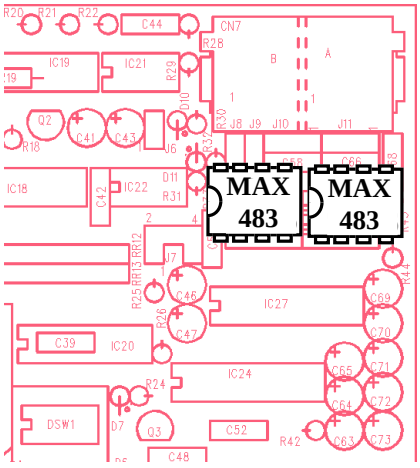
After reset or power on phase, the /RTS0 signal is forced to high level that mantain the RS 485 driver receiving and that disables the RS 422 transmitter driver; this condition eliminates any conflict on the communication line.



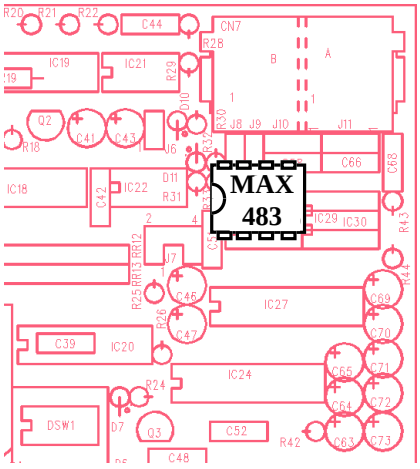
Serial B = ASCI 0 in RS 232



Serial B = ASCI 0 in current loop



Serial B = ASCI 0 in RS 422



Serial B = ASCI 0 in RS 485

FIGURE 32: SERIAL COMMUNICATION DRIVER LOCATION

SOFTWARE

A wide selection of software development tools can be obtained, allowing use of the module as a system for its own development, both in assembler and in other high level languages; in this way the User can easily develop all the requested application programs in a very short time. Generally all software packages available for the mounted microprocessor, or for the Z80 and Z180 family, can be used, i.e.:

GET 80
It is a complete program with Editor, Communication driver, and Mass Memory management for all Z80 family cards. This program, developed by **grifo®**, allows to operate in the best conditions when **GDOS**, **FGDOS** or **xGDOS MCI** software tools are used; **GET 80** is supplied when one of these tools is ordered and it is personalized with name and general data of the customer. A useful list of pull down menus and the possibility of using mouse, make program use very comfortable. **GET 80** program can be executed both on MS-DOS system and on **MACINTOSH** computers too, through SOFT-PC program. It is supplied on MS-DOS 3”1/2 floppy disk with the documentation on **GDOS 80** manual.

GDOS 183
It is a complete development Tool for **GPC® 184** card. It is supplied together with **GET 80** program to allow an easy and immediate use of this powerful development system. GDOS is divided in two different structures : the first one works on PC maintaining serial communication with the second one. The second structure is on EPROM, it works on board of the card and it is an efficient operating system that executes many low level functions and, at the same time, it allows high level language use. The combination of the said structures results in a complete machine, in fact the card uses PC resources (like floppy disk, hard disk, printer, keyboard, monitor, etc.) as its own peripheral devices. This resulting “virtual machine” performs operation in a transparent way for the User, so this latter can operate with the same modality of standard PC languages. It is really interesting the compatibility of **GDOS** with all CP/M program and languages; so, if the User has experience, knowledge or developed applications with CP/M, he can use immediately **GDOS**, without any changes.
Moreover, **GDOS** can manage all memory devices exceeding 64K Bytes as RAM disk and ROM disk. The on board RAM devices can directly be used performing data read and write operations with the confortable file formats.
This software tools is supplied on EPROM with MS-DOS **GET 80** floppy disk, some examples, utilities and the operating system documentation.

FGDOS 183
It is really similar to **GDOS**, but it can program and erase the on board **FLASH EPROM** with the application program developed from the User. In this way the external EPROM programmer is not necessary to store definitely the program and it is possible to modify or to add code directly on the installed machine, through a portable PC.
This software tools is supplied on **FLASH EPROM** with **MS-DOS GET 80** floppy disk, some examples, utilities and the operating system documentation.

xGDOS MCI 183
It is a version of **GDOS** or **FGDOS** sofware tools, capable of **PCMCIA** Memory Card management. Using **MCI 64** card, the GDOS operating system manages memory cards as RAM disk or ROM disk. All applications with data acquisition and data logging can be realized with high level languages that manage data on files, with a fast development time and without any software complication.
This software tool is supplied on **EPROM** or **FLASH EPROM** with **MS-DOS GET 80** floppy disk, some examples, utilities and the operating system documentation.

PASCAL 80
It is an efficient and complete **PASCAL Compiler** for **Z80** family cards, with features similar to Release 3.0 of Borland **Turbo PASCAL**. It must work together with any **GDOS** version and it can exceed the 64K memory limits of Z80 family microprocessors through **OVERLAY** modality. More than one application program can be saved in RAM and/or ROM disks and subsequently executed. The terminal emulation of **GET 80** program support the typical full screen PASCAL Editor, including the attributes management.
This program is supplied as **ROM DISK** file in **GDOS EPROM** or **FLASH EPROM** and on MS-DOS floppy disk with some example and manual.

HI TECH C 80
Professional C Cross Compiler of Hi-Tech Software Inc. This Compiler is terribly fast and it generates a small quantity of code. This result is due to advanced techniques in optimizing the generated code based on Artificial Intelligence techniques which allow to get a very compact and very fast code. The package includes: IDE, Compiler, Code optimizer, Assembler, Linker, Remote Debugger and so on. This tool is Full ANSI/ISO Standard and Full Library Source Code. Once the porting of the Remote-Debugger module is done, this tool allows the user the software debugging directly on the hardware that he is experimenting. This type of specilization of the **Remote Debugger** is available from now ant it is supplied with all **grifo®** CPU cards. This software package is on 3" 1/2 diskettes under MS-DOS format along with user manual. This version supports these following CPUs: Z80, Z180, 84C011, 84C11, 84C013, 80C13, 84C015, 84C15, 64180, NCS800, Z181, Z182.

DDS MICRO C: low cost ross compiler for C source program. It is a powerful software tool that includes editor, C compiler (integer), assembler, optimizer, linker, library, and remote debugger, in one easy to use integrated development environment. There are also included the library sources and many utilities programs.

NOICE: It is a PC hosted debugger consists of a target specific DOS program, NOICExxx.EXE, and a target resident monitor program. The two programs comunicate via RS 232. NOICE includes: source level debug; a disassembler; a file viewer; memory display and editing; a virtually unlimited number of breakpoints; hardware free single step; definition of symbols; the ability to record and play back files of commands; on line help.

RSD 183

This software tools is a **Remote Symbolic Debugger** with two operating mode. The first one is a monitor debugger modality with software emulation on P.C.; the second is a remote monitor debugger modality that execute code directly on the card. Trough serial communication the User can: down load an HEX file and associated symbol table, debug code in symbolic mode, execute code in step to step mode or in real time mode, set breakpoint, dump and modify memory and registers, etc. RSD software tool supports both **Z80** and **Z180** instrunction sets. Really interesting is the program execution management, in fact many hardware and software breakpoint are supported. **RSD** can be used together with assembler tools, like **ZASM 80**, and C Compiler **CC 80**.
It is supplied on EPROM and on MS-DOS floppy disk with technical manual.

ZASM 80

It is a macro cross assemler that operates on any PC with MS-DOS operating system. It supports both **Z80** and **Z180** instruction sets. The generated code can be debugged on PC, through software simulation, or directly on target card, through remote modality, using **RSD** software tools. ZASM 80 is compatible with C Compiler **CC 80** of which it assemble the compilation result.
It is supplied on MS-DOS floppy disk with technical manual.

CC 80

It is a complete **C Compiler** with ANSI/ISO standard, provided of floating point procedure, that can generate code for Z80 and Z180 family microprocessors. It works together with cross assembler **ZASM 80** and Symbolic Debugger **RSD**.
It is supplied on MS-DOS floppy disk with technical manual.

CBZ 80

Complete BASIC compiler, for CPU family Z80 and compatible, capable to generate a very compact and very fast code. It works only matched to any GDOS version. CBZ 80 allows to override the 64 KByte of addressing barries typical of family Z80. This can be done using the CHAIN technique provided by GDOS matched to the possibility to manage RAM disk and ROM disk provided by several **ABACO®** cards. Using it with the powerful editor included in GET80 allows to experiment a powerful work tool to create any application program in an extremly efficent and comfortable way. The program is provided in EPROM with GDOS operating system and in a floppy disk which included also the manual and a set of example programs.

DEVICES MAP AND ADDRESSES

INTRODUCTION

In this chapter are reported all informations about card use, related to hardware features of **GPC® 183**. For example the registers addresses, the memory and peripheral devices allocation are described below.

ON BOARD DEVICES ADDRESSES

The on board devices addresses are managed from a control logic, realized with CMOS gates. This control logic allocates memory and peripheral devices with very low power consumption and simple software management.
The control logic has been designed to control the memory and the I/O peripherals addresses in a separate manner. The Z8S180 microprocessor directly addresses in total 64K bytes of memory and 256 I/O registers and the control logic provides 1032K Byte on board memory and peripheral devices allocattion inside these addresses spaces. The maps management is completely driven by software through the MMU circuit programmation: the used memory can be selected and divided in some size definible segments. About I/O maps the control logic avoids every conflicts problems between CPU internal and external peripherals.
Summarizing the control logic allocates:

- **ABACO®** I/O BUS
- Up to 512K Byte of EPROM or FLASH EPROM on IC 5
- Up to 512K Byte of SRAM on IC 4
- Up to 8K Byte of serial EEPROM on IC 10
- A/D converter
- Configuration dip switch DSW1
- Buzzer
- Activity LEDs
- Watch dog circuitery

The addresses of all these devices are described in the following paragraphs and can't be set with different values. If some different specific maps are required, please contact directly **grifo®**.

I/O ADDRESSES

The on board control logic manages the allocation of all the peripheral devices registers in the microprocessor I/O space, that is 256 bytes long. Next table shows names, addresses, meanings and directions of peripheral device registers (including the internal microprocessor ones). For a detailed description of the registers function, please refer to next chapter "PERIPHERAL DEVICES SOFTWARE DESCRIPTION".

DEVICES	REG.	ADDRESS	R/W	FUNCTION
ASCI	ASCI	00H÷09H	R/W	Internal microprocessor registers, for asyncronous serial line
CSI/O	CSIO	0AH÷0BH	R/W	Internal microprocessor registers, for Clocked Serial I/O Port management
TIMER	TMR	0CH÷1FH	R/W	Internal microprocessor registers, for Timer/Counter management
DMA	DMA	20H÷32H	R/W	Internal microprocessor registers, for DMA lines management
INTERRUPT	INT	33H÷35H	R/W	Internal microprocessor registers, for interrupts management
REFRESH	RCR	36H÷37H	R/W	Internal microprocessor registers, for Refresh circuit management
MMU	MMU	38H÷3AH	R/W	Internal microprocessor registers, for Memory Management Unit management
I/O	ICR	3BH÷3FH	R/W	Internal microprocessor registers, for I/O control management
ACT. LED	LD1	40H	R/W	Activity LED LD1 management register.
BUZZER	BUZ	40H	R/W	Buzzer management register.
DSW1	DSW1	40H	R	DSW1, LD1, buzzer acquisition register.
A/D	ADC	40H	R/W	A/D TLC2543 management register.
EEPROM	EE	40H	R/W	EEPROM on IC10 management registern.
RTS1 / CTS1	HAND	40H	R/W	Serial line A handshake management register (/RTS1, /CTS1).
W. DOG	RWD	44H	W	External watch dog retrigger register.
LED SPOT	LD6	44H	R	Spot LED LD6 management register.
INPUT	INP	44H	R	Four input lines acquisition register.

FIGURE 33: I/O ADDRESSING TABLE - PART I

DISP.	REG.	IND.	R/W	FUNCTION
RUN / DEBUG	RUNDEB	44H	R	RUN / DEBUG congifuration acquisition register.
PPI 82C55	PDA	48H	R/W	Port A data register.
	PDB	49H	R/W	Port B data register.
	PDC	4AH	R/W	Port C data register.
	CNT	4BH	R/W	Control and command register.
ABACO® I/O BUS	/CS1	50H÷57H	R/W	ABACO® I/O BUS addresses that enable /CS1.
	/CS2	58H÷5FH	R/W	ABACO® I/O BUS addresses that enable /CS2.
	I/O BUS	50H÷EFH	R/W	
Real Time Clock	SEC1	F0H	R/W	Data register for seconds units.
	SEC10	F1H	R/W	Data register for seconds decines.
	MIN1	F2H	R/W	Data register for minutes units.
	MIN10	F3H	R/W	Data register for minutes decines.
	HOU1	F4H	R/W	Data register for hours units.
	HOU10	F5H	R/W	Data register for hours decines and AM/PM.
	DAY1	F6H	R/W	Data register for day units.
	DAY10	F7H	R/W	Data register for day decines.
	MON1	F8H	R/W	Data register for month units.
	MON10	F9H	R/W	Data register for month decines.
	YEA1	FAH	R/W	Data register for year units.
	YEA10	FBH	R/W	Data register for year decines.
	WEE	FCH	R/W	Data register for week day.
	REGD	FDH	R/W	Control register D.
	REGE	FEH	R/W	Control register E.
	REGF	FFH	R/W	Control register F.

FIGURE 34: I/O ADDRESSING TABLE - PART II

ABACO® I/O BUS ADDRESSES

The **GPC® 183** control logic defines **ABACO®** I/O BUS addresses and only these addresses must be used to manages correctly the BUS. As described in following "I/O ADDRESSES" table, only the addresses from 50H to EFH are available for **ABACO®** I/O BUS. Any I/O operations at each one of these adrresses enables the /IORQ signal and the other control signals of CN1 connector. In the addresses subranges 50H÷57H and 58÷5FH the signales /CS1 and /CS2 respectively are enabled. They are used for external peripheral devices coded selection.

MEMORY ADDRESSES

The maximum 1032K bytes of memory, are allocated on the board as below described:

- Up to 512K bytes of EPROM or FLASH EPROM allocated in memory space.
- Up to 512K bytes of SRAM allocated in memory space.
- Up to 8K bytes of serial EEPROM allocated in I/O space.

GPC® 183 can directly manage no more than 64K bytes of memory that is the microprocessor logic addressable space. On the board this logic space can be divided in three separated segments: each ones of these segment have software programmable dimension and start address. The CPU internal MMU circuit divides the logical space directly managed by the microprocessor into these 3 segments and it allocates them in the physical memory devices space. The MMU circuit is software programmable with I/O operations to three specific registers in a fast and comfortable manner. So MMU allows software managements of a physical memory space very larger than microprocessor memory space.
The following figure describes available memory configurations; for further informations on MMU use and segments meaning (Common Area 0, Common Area 1 and Bank Area), please refer to appendix B, while for memory devices location and configuration refer to figures 24 and 31.
After power on or reset phase, the MMU circuit allocates all the logical 64K space at the beginning of the physical space, therefore the card starts execution of code saved at address 0000H of EPROM or FLASH EPROM on IC5.

The memory size and type configurations must be selected both according to used software tools and user requests and/or application features. The card configuration for the selected memory device types and sizes on IC4 and IC5 sockets, is performed with some comfortable jumpers, as described in "MEMORY SELECTION" chapter.

Some software tools, i.e. GDOS, self manage the MMU circuit to use all the available memories at high level witout User intervention.

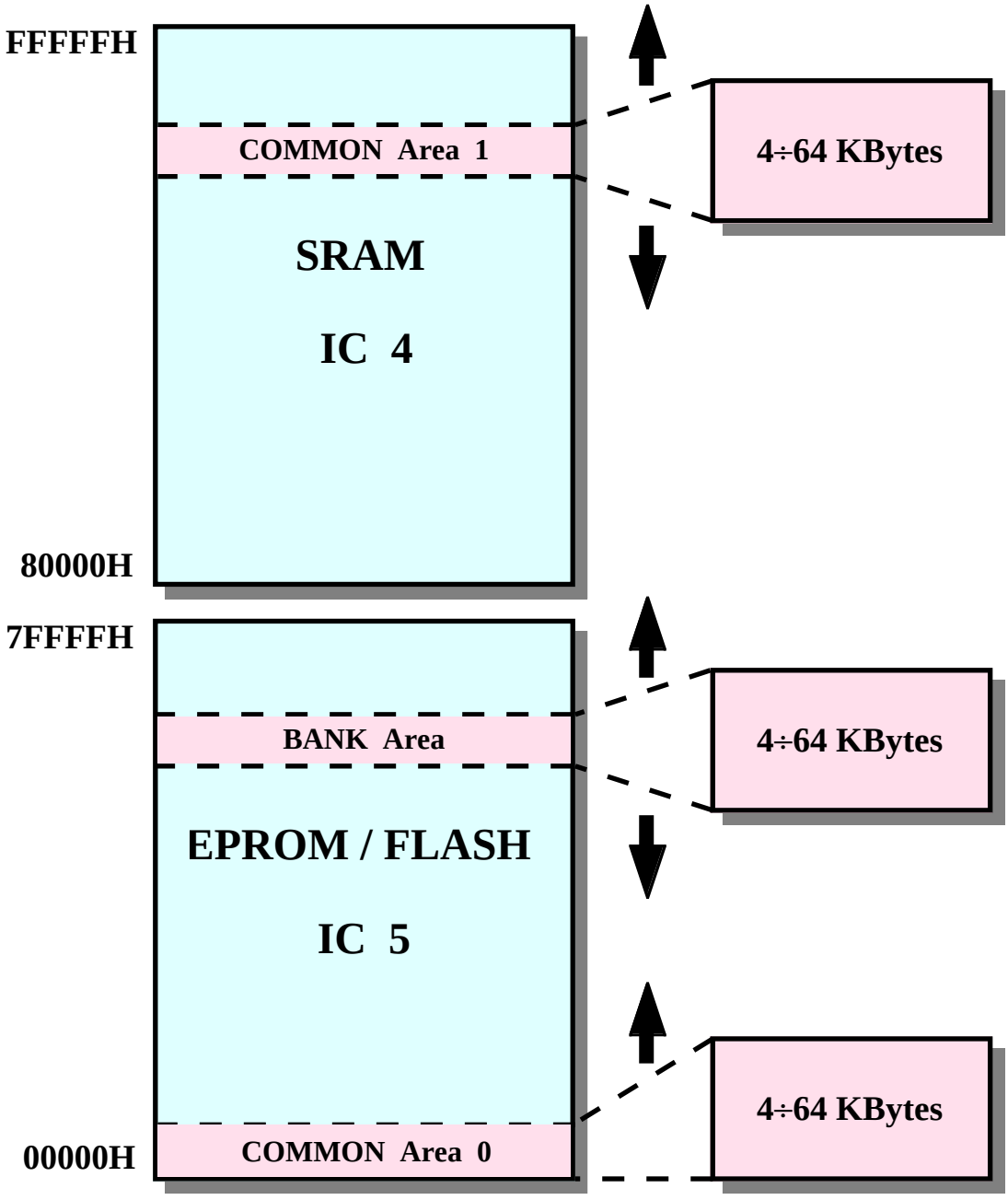


FIGURE 35: MEMORY ALLOCATION

In the previous paragraphes are described the external registers addresses, while in this one there is a specific description of registers meaning and function (please refer to I/O addresses table, for the registers names and addresses values). For a more detailed description of the devices, please refer to manufacturing company documentation; for microprocessor internal peripheral devices, not described in this paragraph, refer to appendix A. In the following paragraphs the D7÷D0 indication denotes the eight bits of the combination used in I/O operations.

BUZZER

Buzzer is activated by performing a "write operation" with bit D1=1 at the address of register BUZ; vice versa buzzer is disabled by performing the same operation with bit D1=0. Also, it is possible to read the status of buzzer by performing a read operation from the address of register BUZ and examining bit D1. The remaining 7 bits of register LD4BZ must be defined according to previous setting for avoiding status modifications on other devices, in this case acticity LED LD1, A/D converter, serial EEPROM and handshakes.
BUZ register is reset (all bits to 0) after Reset o r power on, maintaining disabled the buzzer circuit.

ACTIVITY LED

Activity LED LD1 is enabled by performing a "write operation" with bit D0=1 at the address of register LD1; vice versa LED is disabled by performing the same operation with bit D0=0. Also, it is possible to read the status of LED by performing a read operation from the address of register LED1and examining bit D0. The remaining 7 bits of register LD1 must be defined according to previous setting for avoiding status modifications on other devices, in this case buzzer, A/D converter, serial EEPROM and handshakes.
LD1 register is reset (all bits to 0) after Reset o r power on, maintaining disabled the activity LED.

EXTERNAL WATCH DOG

Retrigger operation of **GPC® 183** external watch dog circuit is performed with a simple write operation at the address of register RWD. This register shares the same address of other on board peripherals, but no conflict are generated in fact retrigger operation is an output operation and the output data has no effect. To avoid external watch dog activation is necessary to retrigger its circuit at regular time periods and the duration of these periods must be smaller than intervention time. If retrigger doesn't happen as before described and J6 is connected, when intervention time is elapsed, the card is reset. Watch dog activation is visualized by LED LD5.

SPOT LED

Spot LED LD6 is enabled by performing a "read operation" fromo the address of register SPOT. This operation enables the LED for an interval of about 50 msec then the LED turns off automatically. The value READ FROM the SPOT register is meaningless.
The main purpose of this LED is to indicate the working condition of application program without introducing programming difficulties or to signal efficently the presence of an event that requires a prompt reaction.

DIP SWITCH DSW1 AND RUN/DEBUG

The on board DSW1 dip switch status can be obtained by software, through a simple "read operation" at the DSW1 register address. The corrispondence between register bits and dip switch is as follows:

D6 -> DSW1.3
D5 -> DSW1.2
D4 -> DSW1.1

As shown above, only 3 bits in the combination read are affected by dip swithces status.
Switch DSW1.4 is the RUN or DEBUG selector, modality specific of some **grifo®** software packages. Its status can be acquired performing a read operation from the address corresponding to register RUNDEB and examining bit D7. Please remark that, by default, logic level 0 corresponds to RUN mode while logic level 1 corresponds to DEBUG mode.
Reading DSW1 register by software, the user obtains a negated bits combination, in fact "**ON**" position corresponds to logic level **0** and "**OFF**" position cooresponds to logic level **1**.

SERIAL EEPROM

For software management of serial EEPROM moule of IC10, please refer to specific manufacturer documentation. This manual reports no software information because management of this component is complex and requires a deep knowledge, anyway the user can use the demo programs supplied with the card. Please remark that first 32 bytes (0÷31) are reserved so they should not be changed. The board control logic alloes to realize a serial communication with I^2C bus standard protocol, through the bits of the specific register EE. The only necessary information is the electric connection:

DATA line (SDA) -> D2 (input)
DATA line (SDA) -> D3 (output)
CLOCK line (SCL) -> D4 (output)

The remaining bits of register EE must be defined according to previous setting for avoiding status modifications on other devices, in this case buzzer, A/D converter, sctivity LED and handshakes.
Please remark that A0, A1 and A2 of this component's slave address are bound to logic 0.
Logic 0 means a connection to 0 Vdc and logic 1 means a connection to 5 Vdc.

A/D CONVERTER

For software management of optional A/D converter on IC28, please refer to specific manufacturer documentation. This manual reports no software information because management of this component is complex and requires a deep knowledge, anyway the user can use the demo programs supplied with the card. The board control logic alloes to realize a serial communication through the bits of the specific register ADC. The only necessary information is the electric connection:

D3 (input) -> linea DATA OUT
D5 (output)-> linea /CS
D6 (output)-> linea DATA IN
D7 (output)-> linea I/O CLOCK

The remaining 7 bits of register LD1 must be defined according to previous setting for avoiding status modifications on other devices, in this case buzzer, activity LED, serial EEPROM and handshakes. Logic 0 means a connection to 0 Vdc and logic 1 means a connection to 5 Vdc.

DIGITAL INPUTS

Connector CN5 features 4 digital input TTL signals (please refer to paragraph “CONNECTORS”) that can be acquired by software performing a read operation from the allocation address of register INP. Correspondance between register bits and input signals is:

D0 -> IN0
D1 -> IN1
D2 -> IN2
D3 -> IN3

As shown above, only the least significant nibble (four bits) repost the four inputs status.
Logic 0 means a connection to 0 Vdc and logic 1 means a connection to 5 Vdc.

HANDSHAKE OF SERIAL LINE A

Serial line ASCI 1 of microprocessor is not provided with hardware handshake signals so they are generated by an on board circuitery that can be software managed through the bits of the specific register HAND. Correspondance between register bits and input signals is:

D7 (input) -> /CTSA
D2 (output)-> /RTSA

Logic 0 means active logic status of corresponding RS 232 signal and logic 1 means deactive logic status of corresponding RS 232 signal.
This circuitery makes **GPC® 183** the ideal component for communication management, in fact it is provided with two complete asynchronous serial lines and one synchronous serial line.

PPI 82C55

This external peripheral device is managed through 4 registers: one status register (CNT) and three data registers (PDA, PDB, PDC). The data registers are available both for read operation (to obtain signal status) and for write operation (to set signal status) with the corrispondence described in figure 23. The PPI 82C55 can work in three different modes:

MODE 0 = it provides two 8 bits bidirectional ports (A,B) and two 4 bits bidirectional ports (C LOW, C HIGH); output signals are latched and input signals are not latched; no handshake signals are provided.

MODE 1 = it provides two 12 bits ports (A+C LOW and B+C HIGH) where ports A and B are used as 8 I/O lines and port C are used as 4 handshake lines. Both inputs and outputs are latched.

MODE 2 = it provides a 13 bits port (A+C3÷7) where port A is used as 8 I/O lines and the 5 bits of port C are used as handshake, and a 11 bits port (B+C0÷2) where port B is used as 8 I/O lines and the 3 bits of port C are used as handshakes. Both inputs and outputs are latched.
The device is programmed writing an 8 bits word in the status register CNT, with the following bit meaning:

CNT = SF M1 M2 A CH M3 B CL
where

SF	= mode Set Flag: if actived (1) the device is enabled for standard I/O operation
M1 M2	= mode selection:
0 0	= mode 0
0 1	= mode 1
1 X	= mode 2
A	= port A direction: 1=input; 0=output
CH	= port C HIGH direction: 1=input; 0=output
M3	= mode selection: 1=mode 1; 0=mode 0
B	= port B direction: 1=input; 0=output
CL	= port C LOW direction: 1=input; 0=output

After Reset o r power on PPI 82C55 is programmed in mode 0 with all three ports in input; in this way any connection of PPI 82C55 signals can be used without conflict problems.

CPU INTERNAL PERIPHERALS

The decriptions of the registers that manages the CPU internal peripheral devices (ASCI, CSI/O, TIMER, DMA, INTERRUPT, REFRESH, MMU, I/O) is available in the appendix A. Whenever this information are still insufficient, please refer to specific documentation of the manufacturing company.

REAL TIME CLOCK

This peripherial is allocated in 16 consecutives I/O addresses, 3 of which correspond to status registres while the remaining 13 are for datas. Data registers are used both for read operations (of the current time and date) and write operations (to initialize the time and date) just like the status registers which are used in write operations (to program the operative mode) and in read operations (to acquire the RTC status). Here follows a list of the RTC data registers' meanings:

SEC1	- Units of seconds	- 4 least significant bits of SEC1.3÷SEC1.0
SEC10	- Decines of secondi	- 3 least significant bits of SEC10.2÷SEC10.0
MIN1	- Units of minutes	- 4 least significant bits of MIN1.3÷MIN1.0
MIN10	- Decines of minutes	- 3 least significant bits of MIN10.2÷MIN10.0
HOU1	- Units of hours	- 4 least significant bits of HOU1.3÷HOU1.0
HOU10	- Decines of hours	- 2 least significant bits of HOU10.1÷HOU10.0 The third bit of HOU10.2 indicates AM/PM
DAY1	- Units of day number	- 4 least significant bits of DAY1.3÷DAY1.0
DAY10	- Decines of day number	- 2 least significant bits of DAY10.1÷DAY10.0
MON1	- Units of month	- 4 least significant bits of MON1.3÷MON1.0
MON10	- Decines of month	- 1 least significant bit of MON10.0
YEA1	- Units of year	- 4 least significant bits of YEA1.3÷YEA1.0
YEA10	- Decines of year	- 4 least significant bits of YEA10.3÷YEA10.0
WEE	- Day of the week	- 3 least significant bits of WEE.2÷WEE.0

For this last register the three least significant bits mean:

WEE.2	WEE.1	WEE.0	Day of the week
0	0	0	Sunday
0	0	1	Monday
0	1	0	Tuesday
0	1	1	Wednesday
1	0	0	Thursday
1	0	1	Friday
1	1	0	Saturday

The meaning of the three control registers is:

bit 7 6 5 4 3 2 1 0
REG D = NU NU NU NU 30S IF B H
where:

NU = Not used.

30S = If high (1) itallowes a 30 seconds correction of the time. Once set the RTC seconds are reset and the minutes increased, if the previous seconds was equal or greater than 30.

IF = It manages the RTC interrupt status. When read it shows the current interrupt status (1 active and viceversa), when reset to 0 it disables the RTC interrupt signal if the interrupt mode is selected.

B = Indictes whether R/W operations can be performed on the registers:
1 -> operations are not permitted and viceversa.

H = If high (1) it stores the written time and date.

bit 7 6 5 4 3 2 1 0

REG E = NU NU NU NU T1 T0 I M

where:

NU = Not used.

T1 T0 = Determin the duration of the internal counters interrupt cycle.

0	0	->	1/64 second
0	1	->	1 second
1	0	->	1 minute
1	1	->	1 hour

I = It defines the interrupt operating mode:

1 -> it selects interrupt mode: when the selected duration elapses the interrupt is enabled and then disabled only with a reset of bit IF of control register D;

0 -> it selects the standard mode: when the selected duration elapses the interrupt is enabled and then disabled only after 7,8 msec.

M = It mask the interrupt status:

1 -> interrupt masked: the RTC interrupt signal is always disabled;

0 -> interrupt not masked: the RTC interrupt signal reflects interrupt status.

bit 7 6 5 4 3 2 1 0

REG F = NU NU NU NU T 24/12 S R

where:

NU = Not used.

T = It determines from which internal counter to take the counting signal:

1 -> main counter (fast counter for test);

0 -> 15^{th} counter.

24/12 = It determines the hours counting mode:

1 -> 0÷23;

0 -> 1-12 with AM/PM.

S = If high (1) it stops the clock time counting until the next enabling (0).

R = If high (1) it resets all the internal counters.

EXTERNAL CARDS

GPC® 183 can be connected to a wide range of block modules and operator interface system produced by **grifo®**, or to many system of other companies.The on board resources can be expanded with a simple connection to the numerous peripheral **grifo®** boards,both intelligent and not, thanks to its standard **ABACO®** I/O BUS connector. Even single EURO cards with BUS **ABACO®** can be connected, by using the proper mother boards.
Hereunder some of these cards are briefly described; ask the detailed information directly to **grifo®**, if required.

ADC 812

Analog to Digital Converter, 12 bits, multi range

DAS (Data Acquisition System) multi range 8 channels 12 bit A/D conversion lines; track and hold; 6µs conversion time; range ±10, ±5, +10, +5Vdc or 0÷20, 4÷20mA; analog inputs connections through quick terminal screw connectors; **ABACO®** I/O BUS interface; direct mounting for DIN 247277-1 and 3 rails; 4 type dimension.

DAC 212

Digital to Analog Converter 12 bits, multi range

Digital to Analog converter; multi range 2 channels 12 bits ± 10, +10 Vdc output; analog outputs connections through quick terminal screw connectors; **ABACO®** I/O BUS interface; direct mounting for DIN 247277-1 and 3 rails; 4 type dimension.

CAN 14

Control Area Network, 1 channel, galvanically insulated

UART CAN SJA1000; 1 serial channels galvanically insulated; **ABACO®** I/O BUS interface; 4 type dimension; support of CAN 2.0B protocol; transfer rate up to 1M bit/sec; direct mounting for DIN 247277-1 and 3 rails.

KDL xxx - KDF xxx

Keyboard Display interface - LCD or Fluorescent

Interface with Fluorescent or LCD display, LEDs backlit, 20x2 or 20x4 characters; up to 24 keys matrix keyboard connector. It is directly driven by 16 TTL I/O lines; High level languages supported.

QTP 24 - QTP 24P

Quick Terminal Panel 24 keys with Parallel interface

Intelligent user panel equipped with Fluorescent or LCD display, LEDs backlit, 20x2 or 20x4 characters; RS 232, RS 422, RS 485 or current loop serial line; serial E2 for set up and message. Pssibility of re-naming keys, LEDs and panel name by inserting label with new name into the proper slot; 24 Keys and 16 LEDs with blinking attribute and buzzer manageable by software; built in power supply; RTC option, reader of magnetic badge and relay. The QTP 24P is low cost no intelligent (passive) version. It is directly driven from 16 TTL I/O lines; high level languages supported.

QTP 16 - QTP 16P

Quick Terminal Panel 16 keys with Parallel interface

Intelligent user panel equipped with Fluorescent or LCD display, LEDs backlit, 20x2 or 20x4 characters; RS 232, RS 422, RS 485 or current loop serial line; serial E2 for set up and messages; buzzer manageable by software; 4 readable auxiliary opto in lines; power supply 5 Vdc. The QTP 16P is low cost no intelligent (passive) version. It is directly driven from 16 TTL I/O lines.

QTP G28

Quick Terminal Panel - LCD Graphic, 28 keys

LCD display 240x128 pixels, CFC backlit; Optocoupled RS 232 line and additional RS 232/422/485/ Current Loop line; CAN line controller; E^2 for set up; RTC and RAM lithium backed; primary graphic object; possibility of re-naming keys, LEDs and panel name; 28 keys and 16 LEDs with blinking attribute and buzzer manageable by software; Buzzer; built in power supply; reader of magnetic badge and relay option.

OBI N8 - OBI P8

Opto BLOCK Input NPN-PNP

Interface between 8 NPN, PNP optocoupled and displayed input lines, with screw terminal and **ABACO®** standard I/O 20 pins connector; power supply section; connection for DIN Ω rails.

TBO 01 - TBO 08

Transistor BLOCK Output

Interface for **ABACO®** standard I/O 20 pins connector; 16 or 8 transistor output lines 45 Vdc 3 A open collector; screw terminal; optocoupled and displayed lines; connection for DIN 247277-1 and 3 rails.

XBI R4 - XBI T4

miXed BLOCK Input-Output

Interface for **ABACO®** standard I/O 20 pins connector; 4 Relays 3A with MOV or 4 optocoupled Transistors 3A open collectors; 4 input lines optocoupled; screw terminal; connection for DIN Ctype and Ω rails.

FBC xxx

Flat Block Contactxxx pins

This interconnection system "wire to board" allows the connection to many type of flat cable connectors to terminal for external connections. Connection for DIN Ω rails.

IBC 01

Interface Block Comunication

Conversion card for serial communication, 2 RS 232 lines; 1 RS 422-485 line; 1 optical fibre line; selecatble DTE/DCE interface; quick connection for DIN 46277-1 and 3 rails.

DEB 01

Didactis Experimental Board

Supporting card for 16 TTL I/O lines use. It includes: 16 keys, 16 LEDs, 4 digits, 16 keys matrix keyboard, Centronics printer interface, LCD display and fluorescent display interface, **GPC® 68** I/O connector, field connection with screw terminal.

MCI 64

Memory Cards Interfaces 64 MBytes

Interfacing card for managing 68 pins PCMCIA memory cards, it is directly driven from any **ABACO®** I/O standard connector; High level languages GDOS supported.

ZBR xxx

Zipped BLOCK Relays xx Input + xx Output

Peripheral cards family, relays outputs, equipped with housing for Ω rails mounting. Double power supply built in; 5Vdc section for powering the on board logic and an external CPU cards; second section, galvanically coupled, for the optocoupled input lines. All I/O lines are displayed by LEDs. Relays contacts are 3A and are MOV protected. All I/O connections are availables on quick terminal connectors. 1 connector interface to **ABACO®** I/O BUS. The ZBR serie represent the ideal complement for cards 3 and 4 type. The ZBR cards can be directly driven, through the PC parallel port, by using the PCC A26 low cost interface card. ZBR 324 -> 32 opto in, 24 relays; ZBR 246 -> 24 opto in, 16 relays; ZBR 168 -> 16 opto in, 8 relays; ZBR 84 -> 8 opto in, 4 relays.

ZBT xxx

Zipped BLOCK Transistors xx Input + xx Output

Peripheral cards family having optocoupled outputs and 3A transistor in open collector. Cards are equipped with housing for Ω rails mounting. Double power supply built in; 5Vdc section for powering the on board logic and an external CPU cards; second section, galvanically coupled, for the optocoupled input lines. All I/O lines are displayed by LEDs. All output transistors are equipped with protection against inductive loads. All I/O connections are availables on easy quick terminal connectors. Connector interface to **ABACO®** I/O BUS. The ZBT serie represent the ideal complement for cards 3 and 4 type. The ZBT cards can be directly driven, through the PC parallel port, by using the PCC A26 low cost interface card. ZBT 324 -> 32 opto in, 24 transistors; ZBT 246 -> 24 opto in, 16 transistors; ZBT 168 -> 16 opto in, 8 transistors; ZBT 84 -> 8 opto in, 4 transistors.

ABB 03

ABACO® Block BUS 3 slots

3 slots **ABACO®** mother board; 4 TE pitch connectors; **ABACO®** I/O BUS connector; screw terminal for power supply; connection for DIN C type and Ω rails.

ABB 05

ABACO® Block BUS 5 slots

5 slots **ABACO®** mother board with power supply. Double power supply built in; 5Vdc 2,5A section for powering the on board logic; second section at 24Vdc 400mA galvanically coupled, for the optocoupled input lines. Auxiliary connector for **ABACO®** I/O BUS. Connection for DIN Ω rails.

IPC 52

Intelligent Peripheral Controller, 24 analogic input

This intelligent peripheral card acquires 24 indipendent analogic input lines: 8 PT 100 or PT 1000 sensors, 8 J,K,S,T termocouples, 8 analog input ±2Vdc or 4÷20mA; 16 bits + sign A/D section; 0.1 °C resolution; 32K RAM for local data logging; buzzer; 16 TTL I/O lines; 5 or 8 conversion per second; facility of networking up to 127 IPC 52 cards using serial line. BUS interfacing or through RS 232, RS 422, RS 485 or current loop line. Only 5Vdc power supply.

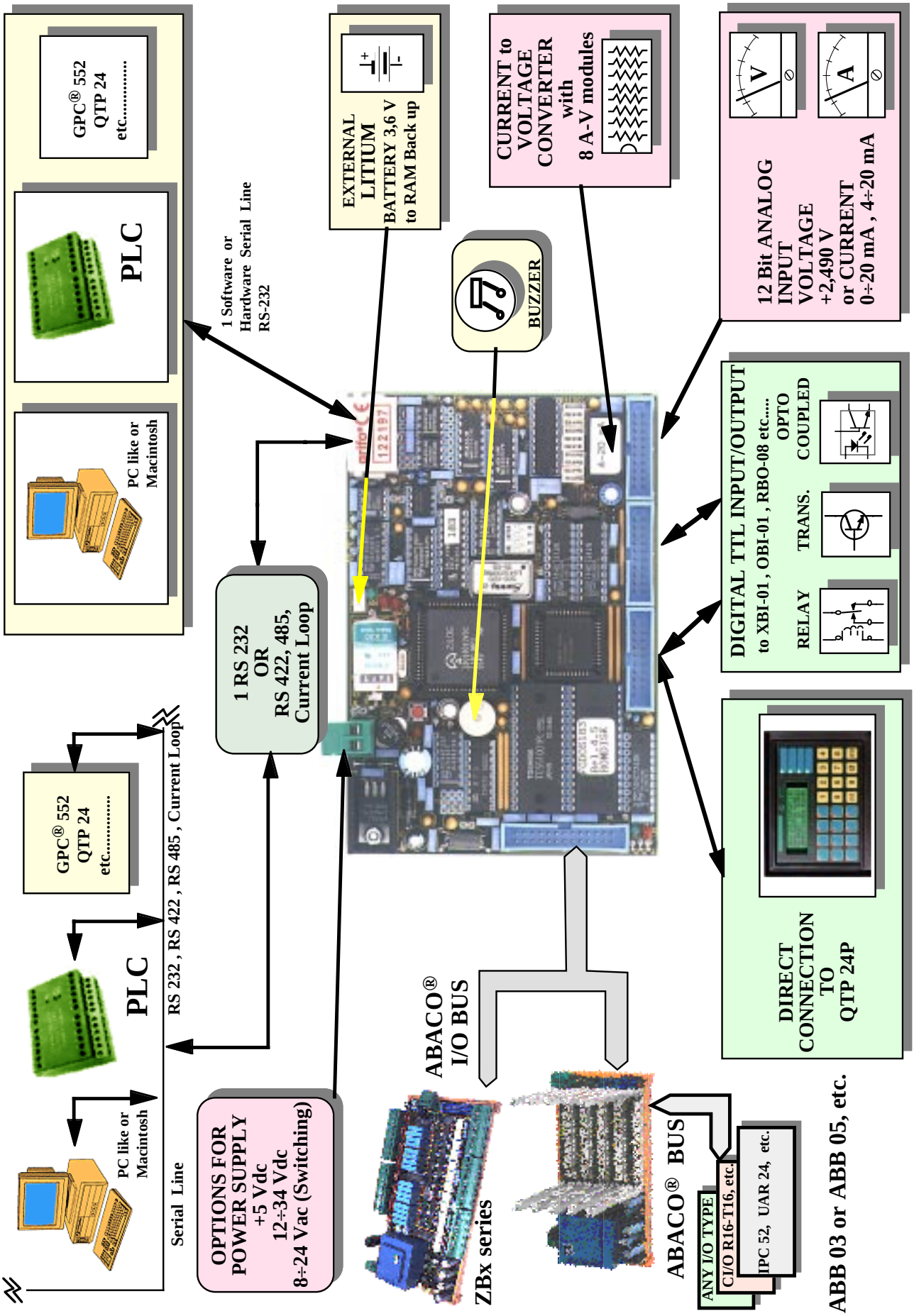


FIGURE 36: GPC®183 AVAILABLE CONNECTIONS DIAGRAM

BIBLIOGRAPHY

In this chapter there is a complete list of technical books, where the user can find all the necessary documentations on the components mounted on **GPC® 183**.

Data book Manual TEXAS INSTRUMENTS: *The TTL Data Book - SN54/74 Families*
Data book Manual TEXAS INSTRUMENTS: *RS-422 and RS-485 Interface Circuits*
Manual TEXAS INSTRUMENTS: *Linear Circuits Dtata Book - Volume 1 and 3*

Data book NEC: *Memory Products*
Manual NEC: *Microprocessors and Peripherals - Volume 3*

Manual SGS-THOMSON: *Programmable logic manual - GAL products*

Data book HEWLETT PACKARD: *Optoelectronics Designer's Catalog*

Data book MAXIM: *New Releases Data Book - Volume 4*
Data book MAXIM: *Integrated Circuits Data Book*

Manual HEWLETT PACKARD: *Optoelectronics Designer's Catalog*

Manual MAXIM: *New Releases Data Book - Volume 4*
Manual MAXIM: *New Releases Data Book - Volume 5*

Manual XICOR: *Data Book*

Data book SEIKO EPSON: *REAL TIME CLOCK MODULE RTC-72421 Application manual*

Manual NATIONAL SEMICONDUCTOR: *Linear Databook - Volume 1*

Data book ZILOG: *Z80S180/Z8L180 Enhanced Z180 Microprocessor*

Data book TOSHIBA: *Mos Memory Products*

For further information and upgrades please refer to specific internet web pages of the manufacturing companies.

Z80180/Z8S180/ Z8L180 SL1919

ENHANCED Z180 MICROPROCESSOR

FEATURES

- Code Compatible with Zilog Z80® CPU
- Extended Instructions
- Two Chain-Linked DMA Channels
- Low Power-Down Modes
- On-Chip Interrupt Controllers
- Three On-Chip Wait-State Generators
- On-Chip Oscillator/Generator
- Expanded MMU Addressing (up to 1 MB)
- Clocked Serial I/O Port
- Two 16-Bit Counter/Timers
- Two Enhanced UARTs (up to 512 Kbps)
- Clock Speeds: 6, 8, 10, 20, 33 MHz
- Operating Range: 5V (3.3V@ 20 MHz)
- Operating Temperature Range: 0°C to +70°C
- -40°C to +85°C Extended Temperature Range
- Three Packaging Styles
  - 68-Pin PLCC
  - 64-Pin DIP
  - 80-Pin QFP

GENERAL DESCRIPTION

The enhanced Z80180/Z8S180/Z8L180™ significantly improves on the previous Z80180 models while still providing full backward compatibility with existing Zilog Z80 devices. The Z80180/Z8S180/Z8L180 now offers faster execution speeds, power saving modes, and EMI noise reduction.

This enhanced Z180 design also incorporates additional feature enhancements to the ASCIs, DMAs, and I_{CC} STANDBY Mode power consumption. With the addition of "ESCC-like" Baud Rate Generators (BRGs), the two ASCIs now have the flexibility and capability to transfer data asynchronously at rates of up to 512 Kbps. In addition, the ASCI receiver has added a 4-byte First In First Out (FIFO) which can be used to buffer incoming data to reduce the incidence of overrun errors. The DMAs have been modified to allow for a "chain-linking" of the two DMA channels when set to take their DMA requests from the same peripherals device. This feature allows for non-stop DMA operation between the two DMA channels, reducing the amount of CPU intervention (Figure 1).

Not only does the Z80180/Z8S180/Z8L180 consume les power during normal operations than the previous mode it has also been designed with three modes intended to fu ther reduce the power consumption. Zilog reduced I_{CC} pow er consumption during STANDBY Mode to a minimum c 10 µA by stopping the external oscillators and interna clock. The SLEEP mode reduces power by placing th CPU into a "stopped" state, thereby consuming less cu rent while the on-chip I/O device is still operating. Th SYSTEM STOP mode places both the CPU and the or chip peripherals into a "stopped" mode, thereby reducin power consumption even further.

A new clock doubler feature has been implemented in th Z80180/Z8S180/Z8L180 device that allows the progra mer to double the internal clock from that of the externa clock. This provides a systems cost savings by allowin the use of lower cost, lower frequency crystals instead c the higher cost, and higher speed oscillators.

The Enhanced Z180 is housed in 80-pin QFP, 68-pi PLCC, and 64-pin DIP packages.

Notes: All Signals with a preceding front slash, "/" are active Low, for example, B/W (WORD is active Low); /B/W (BYTE is active Low, only). Alternatively, an overslash may be used to signify active Low, for example $\overline{WR}$

Power connections follow conventional descriptions be low:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

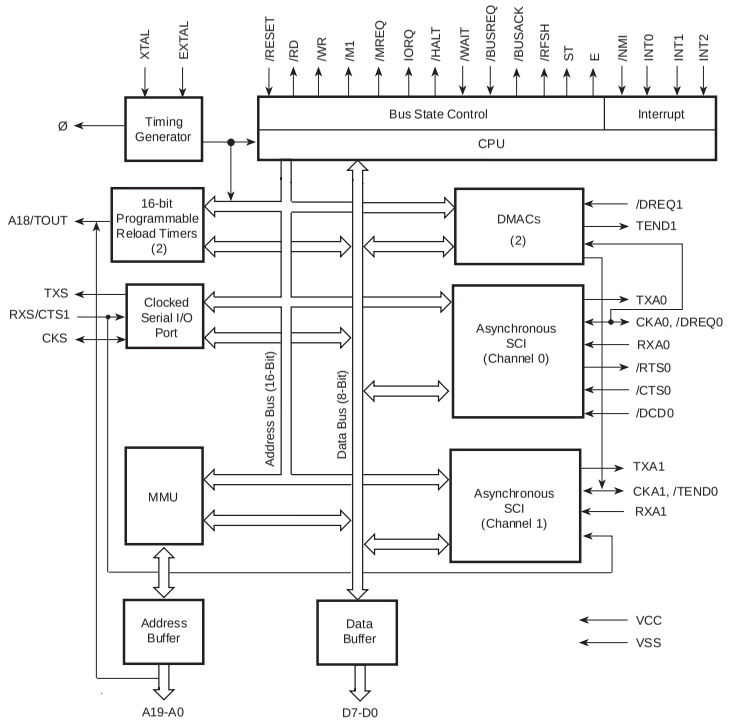


Figure 1. Z80180/Z8S180/Z8L180 Functional Block Diagram

HALT and Low-Power Operating Modes. The Z80180/Z8S180/Z8L180 can operate in seven modes with respect to activity and power consumption:

- Normal Operation
- HALT Mode
- IOSTOP Mode
- SLEEP Mode
- SYSTEM STOP Mode
- IDLE Mode
- STANDBY Mode (with or without QUICK RECOVERY)

Normal Operation. The Z80180/Z8S180/Z8L180 processor is fetching and running a program. All enabled functions and portions of the device are active, and the HALT pin is High.

HALT Mode. This mode is entered by the HALT instruction. Thereafter, the Z80180/Z8S180/Z8L180 processor continually fetches the following opcode but does not execute it, and drives the HALT, ST and M1 pins all Low. The oscillator and PHI pin remain active, interrupts and bus granting to external masters, and DRAM refresh can occur and all on-chip I/O devices continue to operate including the DMA channels.

The Z80180/Z8S180/Z8L180 leaves HALT mode in response to a Low on RESET, on to an interrupt from an enabled on-chip source, an external request on NMI, or an enabled external request on INT0, INT1, or INT2. In case of an interrupt, the return address will be the instruction following the HALT instruction; at that point the program can either branch back to the HALT instruction to wait for another interrupt, or can examine the new state of the system/application and respond appropriately.

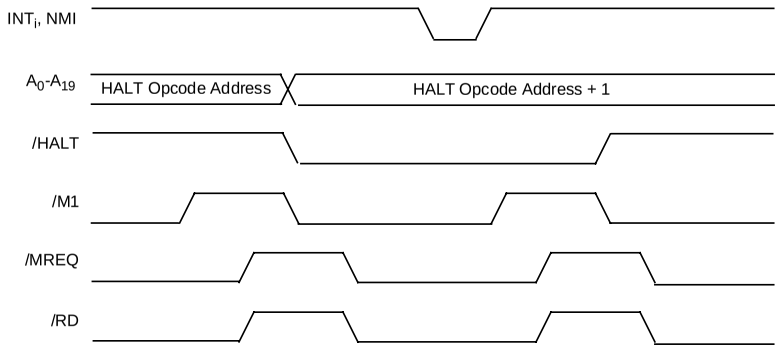


Figure 13. HALT Timing

SLEEP Mode. This mode is entered by keeping the IOSTOP bit (ICR5) bits 3 and 6 of the CPU Control Register (CCR3, CCR6) all zero and executing the SLP instruction. The oscillator and PHI output continue operating, but are blocked from the CPU core and DMA channels to reduce power consumption. DRAM refresh stops but interrupts and granting to external master can occur. Except when the bus is granted to an external master, A19-0 and all control signals except /HALT are maintained High. /HALT is Low. I/O operations continue as before the SLP instruction, except for the DMA channels.

The Z80180/Z8S180/Z8L180 leaves SLEEP mode in response to a low on /RESET, an interrupt request from an on-chip source, an external request on /NMI, or an external request on /INT0, 1, or 2.

If an interrupt source is individually disabled, it cannot bring the Z80180/Z8S180/Z8L180 out of SLEEP mode. If an interrupt source is individually enabled, and the IEF bit is 1 so that interrupts are globally enabled (by an EI instruction), the highest priority active interrupt will occur, with the return address being the instruction after the SLP instruction. If an interrupt source is individually enabled, but the IEF bit is 0 so that interrupts are globally disabled (by a DI instruction), the Z80180/Z8S180/Z8L180 leaves SLEEP mode by simply executing the following instruction(s).

This provides a technique for synchronization with high-speed external events without incurring the latency imposed by an interrupt response sequence. Figure 14 shows the timing for exiting SLEEP mode due to an interrupt request. Note that the Z80180/Z8S180/Z8L180 takes about 1.5 clocks to restart.

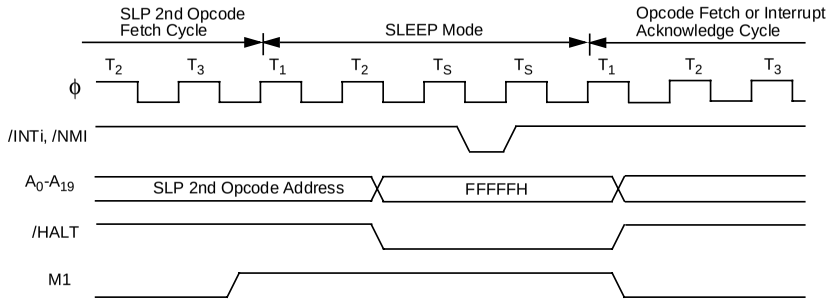


Figure 14. SLEEP Timing

IOSTOP Mode. IOSTOP mode is entered by setting the IOSTOP bit of the I/O Control Register (ICR) to 1. In this case, on-chip I/O (ASCI, CSI/O, PRT) stops operating. However, the CPU continues to operate. Recovery from IOSTOP mode is by resetting the IOSTOP bit in ICR to 0.

SYSTEM STOP Mode. SYSTEM STOP mode is the combination of SLEEP and IOSTOP modes. SYSTEM STOP mode is entered by setting the IOSTOP bit in ICR to 1 followed by execution of the SLP instruction. In this mode, on-chip I/O and CPU stop operating, reducing power consumption, but the PHI output continues to operate. Recovery from SYSTEM STOP mode is the same as recovery from SLEEP mode except that internal I/O sources (disabled by IOSTOP) cannot generate a recovery interrupt.

IDLE Mode. Software can put the Z80180/Z8S180/Z8L180 into this mode by setting the IOSTOP bit (ICR5) to 1, CCR6 to 0, CCR3 to 1 and executing the SLP instruction. The oscillator keeps operating but its output is blocked to all circuitry including the PHI pin. DRAM refresh and all internal devices stop, but external interrupts can occur. Bus granting to external masters can occur if the BREST bit in the CPU control Register (CCR5) was set to 1 before IDLE mode was entered.

The Z80180/Z8S180/Z8L180 leaves IDLE mode in response to a Low on RESET, an external interrupt request on NMI, or an external interrupt request on /INT0, /INT1 or /INT2 that is enabled in the INT/TRAP Control Register. As previously described for SLEEP mode, when the Z80180/Z8S180/Z8L180 leaves IDLE mode due to an NMI, or due to an enabled external interrupt request when the IEF flag is 1 due to an EI instruction, it starts by performing the interrupt with the return address being that of the instruction after the SLP instruction.

If an external interrupt enables the INT/TRAP control register while the IEF1 bit is 0, Z80180/Z8S180/Z8L180 leaves IDLE mode; specifically, the processor restarts by executing the instructions following the SLP instruction.

Figure 15 shows the timing for exiting IDLE mode due to an interrupt request. Note that the Z80180/Z8S180/Z8L180 takes about 9.5 clocks to restart.

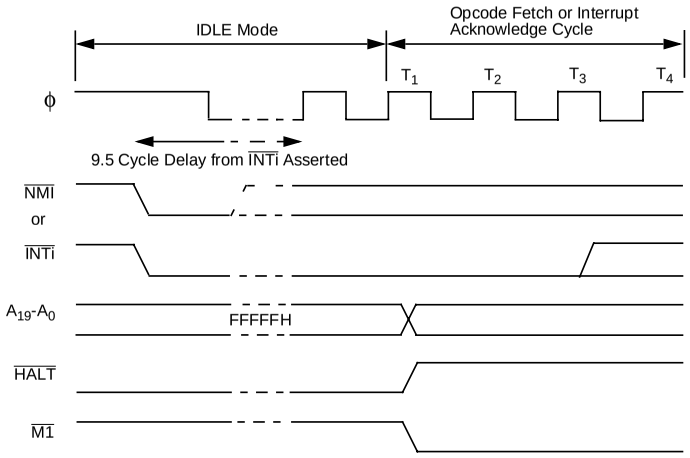


Figure 15. Z80180/Z8S180/Z8L180 IDLE Mode Exit due to External Interrupt

While the Z80180/Z8S180/Z8L180 is in IDLE mode, it will grant the bus to an external master if the BREXT bit (CCR5) is 1. Figure 16 shows the timing for this sequence. Note that the part takes 8 clock cycles longer to respond to the Bus Request than in normal operation.

After the external master negates the Bus Request, the Z80180/Z8S180/Z8L180 disables the PHI clock and remains in IDLE mode.

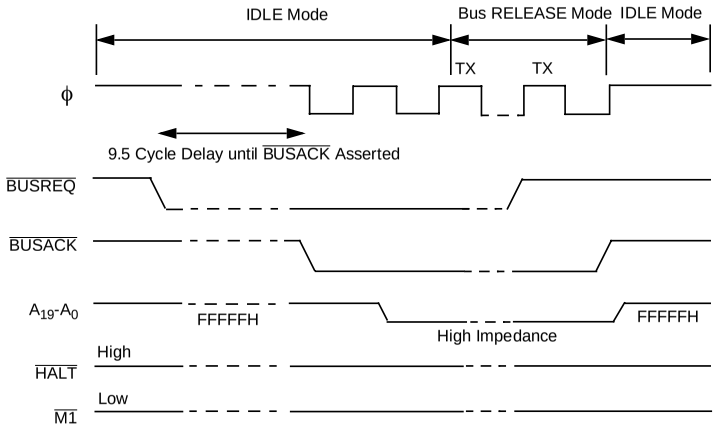


Figure 16. Bus Granting to External Master in IDLE Mode

STANDBY Mode (With or Without QUICK RECOVERY). Software can put the Z80180/Z8S180/Z8L180 into this mode by setting the IOSTOP bit (ICR5) to 1 and CCR6 to 1, and executing the SLP instruction. This mode stops the on-chip oscillator and thus draws the least power of any mode, less than 10μμA.

As with IDLE mode, the Z80180/Z8S180/Z8L180 will leave STANDBY mode in response to a Low on RESET or on NMI, or a Low on INT0-2 that is enabled by a 1 in the corresponding bit in the INT/TRAP Control Register, and will grant the bus to an external master if the BREXT bit in the CPU Control Register (CCR5) is 1. But the time required for all of these operations is greatly increased by the need to restart the on-chip oscillator and ensure that it has stabilized to square-wave operation.

When an external clock is connected to the EXTAL pin rather than a crystal to the XTAL and EXTAL pins, and the external clock runs continuously, there is little need to use STANDBY mode because there is no time required to restart the oscillator, and other modes restart faster. However, if external logic stops the clock during STANDBY mode (for example, by decoding HALT Low and M1 High for several clock cycles), then STANDBY mode can be useful to allow the external clock source to stabilize after it is re-enabled.

When external logic drives RESET Low to being a Z80180/Z8S180/Z8L180 out of STANDBY mode, and a crystal is used or an external clock source has been stopped, the external logic must hold RESET Low until the on-chip oscillator or external clock source has restarted and stabilized.

The clock stability requirements of the Z80180/Z8S180/Z8L180 are much less in the divide-by-two mode that's selected by a Reset sequence and thereafter controlled by the Clock Divide bit in the CPU Control Register (CCR7). Because of this, software should:

a. Program CCR7 to 0 to select divide-by-two mode, before the SLP instruction that enters STANDBY mode, and.

b. After a Reset, interrupt or in-line restart after the SLP 01 instruction, delay programming CCR7 back to 1 to set divide-by-one mode, as long as possible to allow additional clock stabilization time.

If software sets CCR6 to 1 before the SLP instruction places the MPU in STANDBY mode, the value in the CCR3 bit determines how long the Z80180/Z8S180/Z8L180 will wait for oscillator restart and stabilization when it leaves STANDBY mode due to an external interrupt request. If CCR3 is 0, the Z80180/Z8S180/Z8L180 waits 217 (131,072) clock cycles, while if CCR3 is 1, it waits only 64 clock cycles. The latter is called QUICK RECOVERY mode. The same delay applies to granting the bus to an

external master during STANDBY mode, when the BREXT bit in the CPU Control Register (CCR5) is 1.

As described previously for SLEEP and IDLE modes, when a Z80180/Z8S180/Z8L180 leaves STANDBY mode due to $\overline{NMI}$ Low, or when it leaves STANDBY mode due to an enabled $\overline{INT0}$-2 low when the IEF, flag is 1 due to an IE instruction, it starts by performing the interrupt with the return address being that of the instruction following the SLP instruction. If the Z80180/Z8S180/Z8L180 leaves STANDBY mode due to an external interrupt request that's enabled in the INT/TRAP Control Register, but the IEF, bit is 0 due to a DI instruction, the processor restarts by executing the instruction(s) following the SLP instruction. If $\overline{INT0}$, or $\overline{INT1}$ or 2 goes inactive before the end of the clock stabilization delay, the Z80180/Z8S180/Z8L180 stays in STANDBY mode.

Figure 17 shows the timing for leaving STANDBY mode due to an interrupt request. Note that the Z80180/Z8S180/Z8L180 takes either 64 or 217 (131,072) clocks to restart, depending on the CCR3 bit.

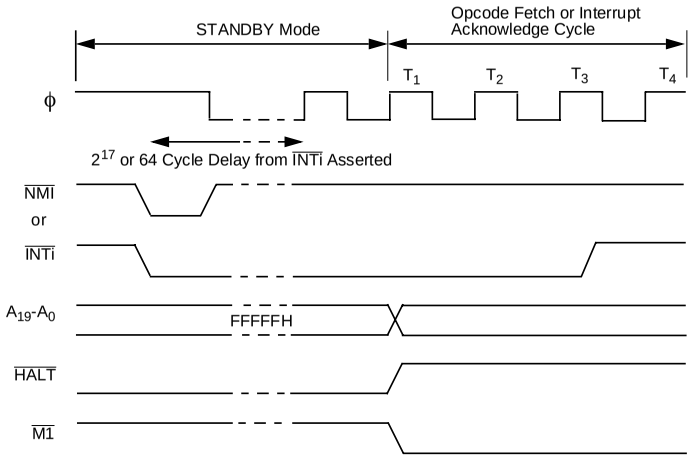


Figure 17. Z80180/Z8S180/Z8L180 STANDBY Mode Exit due to External Interrupt

While the Z80180/Z8S180/Z8L180 is in STANDBY mode, it will grant the bus to an external master if the BREXT bit (CCR5) is 1. Figure 18 shows the timing of this sequence. Note that the part takes 64 or 217 (131,072) clock cycles to grant the bus depending on the CCR3 bit.

The latter (non-Quick-Recovery) case may be prohibitive for many “demand driven” external masters. If so, QUICK RECOVERY or IDLE mode can be used.

CPU CONTROL REGISTER

CPU Control Register (CCR). This register controls the basic clock rate, certain aspects of Power-Down modes, and output drive/low noise options (Figure 31).

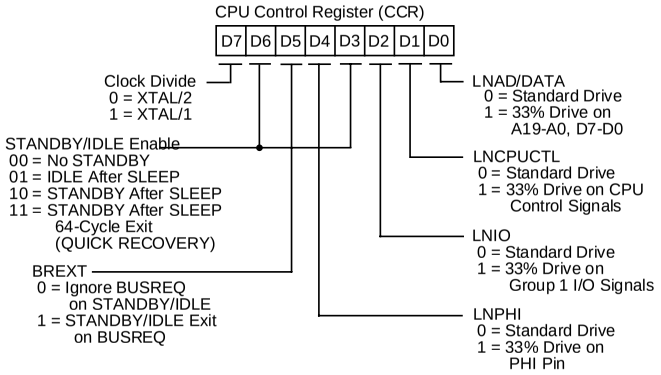


Figure 31. CPU Control Register (CCR) Address 1FH

Bit 7. Clock Divide Select. If this bit is 0, as it is after a Reset, the Z80180/Z8S180/Z8L180 divides the frequency on the XTAL pin(s) by two to obtain its master clock PHI. If this bit is programmed as 1, the part uses the XTAL frequency as PHI without division.

If an external oscillator is used in divide-by-one mode, the minimum pulse width requirement given in the AC Characteristics must be satisfied.

Bits 6 and 3. STANDBY/IDLE Control. When these bits are both 0, a SLP instruction makes the Z80180/Z8S180/Z8L180 enter SLEEP or SYSTEM STOP mode, depending on the IOSTOP bit (ICR5).

When D6 is 0 and D3 is 1, setting the IOSTOP bit (ICR5) and executing a SLP instruction puts the Z80180/Z8S180/Z8L180 into IDLE mode in which the on-chip oscillator runs, but its output is blocked from the rest of the part, including PHI out.

When D6 is 1 and D3 is 0, setting IOSTOP (ICR5) and executing a SLP instruction puts the part into STANDBY mode, in which the on-chip oscillator is stopped and the part allows 217 (128K) clock cycles for the oscillator to stabilize when it's restarted.

When D6 and D3 are both 1, setting IOSTOP (ICR5) and executing a SLP instruction puts the part into QUICK RECOVERY STANDBY mode, in which the on-chip oscillator is stopped, and the part allows only 64 clock cycles for the oscillator to stabilize when it's restarted.

The latter section, HALT and LoW POWER Modes, describes the subject more fully.

Bit 5 BREXT. This bit controls the ability of the Z8S180/Z8L180 to honor a bus request during STANDBY mode. If this bit is set to 1 and the part is in STANDBY mode, a BUSREQ is honored after the clock stabilization timer is timed out.

Bit 4 LNPHI. This bit controls the drive capability on the PHI Clock output. If this bit is set to 1, the PHI Clock output will be reduced to 33 percent of its drive capability.

Bit 2 LNIO. This bit controls the drive capability of certain external I/O pins of the Z8S180/Z8L180. When this bit is set to 1, the output drive capability of the following pins is reduced to 33percent of the original drive capability:

- /RTSO/TxS
- CKA1
- CKAO
- TXAO
- TXAI
- TOUT

Bit 1 LNCPUCTL. This bit controls the drive capability of the CPU Control pins. When this bit is set to 1, the output drive capability of the following pins is reduced to 33percent the original drive capability:

- /BUSACK
- /RD
- /WR
- /M1
- /MREQ
- /IORQ
- /RFSH
- /HALT

Bit 0 LNAD/DATA. This bit controls the drive capability of the Address/Data bus output drivers. If this bit is set to 1, the output drive capability of the Address and Data bus output is reduced to 33percent of its original drive capability.

Clocked Serial I/O (CSI/O). The CSIO channel provides a half-duplex serial transmitter and receiver. This channel can be used for simple high-speed data connection to another microprocessor or microcomputer**.** TRDR is used for both CSI/O transmission and reception. Thus, the system design must ensure that the constraints of half-duplex operation are met (Transmit and Receive operation cannot occur simultaneously). For example, if a CSI/O transmission is attempted while the CSI/O is receiving data, a CSI/O will not work. Also note that TRDR is not buffered. Therefore, attempting to perform a CSI/O transmit while the previous transmit data is still being shifted out causes the shift data to be immediately updated, thereby corrupting the transmit operation in progress. Similarly, reading TRDR while a transmit or receive is in progress should be avoided.

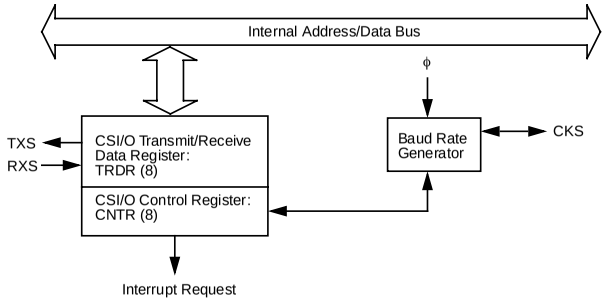


Figure 7. CSIO Block Diagram

OPERATION MODES

Z80® versus 64180 Compatibility. The Z80180/Z8S180/Z8L180 is descended from two different "ancestor" processors, Zilog's original Z80 and the Hitachi 64180. The Operating Mode Control Register (OMCR), shown in Figure 8, can be programmed to select between certain Z80 and 64180differences.

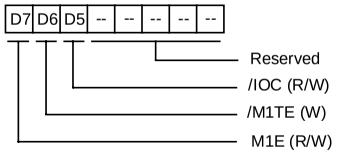


Figure 8. Operating Control Register (OMCR: I/O Address = 3EH)

M1E (M1 Enable). This bit controls the M1 output and is set to a 1 during reset.

When M1E=1, the M1 output is asserted Low during the opcode fetch cycle, the INT0 acknowledge cycle, and the first machine cycle of the NMI acknowledge.

On the Z80180/Z8S180/Z8L180, this choice makes the processor fetch an RETI instruction once, and when fetching an RETI from zero-wait-state memory will use three clock machine cycles, which are not fully Z80-timing compatible but are compatible with the on-chip CTCs.

When M1E=0, the processor does not drive M1 Low during instruction fetch cycles, and after fetching an RETI instruction once with normal timing, it goes back and re-fetches the instruction using fully Z80-compatible cycles that include driving M1 Low. This may be needed by some external Z80 peripherals to properly decode the RETI instruction. Figure 9 and Table 4 show the RETI sequence when M1E=0.

IASCI REGISTER DESCRIPTION

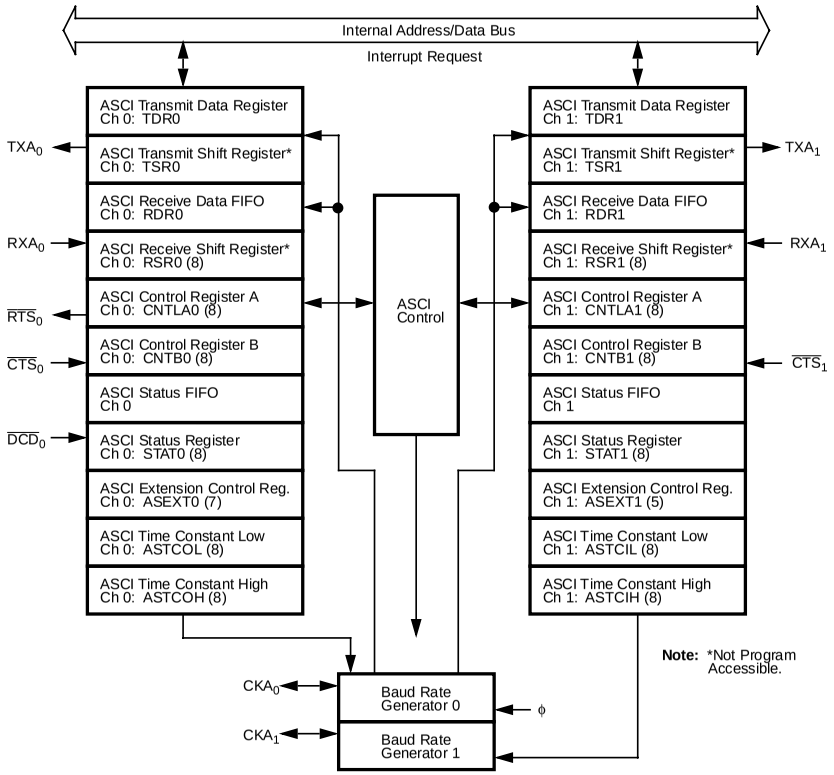


Figure 32. ASCI Block Diagram

The following paragraphs explain the various functions of the ASCI registers.

ASCI Transmit Register 0. When the ASCI Transmit Register receives data from the ASCI Transmit Data Register (TDR), the data is shifted out to the TxA pin. When transmission is completed, the next byte (if available) is automatically loaded from TDR into TSR and the next transmission starts. If no data is available for transmission, TSR IDLEs by outputting a continuous High level. This register is not program accessible

ASCI Transmit Data Register 0,1 (TDR0, 1: I/O address = 06H, 07H). Data written to the ASCI Transmit Data Register is transferred to the TSR as soon as TSR is empty. Data can be written while TSR is shifting out the previous byte of data. Thus, the ASCI transmitter is double buffered.

Data can be written into and read from the ASCI Transmit Data Register. If data is read from the ASCI Transmit Data Register, the ASCI data transmit operation will not be af fected by this read operation

ASCI Receive Shift Register 0,1 (RSR0,1). This registe receives data shifted in on the RxA pin. When full, data i automatically transferred to the ASCI Receive Data Regis ter (RDR) if it is empty. If RSR is not empty when the nex incoming data byte is shifted in, an overrun error occurs This register is not program accessible.

ASCI Receive Data FIFO 0,1 (RDR0, 1:I/O Address = 08H 09H). The ASCI Receive Data Register is a read-only reg ister. When a complete incoming data byte is assemble in RSR, it is automatically transferred to the 4 characte Receive Data First-In First-Out (FIFO) memory. The oldes character in the FIFO (if any) can be read from the Receiv Data Register (RDR). The next incoming data byte can b shifted into RSR while the FIFO is full. Thus, the ASCI re ceiver is well buffered.

ASCI STATUS FIFO

This 4 entry FIFO contains Parity Error, Framing Error, Rx Overrun, and Break status bits associated with each character in the receive data FIFO. The status of the oldest character (if any) can be read from the ASCI status registers as described below

ASCI CHANNEL CONTROL REGISTER A

ASCI Control Register A 0 (CNTLA0: I/O Address = 00H)

Bit	7	6	5	4	3	2	1	0
	MPE	RE	TE	$\overline{RTS0}$	MPBR/ EFR	MOD2	MOD1	MOD0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

ASCI Control Register A 1 (CNTLA1: I/O Address = 01H)

Bit	7	6	5	4	3	2	1	0
	MPE	RE	TE	CKA1D	MPBR/ EFR	MOD2	MOD1	MOD0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Figure 33. ASCI Channel Control Register A

MPE: Multi-Processor Mode Enable (bit 7). The ASCI has a multiprocessor communication mode that utilizes an extra data bit for selective communication when a number of processors share a common serial bus. Multiprocessor data format is selected when the MP bit in CNTLB is set to 1. If multiprocessor mode is not selected (MP bit in CNTLB = 0), MPE has no effect. If multiprocessor mode is selected, MPE enables or disables the "wake-up" feature as follows. If MBE is set to 1, only received bytes in which the MPB (multiprocessor bit) = 1 can affect the RDRF and error flags. Effectively, other bytes (with MPB = 0) are "ignored" by the ASCI. If MPE is reset to 0, all bytes, regardless of the state of the MPB data bit, affect the REDR and error flags. MPE is cleared to 0 during RESET.

RE: Receiver Enable (bit 6). When RE is set to 1, the ASCI transmitter is enabled. When TE is reset to 0, the transmitter is disables and any transmit operation in progress is interrupted. However, the TDRE flag is not reset and the previous contents of TDRE are held. TE is cleared to 0 in IOSTOP mode during RESET.

TE: Transmitter Enable (bit 5). When TE is set to 1, the ASCI receiver is enabled. When TE is reset to 0, the transmitter is disabled and any transmit operation in progress is interrupted. However, the TDRE flag is not reset and the previous contents of TDRE are held. TE is cleared to 0 in IOSTOP mode during RESET.

$\overline{RTS0}$: Request to Send Channel 0 (bit 4 in CNTLA only). If bit 4 of the System Configuration Register is 0, th $\overline{RTS0}$/TxS pin has the $\overline{RTS0}$ function. $\overline{RTS0}$ allows th ASCI to control (start/stop) another communication devic es transmission (for example, by connecting to that de vice's $\overline{CTS}$ input). $\overline{RTS0}$ is essentially a 1 bit output por having no side effects on other ASCI registers or flags.

Bit 4 in CNTLA1 is used.

CKA1D = 1, CKA1/$\overline{TEND_0}$ pin = $\overline{TEND_0}$

CKA1D = 0, CKA1/$\overline{TEND_0}$ pin = CKA1

Cleared to 0 on reset.

MPBR/EFR: Multiprocessor Bit Receive/Error Flag Re set (bit 3). When multiprocessor mode is enabled (MP i CNTLB = 1), MPBR, when read, contains the value of th MPB bit for the last receive operation. When written to 0 the EFR function is selected to reset all error flags (OVRN FE, PE and BRK in the ASEXT Register) to 0. MPBR/EFF is undefined during RESET.

MOD2, 1, 0: ASCI Data Format Mode 2, 1, 0 (bits 2-0). These bits program the ASCI data format as follows.

MOD2
= 0→7 bit data
= 1→8 bit data

MOD1
= 0→No parity
= 1→Parity enabled

MOD0
= 0→1 stop bit
= 1→2 stop bits

The data formats available based on all combinations o MOD2, MOD1, and MOD0 are shown in Table 5-6.

Table 5. Data Formats

MOD2	MOD1	MOD0	Data Format
0	0	0	Start + 7 bit data + 1 stop
0	0	1	Start + 7 bit data + 2 stop
0	1	0	Start + 7 bit data + parity + 1 sto
0	1	1	Start + 7 bit data + parity + 2 sto
1	0	0	Start + 8 bit data + 1 stop
1	0	1	Start + 8 bit data + 2 stop
1	1	0	Start + 8 bit data + parity + 1 sto
1	1	1	Start + 8 bit data + parity + 2 sto

ASCI CHANNEL CONTROL REGISTER B

ASCI Control Register B 0 (CNTLB0: I/O Address = 02H)
ASCI Control Register B 1 (CNTLB1: I/O Address = 03H)

Bit	7	6	5	4	3	2	1	0
	MPBT	MP	$\overline{CTS}$/ PS	PEO	DR	SS2	SS1	SS0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Figure 34. ASCI Channel Control Register B

MPBT: Multiprocessor Bit Transmit (bit 7). When multiprocessor communication format is selected (MP bit = 1), MPBT is used to specify the MPB data bit for transmission. If MPBT = 1, then MPB = 1 is transmitted. If MPBT = 0, then MPB = 0 is transmitted. MPBT state is undefined during and after RESET.

MP: Multiprocessor Mode (bit 6). When MP is set to 1, the data format is configured for multiprocessor mode based on the MOD2 (number of data bits) and MOD0 (number of stop bits) bits in CNTLA. The format is as follows.

Start bit + 7 or 8 data bits + MPB bit + 1 or 2 stop bits

Note that multiprocessor (MP=1) format has no provision for parity. If MP = 0, the data format is based on MOD0, MOD1, MOD2, and may include parity. The MP bit is cleared to 0 during RESET.

$\overline{CTS}$/PS: Clear to Send/Prescale (bit 5). When read, /CTS/PS reflects the state of the external /CTS input. If the /CTS input pin is HIGH, /CTS/PS will be read as 1. Note that when the /CTS input pin is HIGH, the TDRE bit is inhibited (i.e. held at 0). For channel 1, the /CTS input is multiplexed with RXS pin (Clocked Serial Receive Data). Thus, /CTS/PS is only valid when read if the channel CTS1E bit = 1 and the /CTS input pin function is selected The read data of /CTS/PS is not affected by RESET.

If the SS2-0 bits in this register are not 111, and the BRC mode bit in the ASEXT register is 0, then writing to this bi sets the prescale (PS) control as described in the followin "Clock Modes" section. Under those circumstances, a 0 in dicates a divide by 10 prescale function while a 1 indicate divide by 30. The bit resets to 0.

PEO: Parity Even Odd (bit 4). PEO selects oven or odd parity. PEO does not affect the enabling/disabling of parit (MOD1 bit of CNTLA). If PEO is cleared to 0, even parit is selected. If PEO is set to 1, odd parity is selected. PEC is cleared to 0 during RESET.

DR: Divide Ratio (bit 3). If the X1 bit in the ASEXT regis ter is 0, this bit specifies the divider used to obtain bau rate from the data sampling clock. If DR is reset to 0, di vide- by-16 is used, while if DR is set to 1 divide-by-64 i used. DR is cleared to 0 during RESET.

SS2,1,0: Source/Speed Select 2,1,0 (bits 2-0). First, these bits are 111, as they are after a Reset, the CKA pi

is used as a clock input, and is divided by 1, 16, or 64 depending on the DR bit and the X1 bit in the ASEXT register.

If these bits are not 111 and the BRG mode bit is ASEXT is 0, then these bits specify a power-of-two divider for the PHI clock as shown in Table 9.

Setting or leaving these bits as 111 makes sense for a channel only when its CKA pin is selected for the CKA function. CKAO/CKS has the CKAO function when bit 4 of the System Configuration Register is 0. $\overline{DCD0}$/CKA1 has the CKA1 function when bit 0 of the Interrupt Edge registe is 1.

Table 6. Divide Ratio

SS2	SS1	SS0	Divide Ratio
0	0	0	÷1
0	0	1	÷2
0	1	0	÷4
0	1	1	÷8
1	0	0	÷16
1	0	1	÷32
1	1	0	÷64
1	1	1	External Clock

ASCI STATUS REGISTER 0, 1 (STAT0, 1)

Each channel status register allows interrogation of ASCI communication, error and modem control signal status, and enabling or disabling of ASCI interrupts.

ASCI Status Register 0 (STAT0: I/O Address = 04H)

Bit	7	6	5	4	3	2	1	0
	RDRF	OVRN	PE	FE	RE	$\overline{DCD}_0$	TDRE	TIE
	R	R	R	R	R/W	R	R	R/W

ASCI Status Register 1 (STAT1: I/O Address = 05H)

Bit	7	6	5	4	3	2	1	0
	RDRF	OVRN	PE	FE	RE	CTSIE	TDRE	TIE
	R	R	R	R	R/W	R/W	R	R/W

Figure 35. ASCI Status Registers

RDRF: Receive Data Register Full (bit 7). RDRF is set to 1 when an incoming data byte is loaded into an empty Rx FIFO. Note that if a framing or parity error occurs, RDRF is still set and the receive data (which generated the error) is still loaded into the FIFO. RDRF is cleared to 0 by reading RDR and last character in the FIFO from IOSTOP mode, during RESET and for ASCI0 if the /DCD0 input is auto-enabled and is negated (High).

OVRN: Overrun Error (bit 6). An overrun condition occurs if the receiver has finished assembling a character but the Rx FIFO is full so there is no room for the character. However, this status bit is not set until the last character received before the overrun becomes the oldest byte in the FIFO. This bit is cleared when software writes a 1 to the EFR bit in the CNTLA register, and also by Reset, i IOSTOP mode, and for ASCI0 if the /DCD0 pin is auto en abled and is negated (High).

Note that when an overrun occurs, the receiver does nc place the character in the shift register into the FIFO, no any subsequent characters, until the last good characte has come to the top of the FIFO so that OVRN is set, an software then writes a 1 to EFR to clear it.

PE: Parity Error (bit 5). A parity error is detected when parity checking is enabled by the MOD1 bit in the CNT1LA register being 1, and a character has been assembled in which the parity does not match the PEO bit in the CNTLB register. However, this status bit is not set until/unless the error character becomes the oldest one in the RxFIFO. PE is cleared when software writes a 1 to the EFR bit in the CNTRLA register, and also by Reset, in IOSTOP mode, and for ASCI0 if the /DCD0 pin is auto-enabled and is negated (High).

FE: Framing Error (bit 4). A framing error is detected when the stop bit of a character is sampled as 0/Space. However, this status bit is not set until/unless the error character becomes the oldest one in the RxFIFO. FE is cleared when software writes a 1 to the EFR bit in the CNTLA register, and also by Reset, in IOSTOP mode, and for ASCIO if the /DCDO pin is auto-enabled and is negated (High).

REI: Receive Interrupt Enable (bit 3). RIE should be set to 1 to enable ASCI receive interrupt requests. When RIE is 1, the Receiver requests an interrupt when a character is received and RDRF is set, but only if neither DMA channel has its Request-routing field set to receive data from this ASCI. That is, if SM1-0 are 11 and SAR17-16 are 10, or DIM1 is 1 and IAR17-16 are 10, then ASCI1 doesn't request an interrupt for RDRF. If RIE is 1, either ASCI requests an interrupt when OVRN, PE or FE is set, and ASCI0 requests an interrupt when /DCD0 goes High. RIE is cleared to 0 by Reset.

$\overline{DCD0}$: Data Carrier Detect (bit 2 STAT0). This bit is se to 1 when the pin is High. It is cleared to 0 on the first rea of STAT0 following the pin's transition from High to Lov and during RESET. Bit 6 of the ASEXT0 register is 0 to se lect auto-enabling, and the pin is negated (High). Channe 1 has an external $\overline{CTS1}$ input which is multiplexed with th receive data pin RSX for the CSI/O.

Bit 2 = 0; Select RXS function.

Bit 2 = 1; Select $\overline{CTS1}$ function.

TDRE: Transmit Data Register Empty (bit 1). TDRE = indicates that the TDR is empty and the next transmit dat byte is written to TDR. After the byte is written to TDR TDRE is cleared to 0 until the ASCI transfers the byte fron TDR to the TSR and then TDRE is again set to 1. TDRE i set to 1 in IOSTOP mode and during RESET. On ASCIO if the $\overline{CTS0}$ pin is auto-enabled in the ASEXT0 register and the pin is High, TDRE is reset to 0.

TIE: Transmit Interrupt Enable (bit 0). TIE should be se to 1 to enable ASCI transmit interrupt requests. If TIE = 1 an interrupt will be requested when TDRE = 1. TIE i cleared to 0 during RESET.

ASCI TRANSMIT DATA REGISTERS

Register addresses 06H and 07H hold the ASCI transmit data for channel 0 and channel 1, respectively.

Channel 0

Mnemonics TDR0

Address (06H)

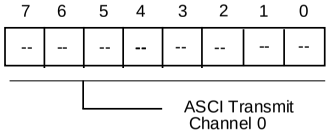


Figure 36. ASCI Register

Channel 1

Mnemonics TDR1

Address (07H)

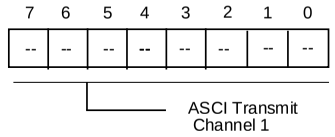


Figure 37. ASCI Register

ASCI Receive Register

Register addresses 08H and 09H hold the ASCI receive data for channel 0 and channel 1, respectively.

Channel 0

Mnemonics TSR0 --

Address (08H)

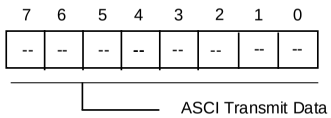


Figure 38. ASCI Receive Register Channel 0

Channel 1--

Mnemonics TSR1

Address (09H)

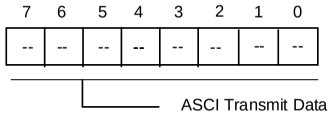


Figure 39. ASCI Receive Register Channel 1R

CSI/O CONTROL/STATUS REGISTER

(CNTR: I/O Address = 0AH). CNTR is used to monitor CSI/O status, enable and disable the CSI/O, enable and disable interrupt generation, and select the data cloc speed and source.

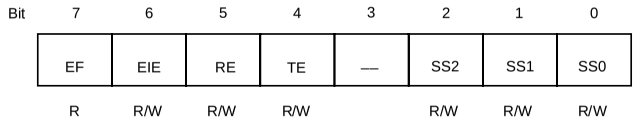


Figure 40. CSI/O Control Register

EF: End Flag (bit 7). EF is set to 1 by the CSI/O to indicate completion of an 8-bit data transmit or receive operation. If EIE (End Interrupt Enable) bit = 1 when EF is set to 1, a CPU interrupt request is generated. Program access of TRDR only occurs if EF = 1. The CSI/O clears EF to 0 when TRDR is read or written. EF is cleared to 0 during RESET and IOSTOP mode.

EIE: End Interrupt Enable (bit 6). EIE is set to 1 to generate a CPU interrupt request. The interrupt request is inhibited if EIE is reset to 0. EIE is cleared to 0 during RESET.

RE: Receive Enable (bit 5). A CSI/O receive operation is started by setting RE to 1. When RE is set to 1, the data clock is enabled. In internal clock mode, the data clock is output from the CKS pin. In external clock mode, the clock is input on the CKS pin. In either case, data is shifted in on the RXS pin in synchronization with the (internal or external) data clock. After receiving 8 bits of data, the CSI/O automatically clears RE to 0, EF is set to 1, and an interrupt (if enabled by EIE = 1) is generated. RE and TE are neve both set to 1 at the same time. RE is cleared to 0 durin RESET and ISTOP mode.

Transmit Enable (bit 4). A CSI/O transmit operation is started by setting TE to 1. When TE is set to 1, the data clock is enabled. When in internal clock mode, the data clock is output from the CKS pin. In external clock mode, the clock is input on the CKS pin. In either case, data is shifted out on the TXS pin synchronous with the (internal or external) data clock. After transmitting 8 bits of data, the CSI/O automatically clears TE to 0, EF is set to 1, and an interrupt (if enabled by EIE = 1) is generated. TE and RE are never both set to 1 at the same time. TE is cleared to 0 during RESET and IOSTOP mode.

SS2, 1, 0: Speed Select 2, 1, 0 (bits 2-0). SS2, SS1 and SS0 select the CSI/O transmit/receive clock source and speed. SS2, SS1 and SS0 are all set to 1 during RESET. Table 10 shows CSI/O Baud Rate Selection.

Table 7. CSI/O Baud Rate Selection

SS2	SS1	SS0	Divide Ratio
0	0	0	÷20
0	0	1	÷40
0	1	0	÷80
0	1	1	÷160
1	0	0	÷320
1	0	1	÷640
1	1	0	÷1280
1	1	1	External Clock Input (less than ÷20.)

After RESET, the CKS pin is configured as an external clock input (SS2, SS1, SS0 = 1). Changing these values causes CKS to become an output pin and the selected clock is output when transmit or receive operations are enabled.

CSI/O Transmit/Receive Data Register

(TRDR: I/O Address = 0BH).

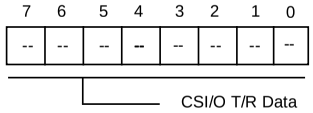


Figure 41. CSI/O Transmit/Receive Data Register 1R

Timer Reload Register 0L

RLDR0L

Timer Data Register Channel 0L

TMDR0L

0CH

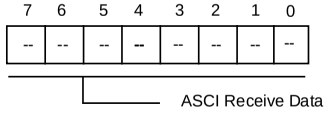


Figure 42. Timer Register Channel OL

Timer Data Register Channel 0H

TMDR0H

0D H

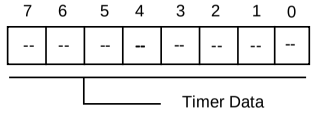


Figure 43. Timer Data Register Channel OH

0E H

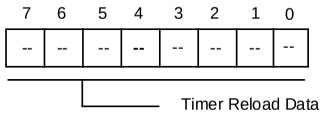


Figure 44. Timer Reload Register Low

Timer Reload Register 0H

RLDR0H

0F H

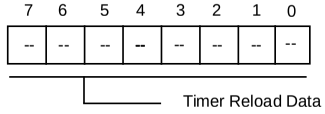


Figure 45. Timer Reload Register Channel

TIMER CONTROL REGISTER (TCR)

TCR monitors both channels (PRT0, PRT1) TMDR status. It also controls enabling and disabling of down counting and interrupts along with controlling output pin A18/TOU for PRT1.

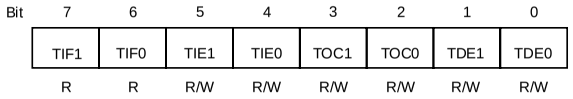


Figure 46. Timer Control Register (TCR: I/O Address = 10H)

TIF1: Timer Interrupt Flag 1 (bit 7). When TMDR1 decrements to 0, TIF1 is set to 1. This generates an interrupt request if enabled by TIE1 = 1. TIF1 is reset to 0 when TCR is read and the higher or lower byte of TMDR1 is read. During RESET, TIF1 is cleared to 0.

TIF0: Timer Interrupt Flag 0 (bit 6). When TMDR0 decrements to 0, TIF0 is set to 1. This generates an interrupt request if enabled by TIE0 = 1. TIF0 is reset to 0 when TCR is read and the higher or lower byte of TMDR0 is read. During RESET, TIF0 is cleared to 0.

TIE1: Timer Interrupt Enable 1 (bit 5). When TIE0 is set to 1, TIF1 = 1 generates a CPU interrupt request. When TIE0 is reset to 0, the interrupt request is inhibited. During RESET, TIE0 is cleared to 0.

TOC1, 0: Timer Output Control (bits 3, 2). TOC1 an TOC0 control the output of PRT1 using the multiplexe TOUT/DREQ pin as shown in Table 11. During RESET TOC1 and TOC0 are cleared to 0. If bit 3 of the IAR1B reg ister is 1, the TOUT function is selected. By programmin TOC1 and TOC0, the TOUT/DREQ pin can be force High, Low, or toggled when TMDR1 decrements to 0.

Table 8. Timer Output Control

TOC1	TOC0		Output
0	0	Inhibited	The TOUT/DREQ pin is not affected by the PRT.
0	1	Toggled	If bit 3 of IAR1B is 1, the TOUT/DREQ pin is toggles or set Low or High as indicated.
1	0	0	
1	1	1	

TDE1, 0: Timer Down Count Enable (bits 1, 0). TDE1 and TDE0 enable and disable down counting for TMDR1 and TMDR0, respectively. When TDEn (n = 0, 1) is set to 1, down counting is stopped and TMDRn is freely read o written. TDE1 and TDE0 are cleared to 0 during RESE and TMDRn will not decrement until TDEn is set to 1.

ASCI EXTENSION CONTROL REGISTER CHANNEL 0 (ASEXT0) AND CHANNEL 1 (ASEXT1)

Note: This register controls functions that have been added to the ASCIs in the Z80180/Z8S180/Z8L180 family.
Note: All bits in this register reset to zero.

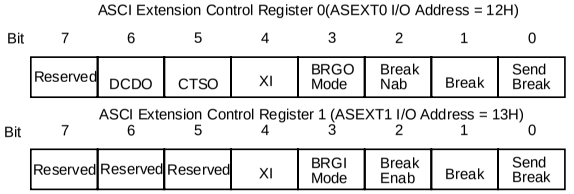


Figure 47. ASCI Extension Control Registers, Channel 0 and 1

DCD0 dis (bit 6, ASCI0 only). If this bit is 0, then the $\overline{DCD0}$ pin "auto-enables" the ASCI0 receiver, such that when the pin is negated/High, the Receiver is held in a RESET state. The state of the $\overline{DCD}$-pin has no effect on receiver operation. In either state of this bit, software can read the state of the $\overline{DCD0}$ pin in the STAT0 register, and the receiver will interrupt on a rising edge of $\overline{DCD0}$.

CTS0 dis (bit 5, ASCI0 only). If this bit is 0, then the $\overline{CTS0}$ pin "auto-enables" the ASCIO transmitter, in that when the pin is negated/high, the TDRE bit in the STAT0 register is forced to 0. If this bit is 1, the state of the $\overline{CTS0}$ pin has no effect on the transmitter. Regardless of the state of this bit, software can read the state of the $\overline{CTS0}$ pin the CNTLB0 register.

X1 (bit 4). If this bit is 1, the clock from the Baud Rate Generator or CKA pin is taken as a "1X" bit clock (this is sometimes called "isochronous" mode). In this mode, receive data on the RXA pin must be synchronized to the clock on the CKA pin, regardless of whether CKA is an input or an output. If this bit is 0, the clock from the Baud Rate Generator or CKA pin is divided by 16 or 64 per the DR bit in CNTLB register, to obtain the actual bit rate. In this mode, receive data on the RxA pin need not be synchronized to a clock.

BRG Mode (bit 3). If the SS2-0 bits in the CNTLB register are not 111, and this bit is 0, this ASCI's Baud Rate Generator divides PHI by 10 or 30, depending on the DR bit in CNTLB, and then by a power of two selected by the SS2-0 bits, to obtain the clock that is presented to the transmit ter and receiver and that can be output on the CKA pin. SS2-0 are not 111, and this bit is 1, the Baud Rate Gener ator divides PHI by twice (the 16-bit value programme into the Time Constant Registers, plus two). This mode i identical to the operation of the baud rate generator in th ESCC.

Break Enable (bit 2). If this bit is 1, the receiver will detec Break conditions and report them in bit 1, and the transmit ter will send Breaks under the control of bit 0.

Break Detect (bit 1). The receiver sets this read-only b to 1 when an all-zero character with a Framing Error be comes the oldest character in the Rx FIFO. The bit i cleared when software writes a 0 to the EFR bit in CNTL register, also by Reset, by IOSTOP mode, and for ASCI if the $\overline{DCD0}$ pin is auto-enabled and is negated (high).

Send Break (bit 0). If this bit and bit 2 are both 1, the trans mitter holds the TXA pin low to send a Bread condition The duration of the Bread is under software control (one c the PRTs or CTCs can be used to time it). This bit reset to 0, in which state TXA carries the serial output of th transmitter.

Timer Data Register Channel 1L

Mnemonic TMDR1L

Address 14

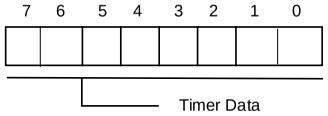


Figure 48. Timer Data Register 1L

Timer Data Register Channel 1H

Mnemonic TMDR1H

Address 15

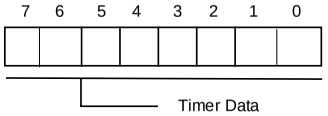


Figure 49. Timer Data Register 1H

Timer Reload Register Channel 1L

Mnemonic RLDR1L

Address 16

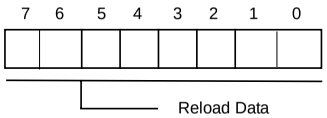


Figure 50. Timer Reload Channel 1L

Timer Reload Register Channel 1L

Mnemonic RLDR1H

Address 17

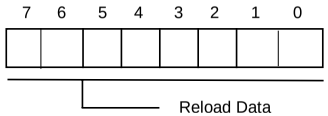


Figure 51. Timer Relaod Register Channel 1L

Free Running Counter (Read Only)

Mnemonic FRC

Address 18

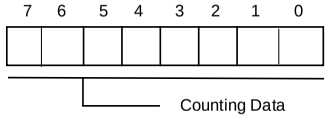


Figure 52. Free Running Counter

ASCI TIME CONSTANT REGISTERS

If the SS2-0 bits of the CNTLA register are not 111, and the BRG Mode bit in the ASEXT register is 1, the ASCI divides the PHI clock by twice (the 16-bit value in these registers, plus two), to obtain the clock that is presented to the transmitter and receiver for division by 1, 16, or 64 and that can be output on the CKA1 pin.

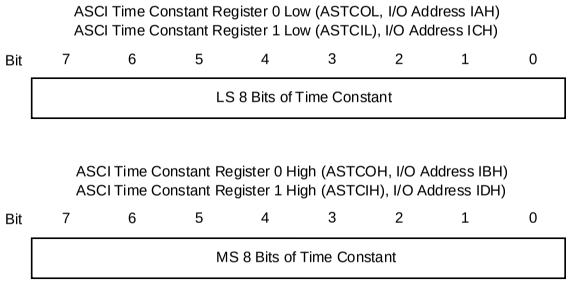


Figure 53. ASCI Time Constant Registers

CLOCK MULTIPLIER REGISTER (Z180 MPU ADDRESS 1EH)

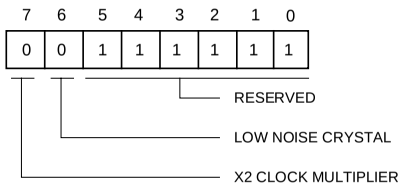


Figure 54. Clock Multiplier Register

Bit 7. X2 Clock Multiplier Mode. When this bit is set to 1, this allows the programmer to double the internal clock from that of the external clock. This feature will only operated effectively with frequencies of 10-16 MHz (20-32MHz internal). When this bit is set to 0, the Z80180/Z8S180/Z8L180 device will operate in normal mode. Upon powerup, this feature is disabled.

Bit 6. Low Noise Crystal Option. Setting this bit to 1 will enable the low noise option for the EXTAL and XTAL pins. This option reduces the gain, in addition to reduction the output drive capability to 30% of its original drive capability. The Low Noise Crystal Option is recommended in the use of crystals for PCMCIA applications where the crystal may be driven too hard by the oscillator. Setting this bit to 0 will select for normal operation of the EXTAL and XTAL pins. The default for this bit is 0.

Note: Operating restrictions for device operation are listed below. If low noise option is required, and normal device operation is needed, use the clock multiplier feature.

Table 9. Low Noise Option

Low Noise ADDR 1E, bit 6=1	Normal ADDR 1E, bit 6=0
20 MHz @ 4.5V, 100°C	33 MHz @ 4.5V, 100°C
10 MHz @ 3.0V, 100°C	20 MHz @ 3.0V, 100°C

DMA SOURCE ADDRESS REGISTER CHANNEL 0

(SAR0: I/O Address = 20H to 22H) specifies the physical source address for channel 0 transfers. The register contains 20 bits and can specify up to 1024 KB memory addresses or up to 64 KB I/O addresses. Channel 0 source can be memory, I/O, or memory mapped I/O. For I/O, the MS bits of this register identify the Request Handshake signal.

DMA Source Address Register, Channel 0L

Mnemonic SAR0L

Address 20

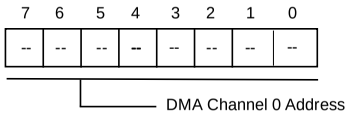


Figure 55. DMA Source Address Register 0L

DMA Source Address Register Channel 0B

Mnemonics SAR0B

Address 22

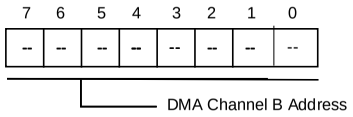


Figure 57. DMA Source Address Register 0B

DMA Source Address Register, Channel 0H

Mnemonic SAR0H

Address 21

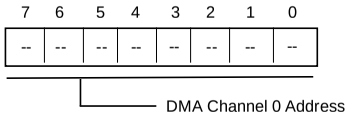


Figure 56. DMA Source Address Register 0H

DMA DESTINATION ADDRESS REGISTER CHANNEL 0

(DAR0: I/O Address = 23H to 25H) specifies the physical destination address for channel 0 transfers. The register con tains 20 bits and can specify up to 1024 KB memory addresses or up to 64 KB I/O addresses. Channel 0 destination ca be memory, I/O, or memory mapped I/O. For I/O, the MS bits of this register identify the Request Handshake signal fo channel 0.

DMA Destination Address Register Channel 0L

Mnemonic DAR0L

Address 23

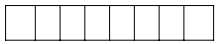


Figure 58. DMA Destination Address Register Channel 0L

DMA Destination Address Register Channel 0H

Mnemonic DAR0H

Address 24

Figure 59. DMA Destination Address Register Channel 0H

DMA Destination Address Register Channel 0B

Mnemonic DAR0B

Address 25

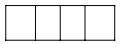


Figure 60. DMA Destination Address Register Channel 0B

Note: In the R1 and Z Mask, these DMA registers ar expanded from 4 bit to 3 bits in the package version of CP 68

A19*	A18	A17	A16	DMA Transfer Request
X	X	0	0	DREQ0
X	X	0	1	TDR0 (ASCI0)
X	X	1	0	TDR1 (ASCI1)
X	X	1	1	Not Used

DMA BYTE COUNT REGISTER CHANNEL 0

(BCRO: I/O Address = 26H to 27H) specifies the number of bytes to be transferred. This register contains 16 bits and ma specify up to 64 KB transfers. When one byte is transferred, the register is decremented by one. If “n” bytes should b transferred, “n” must be stored before the DMA operation.

Note: All DMA Count Register channels are undefined during reset.

DMA Byte Count Register Channel 0L

Mnemonic BCR0L

Address 26

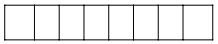


Figure 61. DMA Byte Count Register 0L

DMA Byte Count Register Channel 0H

Mnemonic BCR0H

Address 27

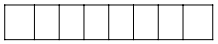


Figure 62. DMA Byte Count Register 0H

DMA Byte Count Register Channel 1L

Mnemonic BCR1L

Address 2E

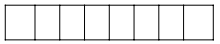


Figure 63. DMA Byte Count Register 1L

DMA Byte Count Register Channel 0H

Mnemonic BCR1H

Address 2F

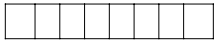


Figure 64. DMA Byte Count Register 0H

DMA MEMORY ADDRESS REGISTER CHANNEL 1

(MAR1: I/O Address = 28H to 2AH) specifies the physical memory address for channel 1 transfers. This may be destina tion or source memory address. The register contains 20 bits and may specify up to 1024 KB memory address.

DMA Memory Address Register, Channel 1L

Mnemonic MAR1L

Address 28

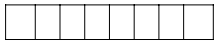


Figure 65. DMA Memory Address Register, Channel 1L

DMA Memory Address Register, Channel 1B

Mnemonic MAR1B

Address 2A

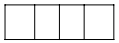


Figure 67. DMA Memory Address Register, Channel 1B

DMA Memory Address Register, Channel 1H.

Mnemonic MAR1H

Address 29

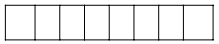


Figure 66. DMA Memory Address Register, Channel 1H

DMA I/O ADDRESS REGISTER CHANNEL 1

(IAR1: I/O Address = 2BH to 2DH) specifies the I/O address for channel 1 transfers. This may be destination or source I/O address. The register contains 16 bits of I/O address; its most significant byte identifies the Request Handshake signal and controls the Alternating Channe feature.

All bits in IAR1B reset to 0.

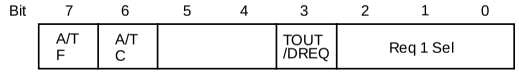


Figure 68. IAR MS Byte Register (IARIB: I/O Address 2DH)

DMA I/O Address Register Channel 1L

Mnemonic IAR1L

Address 2B

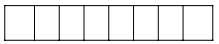


Figure 69. DMA I/O Address Register Channel 1L

DMA I/O Address Register Channel 1H

Mnemonic IAR1H

Address 2C

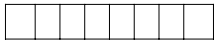


Figure 70. DMA I/O Address Register Channel 1H

DMA I/O Address Register Channel 1B

Mnemonic IAR1B

Address 2D

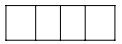


Figure 71. DMA I/O Address Register Channel 1B

DMA STATUS REGISTER (DSTAT)

DSTAT is used to enable and disable DMA transfer and DMA termination interrupts. DSTAT also indicates DMA transfer status, in other words, completed or in progress.

Mnemonic DSTAT

Address 30

Bit	7	6	5	4	3	2	1	0
	DE1	DE0	$\overline{DWE1}$	$\overline{DWE0}$	DIE1	DIE0	—	DME
	R/W	R/W	W	W	R/W	R/W		R

Figure 72. DMA Status Register (DSTAT: I/O Address = 30H)

DE1: DMA Enable Channel 1 (bit 7). When DE1 = 1 and DME = 1, channel 1 DMA is enabled. When a DMA transfer terminates (BCR1 = 0), DE1 is reset to 0 by the DMAC. When DE1 = 0 and the DMA interrupt is enabled (DIE1 = 1), a DMA interrupt request is made to the CPU.

To perform a software write to DE1, DWE1 should be written with 0 during the same register write access. Writing DE1 to 0 disables channel 1 DMA, but DMA is restartable. Writing DE1 to 1 enables channel 1 DMA and automatically sets DME (DMA Main Enable) to 1. DE1 is cleared to 0 during RESET.

DE0: DMA Enable Channel 0 (bit 6). When DE0 = 1 and DME = 1, channel 0 DMA is enabled. When a DMA transfer terminates (BCR0 = 0), DE0 is reset to 0 by the DMAC. When DE0 = 0 and the DMA interrupt is enabled (DIE0 = 1), a DMA interrupt request is made to the CPU.

To perform a software write to DE0, DWE0 should be written with 0 during the same register write access. Writing DE0 to 0 disables channel 0 DMA. Writing DE0 to 1 enables channel 0 DMA and automatically sets DME (DMA Main Enable) to 1. DE0 is cleared to 0 during RESET.

$\overline{DWE1}$: DE1 Bit Write Enable (bit 5). When performing any software write to DE1, DWE1 should be written with 0 during the same access. DWE1 always reads as 1.

$\overline{DWE0}$: DE0 Bit Write Enable (bit 4). When performing any software write to DE0, DWE0 should be written with 0 during the same access. DWE0 always reads as 1.

DIE1: DMA Interrupt Enable Channel 1 (bit 3). When DIE0 is set to 1, the termination channel 1 DMA transfe (indicated when DE1 = 0) causes a CPU interrupt reques to be generated. When DIE0 = 0, the channel 0 DMA ter mination interrupt is disabled. DIE0 is cleared to 0 during RESET.

DIE0: DMA Interrupt Enable Channel 0 (bit 2). When DIE0 is set to 1, the termination channel 0 of DMA transfe (indicated when DE0=0) causes a CPU interrupt request t be generated. When DIE0=0, the channel 0 DMA termina tion interrupt is disabled. DIE0 is cleared to 0 during RE SET.

DME: DMA Main Enable (bit 0). A DMA operation is onl enabled when its DE bit (DE0 for channel 0, DE1 for chan nel 1) and the DME bit is set to 1.

When $\overline{NMI}$ occurs, DME is reset to 0, thus disabling DMA activity during the $\overline{NMI}$ interrupt service routine. To restar DMA, DE- and/or DE1 should be written with 1 (even if the contents are already 1). This automatically sets DME to 1 allowing DMA operations to continue. Note that DME can not be directly written. It is cleared to 0 by $\overline{NMI}$ or indirectly set to 1 by setting DE0 and/or DE1 to 1. DME is cleared to 0 during RESET.

DMA MODE REGISTER (DMODE).

DMODE is used to set the addressing and transfer mode for channel 0.

Mnemonic DMODE

Address 31H

Bit	7	6	5	4	3	2	1	0
	—	—	DM1	DM0	SM1	SM0	MMOD	—
			R/W	R/W	R/W	R/W	R/W	

Figure 73. DMA Mode Register (DMODE: I/O Address = 31H)

DM1, DM0: Destination Mode Channel 0 (bits 5,4) specifies whether the destination for channel 0 transfers is memory or I/O, and whether the address should be incremented or decremented for each byte transferred. DM1 and DM0 are cleared to 0 during RESET.

Table 10. Channel 0 Destination

DM1	DM0	Memory I/O	Memory Increment/Decrement
0	0	Memory	+1
0	1	Memory	–1
1	0	Memory	fixed
1	1	I/O	fixed

SM1, SM0: Source Mode Channel 0 (bits 3, 2) specifies whether the source for channel 0 transfers is memory o I/O, and whether the address should be incremented o decremented for each byte transferred.

Table 11. Channel 0 Source

SM1	SM0	Memory I/O	Memory Increment/Decrement
0	0	Memory	+1
0	1	Memory	–1
1	0	Memory	fixed
1	1	I/O	fixed

Table 12 shows all DMA transfer mode combinations of DM0, DM1, SM0, and SM1. Since I/O to/from I/O transfers are not implemented, 12 combinations are available.

Table 12. Transfer Mode Combinations

DM1	DM0	SM1	SM0	Transfer Mode	Address Increment/Decrement
0	0	0	0	Memory→Memory	SAR0+1, DAR0+1
0	0	0	1	Memory→Memory	SAR0–1, DAR0+1
0	0	1	0	Memory*→Memory	SAR0 fixed, DAR0+1
0	0	1	1	I/O→Memory	SAR0 fixed, DAR0+1
0	1	0	0	Memory→Memory	SAR0+1, DAR0–1
0	1	0	1	Memory→Memory	SAR0–1, DAR0–1
0	1	1	0	Memory*→Memory	SAR0 fixed, DAR0–1
0	1	1	1	I/O→Memory	SAR0 fixed, DAR0–1
1	0	0	0	Memory→Memory*	SAR0+1, DAR0 fixed
1	0	0	1	Memory→Memory*	SAR0–1, DAR0 fixed
1	0	1	0	Reserved	
1	0	1	1	Reserved	
1	1	0	0	Memory→I/O	SAR0+1, DAR0 fixed
1	1	0	1	Memory I/O	SAR0–1, DAR0 fixed
1	1	1	0	Reserved	
1	1	1	0	Reserved	

Note: * Includes memory mapped I/O.

MMOD: Memory Mode Channel 0 (bit). When channel 0 is configured for memory to/from memory transfers there is no Request Handshake signal to control the transfer timing. Instead, two automatic transfer timing modes are selectable: burst (MMOD = 1) and cycle steal (MMOD = 0). For burst memory to/from memory transfers, the DMAC takes control of the bus continuously until the DMA transfer completes (as shown by the byte count register = 0). In cycle steal mode, the CPU is given a cycle for each DMA byte transfer cycle until the transfer is completed.

For channel 0 DMA with I/O source or destination, the se lected Request signal times the transfer and thus MMOI is ignored. MMOD is cleared to 0 during RESET.

DMA/WAIT CONTROL REGISTER (DCNTL)

DCNTL controls the insertion of wait states into DMAC (and CPU) accesses of memory or I/O. Also, it defines the Request signal for each channel as level or edge sense.

DCNTL also sets the DMA transfer mode for channel 1 which is limited to memory to/from I/O transfers.

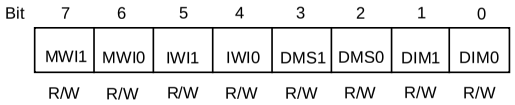


Figure 74. DMA/WAIT Control Register (DCNTL: I/O Address = 32H)

MWI1, MWI0: Memory Wait Insertion (bits 7-6). Specifies the number of wait states introduced into CPU or DMAC memory access cycles. MWI1 and MWI0 are set to 1 during RESET.

MWI1	MWI0	Wait State
0	0	0
0	1	1
1	0	2
1	1	3

IWI1, IWI0: I/O Wait Insertion (bits 5-4). Specifies the number of wait states introduced into CPU or DMAC I/O access cycles. IWI1 and IWI0 are set to 1 during RESET. See the section on Wait-State Generation for details.

IWI1	IWI0	Wait State
0	0	0
0	1	2
1	0	3
1	1	4

DMS1, DMS0: DMA Request Sense (bits 3-2). DMS and DMS0 specify the DMA request sense for channel and channel 1 respectively. When reset to 0, the input i level sense. When set to 1, the input is edge sense. DMS and DMS0 are cleared to 0 during RESET.

DMSi	Sense
1	Edge Sense
0	Level Sense

Typically, for an input/source device, the associated DM bit should be programmed as 0 for level sense becaus the device has a relatively long time to update its Reques signal after the DMA channel reads data from it in the firs of the two machine cycles involved in transferring a byte.

An output/destination device has much less time to updat its Request signal, after the DMA channel starts a write op eration to it, as the second machine cycle of the two cycle involved in transferring a byte. With zero-wait state I/O cy cles, which apply only to the ASCIs, it is impossible for device to update its Request signal in time, and edge sens ing must be used.

With one-wait-state I/O cycles (the fastest possible except for the ASCIs), it is unlikely that an output device will be able to update its Request in time, and edge sense is required.

DIM1, DIM0: DMA Channel 1 I/O and Memory Mode (bits 1-0). Specifies the source/destination and address modifier for channel 1 memory to/from I/O transfer modes DIM1 and DIM0 are cleared to 0 during RESET.

Table 13. Channel 1 Transfer Mode

DIM1	DMI0	Transfer Mode	Address Increment/Decrement
0	0	Memory→I/O	MAR1 +1, IAR1 fixed
0	1	Memory→I/O	MAR1–1, IAR1 fixed
1	0	I/O→Memory	IAR1 fixed, MAR1 + 1
1	1	I/O→Memory	IAR1 fixed, MAR1 –1

INTERRUPT VECTOR LOW REGISTER

Mnemonic: IL

Address 33

Bits 7-5 of IL are used as bits 7-5 of the synthesized interrupt vector during interrupts for the $\overline{INT1}$ and $\overline{INT2}$ pins and for the DMAs, ASCIs, PRTs, and CSI/O. These three bits are cleared to 0 during Reset (Figure 75).

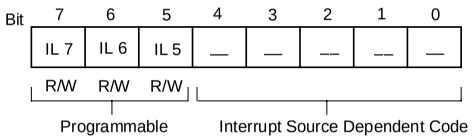


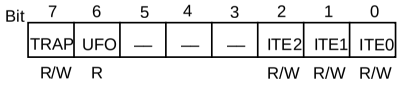
Figure 75. Interrupt Vector Low Register (IL: I/O Address = 33H)

INT/TRAP CONTROL REGISTER

Mnemonics ITC

Address 34

INT/TRAP Control Register (ITC, I/O Address 34H). This register is used in handling TRAP interrupts and to enable or disable Maskable Interrupt Level 0 and the $\overline{INT1}$ and $\overline{INT2}$ pins.



TRAP (bit 7). This bit is set to 1 when an undefined Opcode is fetched. TRAP can be reset under program control by writing it with a 0, however, it cannot be written with 1 under program control. TRAP is reset to 0 during RESET.

UFO: Undefined Fetch Object (bit 6). When a TRAP interrupt occurs, the contents of UFO allow determination of the starting address of the undefined instruction. This is necessary since the TRAP may occur on either the second or third byte of the Opcode. UFO allows the stacked PC value to be correctly adjusted. If UFO = 0, the first Opcode should be interpreted as the stacked PC-1. If UFO = 1, the first Opcode address is stacked PC-2. UFO is Read-Only

ITE2, 1, 0: Interrupt Enable 2, 1, 0 (bits 2-0). ITE2 and ITE1 enable and disable the external interrupt inputs /INT2 and /INT1, respectively. ITE0 enables and disables interrupts from the on-chip ESCC, CTCs and Bidirectional Centronics controller as well as the external interrupt input /INT0. A 1 in a bit enables the corresponding interrupt level while a 0 disables it. A Reset sets ITE0 to 1 and clears ITE1 and ITE2 to 0.

TRAP Interrupt. The Z80180/Z8S180/Z8L180 generates a non-maskable (not affected by the state of IEF1) TRAP interrupt when an undefined Opcode fetch occurs. This feature can be used to increase software reliability, implement an "extended" instruction set, or both. TRAP may occur during Opcode fetch cycles and also if an undefined

Opcode is fetched during the interrupt acknowledge cycle for $\overline{INT}_0$ when Mode 0 is used.

When a TRAP interrupt occurs, the Z80180/Z8S180/Z8L180 operates as follows:

1. The TRAP bit in the Interrupt TRAP/Control (ITC) register is set to 1.
2. The current PC (Program Counter) value, reflecting the location of the undefined Opcode, is saved on the stack.
3. The Z80180/Z8S180/Z8L180 vectors to logical address 0. Note that if logical address 0000H is mapped to physical address 00000H, the vector is the same as for RESET. In this case, testing the TRAP bit in ITC will reveal whether the restart at physica address 00000H was caused by RESET or TRAP.

All TRAP interrupts occur after fetching an undefined second Opcode byte following one of the "prefix" Opcodes CBH, DDH, EDH, or FDH, or after fetching an undefined third Opcode byte following one of the "double prefix" Opcodes DDCBH or FDCBH.

The state of the Undefined Fetch Object (UFO) bit in ITC allows TRAP software to correctly "adjust" the stacked PC depending on whether the second or third byte of the Opcode generated the TRAP. If UFO=0, the starting address of the invalid instruction is equal to the stacked PC-1. If UFO=1, the starting address of the invalid instruction is equal to the stacked PC-2.

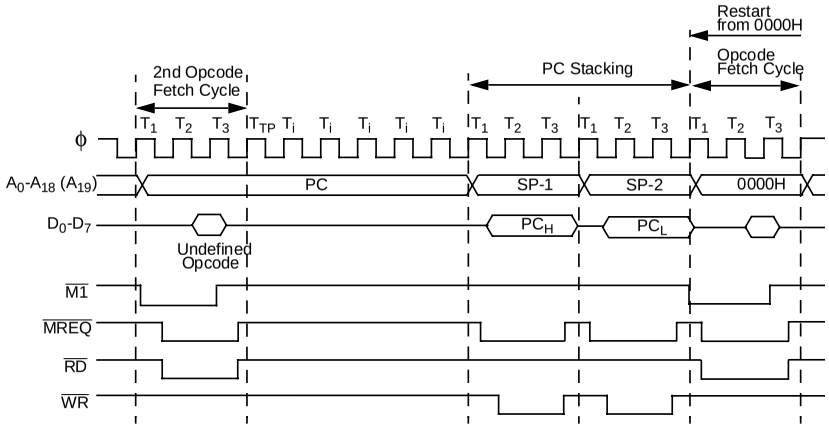


Figure 76. TRAP Timing-2nd Opcode Undefined

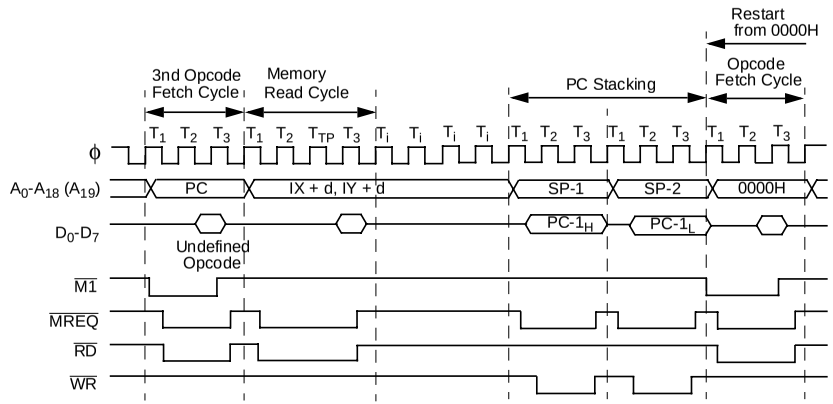


Figure 77. TRAP Timing-3rd Opcode Undefined

REFRESH CONTROL REGISTER

Mnemonic RCR

Address 36

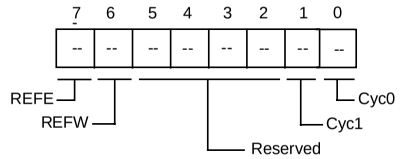


Figure 78. Refresh Control Register (RCA: I/O Address = 36H)

The RCR specifies the interval and length of refresh cycles, while enabling or disabling the refresh function.

REFE: Refresh Enable (bit 7). REFE = disables the re fresh controller while REFE = 1 enables refresh cycle in sertion. REFE is set to 1 during RESET.

REFW: Refresh Wait (bit 6). REFW = 0 causes the re fresh cycle to be two clocks in duration. REFW = 1 cause the refresh cycle to be three clocks in duration by adding refresh wait cycle (TRW). REFW is set to 1 during RESET

CYC1, 0: Cycle Interval (bit 1,0). CYC1 and CYC0 spec ify the interval (in clock cycles) between refresh cycles. I the case of dynamic RAMs requiring 128 refresh cycles ev ery 2 ms (0r 256 cycles in every 4 ms), the required refresh interval is less than or equal to 15.625 µs. Thus, the under lined values indicate the best refresh interval depending on CPU clock frequency. CYC0 and CYC1 are cleared t 0 during RESET (see Table 14).

Table 14. DRAM Refresh Intervals

CYC1	CYC0	Insertion Interval	Time Interval Ø: 10 MHz	8 MHz	6 MHz	4 MHz	2.5 MHz
0	0	10 states	(1.0 µs)*	(1.25 µs)*	1.66 µs	2.5 µs	4.0 µs
0	1	20 states	(2.0 µs)*	(2.5 µs)*	3.3 µs	5.0 µs	8.0 µs
1	0	40 states	(4.0 µs)*	(5.0 µs)*	6.6 µs	10.0 µs	16.0 µs
1	1	80 states	(8.0 µs)*	(10.0 µs)*	13.3 µs	20.0 µs	32.0 µs

Note: *calculated interval

Refresh Control and Reset. After RESET, based on the initialized value of RCR, refresh cycles will occur with an interval of 10 clock cycles and be 3 clock cycles in duration.

Dynamic RAM Refresh Operation

1. Refresh Cycle insertion is stopped when the CPU is in the following states:
   a. During RESET
   b. When the bus is released in response to $\overline{BUSREQ}$.
   c. During SLEEP mode.
   d. During $\overline{WAIT}$ states.
2. Refresh cycles are suppressed when the bus is released in response to $\overline{BUSREQ}$. However, the refresh timer continues to operate. Thus, the time at which the first refresh cycle occurs after th Z80180/Z8S180/Z8L180 re-acquires the bus depends on the refresh timer and has no timing relationship wit the bus exchange.
3. Refresh cycles are suppressed during SLEEP mode If a refresh cycle is requested during SLEEP mode the refresh cycle request is internally "latched" (unt replaced with the next refresh request). The "latched refresh cycle is inserted at the end of the first machin cycle after SLEEP mode is exited. After this initia cycle, the time at which the next refresh cycle occur depends on the refresh time and has no relationshi with the exit from SLEEP mode.
4. The refresh address is incremented by one for eac successful refresh cycle, not for each refresh. Thus independent of the number of "missed" refres requests, each refresh bus cycle will use a refres address incremented by one from that of the previou refresh bus cycles.

MMU COMMON BASE REGISTER

Mnemonic CBR

Address 38

MMU Common Base Register (CBR). CBR specifies th base address (on 4 KB boundaries) used to generate a 20 bit physical address for Common Area 1 accesses. All bit of CBR are reset to 0 during RESET.

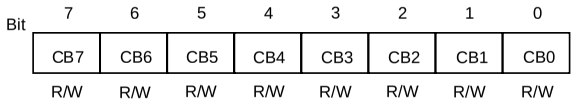


Figure 79. MMU Common Base Register (BBR: I/O Address = 38H)

MMU BANK BASE REGISTER (BBR).

Mnemonic BBR

Address 39

BBR specifies the base address (on 4 KB boundaries used to generate a 19-bit physical address for Bank Area accesses. All bits of BBR are reset to 0 during RESET.

Bit	7	6	5	4	3	2	1	0
	BB7	BB6	BB5	BB4	BB3	BB2	BB1	BB0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Figure 80. MMU Bank Base Register (BBR: I/O Address = 39H)

MMU COMMON/BANK AREA REGISTER (CBAR).

Mnemonic CBAR

Address 3A

CBAR specifies boundaries within the Z80180/Z8S180/Z8L180 64 KB logical address space fo up to three areas; Common Area), Bank Area and Com mon Area 1.

MMU Common/Bank Area Register (CBAR: I/O Address = 3 AH)

Bit	7	6	5	4	3	2	1	0
	CA3	CA2	CA1	CA0	BA3	BA2	BA1	BA0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Figure 81. MMU Common/Bank Area Register (CBAR: I/O Address = 3 AH

CA3-CA0:CA (bits 7-4). CA specifies the start (Low) address (on 4 KB boundaries) for the Common Area 1. This also determines the last address of the Bank Area. All bits of CA are set to 1 during RESET.

BA-BA0 (bits 3-0). BA specifies the start (Low) addres (on 4 KB boundaries) for the Bank Area. This also deter mines the last address of the Common Area 0. All bits o BA are set to 1 during RESET.

OPERATION MODE CONTROL REGISTER

Mnemonic OMCR

Address 3E

The Z80180/Z8S180/Z8L180 is descended from two different "ancestor" processors, Zilog's original Z80 and the Hitachi 64180. The Operating Mode Control Register (OMCR) can be programmed to select between certain differences between the Z80 and the 64180.

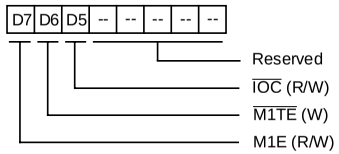


Figure 82. Operating Control Register (OMCR: I/O Address = 3EH)

M1E (M1 Enable). This bit controls the M1 output and i set to a 1 during reset.

When M1E=1, the M1 output is asserted Low during th opcode fetch cycle, the INT0 acknowledge cycle, and th first machine cycle of the NMI acknowledge.

On the Z80180/Z8S180/Z8L180, this choice makes th processor fetch an RETI instruction once, and when fetch ing an RETI from zero-wait-state memory will use thre clock machine cycles which are not fully Z80-timing com patible but are compatible with the on-chip CTCs.

When MIE=0, the processor does not drive M1 Low durin instruction fetch cycles, and after fetching an RETI instruc tion once with normal timing, it goes back and re-fetche the instruction using fully Z80-compatible cycles that in clude driving M1 Low. This may be needed by some exter nal Z80 peripherals to properly decode the RETI instruc tion.I/O Control Register (ICR).

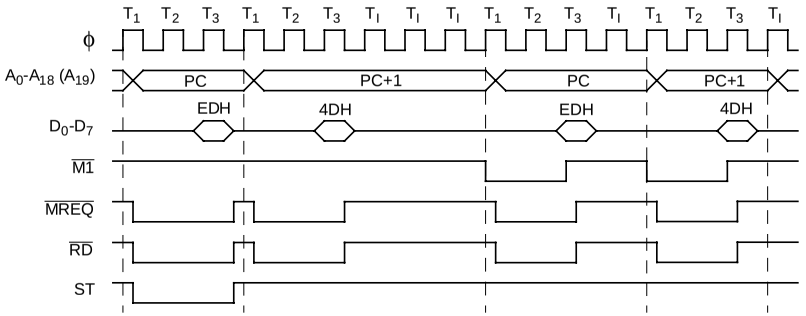


Figure 83. RETI Instruction Sequence with MIE=0

ICR allows relocating of the internal I/O addresses. ICR also controls enabling/disabling of the IOSTOP mode (Figure 84)

Bit	7	6	5	4	3	2	1	0
	IOA7	IOA6	IOSTP	--	--	--	--	--
	R/W	R/W	R/W					

Figure 84. I/O Control Register (ICR: I/O Address = 3FH)

IOA7, 6: I/O Address Relocation (bits 7,6). IOA7 and IOA6 relocate internal I/O as shown in Figure 85. Note that the high-order 8 bits of 16-bit internal I/O address are al ways 0. IOA7 and IOA6 are cleared to 0 during Reset.

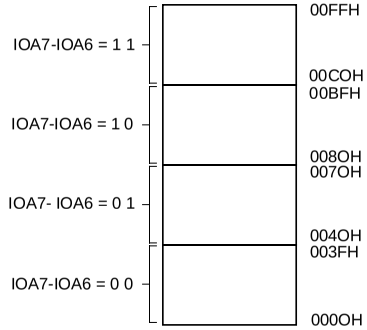


Figure 85. I/O Address Relocation

IOSTP. IOSTOP Mode (bit 5). IOSTOP mode is enabled when IOSTP is set to 1. Normal I/O operation resumes when IOSTOP is reprogrammed or Reset to 0

APPENDIX B: ELECTRIC DIAGRAMS

In this appendix are available some electric diagrams of the most frequently used **GPC® 183** interfaces. All these interface can be yourself produced and some of them are standard **grifo®** cards and, if required, they can be directly ordered.

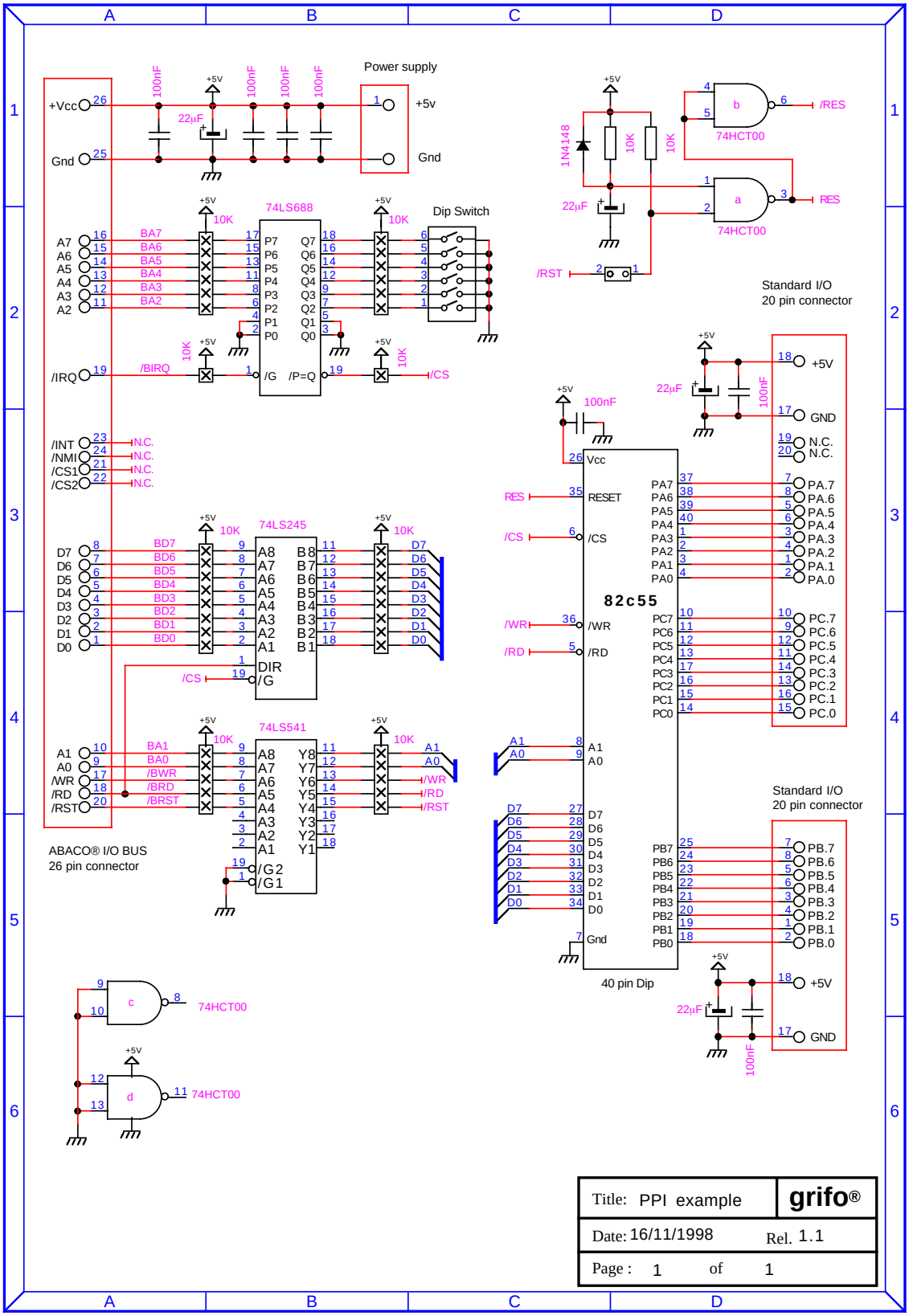


FIGURE B1: PPI EXPANSION ELECTRIC DIAGRAM

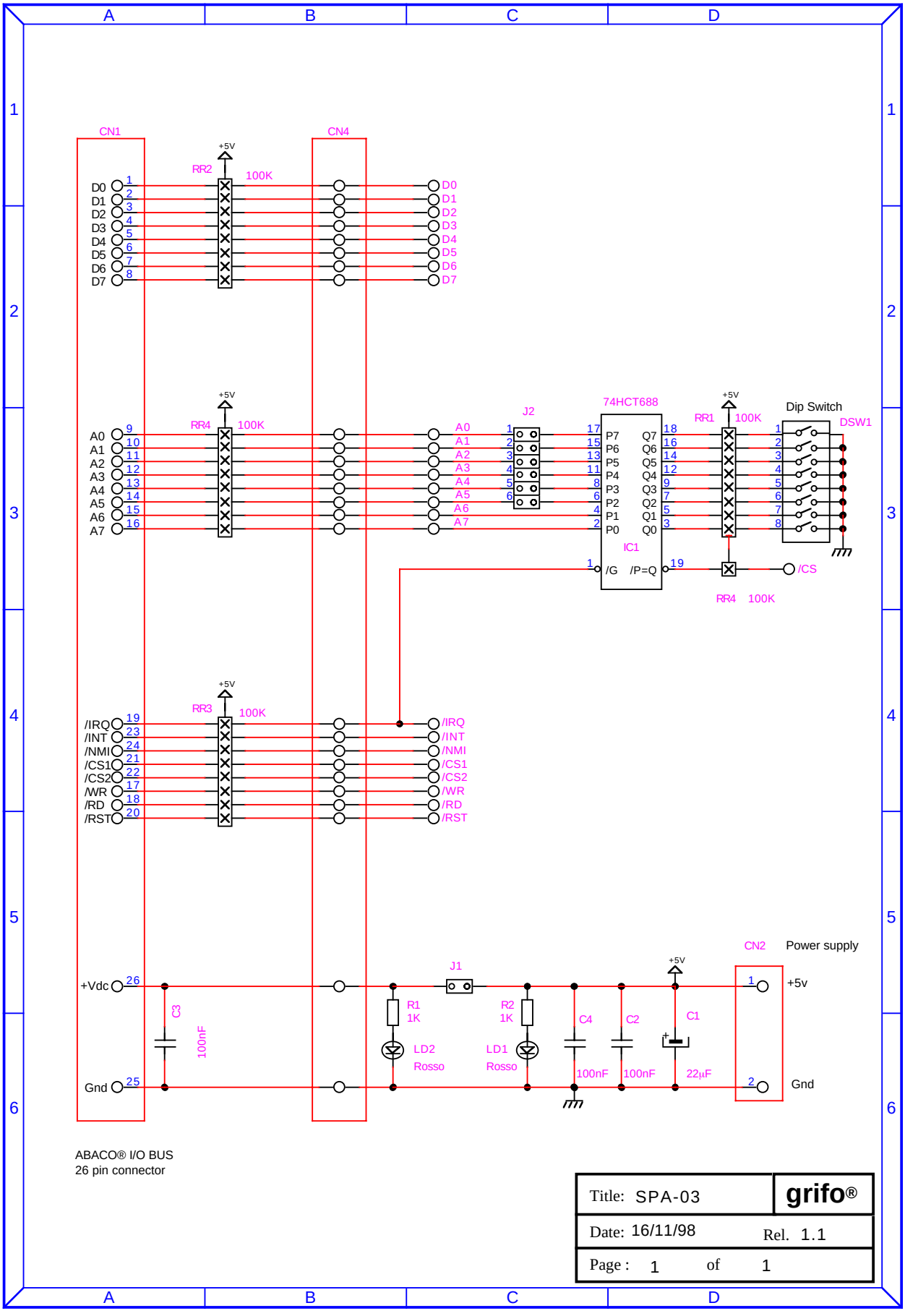


FIGURE B2: SPA 03 ELECTRIC DIAGRAM

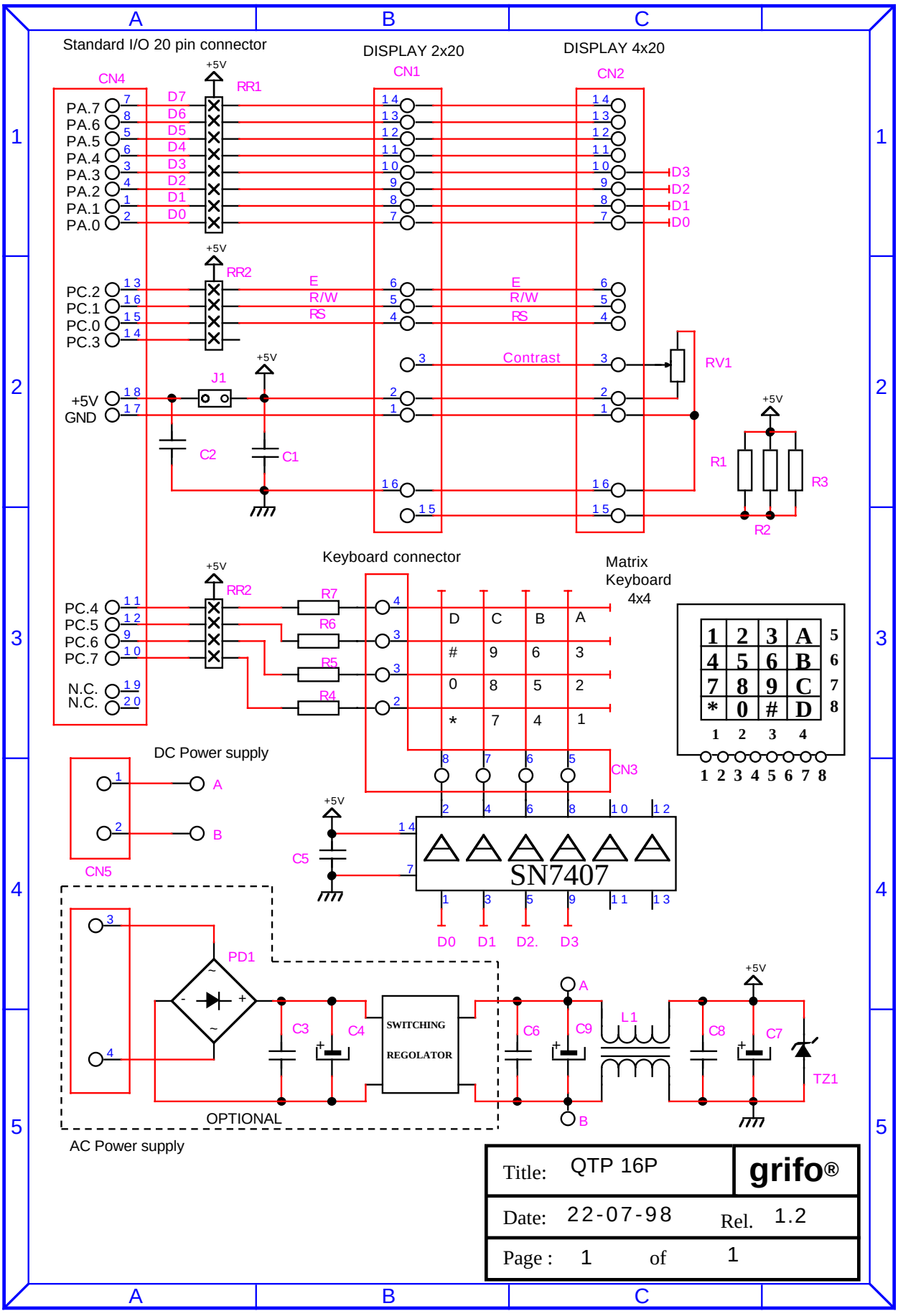


FIGURE B3: QTP 16P ELECTRIC DIAGRAM

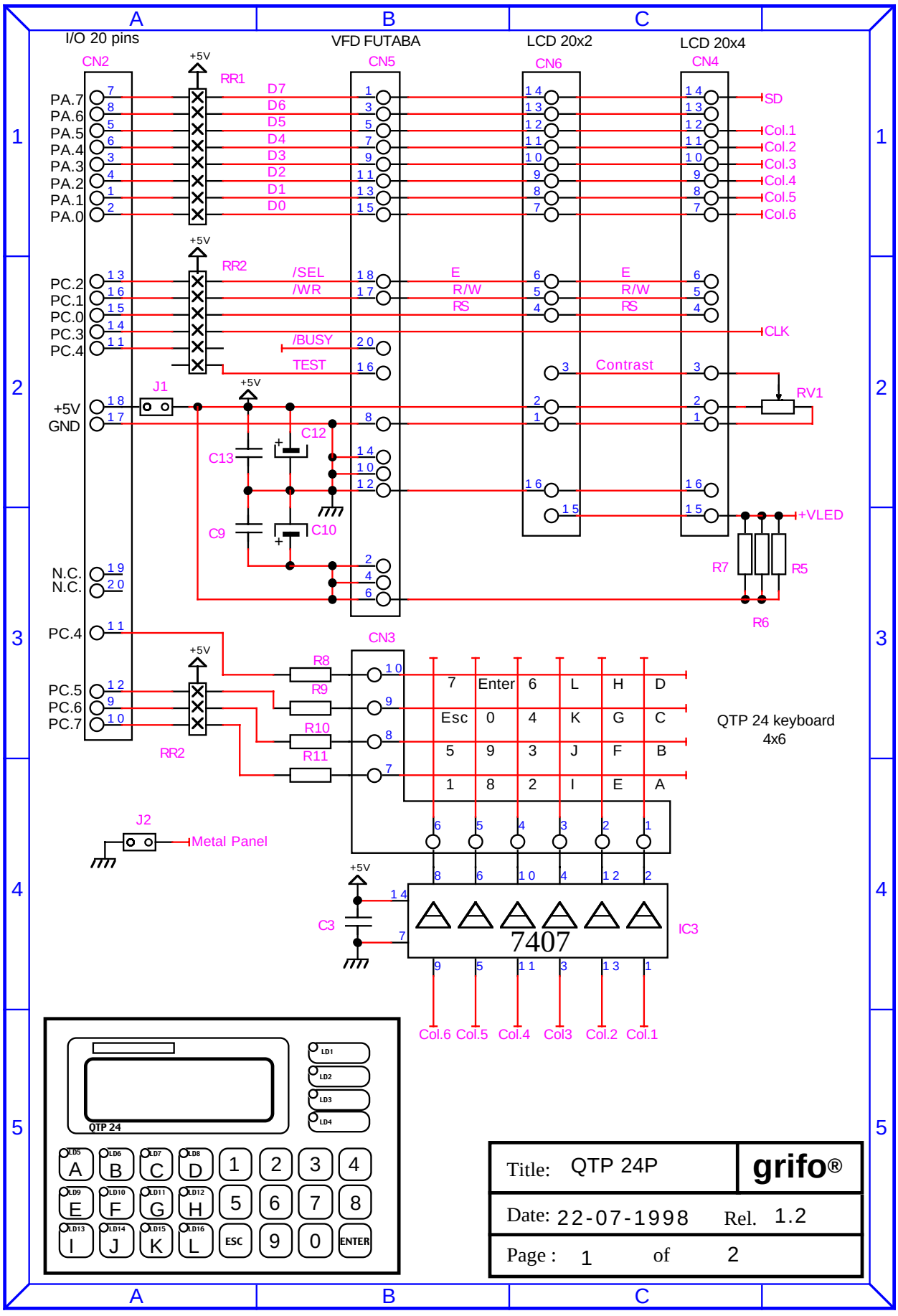


FIGURE B4: QTP 24P ELECTRIC DIAGRAM (1 OF 2)

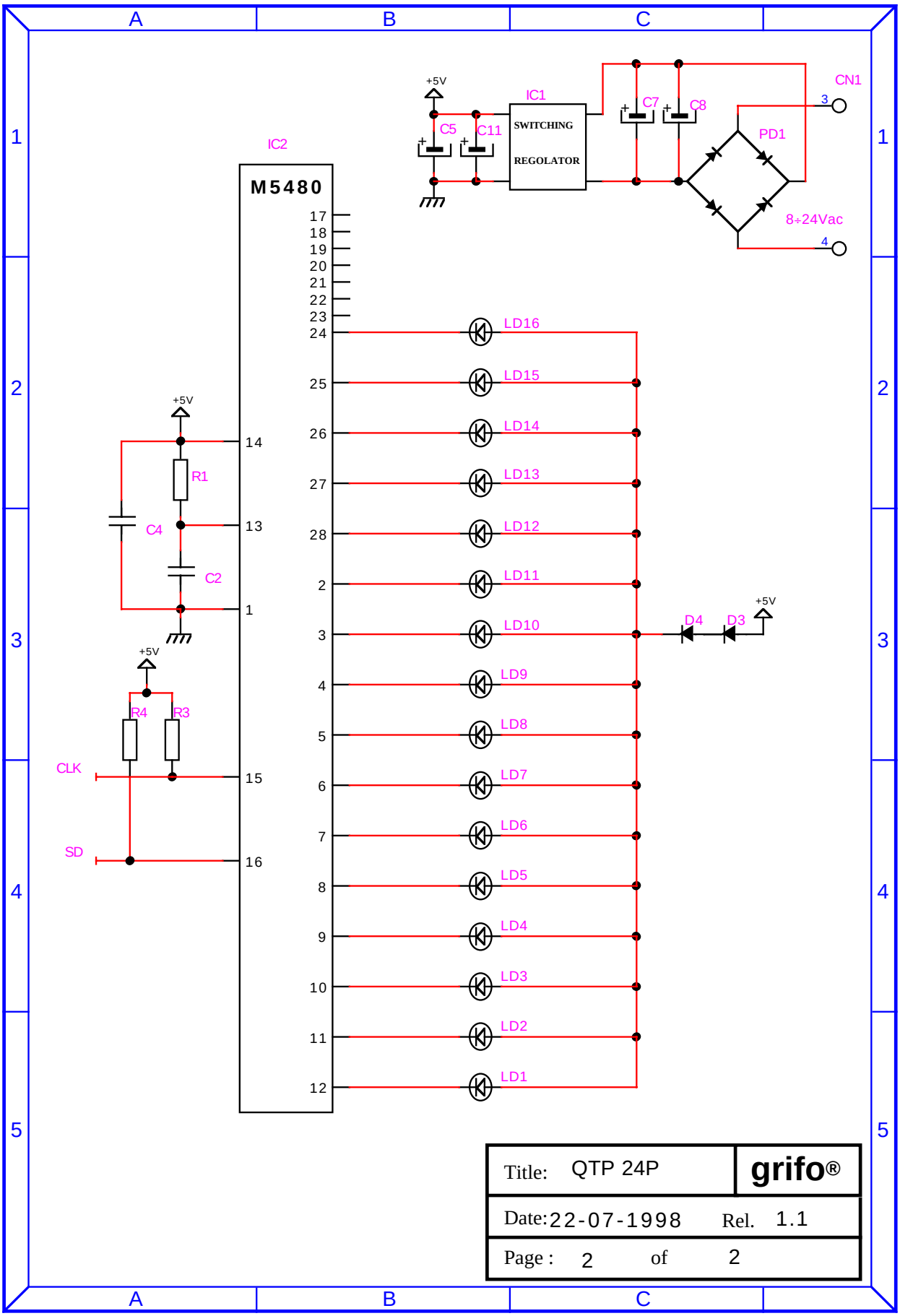


FIGURE B5: QTP 24P ELECTRIC DIAGRAM (2 OF 2)

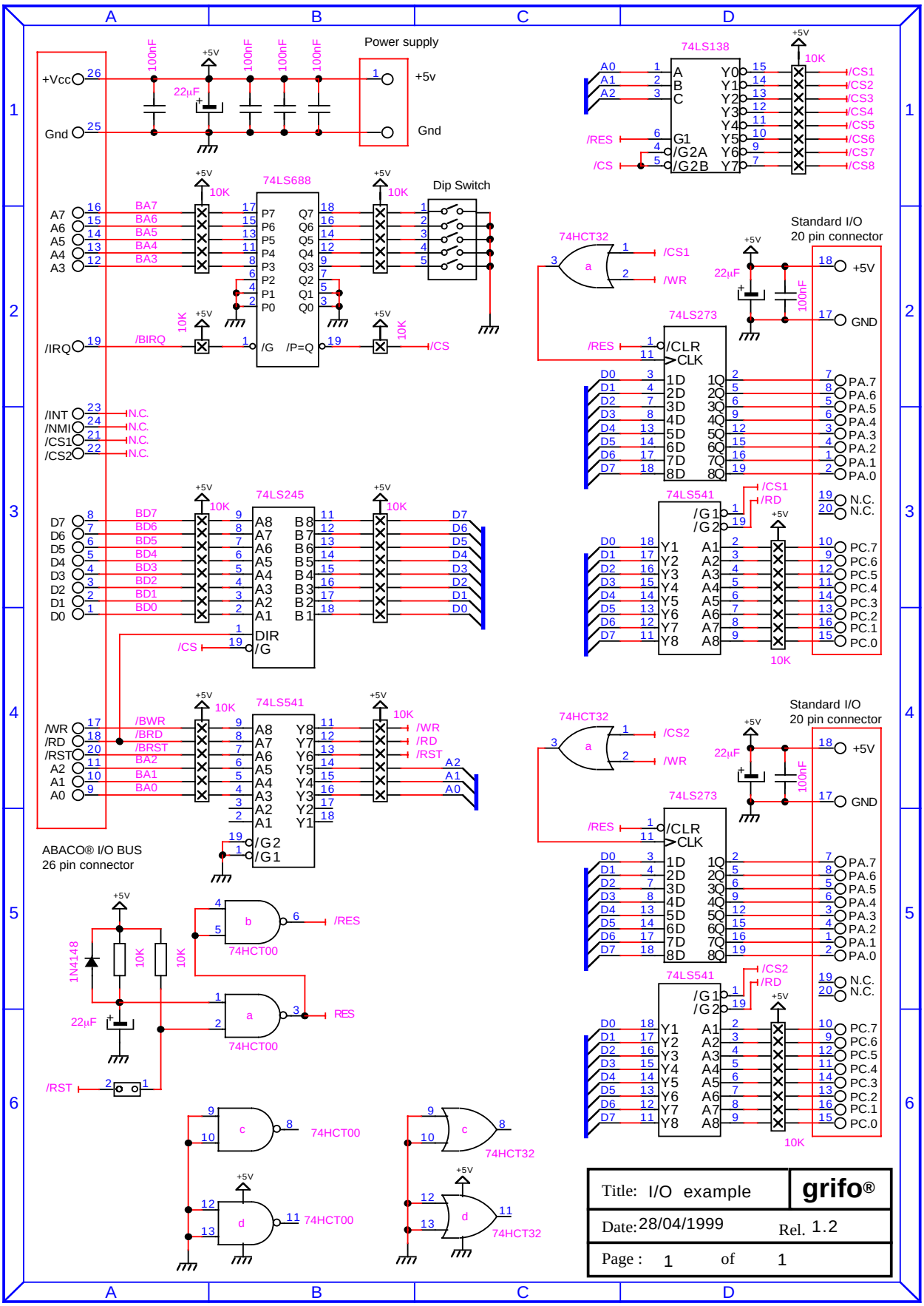


FIGURE B6: ABACO® I/O BUS INPUT OUTPUT ELECTRIC DIAGRAM

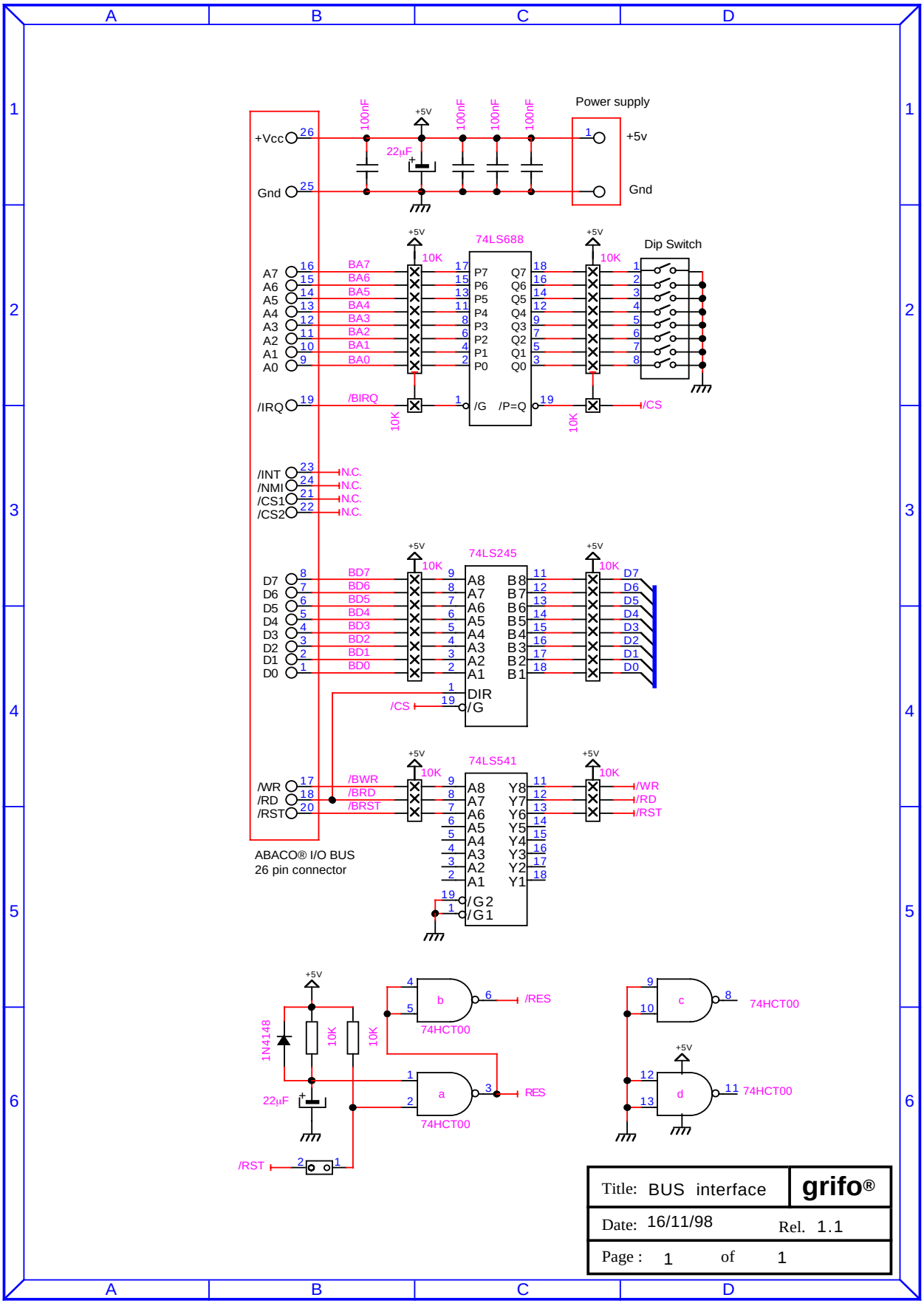


FIGURE B7: BUS INTERFACE ELECTRIC DIAGRAM

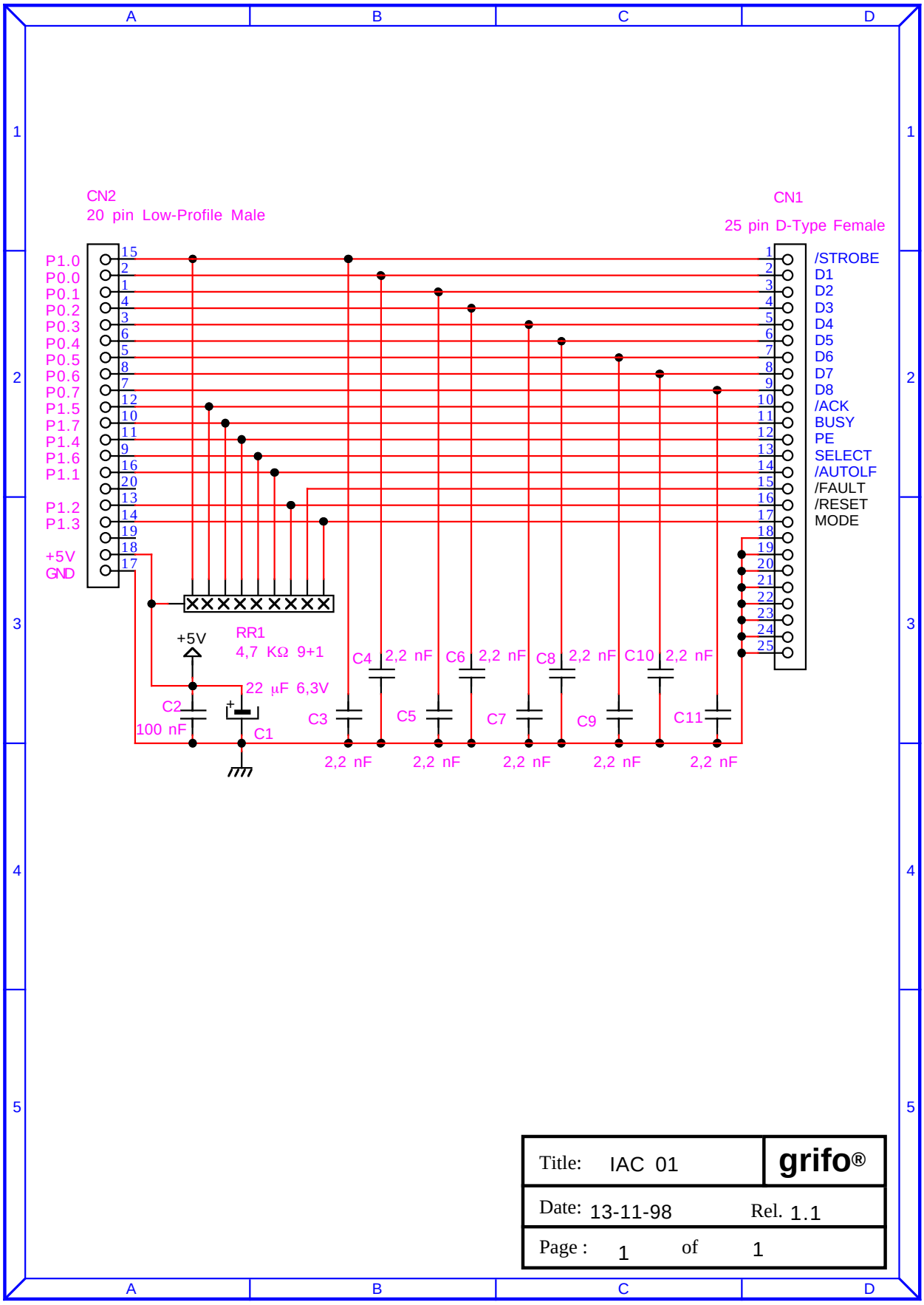


FIGURE B8: IAC 01 ELECTRIC DIAGRAM

APPENDIX C: ALPHABETICAL INDEX

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