GPC® 15R
General Purpose Controller Z84C15

TECHNICAL MANUAL

Single Euro size 100x160mm with interface to ABACO® I/O BUS; 84C15 CPU with 20 MHz crystal; up to 512K EPROM or 512K FLASH EPROM and up to 512K SRAM; through FGDOS the memory that exceeds 64K is managed as RAM/ROM disk; serial EEPROM up to 8K; up to 12 way Dip Switch and configuration jumper readable by software; one activity LED driven through software; 2 RS 232 serial lines, one configurable in RS 422, RS 485 or Current Loop, software selectable baud rate, up to 115.2 Kbaud; up to 24 I/O TTL lines; 16 optocoupled TTL inputs; 8 relay outputs 3A protected by MOV; four 8 bits timer counters I/O connector; optional backed SRAM with optional Real Time Clock able to up date day, month, year, week day, seconds, minutes and hours; Watch Dogs resettable by software and displayed through LEDs; galvanically isolated power supply through mains 220 Vac or two separated tensions of 8÷24 Vac; wide range of base software and developement tools that allow card use with only a standard PC, connected through serial line. Among these: FGDOS 15R; PASCAL 80; CBZ 80; NSB8; RSD 15A; HI TECH C 80; GET 80; DDS MICROC 85; NO ICE Z80; etc.
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For specific informations on the components mounted on the card, please refer to the Data Book of the builder or second sources.

SYMBOLS DESCRIPTION

In the manual could appear the following symbols:

⚠️  Attention: Generic danger

⚡️  Attention: High voltage

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INTRODUCTION

The use of these devices has turned - IN EXCLUSIVE WAY - to specialized personnel.

The purpose of this handbook is to give the necessary information to the cognizant and sure use of the products. They are the result of a continual and systematic elaboration of data and technical tests saved and validated from the manufacturer, related to the inside modes of certainty and quality of the information.

The reported data are destined- IN EXCLUSIVE WAY- to specialized users, that can interact with the devices in safety conditions for the persons, for the machine and for the environment, impersonating an elementary diagnostic of breakdowns and of malfunction conditions by performing simple functional verify operations , in the height respect of the actual safety and health norms.

The informations for the installation, the assemblage, the dismantlement, the handling, the adjustment, the reparation and the contingent accessories, devices etc. installation are destined - and then executable - always and in exclusive way from specialized warned and educated personnel, or directly from the TECHNICAL AUTHORIZED ASSISTANCE, in the height respect of the manufacturer recommendations and the actual safety and health norms.

The devices can't be used outside a box. The user must always insert the cards in a container that respect the actual safety normative. The protection of this container is not threshold to the only atmospheric agents, but specially to mechanic, electric, magnetic, etc. ones.

To be on good terms with the products, is necessary guarantee legibility and conservation of the manual, also for future references. In case of deterioration or more easily for technical updates, consult the AUTHORIZED TECHNICAL ASSISTANCE directly.

To prevent problems during card utilization, it is a good practice to read carefully all the informations of this manual. After this reading, the user can use the general index and the alphabetical index, respectly at the begining and at the end of the manual, to find information in a faster and more easy way.

CARD VERSION

The present handbook is reported to the GPC® 15R card release 130395 and later. The validity of the bring informations is subordinate to the number of the card release. The user must always verify the correct correspondence among the two denotations. On the card the release number is present in more points both board printed diagram (serigraph) and printed circuit (for example near capacitor C4 on the component side and under transformer TF1 on the solder side).
GPC® 15R is a powerful, low cost, controller module capable of operating in stand alone mode or as an intelligent peripheral, and/or remoted, in a wider telecontrol or acquisition network. The board is designed to solve in autonomy several problems of industrial sector and, when necessary, it can be improved in power and application possibilities through threads the on board ABACO® I/O BUS.

The card is provided with a series of standard connectors that make easier to install the system installation, it is also provided with comfortable quick release screw terminal connectors for all the I/O signals from the external world.

The GPC® 15R board is secured in a plastic mount for connection to Omega rails DIN 46277-1 and DIN 46277-3, thereby dispensing with the need of rack and allowing a cheaper mounting direct to the electrical control panel. It also features several power supply possibilities, including mains power supply.

The powerful and easy-to-use ROM-based FGDOS Operating System makes easy to program the board and to take advantage of its many resources. FGDOS supports high level languages like BASIC, PASCAL, C and so on, places at user’s disposal all the memory resources as ROM/RAM Disks, allowing an immediate high-level use of these devices, manages PCMCIA RAM Cards through the MCI 64 board and on-board serial EEPROMs directly. In addition, FGDOS manages directly LCDs, fluorescent displays and a matrix keyboard. The KDL-224 series boards allow an immediate use of these devices management features, while the QTP24P Operator Panel represents a valid low-cost solution to integrate display and keyboard in a single object. This Panel, offered in open frame version, has the same esthetics of QTP24 but can be controlled directly by GPC® 15R because it is designed to work without an on-board controller. FGDOS can also write the user program in a FLASH memory without need of external hardware.

The GPC® 15R is equipped with a series of standard ABACO® connectors allowing immediate use of the many BLOCK I/O interface, or enabling a simple and inexpensive connections to equipment made by the user, or by third parties.

- Size 100x245 mm with container for DIN 46277-1 and DIN 46277-3;
- CPU 84C15 code compatible to Z80 with 20 MHz quartz;
- 16 or 24 TTL I/O lines, software manageable, byte-level directionality, driven through PPI 82C55;
- 16 optocoupled Input lines, visualized through LEDs and capable to generate interrupts, software managed by the Z84C15-inside PIO section. Input lines are supplied by the board and need just an NPN driver, or an unbounded relay contact;
- 8 output lines with 3A relays, visualized by LEDs and provided with transient suppressors;
- 2 software readable Dip Switch up to 12 dips;
- Up to 512 K di FLASH EPROM or 512 K of EPROM and 512 K SRAM. Through FGDOS the memory that exceeds 64K is managed as RAM/ROM disk. It is possible deleting and re-programming the on board FLASH, automatically, with the User program;
- Up to 8K backed SRAM with Lithium battery and Real Time Clock able to up date day, month, year, week day, seconds, minutes and hours.;
- Serial EEPROM from 2 to 64 KBIT;
- 2 RS 232 serial lines, one configurable in RS 422, RS 485 or Current Loop managed by the powerful SIO and software manageable baud rate generators, up to 115.2 KBAud;
- Double Baud Rate generator software programmable from 300 to 115200 Baud;
- Double Watch Dog retriggerable by software;
- Power Failure circuitry capable to generate /NMI;
- Four 8 bits timer counter available to the User and software manageable through the CTC section of Z84C15. The 4 counter signals are optocoupled, visualized through LEDs and already supplied;
- Buzzer circuitry used to generate interrupts or sound feedback;
- Several status and activity LEDs;
- Jumper to switch between operational or debugger modes;
- ABACO® I/O BUS connector;
- Mains power supply on board, capable to supply both I/O and logic sections, such sections are galvanically isolated;
- Wide range of base software and development tools that allow card use with only a standard PC, connected through serial line. Among these: FGDOS 150; PASCAL 80; CBZ 80; NSB8; RSD 150; HI TECH C 80; GET 80; DDS MICROC 85; NO ICE Z80; etc.

MEMORY DEVICES

On the card can be mounted up to 1040K of memory divided with a maximum of 512K Byte EPROM or 512K Byte FLASH EPROM, 512K Byte SRAM, an optional backed SRAM module up to 8K Byte and 8K Byte serial EEPROM. The memory configuration must be chosen considering the application to realize or the specific requirements of the User. Normally the card is provided with 128K RAM, all different configurations must be specified by the User, at the moment of the order. By means of the serial EEPROM and the backed SRAM module, memory can keep data also in absence of power supply. The addressing of memory devices is controlled by a specific on-board control logic, that provides to allocate the devices in the microprocessor address space. For further information about memory configuration, sockets description and jumpers connection, please refer to chapter "HARDWARE", "PERIPHERAL DEVICES SOFTWARE DESCRIPTION" and to the paragraph "MEMORY SELECTION".

SERIAL COMMUNICATION

The serial communication lines are completely software configurable for protocol and speed (from 300 to 115200 Baud); simply by programming the microprocessor SIO and the on board baud rate generator, the User can set the Baud Rate, stop bits number, length of character, parity and handshake of each serial line. For further information about these programmable sections, please refer to chapter "BAUD RATE GENERATOR" and to appendix B of this manual.

One of the two serial lines is always buffered with RS 232 electric protocol, while the second one is hardware configurable in fact connecting some jumpers, the User can select the electric standard interface between RS 232, RS 422, RS 485 and Current Loop: for RS 422-485 the transmitter activation and the line direction can be set by software. The chapter "SERIAL COMMUNICATION SELECTION" contains a detailed description of available hardware configurations.

Normally the card is provided with two RS 232 interfaces and a different configuration must be specified when ordering.
SIO

Microprocessor peripheral device that manages two lines for serial communication. It can be used to connect to external systems capable to support RS 232, RS 422, RS 485 and Current Loop electric protocols. Simply by programming four registers allocated in the microprocessor I/O addressing space, the User can set the baud rate, stop bits number, length of character, parity and handshake of each serial line.

TIMER COUNTER

It is a microprocessor peripheral device that manages four 8 bit timer counters. Each channel can be set with a different prescaler and with a different operating mode (timer with external trigger, counter of rising edge or falling edge, etc.), including eventual interrupt generation. CTC is connected to the external electronics by eight digital signals and it is completely driven by software programming four registers allocated in microprocessor I/O addressing space, by a specific control logic.

PIO TTL I/O LINES

It is a microprocessor peripheral device that manages 16 TTL I/O lines divided in two 8 bit parallel ports. The lines direction is software settable at bit level and interrupts can be generated. In this way an external status can obtain CPU control in any condition, with a fast response time. The PIO is completely driven by software programming four registers allocated in microprocessor I/O addressing space, by a specific control logic.

CONTROL LOGIC

The addresses of all peripheral device's registers and of memory devices on GPC® 15R are assigned through a specific control logic that allocates all these devices in the microprocessor addressing space.
For further information please refer to chapter "ADDRESSES AND MAPS" of this manual.

MEMORY MANAGEMENT UNIT

A specific MMU section has been designed to manage in a practical and efficient way the memory configurations that the GPC® 15R board can assume. The use is provided with a 64K work area, which can be easily allocated anywhere in the 1024K maximum memory space.

BUZZER

On GPC® 15R there is a circuit to emit a fixed sound, based on a capacitive buzzer. This circuit can be enabled and disabled by software by the control logic and it can be used to manage alarm, sound feed back, etc.
FIGURE 1: BLOCK DIAGRAM
CLOCK DEVICES

On GPC® 15R there are two separate circuits with crystal to generate the clock signal for the microprocessor (20 MHz) and the timing signal for baud rate generator section (4.9152 MHz). The choice of using two circuits and as many separated crystals, has the advantage to change the microprocessor working speed (when best performances are required) without additional changes in communication software or firmware. The best time performances are always obtained both for execution time and serial communication, fulfilling the User necessity.

PPI 82C55 TTL I/O LINES

It manages 24 TTL I/O lines divided in three 8 bit parallel ports. The lines direction is software settable at byte level. These I/O lines allow the possibility to connect several devices (for example: User interfaces) even when the handshake is completely software driven. The PPI 82C55 is completely driven by software programming four registers allocated in microprocessor I/O addressing space, by a specific control logic. In the basic version of the board an 8 pins Dip Switch (DSW1) is installed on one of the ports; to use also these eight signals the User just needs to remove the Dip Switch (which is mounted on a socket) and replace it with a 16 pins socket connector.

WATCH DOG SECTIONS

GPC® 15R is provided with two separated Watch Dog circuits that can reset the card at programmable time intervals, if not retriggered. Watch dog circuits are used when the User want to exit from endless loops or to reset anomalous conditions not estimated by application program. There is a monostable section, inside the microprocessor, with programmable intervention time and a monostable/astable section, outside the microprocessor, with 700 ms fixed intervention time. By software the User can perform a complete management of the devices, using specific registers allocated in microprocessor I/O addressing space.

BOARD CONFIGURATION

To make the board and the applications program developed for it easier to configure a 4 pins Dip Switch (DSW1), an 8 pins Dip Switch (DSW2) and two jumpers (J9 and J13) have been installed. One of the jumpers (J13) has the purpose to select the RUN/DEBUG modality and to configure the management software. The possibility to read by software the status of these devices allows the User the chance to manage several working conditions through an unique program without no need to employ more input signals (characteristic applications are: language selection, program parameter determination, working modalities selection, etc.). Should the DSW2 not to be used, the 8 generic TTL I/O lines of PPI port B are available, as describe in the paragraph "DSW2 - PPI 82C55 PORT B I/O SOCKET".
GALVANICALLY ISOLATED INPUTS/OUTPUTS

One of the main features of GPC® 15R board is the presence of galvanically isolated I/O lines, that can be used directly as interface to the external world. Totally, the board is provided with 16 optocoupled NPN digital inputs, 4 optocoupled NPN inputs for counters and eight 3 A relay outputs. We would want to remark to the User that the board generates also the tension needed to supply the optocoupled inputs (+Vopto); for this it is possible to connect sensor and actuators directly to the board, without any other interfacement devices.

REAL TIME CLOCK

The optional backed SRAM module instalable on IC27 can also have a Real Time Clock capable of a completely autonomous management of hours, minutes, seconds, day of month, month, year and day of week. The device is completely software programmable through 8 registers mapped in the CPU I/O.

CPU

The GPC® 15R board uses the powerfull microprocessors 84C15 produced by ZILOG. This 8 bit microprocessor is code compatible with standard Z80 CPU and it has an extended instruction set, fast execution time, fast data handling and an efficient vectorized interrupt management. Some of the most important 84C15 features are its internal peripheral devices, as below described:

- 16 I/O lines programmable at bit level, capable to generate interrupts (PIO);
- four 8 bit timers counters, with programmable prescaler (CTC);
- 2 synchronous or asynchronous serial lines, provided of hardware handshake signals (SIO);
- watch dog timer;
- wait state generator;
- programmable clock frequency;
- interrupt controller;
- idle mode or power down mode.

For further information, please refer to specific documentation of the manufacturing company, or to appendix B of this manual.

ABACO® I/O BUS

One of the most important features of GPC® 15R is its possibility to be interfaced to industrial ABACO® I/O BUS. Thanks to its standard ABACO® I/O BUS connector, the card can be connected to some of the numerous grifo® boards, both intelligent and not. For example the user can directly use cards for analog signals acquisition (A/D like ABC 04 or ABB 08), cards for analog signals generation (D/A), cards for digital I/O signals management, cards with timers and counters, cards for temperature controls, etc. also custom boards designed to satisfy specific needs of the end user. Using ABB 03 or ABB 05 mother boards it is possible manage all the BUS ABACO® single EURO cards. So GPC® 15R becomes the right component for each industrial automation system, in fact ABACO® I/O BUS makes the card easily expandable with the best price/performance ratio.
ON BOARD POWER SUPPLY

One of the most interesting features of GPC® 15R is its on-board power supply section. In fact, a specific circuitry can generate the needed voltages with mains 220 Vac as input. The board uses two galvanically isolated supply sources: one generates +5 Vdc for logic sections and the other one generates +24 Vdc for optocoupled inputs; power supply sections have been designed to reduce the current consumption of the board, so they cannot be used to supply external devices whose requirements exceed 200 mA on +5 Vdc e 2.4 W on +Vopto. This limitation can be easily overridden by providing to the GPC® 15R board two external supplies (alternated or continuous) through connector CN1&13, these supplies can be picked within a wide range of values normally available in the electric racks (for further informations please refer to the paragraph “POWER SUPPLY VOLTAGES SELECTION”). The above described design selection make the board extremely reliable and cheap.

POWER FAILURE CIRCUITRY

On-board Power Failure circuitry is capable to generate an /NMI (Not Maskable Interrupt) if the alternate voltage in output from the transformer is missing. This way the User application program can detect the situation and take advantage of the residual charge of the power supply section. Through the correct choice of an RC group, it is possible to decide the intervent time of the circuitry. This flexibility allows the User to set the most appropriate intervent time being able anyway to take advantage of a circuitry that can even feel the absence of a half-wave.

For further informations about the above described devices, please refer to the manufacturer documentations or to appendix B of this manual.
TECHNICAL FEATURES

GENERAL FEATURES

On board resources:

- 16 (24) Input/Output TTL programmable (PPI 82C55)
- 16 inouts optocoupled NPN (PIO)
- 8 outputs 3 A relays
- 4 Timer Counter with 8 bit, optocoupled in NPN (CTC)
- 1 bidirectional RS 232 line
- 1 bidirectional RS 232, RS 422, RS 485 or Current Loop line
- 1 external astable or monostable Watch Dog
- 1 internal monostable Watch Dog
- 1 local reset key
- 1 Real Time Clock (RTC)
- 1 Buzzer
- 2 Dip Switch up to 12 dips
- 1 Power Failure circuitry
- 1 ABACO\textsuperscript{®} I/O BUS

Addressable memory:

- IC 32: EPROM from 128K x 8 to 512K x 8
- FLASH EPROM from 128K x 8 to 512K x 8
- IC 29: SRAM from 128K x 8 to 512K x 8
- IC 27: SRAM from 2K x 8 to 8K x 8
- IC 37: serial EEPROM from 256 byte to 8192 byte

On board CPU:

- ZILOG 84C15 with 20 MHz quartz

Watch Dog intevent time:

- 700 msec (settable through an RC network)

PHYSICAL FEATURES

Connectors:

- CN1: 2 pins quick release screw terminal connector
- CN2: 11 pins quick release screw terminal connector
- CN3: 9 pins female D connector
- CN4: 9 pins quick release screw terminal connector
- CN5: 9 pins female D connector
- CN6: 9 pins quick release screw terminal connector
- CN7: 9 pins female D connector
- CN8: 5 pins quick release screw terminal connector
- CN9: 20 pins low profile vertical M connector
- CN10: 10 pins low profile vertical M connector
- CN11: 26 pins low profile vertical M connector
- CN12: 5 pins low profile vertical M connector
- CN1&13: 4 pins quick release screw terminal connector
- CN14: 2 pins low profile vertical M connector

Size:

- 100 x 245 mm

Weight:

- 980 g
Temperature range: from 10 to 40 Centigrad degrees

Relative humidity: 20% up to 90% (without condense)

ELECTRIC FEATURES

Fuse F1: 1 A; 250 V delayed
Fuse F2: 400 mA; 250 V delayed
Fuse F3: 100 mA; 250 V delayed

Supply voltages: 220 Vac; 50 Hz (mains power supply)
8÷24 Vac (low voltage power supply)

Current consumption:

- Mains power supply
  - on +5 Vdc: 120÷430 mA for the board
  - 300 mA for external loads
  - on +V Opto: 200 mA for NPN optocoupled inputs
  - 2.4 W for external loads
  - on +Va: 300 mA minus current consumption on +5V multiplied by 1.4

- Low voltage power supply
  - on +5 Vdc: 120÷430 mA for the board
  - 900 mA for external loads
  - on +V Opto: 200 mA per ingressi optoisolati NPN
  - 12.5 W for external loads
  - on +Va: 900 mA minus current consumption on +5V multiplied by 1.4

Maximum voltage on relays: 24 Vac
To connect the relays to an higher voltage value please contact grifo®
INSTALLATION

In this chapter there are the information for a right installation and correct use of the card. The User can find the location and functions of each connectors, jumpers and some explanatory diagrams.

CONNECTIONS

The GPC® 15R board has 14 connectors that can be linkeded to other devices or directly to the field, according to system requirements. In this paragraph there are connectors pin out, a short signals description (including the signals direction), connectors location (see figure 39) and some electrical diagrams that show the on board circuit of each connector.

CN10 - CTC I/O CONNECTOR

CN10 is a 10 pins, male, vertical, low profile connector with 2.54 mm pitch. On CN10 connector are available the input and output signals of each channels of the on board CTC timers counters. all CN1 signals follow TTL standard.

![CN10 Connector Diagram]

Signals description:

- **C/Tn** = I - Clock Trigger for the n-th counter of the TTL CTC. If the signal to connect is open connector the optocoupled input section (CN8) can be installed. In this case there will be a logical OR between the TTL input and the corresponding optocoupled input.
- **ZC/Tn** = O - Zero Count Timer of n-th TTL counter.
- **Vdc** = O +5 Vdc power supply.
- **GND** = - Ground signal.
FIGURE 4: CTC CONNECTION DIAGRAM
CN8 - CONNECTOR FOR CTC OPTOCOUPLED INPUTS

CN8 is a 5 pins quick release screw terminal connector. By CN8 the 4 on board counter signals can be reached through 4 optocoupled inputs. The common open collector terminal and the optocoupled section power supply ground signal are available on the connector.

![CN8 Connector Diagram](image)

**FIGURE 5: CN8 - CONNECTOR FOR CTC OPTOCOUPLED INPUTS**

Signals description:

- **IN C/Tn** = I - Clock Trigger of n-th CTC counter in open collector NPN.
- **GND Opto** = - Optocoupled section power supply ground signal.

CN14 - CONNECTOR FOR EXTERNAL BACK UP BATTERY

CN14 is a 2 pins, male, vertical, low profile connector with 2.54 mm pitch. Through CN14 an external Lithium battery that keeps alive data in SRAM even when power supply fails can be connected.

![CN14 Connector Diagram](image)

**FIGURE 6: CN14 - EXTERNAL BACK UP BATTERY CONNECTOR**

Signals description:

- **+Vbat** = I - Positive terminal of external back up battery
- **GND** = - Negative terminal of external back up battery
CN1 - MAINS POWER SUPPLY CONNECTOR

CN1 is a 2 pins quick release screw terminal connector. Through CN1 mains power supply for both the galvanically isolated sections of the board must be provided (for further informations please refer to the paragraph “POWER SUPPLY VOLTAGES SELECTION”).

![Figure 7: CN1 - MAINS POWER SUPPLY CONNECTOR](image)

Signals description:

\[220 \text{ Vac} = I\] - Mains power supply 220 Vac signals.

CN1&13 - LOW VOLTAGE POWER SUPPLY CONNECTOR

CN1&13 is a 4 pins quick release screw terminal connector. Through CN1&13 two low voltage tensions to supply both the galvanically isolated sections of the board must be provided (for further informations please refer to the paragraph “POWER SUPPLY VOLTAGES SELECTION”).

![Figure 8: CN1&13 - LOW VOLTAGE POWER SUPPLY CONNECTOR](image)

Signals description:

\[V1 = I\] - Low voltage power supply for optocoupled inputs (8÷24 Vac; 12÷34Vdc).
\[V2 = I\] - Low voltage power supply for on-board logic (8÷24 Vac; 12÷34Vdc).
CN4 - CONNECTOR FOR PIO PORT B OPTOCOUPLED INPUT SIGNALS

CN4 is a 9 pins quick release screw terminal connector. Through CN4 8 out of 16 NPN optocoupled inputs (connected to PIO port B) are reachable. The common open collector terminal and the optocoupled section power supply ground signal are available on the connector.

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>IN PIO PB.0</td>
</tr>
<tr>
<td>2</td>
<td>IN PIO PB.1</td>
</tr>
<tr>
<td>3</td>
<td>IN PIO PB.2</td>
</tr>
<tr>
<td>4</td>
<td>IN PIO PB.3</td>
</tr>
<tr>
<td>5</td>
<td>IN PIO PB.4</td>
</tr>
<tr>
<td>6</td>
<td>IN PIO PB.5</td>
</tr>
<tr>
<td>7</td>
<td>IN PIO PB.6</td>
</tr>
<tr>
<td>8</td>
<td>IN PIO PB.7</td>
</tr>
<tr>
<td>9</td>
<td>GND Opto</td>
</tr>
</tbody>
</table>

Signals description:

IN PIO PB.n = I - Open collector NPN input connected to n-th port B line.
GND Opto  = - Optocoupled section power supply ground signal.
FIGURE 10: PIO OPTOCOUPLED INPUT SIGNALS CONNECTION DIAGRAM
CN6 - CONNECTOR FOR PIO PORT A OPTOCOUPLED INPUT SIGNALS

CN6 is a 9 pins quick release screw terminal connector. Through CN6 8 out of 16 NPN optocoupled inputs (connected to PIO port A) are reachable. The common open collector terminal and the optocoupled section power supply ground signal are available on the connector.

**Figure 11: CN6 - Connector for PIO port A optocoupled input signals**

Signals description:

- **IN PIO PA.n** = I - Open collector NPN input connected to n-th port B line.
- **GND Opto** = - Optocoupled section power supply ground signal.
DSW2 - SOCKET FOR PPI 82C55 I/O PORT B

DSW2 is a 16 pins socket with 2.54 mm pitch. By disconnecting the octal dip switch from DSW2 the PPI 82C55 port B can be used to manage eight TTL digital input output lines. The connection of the obtained 8 I/O lines with external electronics must be performed with proper flat cable DIL connector.

**Figure 12: DSW2 - Socket for PPI 82C55 I/O Port B**

Signals description:

<table>
<thead>
<tr>
<th>PPI PB.n</th>
<th>= I/O - PPI 82C55 port B n-th digital line.</th>
</tr>
</thead>
<tbody>
<tr>
<td>GND</td>
<td>= - Ground signal.</td>
</tr>
</tbody>
</table>
CN9 - CONNECTOR FOR PPI 82C55 I/O PORTS A AND C

CN9 is a 20 pins low profile vertical male connector with 2.54 mm pitch. On CN9 connector are available PPI 82C55 port A and C signals that equal to 16 I/O digital lines. Any parameter of this device (like signals direction, data management mode, etc.) is completely software definible by programming the device itself. All signals are at TTL level and follow the standard pinout I/O ABACO® pin-out.

**FIGURE 13: CN9 - CONNECTOR FOR PPI 82C55 I/O PORTS A AND C**

Signals description:

- **PPI PA.n** = I/O - PPI 82C55 port A digital line n
- **PPI PC.n** = I/O - PPI 82C55 port C digital line n
- **+5 Vdc** = O - Line connected to +5 Vdc power supply
- **GND** = - Ground signal
- **N.C.** = - Not connected
**Figure 14: PPI Connection Diagram**

- **PPI**
  - PORT A connected to PIN 1-8
  - PORT C connected to PIN 9-16

- **82C55**
  - PORT B connected to PIN 1-8

- **CN9**

- **DSW2**
  - Powered by +5 Vdc
  - PIN 1-8
CN2 - RELAYS OUTPUT CONNECTOR

CN2 is a 11 pins quick release screw terminal connector. Through CN2 the 8 on-board relay outputs can be connected to the external world. The connector features the contacts (normally open) of each output and three common contacts used by three output groups; when making connections the User should remember not to exceed 3 A and 24 Vac on each output.

**Figure 15: CN2 - Relays Output Connector**

Signals description:

| COMMON x:y | - Common contact for relays from x to y. |
| NA OUTn    | - Normally open contact of the n-th relay output. |
Figure 16: Relay outputs connections diagram
CN12 - CONNECTOR FOR EXTERNAL SUPPLY

CN12 is a 5 pins low profile vertical male connector with 2.54 mm pitch. Through CN12 the two galvanically isolated tensions used to supply the board can be reached and used to supply external loads. (for further informations please refer to the paragraph “POWER SUPPLY VOLTAGES SELECTION”).

```
5 - - - +VOpto
4 - - - GND Opto
3 - - - GND
2 - - - +Va
1 - - - +5 Vdc
```

**Figure 17: CN12 - Connector for external supply**

Signals description:

+VOpto = O - Positive terminal of optocoupled section power supply.
GND Opto = - Ground terminal of optocoupled section power supply.
GND = - Ground terminal
+Va = O - Positive terminal of input voltage to the on-board switching power supply section.
+5 Vdc = O - +5 Vdc power supply signal.
CN1 is a 26 pins, male, vertical, low profile connector. Through CN1 the card can be connected to external expansion modules developed by the user or to the numerous grifo® boards, both intelligent and not. All this connector’s signals are at TTL level and follow the ABACO® I/O BUS standard.

**Figure 18: CN1 - ABACO® I/O BUS Connector**

Signals description:

A0÷A7 = O - Address BUS.
D0÷D7 = I/O - Data BUS.
/INT = I - Interrupt request (open collector type).
/NMI = I - Non maskable interrupt (open collector type).
/IORQ = O - Input output request.
/WR = O - Write cycle status.
/RD = O - Read cycle status.
/RESET = O - Reset.
+5 Vdc = I/O - +5 Vdc power supply.
GND = - Ground signal.
/ECS1 = - External chip select 1
/ECS2 = - External chip select 2
CN7 - CONNECTOR FOR RS 232 ON SERIAL LINE A

CN7 is a 9 pins male D connector, which carries the RS 232 signals connected to serial line A. The signals on this connector follow the CCITT specifications DTE interface; signals location on this connector has been designed to reduce problems due to interference.

![Diagram of CN7 Connector]

**Figure 19: CN7 - Connector for RS 232 Communication on Serial Line A**

Signals description:

- **RxD A** = I - RS 232 serial line A: Receive Data.
- **TxD A** = O - RS 232 serial line A: Transmit Data.
- **CTS A** = I - RS 232 serial line A: Clear To Send.
- **RTS A** = O - RS 232 serial line A: Request To Send.
- **GND** = - Ground signal.
- **N.C.** = - Not connected.
CN5 - CONNECTOR FOR RS 232 ON SERIAL LINE B

CN5 is a 9 pins male D connector, which carries the RS 232 signals connected to serial line B. The signals on this connector follow the CCITT specifications DTE interface; signals location on this connector has been designed to reduce problems due to interference.

**FIGURE 20: CN5 - CONNECTOR FOR RS 232 COMMUNICATION ON SERIAL LINE B**

Signals description:

- **RxD B** = I - RS 232 serial line B: Receive Data.
- **TxD B** = O - RS 232 serial line B: Transmit Data.
- **CTS B** = I - RS 232 serial line B: Clear To Send.
- **RTS B** = O - RS 232 serial line B: Request To Send.
- **GND** = - Ground signal.
- **N.C.** = - Not connected.
CN3 - CONNECTOR FOR RS 422, RS 485 AND CURRENT LOOP

CN7 is a 9 pins female D connector, which carries the RS 422, RS 485 and Current Loop signals connected to serial line A. The signals location on this connector has been designed to reduce problems due to interference.

![Diagram of CN3 Connector](image)

**Figure 21: CN3 - Connector for RS 422, RS 485 and Current Loop**

Signals description:

- **RX-RS422** = I - RS 422 serial line B: Receive Data Negative.
- **RX+RS422** = I - RS 422 serial line B: Receive Data Positive.
- **TX-RS422** = O - RS 422 serial line B: Transmit Data Negative.
- **TX+RS422** = O - RS 422 serial line B: Transmit Data Positive.
- **TXRX-RS485** = I - RS 485 serial line B: Receive and Transmit Data Negative.
- **TXRX+RS485** = I - RS 485 serial line B: Receive and Transmit Data Positive.
- **TX-C.L.** = I - Current Loop serial line B: Receive Data Negative.
- **RX+C.L.** = I - Current Loop serial line B: Receive Data Positive.
- **TX+C.L.** = O - Current Loop serial line B: Transmit Data Positive.
- **TX+C.L.** = O - Current Loop serial line B: Transmit Data Positive.
- **GND** = - Ground signal.
FIGURE 22: SERIAL COMMUNICATION CONNECTIONS DIAGRAM
FIGURE 23: RS 232 POINT-TO-POINT CONNECTION EXAMPLE

FIGURE 24: RS 422 POINT-TO-POINT CONNECTION EXAMPLE

FIGURE 25: RS 485 POINT-TO-POINT CONNECTION EXAMPLE
Please remark that in a RS 485 network two forcing resistors (3.3 kΩ) must be connected across the net and two termination resistors (120 Ω) must be placed at its extrem, respectively near the Master unit and the Slave unit at the greatest distance from the Master.

Forcing and terminating circuitry is installed on GPC® 15R board. It can be enabled or disabled through specific jumpers, as explained later.

For further informations please refer to TEXAS INSTRUMENTS Data-Book, "RS 422 and RS 485 Interface Circuits", the introduction about RS 422-485.
**Figure 27:** 4 wires Current Loop point-to-point connection example

**Figure 28:** 2 wires Current Loop point-to-point connection example
Possible Current Loop connections are two: 2 wires and 4 wires. These connections are shown in figures 28 and 29 where it is possible to see the voltage for \( V_{CL} \) and the resistances for current limitation \((R)\). The supply voltage varies in compliance with the number of connected devices and voltage drop on the connection cable.

The choice of the values for these components must be done considering that:
- circulation of a \(20\) mA current must be guaranteed;
- potential drop on each transmitter is about \(2.35\) V with a \(20\) mA current;
- potential drop on each receiver is about \(2.52\) V with a \(20\) mA current;
- in case of shortcircuit each transmitter must dissipate at most \(125\) mW;
- in case of shortcircuit each receiver must dissipate at most \(90\) mW.

For further info please refer to HEWLETT-PACKARD Data Book, (HCPL 4100 and 4200 devices).
I/O CONNECTION

To prevent possible connecting problems between GPC® 15R and the external systems, the user has to read carefully the information of the previous paragraphs and he must follow these instructions:

- For RS 232, RS 422, Current Loop or RS 485 communication signals the User must follow the standard rules of these protocols.

- For all TTL signals the user must follow the rules of this electric standard. The connected digital signal must be always referred to card digital ground (GND). For TTL signals, the 0 Vdc level corresponds to logic state "0", while 5 Vdc level corresponds to logic state "1".

- For the optocoupled input signals: only contacts to be acquired must be connecte. Such contacts (relays, switches, etc.) must connect or not connect the input signal IN xxxxx to GND Opto signal; power supply of these inputs must come from the on-board +Vopto signal, which is generated by a specific galvanically isolated section. For the logic correspondence: an open contact will generate a logic 1 while a closed contact will generate a logic 0 according to the NPN standard.

- For the relays output signals: the contacts must be connected directly to the load to drive (power relays, electrovalves, etc.). The board provides the normally open contact NA OUTn that must not exceed 3A or 24 Vac referenced to each contact's common signal. To have the possibility to drive different loads with different supplies, three separated common signals have been made for as many realys groups made of 3, 3, and 2 elements.

ON BOARD INPUT

GPC® 15R card is provided of twelve dip switches (four on DSW1 and eight on DSW2), that can be read by software, normally used for system configuration (operating mode selection, card number programation inside a network system, firmware configuration, etc.). Reading the Dip Switch registers by software, the User obtain a negated combination, in fact "ON" position corresponds to 0 logic state and "OFF" position corresponds to 1 logic state. Only four of the twelve dip switches are always available on the card, in fact DSW2, connected to PPI 82C55 port B, is mounted on socket and it can be replaced by a proper flat cable DIL connector. The DSW1 and PDB registers are allocated in the microprocessor addressing space by the control logic as described in the paragraph "I/O ADDRESSES". To recognize dip switches location on GPC® 15A, please refer to figure 39.
**VISUAL FEEDBACK**

**GPC® 15R** board is provided with 39 LEDs to signal status conditions, as described in the following table:

<table>
<thead>
<tr>
<th>LEDs</th>
<th>COLOUR</th>
<th>MEANING</th>
</tr>
</thead>
<tbody>
<tr>
<td>LD1÷LD8</td>
<td>Red</td>
<td>Visualize the status of the eight relays outputs NA OUT0÷7. If the LED is on then the contact is closed.</td>
</tr>
<tr>
<td>LD9</td>
<td>Red</td>
<td>Indicates the presence of the +5 Vdc supply voltage.</td>
</tr>
<tr>
<td>LD10</td>
<td>Yellow</td>
<td>Indicates the presence of the +Vopto power supply voltage for the optocoupled inputs.</td>
</tr>
<tr>
<td>LD11</td>
<td>Green</td>
<td>Software managed activity LED.</td>
</tr>
<tr>
<td>LD12</td>
<td>Red</td>
<td>Indicates the activation of the on-board /RESET signal.</td>
</tr>
<tr>
<td>LD13</td>
<td>Red</td>
<td>Indicates the activation of the external Watch Dog circuit.</td>
</tr>
<tr>
<td>LD14</td>
<td>Yellow</td>
<td>Indicates the activation of the on-board buzzer.</td>
</tr>
<tr>
<td>LD15÷LD22</td>
<td>Yellow</td>
<td>Visualize the status of the PIO optocoupled input lines IN PB7÷IN PB0. If the LED is on then the input contact is closed.</td>
</tr>
<tr>
<td>LD23</td>
<td>Green</td>
<td>Indicates that J9 is connected in position 1-2, corresponding to SYNCB signal low status, which means RUN mode selected.</td>
</tr>
<tr>
<td>LD24</td>
<td>Yellow</td>
<td>Indicates that J9 is connected in position 2-3, corresponding to SYNCB signal low status, which means DEBUG mode selected.</td>
</tr>
<tr>
<td>LD25</td>
<td>Red</td>
<td>Indicates the activation of CPU /HALT signal.</td>
</tr>
<tr>
<td>LD26÷LD33</td>
<td>Green</td>
<td>Visualize the status of the PIO optocoupled input lines IN PA7÷IN PA0. If the LED is on then the input contact is closed.</td>
</tr>
<tr>
<td>LD34÷LD37</td>
<td>Green</td>
<td>Visualize the status of the CTC optocoupled input lines IN C/T3÷0. If the LED is on then the input contact is closed.</td>
</tr>
<tr>
<td>LD38</td>
<td>Red</td>
<td>Indicates the activation of on-board /INT signal.</td>
</tr>
<tr>
<td>LD39</td>
<td>Red</td>
<td>Indicates that an external Watch Dog retrigger is in progress.</td>
</tr>
</tbody>
</table>

**FIGURE 30: VISUAL FEEDBACK TABLE**

The main purpose of these LEDs is to give a visual indication of the board status, making easier the operations of system working verify. To easily locate these LEDs on the board, please refer to figure 39.
DIGITAL I/O INTERFACES

Through CN9 (I/O Abaco® standard connector) the GPC® 15R card can be connected to all of the numerous grifo® boards featuring the same standard pin out. Installation of these interface is very easy; in fact only a 20 pins flat cable (code FLT.20+20) or a 26 pins GPC®-side and 20 pins interface-sideflat cable (code FLT.26+20) is required, while the software management of these interfaces is as easy; in fact most of the software packages available for GPC® 15R card are provided with the necessary procedures. Remarkable modules are:

- QTP 16P, QTP 24P, KDL x24, KDF 224, DEB 01, etc. that solve all the local operator interfacing problems. These modules are provided with all the resources needed to obtain a high-level human-machine interface (they feature alphanumeric displays, matrix keyboard and visualization LEDs) at a short distance from GPC® 15R card. The available software drivers allow to manage the operator interface resources directly through the high-level instructions for console management.

- IAC 01, DEB 01: it is an interface for CENTRONICS parallel printer that can be connected with a standard printer cable. The printer is managed by software through the high level instructions of the selected programming language (LPRINT for BASIC, PRINTF for C, etc.).

- MCI 64: it a large mass memory support that can directly manage the PCMCIA memory cards RAM, FLASH, ROM, etc.) in their available sizes. About software the developed drivers provide a complete file system interfacing allowing to access the informations stored in the memory card directly through the high-level file management instructions.

- RBO xx, TBO xx, XBI xx, OBI xx: these are buffer interfaces for I/O TTL signals. With these modules the TTL input signals are converted in NPN or PNP optoisolated inputs and the TTL output signals are converted in relays or transistor optoisolated outputs.

For more informations refer to "EXTERNAL CARDS" chapter and the software tools documentation.

RESET KEY

Key P1 on GPC® 15R allows to activate the on-board /RESET signal (according to the connection of jumper J4). When P1 is presses, the board restarts the execution of the program stored in EPROM from a total reset condition. The main purpose of this key is to be able to exit from infinite loop conditions, especially during debug phases. LED LD13 always lights when key P1 is pressed; while the activation of the /RESET signal is indicated by the lighting of LED LD12. To easily locate the reset key please refer to figure 39.
FIGURE 31: LEDs LOCATION
POWER SUPPLY VOLTAGES SELECTION

GPC® 15R board is provided with an efficient circuitry that solves in an efficient and comfortable way the problem of power supply in any employ condition. Here follows the list of the possible configurations for power supply section:

- **Mains power supply**
  In this configuration the board must be supplied through the 220 Vac mains power that must be provided on pins 1 and 2 of CN1. The board generates in autonomy the +Vdc and +Vopto voltages needed to supply its sections keeping them galvanically isolated. Maximum external loads supported are 100 mA for +Vdc and 300 mA for +Vopto.

- **Low voltage power supply**
  In this configuration the board must be supplied with two tensions galvanically isolated that can be commonly found in the control machines electric racks. In detail:

<table>
<thead>
<tr>
<th></th>
<th>MINIMUM</th>
<th>TYPICAL</th>
<th>MAXIMUM</th>
</tr>
</thead>
<tbody>
<tr>
<td>V1 on CN1&amp;13</td>
<td>8 Vac</td>
<td>18 Vac</td>
<td>24 Vac</td>
</tr>
<tr>
<td></td>
<td>12 Vdc</td>
<td>24 Vdc</td>
<td>34 Vdc</td>
</tr>
<tr>
<td>V2 on CN1&amp;13</td>
<td>8 Vac</td>
<td>18 Vac</td>
<td>24 Vac</td>
</tr>
<tr>
<td></td>
<td>12 Vdc</td>
<td>24 Vdc</td>
<td>34 Vdc</td>
</tr>
</tbody>
</table>

  The board generates in autonomy the +Vdc and +Vopto voltages needed to supply its sections keeping them galvanically isolated. Supported external loads can be up to 900 mA on +5 Vdc and 12.5 W on +Vopto, provided that the two external supplies can erogate enough power.

+Vcc indicates the board's supply and +Vopto indicates the optocoupled inputs section power supply. Please remark that the desired supply section must be explicitly specified in the order; in fact the choice implies a different hardware configuration that must be performed by the grifo® technical personnel.
JUMPERS

On GPC® 15R there are 15 jumpers for card configuration. Connecting these jumpers, the user can define for example the memory type and size, the peripheral devices functionality and so on. Below there is the jumpers list, location and function:

<table>
<thead>
<tr>
<th>JUMPERS</th>
<th>N. PIN</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>J1</td>
<td>3</td>
<td>Connects Power Failure circuitry to /NMI signal.</td>
</tr>
<tr>
<td>J2</td>
<td>3</td>
<td>Selects the external Watch Dog circuitry working mode.</td>
</tr>
<tr>
<td>J3</td>
<td>2</td>
<td>Enables the disactivation of the 8 relays output signals when a /RESET signal is triggered.</td>
</tr>
<tr>
<td>J4</td>
<td>4</td>
<td>Selects the /RESET circuitry connection mode.</td>
</tr>
<tr>
<td>J5, J12</td>
<td>2</td>
<td>Connect the termination resistors to the RS 422 or RS 485 transmission and reception signals.</td>
</tr>
<tr>
<td>J6</td>
<td>4</td>
<td>Selects the communication type (RS 232, RS 422, RS 485, Current Loop) for serial line B.</td>
</tr>
<tr>
<td>J7</td>
<td>5</td>
<td>Selects directionality and activation mode for serial line B in RS 422 or RS 485.</td>
</tr>
<tr>
<td>J8</td>
<td>3</td>
<td>Selects the reception driver for serial line B in RS 422 or RS 485.</td>
</tr>
<tr>
<td>J9</td>
<td>3</td>
<td>Sets the /SYNCB handshake signal status, to switch between RUN or DEBUG mode.</td>
</tr>
<tr>
<td>J10</td>
<td>3</td>
<td>Sets IC 27 for 2 or 8 KBytebacked SRAM.</td>
</tr>
<tr>
<td>J11</td>
<td>3</td>
<td>Sets IC 32 for EPROM or FLASH EPROM.</td>
</tr>
<tr>
<td>J13</td>
<td>2</td>
<td>Sets the DCDB handshake signal status, used as generic user input.</td>
</tr>
<tr>
<td>J14</td>
<td>3</td>
<td>Sets IC 32 for EPROM or FLASH EPROM.</td>
</tr>
<tr>
<td>J15</td>
<td>3</td>
<td>Sets SRAM size on IC 29.</td>
</tr>
</tbody>
</table>

**Figure 32: JUMPERS summarizing table**

The following tables describe all the right connections of GPC® 15R jumpers with their relative functions. To recognize these valid connections, please refer to the board printed diagram (serigraph) or to figure 41 of this manual, where the pins numeration is listed; for recognizing jumpers location, please refer to figure 37. The "*" used in the following tables, denotes the default connection, or on the other hand the connection set up at the end of testing phase, that is the configuration the User receives.
2 PINS JUMPERS

<table>
<thead>
<tr>
<th>JUMPERS</th>
<th>CONNECTION</th>
<th>USE</th>
<th>DEF.</th>
</tr>
</thead>
<tbody>
<tr>
<td>J3</td>
<td>not connected</td>
<td>It does not connect the on-board /RESET signal to the relays management circuitry.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>connected</td>
<td>It connects the on-board /RESET signal to the relays management circuitry. Whenever /RESET signal is activated, the 8 output contacts of the relays are set open.</td>
<td>*</td>
</tr>
<tr>
<td>J5, J12</td>
<td>not connected</td>
<td>They do not connect the termination resistors to the RS 422 or RS 485 transmission and reception signals.</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>connected</td>
<td>They connect the termination resistors to the RS 422 or RS 485 transmission and reception signals.</td>
<td></td>
</tr>
<tr>
<td>J13</td>
<td>not connected</td>
<td>Connects SIO DCDB signal to +5 Vdc, setting a logic status 1.</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>connected</td>
<td>Connects SIO DCDB signal to GND, setting a logic status 0.</td>
<td></td>
</tr>
</tbody>
</table>

**Figure 33: 2 pins jumpers table**

4 PINS JUMPERS

<table>
<thead>
<tr>
<th>JUMPERS</th>
<th>CONNECTION</th>
<th>USE</th>
<th>DEF.</th>
</tr>
</thead>
<tbody>
<tr>
<td>J4</td>
<td>position 1-2</td>
<td>Connects reset circuitry to key P1.</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>position 2-3</td>
<td>Connects reset circuitry to external Watch Dog circuitry.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>position 2-4</td>
<td>Connects reset circuitry to internal Watch Dog circuitry.</td>
<td></td>
</tr>
<tr>
<td>J6</td>
<td>position 1-2</td>
<td>Sets serial line B in RS 232</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>position 2-3</td>
<td>Sets serial line B in Current Loop</td>
<td></td>
</tr>
<tr>
<td></td>
<td>position 2-4</td>
<td>Sets serial line B in RS 422 or RS 485</td>
<td></td>
</tr>
</tbody>
</table>

**Figure 34: 4 pins jumpers table**
### 3 PINS JUMPERS

<table>
<thead>
<tr>
<th>JUMPERS</th>
<th>CONNECTION</th>
<th>USE</th>
<th>DEF.</th>
</tr>
</thead>
<tbody>
<tr>
<td>J1</td>
<td>position 1-2</td>
<td>It does not connect the Power Failure circuitry to /NMI signal.</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>position 2-3</td>
<td>It connects the Power Failure circuitry to /NMI signal.</td>
<td></td>
</tr>
<tr>
<td>J2</td>
<td>position 1-2</td>
<td>Sets astable working mode for external Watch Dog circuitry.</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>position 2-3</td>
<td>Sets monostable working mode for external Watch Dog circuitry.</td>
<td></td>
</tr>
<tr>
<td>J8</td>
<td>position 1-2</td>
<td>Sets IC 20 as reception driver for RS 422 or RS 485.</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>position 2-3</td>
<td>Sets IC 19 as reception driver for RS 422 or RS 485.</td>
<td></td>
</tr>
<tr>
<td>J9</td>
<td>position 1-2</td>
<td>Connects SIO SYNCB signal to +5 Vdc, turning on LD23 and selecting RUN mode.</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>position 2-3</td>
<td>Connects SIO SYNCB signal to GND, turning on LD24 and selecting DEBUG mode.</td>
<td></td>
</tr>
<tr>
<td>J10</td>
<td>position 1-2</td>
<td>Sets IC 27 for backed SRAM or EEPROM of 8 KByte</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>position 2-3</td>
<td>Sets IC 27 for backed SRAM of 2 KByte</td>
<td></td>
</tr>
<tr>
<td>J11</td>
<td>position 1-2</td>
<td>Sets IC 32 for FLASH EPROM</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>position 2-3</td>
<td>Sets IC 32 for EPROM</td>
<td></td>
</tr>
<tr>
<td>J14</td>
<td>position 1-2</td>
<td>Sets IC 32 for FLASH EPROM</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>position 2-3</td>
<td>Sets IC 32 for EPROM</td>
<td></td>
</tr>
<tr>
<td>J15</td>
<td>position 1-2</td>
<td>Sets IC 29 for SRAM of 128K Byte</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>position 2-3</td>
<td>Sets IC 29 for SRAM of 512K Byte</td>
<td></td>
</tr>
</tbody>
</table>

**Figure 35: 3 pins jumpers table**

The "*" used in the following tables, denotes the default connection, or on the other hand the connection set up at the end of testing phase, that is, the configuration the User receives.
5 PINS JUMPER

<table>
<thead>
<tr>
<th>JUMPER</th>
<th>CONNECTION</th>
<th>USE</th>
<th>DEF</th>
</tr>
</thead>
<tbody>
<tr>
<td>J7</td>
<td>position 1-2 and 3-4</td>
<td>Enables 2 wires half duplex RS 485 communication on serial line B.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>position 2-3 and 4-5</td>
<td>Enables 4 wires half or full duplex RS 422 communication on serial line B.</td>
<td>*</td>
</tr>
</tbody>
</table>

**FIGURE 36: 5 PINS JUMPERS TABLE**

The "*" used in the following tables, denotes the default connection, or on the other hand the connection set up at the end of testing phase, that is the configuration the User receives.
FIGURE 37: JUMPERS LOCATION
RESET AND WATCH DOG

On GPC® 15R there are two separated Watch Dog circuits that are really efficient and easy to use. The most important features of the external Watch Dog circuitry are:

- astable mode;
- intervention time fixed at 700 ms (modifiable by hardware);
- enable function by hardware;
- retrigger by software;

Jumper J4 selects the operating mode of external watch dog circuit between monostable (when intervention time is elapsed the circuit become active and it stays active as far as a reset or power on happens) and astable (when intervention time is elapsed the circuit become active, it stays active till the end of reset time and after it is again deactivated). The external Watch Dog intervent is signaled by the lighting of LED LD8.

The most important features of the CPU internal Watch Dog circuitry are:

- monostable mode;
- intervention time programmable by software;
- enable function by software and hardware;
- retrigger by software;

Jumper J4 selects the reset source and at the same time it defines the Watch Dog circuits connection; its available connections don't allow contemporaneously connection of both Watch Dog circuits. In monostable mode when intervention time is elapsed the circuit becomes active and it stays active as far as a reset or power on happens.

In response to a /RESET signal activation and successive deactivation the board restarts the execution of the program stored at address 0000H on IC32 (EPROM or FLASH EPROM). About retrigger operation of internal and external Watch Dog circuits, please refer to paragraph "WATCH DOG" in chapter "PERIPHERAL DEVICES SOFTWARE DESCRIPTION" and to appendix B of this manual.

RELAY OUTPUTS DISABILITATION SELECTION

Through jumper J3 the User selects whether to connect the board's /RESET signal to the relays output abilitation circuitry or not; if such jumper is connected then the relays outputs are disabled on the contacts on CN2 are opened when /RESET signal is activated. Viceversa, if J3 is not connected the /RESET signal has no effect on the relays outputs, that are anyway disabled when a power on occurs. This feature has great importance when a Watch Dog circuitry is being used and the status of the relays outputs must not be changed by the intervent of such circuitry.
CONFIGURATION INPUTS

GPC® 15R is provided with a 4 pins Dip Switch (DSW1), a n 8 pins Dip Switch (DSW2) and two jumper (J9 and J13), the jumper J9 selects the RUN/DEBUG modality, typically used for system configuration and software readable. Most common applications for these devices are working conditions settings or firmware parameters input, etc.

Please remark that Dip Switch DSW2 is installed on a socket and is connected to digital signals of PPI 82C55 port B. These signals are available to the User simply removing the Dip Switch and connecting to socket DSW2 through a proper flat cable DIL connector.

Configuration inputs read modalities can be found in the chapter "PERIPHERAL DEVICES SOFTWARE DESCRIPTION", while to easily locate them on the board please refer to figures 37 and 39.

INTERRUPTS

A remarkable feature of GPC® 15R card is the powerful interrupt management. Here follows a short description of which devices can generate interrupts and their modalities; for further informations about interrupts management please refer to the microprocessor data sheet or to the appendix B of this manual.

- **ABACO® I/O BUS** -> Generates a CPU /NMI if jumper J6 is in position 1-2. Generates normal /INT, without regard for the daisy chain priority, if jumper J6 is in position 7-8.

- **CPU peripherals** -> CPU internal sections CTC, SIO, PIO generate normal or vectored /INT, respecting the daisy chain priority.

The daisy chain on the GPC® 15R board is made only of SIO, PIO and CTC and can be software programmed through one of the microprocessor internam registers. This way the User can always respond promptly and efficiently to any external event, also deciding the priority to assign to the several event sources.

For further informations please refer to appendix B of this manual.
SERIAL COMMUNICATION SELECTION

Serial line A can be buffered only as RS 232 while serial line B can be buffered in RS 232, RS 422, RS 485 or Current Loop. By hardware can be selected which one of these electric standards is used, through jumpers connection (as described in the previous tables) and drivers installation. By software the serial line can be programmed to operate with all the standard physical protocols, in fact the bits per character, parity, stop bits and baud rates can be decided by setting opportunes CPU internal registers. In the following paragraphs there are all the informations on serial communication configurations.

Some devices needed for RS 422, RS 485 and Current Loop configurations are not mounted on the board in standard configuration; this is why each fist non-standard (non-RS 232) serial configuration for line B must be always performed by grifo® technicians. This far the User can change in autonomy the configuration following the informations below:

- SERIAL LINE B IN RS 232 (default configuration)

<table>
<thead>
<tr>
<th>J6</th>
<th>J7</th>
<th>J8</th>
<th>J5, J12</th>
<th>IC17</th>
<th>IC18</th>
<th>IC19</th>
<th>IC20</th>
<th>IC39</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>don't care</td>
<td>don't care</td>
<td>don't care</td>
<td>don't care</td>
<td>don't care</td>
<td>don't care</td>
<td>driver MAX 202</td>
<td></td>
</tr>
</tbody>
</table>

- SERIAL LINE B IN CURRENT LOOP (option .CLOOP)

<table>
<thead>
<tr>
<th>J6</th>
<th>J7</th>
<th>J8</th>
<th>J5, J12</th>
<th>IC17</th>
<th>IC18</th>
<th>IC19</th>
<th>IC20</th>
<th>IC39</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>don't care</td>
<td>position 1-2</td>
<td>don't care</td>
<td>HCPL 4200</td>
<td>HCPL 4100</td>
<td>no device</td>
<td>no device</td>
<td>no device</td>
</tr>
</tbody>
</table>

Please remark that Current Loop serial interface is passive, so it must be connected an active Current Loop serial line, that is a line provided with its own power supply. Current Loop interface can be employed to make both point-to-point and multi-point connections through a 2-wires or a 4-wires connection.

- SERIAL LINE B IN RS 422 (option .RS 422)

<table>
<thead>
<tr>
<th>J6</th>
<th>J7</th>
<th>J8</th>
<th>J5, J12</th>
<th>IC17</th>
<th>IC18</th>
<th>IC19</th>
<th>IC20</th>
<th>IC39</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>position 2-4</td>
<td>position 2-1</td>
<td>(*1)</td>
<td>no device</td>
<td>no device</td>
<td>SN 75176 or MAX 483</td>
<td>SN 75176 or MAX 483</td>
<td>no device</td>
</tr>
</tbody>
</table>

Status of signal /RTSB, which is software managed, allows to enable or disable the transmitter as follows:

/RTSB = low level  = logic state 0  ->  transmitter enabled
/RTSB = high level = logic state 1  ->  transmitter disabled

In point-to-point connections, signal /RTSB can be always kept low (transmitter always enabled), while in multi-point connections transmitter must be enabled only when a transmission is requested.
FIGURE 38: SERIAL COMMUNICATION DRIVERS LOCATION

Serial B in RS 232

Serial B in Current Loop

Serial B in RS 422

Serial B in RS 485
- SERIAL LINE B IN RS 485 (option .RS 485)

<table>
<thead>
<tr>
<th>Pin</th>
<th>Position</th>
<th>IC</th>
</tr>
</thead>
<tbody>
<tr>
<td>J6</td>
<td>position 2-4</td>
<td>IC17 = no device</td>
</tr>
<tr>
<td>J7</td>
<td>position 1-2</td>
<td>IC18 = no device</td>
</tr>
<tr>
<td>J8</td>
<td>position 1-2 and 3-4</td>
<td>IC19 = SN 75176 or MAX 483</td>
</tr>
<tr>
<td>J5, J12</td>
<td>(*1)</td>
<td>IC20 = no device</td>
</tr>
</tbody>
</table>

In this modality the signals to use are pins 1 and 2 of connector CN3, that become transmission or reception lines according to the status of signal /RTSB, managed by software, as follows:

/RTSB = low level = logic state 0 -> transmitter enabled
/RTSB = high level = logic state 1 -> transmitter disabled

This kind of serial communication can be used for multi-point connections, in addition it is possible to listen to own transmission, so the User is allowed to verify the success of transmission. In fact, any conflict on the line can be recognized by testing the received character after each transmission.

(*1) If using the RS 422 or RS 485 serial line, it is possible to connect the terminating circuit on the line by using J5 and J12. This circuit must be always connected in case of point-to-point connections, while in case of multi-point connections it must be connected only in the farthest boards, that is on the edges of the communication line.

When a reset or a power on occur, signal /RTSB is kept to a logic level high, so in one of these two cases driver RS 485 is receiving or RS 422 driver is disabled, avoiding eventual conflicts in communication. For further informations about serial communication please refer to the examples of figures 23÷29 and to appendix B of this manual.
MEMORIES SELECTION

On GPC® 15R can be mounted up to 1040K bytes of memory divided in several configurations, as described in the following table:

<table>
<thead>
<tr>
<th>IC</th>
<th>DEVICE</th>
<th>SIZE</th>
<th>JUMPERS CONNECTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>32</td>
<td>EPROM</td>
<td>128K Byte</td>
<td>J11 and J14 in position 2-3</td>
</tr>
<tr>
<td></td>
<td>EPROM</td>
<td>256K Byte</td>
<td>J11 and J14 in position 2-3</td>
</tr>
<tr>
<td></td>
<td>EPROM</td>
<td>512K Byte</td>
<td>J11 and J14 in position 2-3</td>
</tr>
<tr>
<td></td>
<td>FLASH EPROM</td>
<td>128K Byte</td>
<td>J11 and J14 in position 1-2</td>
</tr>
<tr>
<td></td>
<td>FLASH EPROM</td>
<td>256K Byte</td>
<td>J11 and J14 in position 1-2</td>
</tr>
<tr>
<td></td>
<td>FLASH EPROM</td>
<td>512K Byte</td>
<td>J11 and J14 in position 1-2</td>
</tr>
<tr>
<td>29</td>
<td>SRAM</td>
<td>128K Byte</td>
<td>J15 in position 1-2</td>
</tr>
<tr>
<td></td>
<td>SRAM</td>
<td>512K Byte</td>
<td>J15 in position 2-3</td>
</tr>
<tr>
<td>27</td>
<td>SRAM+RTC</td>
<td>2K Byte</td>
<td>J10 in position 2-3</td>
</tr>
<tr>
<td></td>
<td>SRAM+RTC</td>
<td>8K Byte</td>
<td>J10 in position 1-2</td>
</tr>
<tr>
<td>37</td>
<td>EEPROM</td>
<td>256÷8K Byte</td>
<td>-</td>
</tr>
</tbody>
</table>

**FIGURE 40: MEMORY SELECTION TABLE**

All the above described devices must feature a JEDEC compliant pin out except for the serial EEPROM installed on IC37 that must be requested to grifo® in the ordering phase. To determine the name of the memory devices that can be mounted, please refer to the manufacturer documentation. GPC® 15R is delivered in its default configuration, this means 128K SRAM on IC29; any different memory configuration can be mounted by the User in autonomy or requested to grifo® in the order.

Below are reported the order codes for the several optional memory configurations:

- .EE-08 -> 1K serial EEPROM
- .EE-16 -> 2K serial EEPROM
- .EE-64 -> 8K serial EEPROM
- .512K -> 512K work SRAM
- .2KMOD -> 2K backed SRAM
- .8KMOD -> 8K backed SRAM
- .2KRTC -> 2K backed SRAM with RTC
- .8KRTC -> 8K backed SRAM with RTC

For further informations about memory options and their cost please contact grifo®, while to easily locate the memory devices on the board please refer to figure 39.
FIGURE 41: COMPONENTS MAP
SOFTWARE DESCRIPTION

A wide selection of software development tools can be obtained, allowing use of the module as a system for its own development, both in assembler and in other high level languages; in this way the User can easily develop all the requested application programs in a very short time. Generally all software packages available for the mounted microprocessor, or for the Z80 family, can be used:

GET 80
It is a complete program with Editor, Communication driver, and Mass Memory management for all Z80 family cards. This program, developed by grifo®, allows to operate in the best conditions when GDOS, FGDOS or xGDOS MCI software tools are used; GET 80 is supplied when one of these tools is ordered and it is personalized with name and general data of the customer. A useful list of pull down menus and the possibility of using mouse, make program use very comfortable. GET 80 program can be executed both on MS-DOS system and on MACINTOSH computers too, through SOFT-PC program. It is supplied on MS-DOS 3”1/2 floppy disk with the documentation on GDOS 80 manual.

GDOS 15R
It is a complete development tool for GPC® 15R card. It is supplied together with GET 80 program to allow an easy and immediate use of this powerful development system. GDOS is divided in two different structures: the first one works on PC maintaining serial communication with the second one. The second structure is on EPROM, it works on board of the card and it is an efficient operating system that executes many low level functions and, at the same time, it allows high level language use. The combination of the said structures results in a complete machine, in fact the card uses PC resources (like floppy disk, hard disk, printer, keyboard, monitor, etc.) as its own peripheral devices. This resulting “virtual machine” performs operation in a transparent way for the User, so this latter can operate with the same modality of standard PC languages. It is really interesting the compatibility of GDOS with all CP/M program and languages; so, if the User has experience, knowledge or developed applications with CP/M, he can use immediately GDOS, without any changes. Moreover, GDOS can manage all memory devices exceeding 64K Bytes as RAM disk and ROM disk. The on board RAM devices can directly be used performing data read and write operations with the confortable file formats.
This software tools is supplied on EPROM with MS-DOS GET 80 floppy disk, some examples, utilities and the operating system documentation.

FGDOS 15R
It is really similar to GDOS, but it can program and erase the on board FLASH EPROM with the application program developed from the User. In this way the external EPROM programmer is not necessary to store definitely the program and it is possible to modify or to add code directly on the installed machine, through a portable PC.
This software tools is supplied on FLASH EPROM with MS-DOS GET 80 floppy disk, some examples, utilities and the operating system documentation.

NOICE
It is a PC hosted debugger consists of a target specific DOS program, NOICExxx.EXE, and a target resident monitor program. The two programs communicate via RS 232. NOICE includes: source level debug; a disassembler; a file viewer; memory display and editing; a virtually unlimited number of breakpoints; hardware free single step; definition of symbols; the ability to record and play back files of commands; on line help.
xGDOS MCI 15R
It is a version of GDOS or FGDOS software tools, capable of PCMCIA Memory Card management. Using MCI 64 card, the GDOS operating system manages memory cards as RAM disk or ROM disk. All applications with data acquisition and data logging can be realized with high level languages that manage data on files, with a fast development time and without any software complication. This software tool is supplied on EPROM or FLASH EPROM with MS-DOS GET 80 floppy disk, some examples, utilities and the operating system documentation.

CBZ-80
It is a Basic Compiler that generates a really compact and fast code. It must work together with any GDOS version and it can exceed the 64K memory limits of Z80 family microprocessors through CHAIN modality. More than one application program can be saved in RAM and/or ROM disks and subsequently executed. In conjunction to the powerful GET 80 Editor the CBZ 80 program becomes a comfortable and really efficient development system for any kind of application program. This program is supplied ad ROM DISK file in GDOS EPROM or FLASH EPROM and on MS-DOS floppy disk with some examples and manual.

PASCAL 80
It is an efficient and complete PASCAL Compiler for Z80 family cards, with features similar to Release 3.0 of Borland Turbo PASCAL. It must work together with any GDOS version and it can exceed the 64K memory limits of Z80 family microprocessors through OVERLAY modality. More than one application program can be saved in RAM and/or ROM disks and subsequently executed. The terminal emulation of GET 80 program support the typical full screen PASCAL Editor, including the attributes management.
This program is supplied as ROM DISK file in GDOS EPROM or FLASH EPROM and on MS-DOS floppy disk with some examples and manual.

RSD 15R
This software tools is a Remote Symbolic Debugger with two operating mode. The first one is a monitor debugger modality with software emulation on P.C.; the second is a remote monitor debugger modality that execute code directly on the card. Through serial communication the User can: download an HEX file and associated symbol table, debug code in symbolic mode, execute code in step to step mode or in real time mode, set breakpoint, dump and modify memory and registers, etc. RSD software tool supports both Z80 and Z180 instruction sets. Really interesting is the program execution management, in fact many hardware and software breakpoint are supported. RSD can be used together with assembler tools, like ZASM 80, and C Compiler CC 80. It is supplied on EPROM and on MS-DOS floppy disk with technical manual.

ZASM 80
It is a macro cross assemler that operates on any PC with MS-DOS operating system. It supports both Z80 and Z180 instruction sets. The generated code can be debugged on PC, through software simulation, or directly on target card, through remote modality, using RSD software tools. ZASM 80 is compatible with C Compiler CC 80 of which it assemble the compilation result. It is supplied on MS-DOS floppy disk with technical manual.
CC 80
It is a complete C Compiler with ANSI/ISO standard, provided of floating point procedure, that can generate code for Z80 and Z180 family microprocessors. It works together with cross assembler ZASM 80 and Symbolic Debugger RSD.
It is supplied on MS-DOS floppy disk with technical manual.

HI TECH C 80
Professional C Cross Compiler of Hi-Tech Software Inc. This Compiler is terribly fast and it generates a small quantity of code. This result is due to advanced techniques in optimizing the generated code based on Artificial Intelligence techniques which allow to get a very compact and very fast code. The package includes: IDE, Compiler, Code optimizer, Assembler, Linker, Remote Debugger and so on. This tool is Full ANSI/ISO Standard and Full Library Source Code. Once the porting of the Remote-Debugger module is done, this tool allows the user the software debugging directly on the hardware that he is experimenting. This type of specialization of the Remote-Debugger its available from now ant it is supplied with all grifo® CPU cards’. This software package is on 3” 1/2 diskettes under MS-DOS format along with user manual. This version supports these following CPUs: Z80, Z180, 84C011, 84C11, 84C013, 80C13, 84C015, 84C15, 64180, NCS800, Z181, Z182.

DDS MICRO C 85
Low cost ross compiler for C source program. It is a powerful software tool that includes editor, C compiler (integer), assembler, optimizer, linker, library, and remote debugger, in one easy to use integrated development environment. There are also included the library sources and many utilities programs.
addresses and maps

In this chapter are reported all information about card use, related to hardware and software. For example, the registers addresses and the memory allocation are described below.

on board resources allocation

The card devices addresses are managed by a specific control logic, realized with programmable logic devices. This control logic allocates SRAM, EPROM and peripheral devices in a comfortable way for the User.

The control logic is able to manage separately Input/Output peripherals and on board memory. CPU 84C15 is capable to address directly 64K Byte of memory and 256 I/O addresses, the control logic provides on board memory and peripheral devices allocation inside the 1024K Byte address space.

The maps management is completely driven by software through the MMU circuit programming: the used memory can be selected and divided in 32K Byte size segments. About I/O maps the control logic avoids every conflicts problems between CPU internal and external peripherals.

Summarizing the control logic allocates:

- ABACO® I/O BUS
- Up to 512K Byte of EPROM or 512K FLASH EPROM installed on IC32
- Up to 512K Byte of SRAM installed on IC29
- Up to 8K Byte of serial EEPROM, installed on IC37
- Up to 8K Byte of backed SRAM, installed on IC27
- SIO
- CTC
- PIO
- RTC
- Buzzer
- Baud rate generator
- Memory Management Unit (MMU) circuitry
- Configuration Dip Switch DSW1 and DSW2
- Activity LEDs
- Watch Dog circuits
- Output relays

The addresses of all these devices are described in the following paragraphs and can't be set with different values. If some different specific maps are required, please contact directly grifo®.
I/O MAPPING

The on board control logic manages the allocation of all the peripheral devices registers in the microprocessor I/O space, that is 256 bytes long. Next table shows names, addresses, meanings and directions of peripheral device registers (including the internal microprocessor ones).

<table>
<thead>
<tr>
<th>DEVICE</th>
<th>REG.</th>
<th>ADD.</th>
<th>R/W</th>
<th>MEANING</th>
</tr>
</thead>
<tbody>
<tr>
<td>SRAM+RTC IC 27</td>
<td>B0</td>
<td>00H</td>
<td>R/W</td>
<td>1st byte of data block</td>
</tr>
<tr>
<td></td>
<td>B1</td>
<td>01H</td>
<td>R/W</td>
<td>2nd byte of data block</td>
</tr>
<tr>
<td></td>
<td>:</td>
<td>:</td>
<td>:</td>
<td>:</td>
</tr>
<tr>
<td></td>
<td>:</td>
<td>:</td>
<td>:</td>
<td>:</td>
</tr>
<tr>
<td></td>
<td>B15</td>
<td>0FH</td>
<td>R/W</td>
<td>16th byte of data block</td>
</tr>
<tr>
<td>CTC</td>
<td>RC0</td>
<td>10H</td>
<td>R/W</td>
<td>Counter 0 status and data register</td>
</tr>
<tr>
<td></td>
<td>RC1</td>
<td>11H</td>
<td>R/W</td>
<td>Counter 1 status and data register</td>
</tr>
<tr>
<td></td>
<td>RC2</td>
<td>12H</td>
<td>R/W</td>
<td>Counter 2 status and data register</td>
</tr>
<tr>
<td></td>
<td>RC3</td>
<td>13H</td>
<td>R/W</td>
<td>Counter 3 status and data register</td>
</tr>
<tr>
<td>PPI 82C55</td>
<td>PDA</td>
<td>14H</td>
<td>R/W</td>
<td>Port A data register</td>
</tr>
<tr>
<td></td>
<td>PDB</td>
<td>15H</td>
<td>R/W</td>
<td>Port B data register</td>
</tr>
<tr>
<td></td>
<td>PDC</td>
<td>16H</td>
<td>R/W</td>
<td>Port C data register</td>
</tr>
<tr>
<td></td>
<td>CNT</td>
<td>17H</td>
<td>R/W</td>
<td>Status and command register</td>
</tr>
<tr>
<td>SIO</td>
<td>RDA</td>
<td>18H</td>
<td>R/W</td>
<td>Serial line A data register</td>
</tr>
<tr>
<td></td>
<td>RSA</td>
<td>19H</td>
<td>R/W</td>
<td>Serial line A status register</td>
</tr>
<tr>
<td></td>
<td>RDB</td>
<td>1AH</td>
<td>R/W</td>
<td>Serial line B data register</td>
</tr>
<tr>
<td></td>
<td>RSB</td>
<td>1BH</td>
<td>R/W</td>
<td>Serial line B status register</td>
</tr>
<tr>
<td>PIO</td>
<td>PAD</td>
<td>1CH</td>
<td>R/W</td>
<td>Port A data register</td>
</tr>
<tr>
<td></td>
<td>PAS</td>
<td>1DH</td>
<td>W</td>
<td>Port A control register</td>
</tr>
<tr>
<td></td>
<td>PBD</td>
<td>1EH</td>
<td>R/W</td>
<td>Port B data register</td>
</tr>
<tr>
<td></td>
<td>PBS</td>
<td>1FH</td>
<td>W</td>
<td>Port B control register</td>
</tr>
</tbody>
</table>

**Figure 42: I/O addresses table - part 1**
For a detailed description of the registers function, please refer to next chapter "PERIPHERAL DEVICES SOFTWARE DESCRIPTION".

**FIGURE 43: I/O ADDRESSES TABLE - PART 2**

<table>
<thead>
<tr>
<th>DEVICE</th>
<th>REG.</th>
<th>ADD.</th>
<th>R/W</th>
<th>MEANING</th>
</tr>
</thead>
<tbody>
<tr>
<td>RELAYS</td>
<td>RELE'</td>
<td>24H</td>
<td>R/W</td>
<td>Relay outputs set and get status register</td>
</tr>
<tr>
<td>B.R.G.</td>
<td>BAUD</td>
<td>25H</td>
<td>R/W</td>
<td>Two serial lines baud rate management register</td>
</tr>
<tr>
<td>WD. EXT</td>
<td>RWD</td>
<td>25H</td>
<td>R</td>
<td>External Watch Dog retrigger register</td>
</tr>
<tr>
<td>SRAM I/O</td>
<td>MEMIO</td>
<td>26H</td>
<td>R/W</td>
<td>IC 27 addresses management register</td>
</tr>
<tr>
<td>MEMORY ADDRESS</td>
<td>MEM</td>
<td>27H</td>
<td>R/W</td>
<td>Memory devices addresses management register</td>
</tr>
<tr>
<td>ACT. LED</td>
<td>LD11</td>
<td>27H</td>
<td>W</td>
<td>Activity LED management register</td>
</tr>
<tr>
<td>BUZZER</td>
<td>BUZ</td>
<td>27H</td>
<td>W</td>
<td>Buzzer management register</td>
</tr>
<tr>
<td>DSW1</td>
<td>DSW1</td>
<td>27H</td>
<td>R</td>
<td>DSW1 acquisition register</td>
</tr>
<tr>
<td>ABACO® I/O BUS</td>
<td>/ECS1</td>
<td>30H±3FH</td>
<td>R/W</td>
<td>I/O BUS addresses with abilitation from signal /ECS1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>40H±4FH</td>
<td>R/W</td>
<td>I/O BUS addresses with abilitation from signal /ECS2</td>
</tr>
<tr>
<td>I/O BUS</td>
<td></td>
<td>30H±DFH</td>
<td>R/W</td>
<td>I/O addresses for ABACO® I/O BUS</td>
</tr>
<tr>
<td>INTERN. REGS.</td>
<td>SCRP</td>
<td>EEH</td>
<td>R/W</td>
<td>Register for microprocessor control register pointer</td>
</tr>
<tr>
<td></td>
<td>SCDP</td>
<td>EFH</td>
<td>R/W</td>
<td>Register for microprocessor control data port</td>
</tr>
<tr>
<td>INTERN. W.D.</td>
<td>WDTMR</td>
<td>F0H</td>
<td>R/W</td>
<td>Internal Watch Dog programming register</td>
</tr>
<tr>
<td></td>
<td>WDTCR</td>
<td>F1H</td>
<td>W</td>
<td>Internal Watch Dog access register</td>
</tr>
<tr>
<td>INTER.</td>
<td>INTPR</td>
<td>F4H</td>
<td>W</td>
<td>Interrupt priority setting register</td>
</tr>
</tbody>
</table>
ABACO® I/O BUS ADDRESSES

The GPC® 15R control logic defines ABACO® I/O BUS addresses and only these addresses must be used to manages correctly the BUS. As described in figure 43, only the addresses from 30H to DFH; in addition to this addresses subranges 30H÷3FH and 40H÷4FH are managed so to generate automatically two specific enable signals, respectively /ECS1 and /ECS2. Any I/O operations at each one of these addresses enables the /IORQ (or /ECS1 or /ECS2) signal and the other control signals of connector CN11.

MEMORIES MAPPING

The total 1040K Byte of memory supported by the card are divided this way:

- Up to 512K Byte of EPROM or 512K Byte of FLASH EPROM allocated in the memory space
- Up to 512K Byte of SRAM allocated in the memory space
- Up to 8KByte of backed SRAM allocated in the I/O space
- Up to 8K Byte of serial EEPROM allocated in the I/O space

GPC® 15R can directly manage at most 64K bytes of memory that is the microprocessor logic addressable space. On the board this logic space can be divided in two 32K Byte pages: both SRAM and EPROM can be installed on the low page, while only SRAM can be installed on the high page. MMU circuitry, driven through a simple software management, takes care to divide the addressable space in 32K Byte pages and to make them available directly into the CPU addressing space. It is possible to address indirectly a memory area much greater than the area nomally accessible by the CPU just programming the MEM register. Here follow two figures that show the possible memory devices configurations, for further informations please refer to the paragraph "MEMORY MANAGEMENT UNIT", while to easily locate the memory device refer to figure 39. Some software packages, like GDOS and FGDOS, are capable to manage in autonomy the MMU circuitry to make address in the CPU addressable memory area all the available memory without bothering the User.

When a power on or a reset occur, R/E signal is set to 0, so the board starts executing the code located at the logical address 0000H of page 0 on EPROM or FLASH EPROM installed IC13.
**Figure 44: Memory Mapping with R/E=0**

- **SRAM**
  - IC 29

- **EPROM** or **FLASH EPROM**
  - IC 32

Page n° 0

Page n° 1

Page n° 15
**Figure 45: Memory mapping with R/E=1**
PERIPHERAL DEVICES SOFTWARE DESCRIPTION

In the previous paragraphs are described the external registers addresses, while in this one there is a specific description of registers meaning and function (please refer to I/O addresses table, for the registers names and addresses values). For a more detailed description of the devices, please refer to manufacturing company documentation; for microprocessor internal peripheral devices, not described in this paragraph, refer to appendix B. In the following paragraphs the D7÷D0 and .0÷.7 indications denote the eight bits of the combination used in I/O operations.

EXTERNAL WATCH DOG

Retrigger operation of GPC® 15R external Watch Dog circuit is performed with a simple input operation at the address of register RWD. To avoid external Watch Dog activation it is indispensable to perform retrigger operations at regular time periods and the duration of these periods must be smaller than intervention time. If retrigger doesn't happen as before described and jumper J4 is connected, when intervention time is elapsed, the card is reset. By default the intervention time is about 700 ms.

SERIAL EEPROM

For informations about the management of serial EEPROM module installed on IC37, please refer to the documentation of the software package used to program the board. This technical manual reports no further informations about the serial EEPROM management because this acivity employs a very deep knowledge of the device itself. For this, its complete management is affordable through the high level instructions of the software package being used.

Please remark that the first 32 bytes (0÷31) are reserved so the User should avoid to modify their value. Control logic allows serial EEPROM software management through /SYNCA, DTRA and DTRB SIO signals, these are the connections;

- /SYNCA -> DATA signal input (SDA)
- DTRB -> DATA signal output (SDA)
- DTRA -> CLOCK signal (SCL)

Known the serial EEPROM management circuitry hardware implementation, please remark that signals A0,A1,A2 of this device's slave address are all set to logic 0. Bit logic status 0 corresponds to low logic status (=0V) of the corresponding signal, while bit logic status 1 corresponds to low logic status (=0V).

For further informations about SIO signals management modalities please refer to proper technical documentation of appendix B of this manual.
**ACTIVITY LEDS**

On board control logic allows the management of one activity LEDs, called LD11 through the LD11 register:

- **LD11.7** -> set LD11 status
- **DSW1.3** -> get LD11 status

The LED can be lit performing an output operation to the register **LD11** with the corresponding bit set to logical 1. Of course, the LED can be turned off through the same output operation with the corresponding bit reset to logical 0.

Please remark that register LED has the same allocation address of registers MEM and BUZ, so every write operation to the bits of this register must consider the effects on the other devices. To acquire the status of LED LD11 it is enough to perform a read operation from the I/O address of register DSW and mask bit 3.

Register LD11 is reset (all bits 0) when a reset or a power on occur, so after one of such events the LED is turned off.

**CONFIGURATION INPUTS**

**GPC® 15R** is provided with 14 software acquirable User settable configuration inputs divided as follows.

Dip Switch DSW1 can be acquired by software, performing a simple input operation from the address of DSW1 register. This is the correspondence between Dip Switch signals and DSW1 bits:

- **DSW1.7** -> Dip Switch 1.4
- **DSW1.6** -> Dip Switch 1.3
- **DSW1.5** -> Dip Switch 1.2
- **DSW1.4** -> Dip Switch 1.1
- **DSW1.4** -> LED LD11 status (paragraph “ACTIVITY LED”)
- **DSW1.4** -> buzzer status (see paragraph “BUZZER”)
- **DSW1.4** -> /A15 x IC 29 (see paragraph “MMU”)
- **DSW1.4** -> A12xIC27 (paragraph “BACKED SRAM+RTC”)

Only the most significant nibble is used to read the Dip Switch. The signals are in complemented logic, this means that a dip **ON** gives a logic status 0 on the corresponding bit, while a dip **OFF** gives a logic status 1.

Configuration jumper **J13** is connected to /DCCB SIO signal. Configuration jumper **J9** is connected to /SYNCB SIO signal. Jumper J9 connected in **position 1-2** gives logic status 0, while connection in **position 2-3** gives logic status 1. For further informations about the acquisition of /SYNCB signal status, please refer to the proper technical documentation of appendix B of this manual.

Jumper J9 (RUN/DEBUG) works as selector of RUN modality (position 1-2) or DEBUG modality (position 2-3). This feature is used by some of **grifo®** software packages.

For more informations about how to acquire the status of DSW2, which is connected to the digital lines of PPI 82C55 PORT B, please refer to the paragraph about this latter.
BUZZER

Buzzer is activated by performing a "write operation" with bit D6=1 at the address of register BUZ; vice versa buzzer is disabled by performing the same operation with bit D6=0. The remaining seven bits of BUZ register must be set according to the programmation of activity LED circuitry, in fact BUZ register is allocated at the same I/O address used by LD11 register. The buzzer status can be acquired by software performing an input operation from register DSW1 and masking bit D2.

BUZ.6 -> buzzer management
DSW1.2 -> buzzer status acquisition

BUZ register is reset (all bits to 0) after Reset or power on, maintaining disabled the buzzer circuit.

MEMORY MANAGEMENT UNIT

An efficient MMU circuitry takes care to allocate in the CPU addressing space all the memory devices that can be installed on GPC® 15R. This section can be programmed through the MEM register, which is allocated in the I/O addressing space. The bits of MEM register have the following meaning:

MEM:

MEM.7 -> LD11 (please refer to the paragraph "ACTIVITY LED")
MEM.6 -> BUZ (please refer to the paragraph "BUZZER")
MEM.5 -> A18 x IC32 and /A18 x IC29
MEM.4 -> A17 x IC32 and /A17 x IC29
MEM.3 -> A16 x IC32 and /A16 x IC29
MEM.2 -> A15 x IC32
MEM.1 -> /A15 x IC29
MEM.0 -> A12 x IC27 (please refer to the paragraph "BACKED SRAM+RTC")

Bits D1÷D5 selects the page of IC 29 SRAM or IC 32 EPROM, FLASH EPROM that must be used as low page. Bit D0 defines the backed SRAM+RTC address, allocated in microprocessor I/O space. The described settings are performed by an output operation at the address of register MEM, while by an input operation at the same address, a portion of MMU status is obtained. More precisely only bits D0 and D1 of the input data coincide with MEM bits and the most significative nibble (D4÷D7) coincides with DSW1 status.

BAUD: Bit D7 of this register, named R/E, selects the memory device allocated in the low page (0000H÷7FFFH) of microprocessor logical memory space:

R/E = 0 -> IC 32 EPROM, FLASH EPROM
R/E = 1 -> IC 29 SRAM

The remaining bits of this register are used to program the baud rate of the two on board's serial communication lines.

When a reset or a Power On occur all the bits of MEM register are reset (all bits 0); this means to program the MMU section where the low 32K Bytes page consists of page 0 EPROM or FLASH EPROM installed on IC32 and the high 32K Bytes page consists of page 0 SRAM installed on IC29. Please refer to the following table and figures 36 and 37, for all the possible MMU configurations.
"X" means non significant bit, that is that bit can be "1" or "0" without influencing the setting there described.

**FIGURE 46: MMU SECTION POSSIBLE PROGRAMMING TABLE**

<table>
<thead>
<tr>
<th>32K LOW PAGE</th>
<th>32K HIGH PAGE</th>
<th>MMU</th>
<th>R/E</th>
</tr>
</thead>
<tbody>
<tr>
<td>0: IC 32</td>
<td>0: IC 29</td>
<td>XX0000XXB</td>
<td>0</td>
</tr>
<tr>
<td>1: IC 32</td>
<td>0: IC 29</td>
<td>XX0001XXB</td>
<td>0</td>
</tr>
<tr>
<td>2: IC 32</td>
<td>0: IC 29</td>
<td>XX0010XXB</td>
<td>0</td>
</tr>
<tr>
<td>3: IC 32</td>
<td>0: IC 29</td>
<td>XX0011XXB</td>
<td>0</td>
</tr>
<tr>
<td>4: IC 32</td>
<td>0: IC 29</td>
<td>XX0100XXB</td>
<td>0</td>
</tr>
<tr>
<td>5: IC 32</td>
<td>0: IC 29</td>
<td>XX0101XXB</td>
<td>0</td>
</tr>
<tr>
<td>6: IC 32</td>
<td>0: IC 29</td>
<td>XX0110XXB</td>
<td>0</td>
</tr>
<tr>
<td>7: IC 32</td>
<td>0: IC 29</td>
<td>XX0111XXB</td>
<td>0</td>
</tr>
<tr>
<td>8: IC 32</td>
<td>0: IC 29</td>
<td>XX1000XXB</td>
<td>0</td>
</tr>
<tr>
<td>9: IC 32</td>
<td>0: IC 29</td>
<td>XX1001XXB</td>
<td>0</td>
</tr>
<tr>
<td>10: IC 32</td>
<td>0: IC 29</td>
<td>XX1010XXB</td>
<td>0</td>
</tr>
<tr>
<td>11: IC 32</td>
<td>0: IC 29</td>
<td>XX1011XXB</td>
<td>0</td>
</tr>
<tr>
<td>12: IC 32</td>
<td>0: IC 29</td>
<td>XX1100XXB</td>
<td>0</td>
</tr>
<tr>
<td>13: IC 32</td>
<td>0: IC 29</td>
<td>XX1101XXB</td>
<td>0</td>
</tr>
<tr>
<td>14: IC 32</td>
<td>0: IC 29</td>
<td>XX1110XXB</td>
<td>0</td>
</tr>
<tr>
<td>15: IC 32</td>
<td>0: IC 29</td>
<td>XX1111XXB</td>
<td>0</td>
</tr>
<tr>
<td>0: IC 29</td>
<td>0: IC 29</td>
<td>XX111X0XB</td>
<td>1</td>
</tr>
<tr>
<td>1: IC 29</td>
<td>0: IC 29</td>
<td>XX111X1XB</td>
<td>1</td>
</tr>
<tr>
<td>2: IC 29</td>
<td>0: IC 29</td>
<td>XX110X0XB</td>
<td>1</td>
</tr>
<tr>
<td>3: IC 29</td>
<td>0: IC 29</td>
<td>XX110X1XB</td>
<td>1</td>
</tr>
<tr>
<td>4: IC 29</td>
<td>0: IC 29</td>
<td>XX101X0XB</td>
<td>1</td>
</tr>
<tr>
<td>5: IC 29</td>
<td>0: IC 29</td>
<td>XX101X1XB</td>
<td>1</td>
</tr>
<tr>
<td>6: IC 29</td>
<td>0: IC 29</td>
<td>XX100X0XB</td>
<td>1</td>
</tr>
<tr>
<td>7: IC 29</td>
<td>0: IC 29</td>
<td>XX100X1XB</td>
<td>1</td>
</tr>
<tr>
<td>8: IC 29</td>
<td>0: IC 29</td>
<td>XX011X0XB</td>
<td>1</td>
</tr>
<tr>
<td>9: IC 29</td>
<td>0: IC 29</td>
<td>XX011X1XB</td>
<td>1</td>
</tr>
<tr>
<td>10: IC 29</td>
<td>0: IC 29</td>
<td>XX010X0XB</td>
<td>1</td>
</tr>
<tr>
<td>11: IC 29</td>
<td>0: IC 29</td>
<td>XX010X1XB</td>
<td>1</td>
</tr>
<tr>
<td>12: IC 29</td>
<td>0: IC 29</td>
<td>XX001X0XB</td>
<td>1</td>
</tr>
<tr>
<td>13: IC 29</td>
<td>0: IC 29</td>
<td>XX001X1XB</td>
<td>1</td>
</tr>
<tr>
<td>14: IC 29</td>
<td>0: IC 29</td>
<td>XX000X0XB</td>
<td>1</td>
</tr>
<tr>
<td>15: IC 29</td>
<td>0: IC 29</td>
<td>XX000X0XB</td>
<td>1</td>
</tr>
</tbody>
</table>
SIO

For further informations please refer to technical documentation on appendix B of this manual.

PIO

For further informations please refer to technical documentation on appendix B of this manual.

CTC

For further informations please refer to technical documentation on appendix B of this manual.

INTERNAL WATCH DOG

For further informations please refer to technical documentation on appendix B of this manual.

BACKED SRAM+RTC

On GPC® 15R there is a socket (IC 27) for a 2K or 8K bytes backed SRAM module; the backed SRAM can also include a complete Real Time Clock section. In this paragraph is described the software management of these devices.
The addressable space of IC 27 device varies from 2K to 8K bytes and it is allocated in microprocessor I/O space that is 256 bytes long. For this reason the device is divided in many blocks (or pages), each one 16 bytes long. The data are read or wrote performing first a block selection operation and after an input or output operation at the addresses of these block bytes. The number of blocks varies according to module size:

<table>
<thead>
<tr>
<th>Module Size</th>
<th>Blocks</th>
</tr>
</thead>
<tbody>
<tr>
<td>2K module</td>
<td>128</td>
</tr>
<tr>
<td>8K module</td>
<td>512</td>
</tr>
</tbody>
</table>

and the block selection is performed by programmation of the proper register MEMIO, allocated in I/O space. The bits meanings of this register are:

<table>
<thead>
<tr>
<th>MEMIO.x</th>
<th>Axx x IC 7</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.0</td>
<td>A4 x IC 7</td>
</tr>
<tr>
<td>0.1</td>
<td>A5 x IC 7</td>
</tr>
<tr>
<td>0.2</td>
<td>A6 x IC 7</td>
</tr>
<tr>
<td>0.3</td>
<td>A7 x IC 7</td>
</tr>
<tr>
<td>0.4</td>
<td>A8 x IC 7</td>
</tr>
<tr>
<td>0.5</td>
<td>A9 x IC 7</td>
</tr>
<tr>
<td>0.6</td>
<td>A10 x IC 7</td>
</tr>
<tr>
<td>0.7</td>
<td>A11 x IC 7</td>
</tr>
</tbody>
</table>

Axx signals select the block number used on IC 27 module, in fact they coincide with device addresses.
MEMIO register can be used both for output (block selection) and input (selected block acquisition) operations and it is reset (all bits to 0) after a reset or power on.
The last devices address (A12 x IC 27) that must be used for block selection is managed by MEM register, as described in paragraph “MEMORY MANAGEMENT UNIT”.

For example, if the User has to write the byte AAH to the address 0700H of IC 7 device, the following operations must be executed:

1) Reset D0 bit of register MEM, by executing an output operation at the address of this register. Example: OUT 27H,00H

2) Select block number 70H = set byte 70H in MEMIO register, by executing an output operation at the address of this register. Example: OUT 26H,70H

3) Write byte AAH to the first byte of selected block, by executing an output operation at the address of this register. Example: OUT 00H,AAH

When the IC 7 module is a backed SRAM + RTC device, eight internal registers must be used to set and acquire time and data. These registers always are the last eight addresses of the device size, as described in the following table:

<table>
<thead>
<tr>
<th>REGISTER</th>
<th>ADDRESS 2K</th>
<th>ADDRESS 8K</th>
</tr>
</thead>
<tbody>
<tr>
<td>CNT</td>
<td>07F8H</td>
<td>1FF8H</td>
</tr>
<tr>
<td>SEC</td>
<td>07F9H</td>
<td>1FF9H</td>
</tr>
<tr>
<td>MIN</td>
<td>07FAH</td>
<td>1FFAH</td>
</tr>
<tr>
<td>ORE</td>
<td>07FBH</td>
<td>1FFBH</td>
</tr>
<tr>
<td>SETT</td>
<td>07FCH</td>
<td>1FFCH</td>
</tr>
<tr>
<td>GIO</td>
<td>07FDH</td>
<td>1FFDH</td>
</tr>
<tr>
<td>MES</td>
<td>07FEH</td>
<td>1FFEH</td>
</tr>
<tr>
<td>ANN</td>
<td>07FFH</td>
<td>1FFFH</td>
</tr>
</tbody>
</table>

**FIGURE 47: SRAM+RTC registers addresses table**

With these registers the backed RTC can be read (acquisition of actual time and date), wrote (programmation of new time and date), started, stopped, etc. by using simple and fast I/O operations.
ANN = Y7 Y6 Y5 Y4 Y3 Y2 Y1 Y0
where: Y7÷Y0 = BCD year value (00-99)

MES = 0 0 0 M4 M3 M2 M1 M0
where: M4÷M0 = BCD month value (01-12)

GIO = 0 0 D5 D4 D3 D2 D1 D0
where: D5÷D0 = BCD day of the month value (01-31)

SETT = 0 FT 0 0 0 W2 W1 W0
where: W2 W1 W0 = Day of the week value:
  0  0  1 = Sunday
  0  1  0 = Monday
  0  1  1 = Tuesday
  1  0  0 = Wednesday
  1  0  1 = Thursday
  1  1  0 = Friday
  1  1  1 = Saturday
FT = Counter frequency test

ORE = KS 0 H5 H4 H3 H2 H1 H0
where: KS = RTC counter start
  H5÷H0 = BCD hour value (00-23)

MIN = 0 M6 M5 M4 M3 M2 M1 M0
where: M6÷M0 = BCD minutes value (00-59)

SEC = ST S6 S5 S4 S3 S2 S1 S0
where: S6÷S0 = BCD seconds value (00-59)
ST = RTC counter stop

CNT = W R S C4 C3 C2 C1 C0
dove: W = Write operation selection
  R = Read operation selection
  S = Sign bit of compensation combination
  C4÷C0 = compensation combination

Here follows a short explanation about the meaning of the bits:

Bit R - Read operation selection

Setting bit R to "1" inhibites the Real Time Clock registers update, to prevent partial reads if the read operation should occour during the update.
Resetting bit R to "0" restores the normal operations.
Setting R to "1" when an update has already started doesn't stop the update itself.
Bit W - Write operation selection

Like it happens for bit R, setting bit W to "1" inhibites the Real Time Clock registers update, to allow
the User to write the new values in the register bank.
The new values are copied to the internal counters only when bit W is reset to "0", restoring all normal
operations.
Bits KS, FT and all other bits signed with a "0" must be kept to "0".

Bit S and bits C4÷C0 - Signed compensation combination

Thermal drifts in the clock counting can be compensated up to ±63.07 ppm (Parts per Million) along
a 64 minutes compensation cycle by loading opportune values in the bits S and C4÷C0.
Bits C4÷C0 indicate the entity of the compensation in steps of 2.034 ppm, being C0 the least
significant bit, it is possible to input a correction from 0 to 31 steps, which means a maximum
compensation of 31*2.034=63.07 ppm. When sign bit S is set to "1" indicates a positive correction
(the clock is longer), else the correction is negative (the clock is shorter). This capability should
compensate the maximum thermal drift of the internal quartz.
For example, shold the quartz oscillate at exactly 32768 Hz, setting to "1" all bits C4÷C0 wouls
represent 5.35 seconds per month.

Bit FT - Counter frequency test

The least significant bit of SEC register will toggle exactly 512 times per second if the quartz
oscillates exactly at 32768 Hz when bit FT is set to "1". Any deviation of the toggle frequency reflects
perfectly the drift of the quartz oscillation frequency. For example, a deviation of +10 ppm of the
internal quartz frequency could be compensated setting the bits S and C4÷C0 to -5 (S=0 and
C4÷C0=00101).
During the test chip select and addresses must be well-stable.

Bits ST and KS - Counter Stop and Kick Start

To stop the internal oscillator and so optimize th internal battery duration just set bit ST to "1".
For more safety, restarting the clock involves the manipulation of another bit called KS, "Kick Start".
This is the procedure to restart the clock:

1) Set bit W to "1"
2) Reset bit ST to "0"
3) Set bit KS to "1"
4) Reset bit W to "0"
5) Wait 2 seconds
6) Set bit W to "1"
7) Reset bit KS to "0" - This is essential to optomize the duration of the battery
8) Set the desired time and date
9) Reset bit W to "0"

For further information about RTC use, please refer to manufacturing company documentation.
BAUD RATE GENERATOR

The baud rate generator section generates the right frequency signals that are used by SIO to obtain standard baud rates on its serial communication lines. The available baud rates range from 300 baud to 115.2K baud with six intermediary values and they are programmable by software. The baud rate managements is performed by input and output operations at the address of register BAUD and the bits meanings of this register are:

BAUD = R/E  BB2  BB1  BB0  HS BA2  BA1  BA0

where:
R/E = SRAM/EPROM selection bit (please see paragraph “MMU”)
BB2  BB1  BB0 = Select serial line B baud rate
0  0  0 = Set baud rate at 300 baud (HS=0) or 57600 baud (HS=1)
0  0  1 = Set baud rate at 600 baud (HS=0) or 115200 baud (HS=1)
0  1  0 = Set baud rate at 1200 baud
0  1  1 = Set baud rate at 2400 baud
1  0  0 = Set baud rate at 4800 baud
1  0  1 = Set baud rate at 9600 baud
1  1  0 = Set baud rate at 19200 baud
1  1  1 = Set baud rate at 38400 baud

HS = Selects High Speed baud rates for both serial lines

BA2  BA1  BA0 = Select serial line A baud rate
0  0  0 = Set baud rate at 300 baud (HS=0) or 57600 baud (HS=1)
0  0  1 = Set baud rate at 600 baud (HS=0) or 115200 baud (HS=1)
0  1  0 = Set baud rate at 1200 baud
0  1  1 = Set baud rate at 2400 baud
1  0  0 = Set baud rate at 4800 baud
1  0  1 = Set baud rate at 9600 baud
1  1  0 = Set baud rate at 19200 baud
1  1  1 = Set baud rate at 38400 baud

The User sets the desired baud rate on both serial lines by an output operation on register BAUD and he acquires the programmed baud rates by an input operation on the same register. The possibility to acquire the programmed baud rates of both serial lines is really interesting when some completely separated procedures manage at the same time serial communications. For example, the software can change serial line A baud rate with no modifications on serial line B baud rate, etc.

BAUD register is reset (all bits to 0) after reset or power on, setting baud rate at 300 baud on both serial lines.
**PPI 82C55**

This external peripheral device is managed through 4 registers: one status register (CNT) and three data registers (PDA, PDB, PDC). The data registers are available both for input operation (to obtain signal status) and for output operation (to set signal status) with the correspondence described in figure 42. The PPI 82C55 can work in three different modes:

**MODE 0** = it provides two 8 bits bidirectional ports (A,B) and two 4 bits bidirectional ports (C LOW, C HIGH); output signals are latched and input signals are not latched; no handshake signals are provided.

**MODE 1** = it provides two 12 bits ports (A+C LOW and B+C HIGH) where ports A and B are used as 8 I/O lines and port C are used as 4 handshake lines. Both inputs and outputs are latched.

**MODE 2** = it provides a 13 bits port (A+C3÷7) where port A is used as 8 I/O lines and the 5 bits of port C are used as handshake, and a 11 bits port (B+C0÷2) where port B is used as 8 I/O lines and the 3 bits of port C are used as handshakes. Both inputs and outputs are latched.

The device is programmed writing an 8 bits word in the status register CNT, with the following bits meaning:

\[ \text{CNT} = SF \ M1 \ M2 \ A \ CH \ M3 \ B \ CL \]

where:
- **SF** = mode Set Flag: if activated (1) the device is enabled for standard I/O operation
- **M1 M2** = mode selection:
  - 0 0 = mode 0
  - 0 1 = mode 1
  - 1 X = mode 2
- **A** = port A direction: 1=input; 0=output
- **CH** = port C HIGH direction: 1=input; 0=output
- **M3** = mode selection: 1=mode 1; 0=mode 0
- **B** = port B direction: 1=input; 0=output
- **CL** = port C LOW direction: 1=input; 0=output

After Reset or power on PPI 82C55 is programmed in mode 0 with all three ports in input; in this way any connection of PPI 82C55 signals can be used without conflict problems.
RELAY OUTPUTS

To manage the eight relay outputs provided by GPC® 15R, a readable/writeable register called RELE’ is used. The eight bits of such register have the following correspondence to the outputs on CN2:

<table>
<thead>
<tr>
<th>Bit (D7-D0)</th>
<th>Output (OUT 0-7)</th>
</tr>
</thead>
<tbody>
<tr>
<td>D7</td>
<td>OUT 7</td>
</tr>
<tr>
<td>D6</td>
<td>OUT 6</td>
</tr>
<tr>
<td>D5</td>
<td>OUT 5</td>
</tr>
<tr>
<td>D4</td>
<td>OUT 4</td>
</tr>
<tr>
<td>D3</td>
<td>OUT 3</td>
</tr>
<tr>
<td>D2</td>
<td>OUT 2</td>
</tr>
<tr>
<td>D1</td>
<td>OUT 1</td>
</tr>
<tr>
<td>D0</td>
<td>OUT 0</td>
</tr>
</tbody>
</table>

Performing an output operation to the I/O address assigned to the RELE’ register the status of the eight relay outputs is set, while performing an input operation from the same address the status of the eight outputs is read. The correspondence between the logic status of the bits read and the physical status of the outputs is:

<table>
<thead>
<tr>
<th>Logic</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Output disabled = contact open</td>
</tr>
<tr>
<td>1</td>
<td>Output enabled = contact closed</td>
</tr>
</tbody>
</table>

The possibility to read the outputs' status is very interesting, especially if we consider using the board with J3 disconnected; in fact in any moment and any condition the program running on the board can read the outputs' status and modify it according to its needs. Register RELE’ is reset (all bits 0) when a power on occurs or when J3 is connected and a reset occurs, so as consequence of one of these events all the relay outputs are disabled and all the relays' contacts are open.
EXTERNAL CARDS

GPC® 15R can be connected to a wide range of block modules and operator interface system produced by grifo®, or to many system of other companies. The on board resources can be expanded with a simple connection to the numerous peripheral grifo® boards, both intelligent and not, thanks to its standard ABACO® BUS connector. Even cards with ABACO® I/O BUS can be connected, by using the proper mother boards. Hereunder some of these cards are briefly described; ask the detailed information directly to grifo®, if required.

KDL X24 - KDF 224
Keyboard Display LCD 2,4 rows 24 keys
Interface with Fluorescent or LCD display, LEDs backlit, 20x2 or 20x4 characters; up to 24 keys matrix keyboard connector. It is directly driven by a 20 pins ABACO® I/O standard connector; High level languages supported; standard pinout for telephone keyboard.

QTP 24 - QTP 24P
Quick Terminal Panel 24 keys with Parallel interface
Intelligent user panel equipped with Fluorescent or LCD display, LEDs backlit, 20x2 or 20x4 characters; RS 232, RS 422, RS 485 or current loop serial line; serial E2 for set up and message. Possibility of re-naming keys, LEDs and panel name by inserting label with new name into the proper slot; 24 Keys and 16 LEDs with blinking attribute and buzzer manageable by software; built in power supply; RTC option, reader of magnetic badge and relay. The QTP 24P is low cost no intelligent (passive) version. It is directly driven from 16 TTL I/O lines; high level languages supported.

QTP G28
Quick Terminal Panel - LCD Graphic, 28 keys
LCD display 240x128 pixels, CFC backlit; Optocoupled RS 232 line and additional RS 232/422/485/C. L. line; CAN line controller; E2 for set up; RTC and RAM lithium backed; primary graphic object; possibility of re-naming keys, LEDs and panel name; 28 keys and 16 LEDs with blinking attribute and buzzer manageable by software; Buzzer; built-in power supply; reader of magnetic badge and relay option.

MCI 64
Memory Cards Interfaces 64 MBytes
Interfacing card for managing 68 pins PCMCIA memory cards, it is directly driven from any ABACO® I/O standard connector; High level languages GDOS supported.

IBC 01
Interface Block Communication
Conversion card for serial communication, 2 RS 232 lines; 1 RS 422-485 line; 1 optical fibre line; selectable DTE/DCE interface; quick connection for DIN 46277-1 and 3 rails.
FIGURE 48: POSSIBLE CONNECTIONS DIAGRAM

- **1 RS 232 OR RS 422, 485, Current Loop**
- **AUXILIARY POWER SUPPLY OUTPUT**
- **POWER SUPPLY**
  - 220Vac
  - OR +24Vdc o Vac
- **ON BOARD SWITCHING POWER SUPPLY**
- **BUZZER**
- **4 COUNTERS OR 4 Timers**
- **DIGITAL TTL INPUT/OUTPUT**
  - to XBI-01, OBI-01, RBO-08 etc....
- **RELAY**
- **TRANSISTOR**
- **OPTO COUPLED**
- **8 RELAY OUTPUT**
- **EXTERNAL LITIUM BATTERY**
- **8 + 8 INPUT OPTO COUPLED**
- **4 COUNTERS OPTO COUPLED**
- **ANY I/O TYPE**
- **DAC 16**
- **AAC 06**
- **ABC 08**
- **ABC 04**
- **MOTHERBOARD ABB 03**
- **GUARDIAN® 5552**
- **QTP 24 etc.........**
- **PC like or Macintosh**
- **Serial Line RS 232, RS 422, RS 485, Current Loop**
- **OPTIONAL RS 232**
  - 1 RS 232
  - OR RS 422, 485, Current Loop
- **PLC**
- **RS 232**
- **CURRENT LOOP**
- **OPTIONAL RS 232, RS 422, RS 485**
- **DIGITAL TTL INPUT/OUTPUT to XBI-01, OBI-01, RBO-08 etc....**
- **OPTO COUPLED RELAY TRANSISTOR**
- **OPTO COUPLED**
- **4 COUNTERS**
- **MOTHERBOARD ABB 03**
- **ADC 08**
- **ADC 04**
- **DAC 16**
- **AAC 06**
- **ANY I/O TYPE**
- **8 RELAY OUTPUT**
**OBI N8 - OBI P8**
Opto BLOCC Input NPN-PNP
Interface between 8 NPN, PNP optocoupled and displayed input lines, with screw terminal and **ABACO®** standard I/O 20 pins connector; power supply section; connection for DIN Ω rails.

**TBO 01 - TBO 08**
Transistor BLOCC Output
Interface for **ABACO®** standard I/O 20 pins connector; 16 or 8 transistor output lines 45 Vdc 3 A open collector; screw terminal; optocoupled and displayed lines; connection for DIN 247277-1 and 3 rails.

**RBO 08 - RBO 16**
Relé BLOCC Output
Interface for **ABACO®** standard I/O 20 pins connector; 8 or 16 displayed Relays 3A with MOV; screw terminal; connection for DIN Ctype and Ω rails.

**FBC 20 - FBC 120**
Flat Block Contact 20 vie
Interfaccia tra 2 o 1 connettori a perforazione di isolante (scatolino da 20 vie maschi) e la filatura da campo (morsettiera a rapida estrazione). Attacco rapido per guide tipo DIN 46277-1 e 3.

**DEB 01**
Didactic Experimental Board
Supporting card for 16 TTL I/O lines use. It includes: 16 keys, 16 LEDs, 4 digits, 16 keys matrix keyboard, Centronics printer interface, LCD display and fluorescent display interface, **GPC® 68** I/O connector, field connection with screw terminal.

**XBI 01**
miXed BLOCC Input-Output
Interface for **ABACO®** standard I/O 20 pins connector; 8 transistor output lines 45 Vdc 3A; 8 input lines; screw terminal; optocoupled and displayed I/O lines; connection for DIN 247277-1 and 3 rails.

**XBI R4 - XBI T4**
miXed BLOCC Input-Output
Interface for **ABACO®** standard I/O 20 pins connector; 4 Relays 3A with MOV or 4 optocoupled Transistors 3A open collectors; 4 input lines optocoupled; screw terminal; connection for DIN Ctype and Ω rails.

**ZBR xxx**
Zipped BLOCC Relays xx Input + xx Output
Peripheral cards family, relays outputs, equipped with housing for Ω rails mounting. Double power supply built in; 5Vdc section for powering the on board logic and an external CPU cards; second section, galvanically coupled, for the optocoupled input lines. All I/O lines are displayed by LEDs. Relays contacts are 3A and are MOV protected. All I/O connections are availables on quick terminal connectors. 1 connector interface to **ABACO®** I/O BUS. The ZBR serie represent the ideal complement for cards 3 and 4 type. The ZBR cards can be directly driven, through the PC parallel port, by using the PCC A26 low cost interface card. ZBR 324 -> 32 opto in, 24 relays; ZBR 246 -> 24 opto in, 16 relays; ZBR 168 -> 16 opto in, 8 relays; ZBR 84 -> 8 opto in, 4 relays.
ABB 03
ABACO® Block BUS 3 slots
3 slots ABACO® mother board; 4 TE pitch connectors; ABACO® I/O BUS connector; screw terminal for power supply; connection for DIN C type and Ω rails.

ABB 05
ABACO® Block BUS 5 slots
5 slots ABACO® mother board with power supply. Double power supply built in; 5Vdc 2.5A section for powering the on board logic; second section at 24Vdc 400mA galvanically coupled, for the optocoupled input lines. Auxiliary connector for ABACO® I/O BUS. Connection for DIN Ω rails.

ABC 04 - ABC 08
Analog BLOCK Converter - 4 or 8 lines
Module BLOCK for ABACO® I/O BUS; 4 or 8 analog input lines (tension or current); Voltage input ranges: 0±2.5 Vdc or 0±5 Vdc; Current input range: 0±20 mA; 8, 11 or 10 bits of A/D resolution; conversion time 5 ms or 100 µs; staus LEDs; Connections for DIN 46277-1 and 3.

ZBT xxx
Zipped BLOCK Transistors xx Input + xx Output
Peripheral cards family having optocoupled outputs and 3A transistor in open collector. Cards are equipped with housing for Ω rails mounting. Double power supply built in; 5Vdc section for powering the on board logic and an external CPU cards; second section, galvanically coupled, for the optocoupled input lines. All I/O lines are displayed by LEDs. All output transistors are equipped with protection against inductive loads. All I/O connections are availables on easy quick terminal connectors. Connector interface to ABACO® I/O BUS. The ZBT serie represent the ideal complement for cards 3 and 4 type. The ZBT cards can be directly driven, through the PC parallel port, by using the PCC A26 low cost interface card. ZBT 324 -> 32 opto in, 24 transistors; ZBT 246 -> 24 opto in, 16 transistors; ZBT 168 -> 16 opto in, 8 transistors; ZBT 84 -> 8 opto in, 4 transistors.
Here follows a list of manuals that can be a source of further information about the devices installed on GPC® 15R.

TEXAS INSTRUMENTS Manual: The TTL Data Book - SN54/74 Families
TEXAS INSTRUMENTS Manual: RS-422 and RS-485 Interface Circuits
TEXAS INSTRUMENTS Manual: Linear Circuits Data Book - Volume 1 and 3

SGS-THOMSON Data Book: MEMORIES - Data Book
SGS-THOMSON Data Book: INDUSTRY STANDARD LINEAR ICs - Data Book
SGS-THOMSON Manual: Motion Control Application Manual

NEC Manual: Microprocessors and Peripherals - Volume 3
NEC Manual: Memory Products

TOSHIBA Manual: Photo Couplers - Data Book

AMD Manual: Flash Memory Products

MAXIM Manual: New Releases Data Book - Volume IV

XICOR Manual: Data Book


Please connect to the manufactures Web sites to get the latest version of all manuals and data sheets.
This chapter shows the electric diagram of the most frequently used interfaces for GPC® 15R. Every one of these interfaces can be made by the User in autonomy, while only few of them are grifo® standard boards and can be ordered.

**Figure A1: IAC 01 Electric Diagram**
**Title:** KDL/F-2/424  
**Date:** 22-07-1998  
**Page:** 1 of 1

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**Figure A2: KD x24 Electric Diagram**

- **Diagram Description:**
  - The diagram illustrates the electrical connections and components of the KD x24 device.
  - It shows various components such as resistors (R1, R2, R3, R4, R5, R6, R7, R8, R9, RR1, RR2), capacitors (C1, C2, C3, C4, C5, C6), and integrated circuits (IC1, IC2).
  - The connections are labeled with pin numbers and references to other components like LCD20x2, LCD20x4, Futaba VFD, and external keyboard.

---

**Component List:**
- **Resistors:**
  - R1, R2, R3, R4, R5, R6, R7, R8, R9, RR1, RR2
- **Capacitors:**
  - C1, C2, C3, C4, C5, C6
- **Integrated Circuits:**
  - IC1, IC2
- **Connectors:**
  - CN1, CN2, CN3, CN4, CN5, CN6, CN7

---

**Legend:**
- **VFD FUTABA**
- **LCD 20x2**
- **LCD 20x4**
- **External Keyboard 4x6**

---

**Notes:**
- Legend and note for contrast
- Legend for VFD FUTABA
- Legend for LCD 20x2
- Legend for LCD 20x4
- Legend for External Keyboard 4x6

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**Technical Details:**
- **Title:** KDL/F-2/424
- **Date:** 22-07-1998
- **Page:** 1 of 1
**FIGURE A3: QTP 16P ELECTRIC DIAGRAM**
FIGURE A4: QTP 24P ELECTRIC DIAGRAM - PART 1
FIGURE A5: QTP 24P ELECTRIC DIAGRAM - PART 2

Title: QTP 24P
Date: 22-07-1998
Rel. 1.2
Page: 2 of 2
**Figure A6: SPA 03 Electric Diagram**

- **Title:** SPA-03
- **Date:** 16/11/98
- **Page:** 1 of 1
- **Dip Switch:**
  - DSW1
- **Power supply:**
  - +5V
- **IC1:** 74HCT688
- **Components:**
  - C1: 100µF
  - C2: 100nF
  - C3: 100nF
  - C4: 100nF
  - R1: 1K
  - R2: 1K
  - LD1: Rosso
  - LD2: Rosso
  - CN1-CN4: 26 pin connector
  - ABACO® I/O BUS
  - +5V
  - Gnd

---

*Notes:*
- ABACO® I/O BUS
- 26 pin connector
APPENDIX B: ON BOARD COMPONENTS DESCRIPTION

CPU Z84C15

PRODUCT SPECIFICATION

Z84013/015
Z84C13/Z84C15

IPC INTELLIGENT PERIPHERAL CONTROLLER

FEATURES

- Z84C00 Z80 CPU with Z84C30 CTC, Z84C4X SIO, CGC, Watch Dog Timer (WDT). In addition, Z84C15 and Z84015 have Z84C20 PIO.
- High-speed operation 6, 10 MHz
- 16 MHz operation for Z84C15 only.
- Low power consumption in four operation modes:
  - 41 mA Typ. (Run mode)
  - 6 mA Typ. (Idel1 mode)
  - 50 µA Typ. (Idle2 mode)
  - 0.5 µA Typ. (Stop mode)
- Wide operational voltage range (5V ± 10%)
- TTL/CMOS compatible.
- Z84013 features:
  - Z84C00 Z80 CPU
  - On-chip two channel SIO (Z80 SIO)
  - On-chip four channel Counter Timer Controller (Z80 CTC)
  - Built-in Clock Generator Controller (CGC).
- Built-in Watch Dog Timer (WDT).
- Noise filter to CLK/TRG inputs of the CTC.
- 84-pin PLCC package.

Z84015 features:
- All Z84013 features, plus on-chip two 8-bit ports (Z80 PIO) and 100-pin QFP package.

Z84C13/Z84C15 enhancements to Z84013/Z84015:
- Power-on reset.
- Addition of two chip select pins.
- 32-bit CRC for Channel A of SIO.
- Wait state generator.
- Simplified EV mode selection.
- Schmitt-trigger inputs to transmit and receive clocks of the SIO.
- Crystal divide-by-one mode.
- 100-pin QFP (Z84C15 only)

GENERAL DESCRIPTION

The Intelligent Peripheral Controller (IPC) is a series of highly superintegrated devices with four versions. The Z84C13 and the Z84C15 are upward compatible versions of the Z84013 and the Z84015. The Z84015 is a CMOS 8-bit microprocessor integrated with the CTC, SIO, CGC, WDT and the PIO into a single 100-pin Quad Flat Pack (QFP) package. The Z84013 is the Z84015 without PIO, and is housed in an 84-pin PLCC package. The Z84C13 is the Z84013 with enhancements and the Z84C15 is the Z84015 with enhancements. These high-end superintegrated intelligent peripheral controllers are targeted for a broad range of applications ranging from error correcting modems to enhancement/cost reductions of existing hardware using Z80-based discrete peripherals. Figures 1 and 2 show the difference between the Z84013/015 and the Z84C13/Z84C15.

Hereinafter, use the word IPC on the description covering all versions (Z84C13/Z84C15 and Z84013/Z84015). Use Z84C13/15 on the description that applies only to the Z84C13 and Z84C15, and use Z84013/015 on the description that applies only to the Z84013 and Z84015.
### CPU SIGNALS

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Input/Output, 3-State</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ad-A15</td>
<td>16-1(x13), 6-1, 100-91(x15)</td>
<td>IO</td>
<td>16-bit address bus. Specifies I/O and memory addresses to be accessed. During the refresh period, addresses for refreshing are output. The bus is an input when the external master is accessing the on-chip peripherals.</td>
</tr>
<tr>
<td>D0-D7</td>
<td>63-76(x13), 88-92(x15)</td>
<td>IO</td>
<td>8-bit bidirectional data bus. When the on-chip CPU is accessing on-chip peripherals, these lines are set to output and hold the data to/from on-chip peripherals.</td>
</tr>
<tr>
<td>RD</td>
<td>30(x13), 14(x15)</td>
<td>IO</td>
<td>Read signal. CPU read signal for accepting data from memory or I/O devices. When an external master is accessing the on-chip peripherals, it is an input signal.</td>
</tr>
<tr>
<td>WR</td>
<td>20(x13), 13(x15)</td>
<td>IO</td>
<td>Write signal. This signal is output when data, to be stored in a specified memory or peripheral LSI, is on the MPU data bus. When an external master is accessing the on-chip peripherals, it is an input signal.</td>
</tr>
<tr>
<td>MREQ</td>
<td>23(x13), 17(x15)</td>
<td>IO, 3-State</td>
<td>Memory request signal. When an effective address for memory access is on the address bus, &quot;0&quot; is output. When an external master is accessing the on-chip peripherals, it is an input signal.</td>
</tr>
<tr>
<td>IORQ</td>
<td>21(x13), 15(x15)</td>
<td>IO</td>
<td>I/O request signal. When addresses for I/O are on the lower 8 bits (A7-A0) of the address bus in the I/O operation, &quot;0&quot; is output. In addition, the IORQ signal is output with the MI signal at the time of interrupt acknowledge cycle to inform peripheral LSI of the status of the interrupt response vector when put on the data bus. When an external master is accessing the on-chip peripherals, it is an input signal.</td>
</tr>
<tr>
<td>MI</td>
<td>17(x13), 8(x15)</td>
<td>IO</td>
<td>Machine cycle &quot;11&quot;, MREQ and &quot;0&quot; are output. Together in the operation code fetch cycle, MI is output for every opcode fetch when a two byte opcode is executed. In the maskable interrupt acknowledge cycle, this signal is output together with IORQ. It is 3-stated in EV mode.</td>
</tr>
</tbody>
</table>

---

**PIN DEFINITIONS**

The pin assignment for each device is shown in Figures 3 and 4. Following is the description on each pin. For the description and the pin number, it stated as "x13" or "x15", that applies to both Z84C132/Z84C152 or Z84C152/Z84015. Otherwise, C13 for Z84C132, C15 for Z84015, 013 for Z84013 and 015 for Z84015.
### CPU SIGNALS (Continued)

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Input/Output, State</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>RFSH</td>
<td>25(x13), 7(x15)</td>
<td>Out, 3-State</td>
<td>The refresh signal. When the dynamic memory refresh address is on the low order byte of the address bus, RFSH is active along with MREQ signal. This pin is 3-state in 8V mode.</td>
</tr>
<tr>
<td>INT</td>
<td>25(x12), 18(x15)</td>
<td>Open drain</td>
<td>Maskable interrupt request signal. Interrupt is generated by peripheral LSI. This signal is accepted if the interrupt enable flip-flop (IFF) is set to &quot;1&quot;. The INT signal of on-chip peripherals is internally wired-to-OR without pull-up resistors and requires external pull-up. Also, interrupts from on-chip peripherals go out from this pin.</td>
</tr>
<tr>
<td>INI</td>
<td>56(x3), 60(x15)</td>
<td>In</td>
<td>Non-maskable interrupt request signal. This interrupt request has a higher priority than the maskable interrupt request and does not rely upon the state of the interrupt enable flip-flop (IFF).</td>
</tr>
<tr>
<td>HALT</td>
<td>31(x13), 81(x15)</td>
<td>Out, 3-State</td>
<td>Halt signal. Indicates that the CPU has executed a HALT instruction. This signal is 3-state in 8V mode.</td>
</tr>
<tr>
<td>BUSREQ</td>
<td>15(x13), 120(x15)</td>
<td>In</td>
<td>BUS request signal. BUSREQ requests placement of the address bus, data bus, MREQ, /IORQ, /PR and MWR signals into the high impedance state. BUSREQ is normally wired-off and a pull-up resistor is externally connected.</td>
</tr>
<tr>
<td>BUSACK</td>
<td>20(x13), 12(x15)</td>
<td>Out (G130(x16), Out3-State (C19/C16)</td>
<td>Bus Acknowledge signal. In response to the BUSREQ signal, BUSACK informs peripheral devices that the address bus, data bus, MREQ, /IORQ, /PR, and MWR signals have been placed in the high impedance state. Note: For the Z84013G05, the BUSACK signal will not be generated during 8V mode. For the Z84013G05S and BUSACK will be 5-state during 8V mode.</td>
</tr>
<tr>
<td>WAIT</td>
<td>19(x13), 11(x15)</td>
<td>In (D10/M16), (D0/D10)</td>
<td>Wait signal. WAIT informs the CPU that specified memory or peripheral is not ready for data transfer. As long as WAIT signal is active, MPU is continuously kept in the wait state. Note: For the Z84013G05, the WAIT pin becomes an output to bring pull-on-chip wait state generator during the 8V mode.</td>
</tr>
</tbody>
</table>

### CPU SIGNALS (Continued)

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Input/Output, State</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>ATRF</td>
<td>55(x13), 70(x15)</td>
<td>Out</td>
<td>1-bit auxiliary address bus. Output is the same as A[14:7] (A7) of the address bus. However, during a refresh cycle, this pin outputs the address which is the most significant bit of the 8-bit refresh address signal linked to the low order 7 bits of the address bus.</td>
</tr>
</tbody>
</table>

### CTC SIGNALS

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Input/Output, State</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLKTRG0 - CLXTRG3</td>
<td>75-77(x13), 81-83(x15)</td>
<td>In</td>
<td>External clock trigger input. These four CLK/ TRG pins correspond to four Counter/Timer Channels. In the counter mode, each active edge will cause the down-counter to decrement by one. In timer mode, an active edge will start the timer. It is program selectable whether the active edge is rising or falling.</td>
</tr>
<tr>
<td>ZC/T00 - ZC/T03</td>
<td>65-71(x3), 71-77(x15)</td>
<td>Out</td>
<td>Zero count/blank out signals. In either timer or counter mode, pulses are output when the down-counter has reached zero.</td>
</tr>
</tbody>
</table>

### SIO SIGNALS

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Input/Output, State</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mv/RDYA, Mv/RDYNB</td>
<td>32,52(x13), 30,52(x15)</td>
<td>Out</td>
<td>WaitReady signal A and WaitReady signal B. Used as WAIT or READY depending upon SIO programming. When programmed as WAIT they go active at &quot;0&quot;, alerting the CPU that addressed memory or I/O devices are not ready by requesting the CPU to wait. When programmed as READY, they are active at &quot;1&quot; which determines when a peripheral device associated with a DMA pin is ready to receive data.</td>
</tr>
<tr>
<td>SYNCA, SYNCB</td>
<td>20-22(x13), 31-34(x15)</td>
<td>I/O</td>
<td>Synchronous signals in asynchronous receive mode, they act as ACTS and OCDI. In external sync mode these signals act as inputs. In internal sync mode, they act as outputs.</td>
</tr>
<tr>
<td>RxDA, RxDN</td>
<td>34,52(x13), 32,52(x15)</td>
<td>In</td>
<td>Serial receive data signal</td>
</tr>
</tbody>
</table>
### SIO SIGNALS (Continued)

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Input/Output, 3-State</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>RXC / RXCB</td>
<td>35,51(x13), 33,49(x15)</td>
<td>In</td>
<td>Receive clock signal. In the asynchronous mode, the receive clocks can be 1, 16, 32, or 64 times the data transfer rate.</td>
</tr>
<tr>
<td>TXC / TXCB</td>
<td>35,50(x13), 34,48(x15)</td>
<td>In</td>
<td>Transmitter clock signal. In the asynchronous mode, the transmitter clocks are always 1, 16, 32, or 64 times the data transfer rate.</td>
</tr>
<tr>
<td>TxD (TXD)</td>
<td>37,49(x13), 36,47(x15)</td>
<td>Out</td>
<td>Serial transmit data signal.</td>
</tr>
<tr>
<td>RXD (RXD)</td>
<td>36,48(x13), 38,46(x15)</td>
<td>Out</td>
<td>Data terminal ready signal. When ready, these signals go inactive to enable the terminal transmitter. When not ready, they go inactive to disable the transfer from the terminal.</td>
</tr>
<tr>
<td>RTS (RTS)</td>
<td>39,47(x13), 37,45(x15)</td>
<td>Out</td>
<td>Request to send signal. &quot;0&quot; when transmitting serial data. They are active when enabling their receivers to transmit data.</td>
</tr>
<tr>
<td>CTS (CTS)</td>
<td>40,46(x13), 38,44(x15)</td>
<td>In</td>
<td>Clear to send signal. When &quot;0&quot;, after transmitting these signals the modem is ready to receive serial data. When ready, these signals go active to enable serial data. These signals go inactive to disable transfer from the terminal.</td>
</tr>
<tr>
<td>DCD (DCD)</td>
<td>41,45(x13), 39,43(x15)</td>
<td>In</td>
<td>Data carrier detect signal. When &quot;0&quot;, serial data can be received. These signals are active to enable receivers to transmit data.</td>
</tr>
</tbody>
</table>

### SYSTEM CONTROL SIGNALS

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Input/Output, 3-State</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>IE1</td>
<td>60(x13), 71(x15)</td>
<td>In</td>
<td>Interrupt enable input signal. IE1 is used to control the IEO interrupt when there is more than one interrupt driven peripheral.</td>
</tr>
<tr>
<td>IE0</td>
<td>59(x13), 71(x15)</td>
<td>Out</td>
<td>The interrupt enable output signal in the daisy chain interrupt control. IE0 controls the interrupt of external peripherals. IE0 is active when IE1 is &quot;1&quot; and the CPU is not servicing an interrupt from the on-chip peripherals.</td>
</tr>
<tr>
<td>XCEO</td>
<td>42(C13), 40(C15)</td>
<td>Out</td>
<td>Chip Select 0. Used to access external memory or I/O devices. This pin has been assigned to &quot;CT&quot; pin on Z84001/05. The signal is decoded only from A15-A12 without control signals. Refer to &quot;Functional Description&quot; on-chip select signals for further explanation.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Input/Output, 3-State</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>AC7</td>
<td>40(x13), 42(x15)</td>
<td>Out</td>
<td>Chip Select 1. Used to access external memory or I/O devices. This pin has been assigned to &quot;CT&quot; pin on Z84001/05. The signal is decoded only from A15-A12 without control signals. For details, refer to &quot;Functional Description&quot; on-chip select signals for further explanation.</td>
</tr>
<tr>
<td>WOOUT</td>
<td>41(x13), 71(x15)</td>
<td>Out</td>
<td>Watchdog Timer Output signal. Output pulse width depends on the externally connected pin.</td>
</tr>
<tr>
<td>RESET</td>
<td>28(x13), 9(x15)</td>
<td>In</td>
<td>Reset signal. RESET signal is used to initialize NPU and other devices in the system. Also used to return from the standby state in the STOP or IDLE modes.</td>
</tr>
</tbody>
</table>

### SYSTEM CONTROL SIGNALS (Continued)

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Input/Output, 3-State</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>XTAL1</td>
<td>69(x13), 67(x15)</td>
<td>In</td>
<td>Crystal oscillator connecting terminal. A parallel resonant crystal is recommended. If an external clock source is used as an input to the OSC unit, supply clock goes into this terminal. If external clock is supplied to KLK pin (without OSC unit), this terminal must be connected to &quot;0&quot; or &quot;1&quot;.</td>
</tr>
<tr>
<td>XTAL2</td>
<td>63(x13), 65(x15)</td>
<td>In</td>
<td>Crystal oscillator connecting terminal.</td>
</tr>
<tr>
<td>CLIKIN</td>
<td>67(x13), 69(x15)</td>
<td>In</td>
<td>Single-phase System Clock Input.</td>
</tr>
<tr>
<td>CLKOUT</td>
<td>68(x13), 69(x15)</td>
<td>Out</td>
<td>Single-phase clock output from on-chip Clock Generator/Controller.</td>
</tr>
<tr>
<td>EV</td>
<td>76(x13), 67(x15)</td>
<td>In</td>
<td>Evaluator signal. When &quot;1&quot; is applied to this pin, the CPU is in the Evaluation mode.</td>
</tr>
</tbody>
</table>

Note: For the Z84001/05, together with E1/0, the EV signal outputs the PC into the evaluation mode. When this signal becomes active, the status of INT, AH, AL, and BI is changed to output. When using Z84001/05 that has an external clock, the CPU is electrically disconnected after one machine cycle is executed within EV set to 1 and the EVSET signal to 1. After the execution is finished, the other CPU or Z80/M6800 is changed to its normal operation. This evolves is not 564's status and it should be disconnected by an externally connected circuit. For details, please refer to "Functional Description" on EV mode.
SYSTEM CONTROL SIGNALS (Continued)

Note: For the Z8413/15, to access on-chip resources from the CPU (e.g., I/O, CPU, the CPU is electrically disconnected; A15-40, INH0, INH1, INH2, and INH3 are charged to input O'7. O'0 changes its direction. All input pins and memory are put into high impedance mode when the CPU is set to "I", but BUSACK is 3-state. For details, please refer to "Functional Description" on page 278.

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Input/Output, 3-State</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>ICT</td>
<td>42,44(013), 40,42(015), Note with C13/C15</td>
<td>Out</td>
<td>Test pins. Use in the open state.</td>
</tr>
<tr>
<td>NC</td>
<td>24,37,67,69(x13), flat with x15</td>
<td>Not connected.</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>43,84(x13), 41,90(x15)</td>
<td>Power Supply</td>
<td>+5 Volts</td>
</tr>
<tr>
<td>VSS</td>
<td>22, 63(x13), 18,64(x16)</td>
<td>Power Supply</td>
<td>0 Volts</td>
</tr>
</tbody>
</table>

PIO SIGNALS (for the Z84x15 only)

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Input/Output, 3-State</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>/ASTB</td>
<td>f1(x15)</td>
<td>In</td>
<td>Port A strobe pulse from peripheral device. The signal is used as a handshake between Port A and external circuits. The meaning of this signal depends on the mode of operation selected for Port A (see &quot;PIO Basic Timing&quot;).</td>
</tr>
<tr>
<td>/BSTB</td>
<td>81(x15)</td>
<td>In</td>
<td>Port B strobe pulse from peripheral device. The signal is used as a handshake between Port B and external circuits. The meaning of this signal depends on the mode of operation selected for Port B (see &quot;PIO Basic Timing&quot;).</td>
</tr>
<tr>
<td>ARDY</td>
<td>20(x15)</td>
<td>Out</td>
<td>Register A ready signal. Used as a handshake between Port A and external circuits. The meaning of this signal depends on the mode of operation selected for Port A (see &quot;PIO Basic Timing&quot;).</td>
</tr>
<tr>
<td>BRDY</td>
<td>62(x15)</td>
<td>Out</td>
<td>Register B ready signal. Used as a handshake between Port B and external circuits. The meaning of this signal depends on the mode of operation selected for Port B (see &quot;PIO Basic Timing&quot;).</td>
</tr>
<tr>
<td>PA7-PA6</td>
<td>20-29(x15)</td>
<td>3-State</td>
<td>Port A data signals. Used for data transfer between Port A and external circuits.</td>
</tr>
<tr>
<td>PB7-PB0</td>
<td>53-60(x15)</td>
<td>3-State</td>
<td>Port B data signals. Used for data transfer between Port B and external circuits.</td>
</tr>
</tbody>
</table>

The following pins have different functions between Z8413/15 and Z84C15

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin # X13</th>
<th>Pin # X15</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>RESET</td>
<td>21</td>
<td>9</td>
<td>Functionality is different.</td>
</tr>
<tr>
<td>WRAT</td>
<td>15</td>
<td>15</td>
<td>Functionality is different.</td>
</tr>
<tr>
<td>EV</td>
<td>56</td>
<td>57</td>
<td>Functionality is different.</td>
</tr>
<tr>
<td>NWDOUT</td>
<td>61</td>
<td>73</td>
<td>Push-pull output on Z8413/15, Only.</td>
</tr>
<tr>
<td>ICT</td>
<td>4,40</td>
<td>4,40</td>
<td>(Test pin) on Z8413/15, I/O3 and I/O7 on Z84C15.</td>
</tr>
<tr>
<td>TyCA, TyCB, RoQA and RoQB</td>
<td>34, 36, 52, 51</td>
<td>33, 34, 48, 49</td>
<td>On Z84C15, these signals have Schmitt-triggered inputs.</td>
</tr>
</tbody>
</table>

In EV mode, 3-state on Z84C15/15; remain active on Z8413/15.

FUNCTIONAL DESCRIPTION

The following subsections describe each individual functional unit of the Z8413/15 and Z84C15.

Z84C20 Counter/Timer Logic Unit

This logic unit provides the user with four individual 8-bit Counter/Timer Channels that are compatible with the Z84C20 OTP (Figure 7). The Counter/Timer can be programmed by the CPU for a variety of counting and timing applications. Typical applications include event counting, interrupt and internal counting, and serial baud rate clock generation.

Each of the Counter/Timer Channels, designated Channels 0–3, have an 8-bit prescaler (when used in timer mode) and its own 8-bit counter to provide a wide range of counting resolution. Each of the channels has its own clock/timer input to quantify the counting process and an output to indicate zero crossing/threshold conditions.

With only one internal vector programmed into the logic unit, each channel can generate a unique interrupt vector in response to the interrupt acknowledge cycle.

These two ports have several modes of operation: input, output, bi-directional, or bit control modes. Each pin has two handshake signals (RDY and Sta) which are used to control data transfers. The RDY (ready) indicates that the port is ready for data transfer into the Z8413/15 (strobe) is input to the port that indicates when data transfer has occurred. Each of the pins can be programmed to interface the CPU upon the occurrence of specified status conditions, and generate interrupt vectors when the CPU responds for more information on the operation of this portion of the logic, please refer to the Z84C20 PIO Product Specification and Technical Manual).
284C4x Serial I/O Logic Unit

This logic unit provides the user with two, four-wire, multi-protocol serial I/O channels that are completely compatible with the Z84C4x SIO. Their basic functions are serial-to-parallel and parallel-to-serial converters can be programmed by a CPU for a broad range of serial communications applications. Each channel, designated Channel A and Channel B, is capable of supporting all common synchronous and asynchronous protocols (Master/Slave, Biwire, and SDLC/HDLC, byte or bit oriented - Figure 8).

Z84C4x15 Only. As an enhancement to the Z84C4x15, the Z84C4x15 can handle a 32-bit CRC on Channel A and Schmitt-trigger inputs on the TXC and RXC pins of both channels.
Watch Dog Timer (WDT) Logic Unit

This logic unit has been superimposed into the IPC. It detects an operation error, caused by the program runaway, and returns to normal operation. Figure 9, shows the block diagram of the WDT. Upon Power-On (Reset), the unit is disabled. If WDT is not required, but WDTOUT connects to RESET or any other circuit, it has to be disabled. During the power-down mode of operation (either IDLE or STOP), the Watch Dog Timer is halted.

WDT Output (WDTOUT pin). When the WDT is used, the "0" level signal is output from the WDTOUT pin after a duration of time specified in the WDT0 or WDT1. The output pulse width is one of the following, depending on the WDTOUT pin connection:

- The WDTOUT is connected to the RESET pin. The "0" level is pulled for 500 microseconds (system clock cycles).
- The WDTOUT is connected to a pin other than the RESW pin. The "0" level is kept until the Watch Dog Timer is cleared by software, or reset by RESW pin.

CGC Logic Unit. The IPC has CGC (Clock Generation/Control) unit. This unit is identical to the one with the Z84015 and the 8DCG0, and supports power-down modes of operation. The output from this unit is on the pin called CGCCLK, and is not connected to the system clock internally. The CLKIN pin is the system clock input. The user can connect CGCCLK to CLKIN to utilize the CGC unit for supply external clock from CLKIN pin.

The CGC unit allows a crystal input (XTAL1, XTAL2), or external clock input on the XTAL1 pin. It has clock divide-by-two circuits and generates a half-speed clock to the input.

Z8415COS5. The power-down modes of the IPC vary depending upon whether the system clock is fed from the CGC unit (i.e. CGCCLK to CLKIN) or the external clock source on the CLKIN pin. They also have divide-by-one mode. If the clock is supplied by the CGC unit, all of the modes in "half" state are available. When external clock is provided on the CLKIN pin, XTAL1 is left open (tied to "0" or "1") to avoid metastable conditions to minimize power consumption.

Z84015COS15 Only. If the system clock is provided on the CLKIN pin, none of the power-down modes (except Run mode) is supported.

Z8415COS15 Only. If the system clock is provided on the CLKIN pin, only the IDLE mode is applicable. In this mode, if the HALT instruction is executed, internal clock to the CGC is kept on, "CONTINUE", but the clock to the other components (CPU, PO, SID, and Watch Dog Timer) are stopped. The divide-by-two circuit of the CGC unit can be stopped by programming bit D4 of the WDTMR (see "Programming section"). Upon Power-On Reset, it comes up in divide by two mode.

System Clock Generation

The IPC has a built-in oscillator circuit and the required clock can be easily generated by connecting a crystal to the external terminals (XTAL1, XTAL2). Clock output is the same frequency as half the speed of the crystal frequency. Example of oscillator connections are shown in Figure 10.

Figure 9. Block Diagram of Watch Dog Timer

Figure 10. Circuit Configuration For Crystal
Recommended characteristics of the crystal and the values for the capacitors are as follows (the values will change with crystal frequency):

- **Type of crystal**: Fundamental, parallel type crystal (AT cut is recommended)
- **Frequency tolerance**: Application dependent
- **C<sub>L</sub>**: Load capacitance: Approximately 20pf (acceptable range is 25-35pf)
- **R<sub>a</sub>**: Equivalent series resistance: ±150 ohms
- **V<sub>d</sub>**: Drive level: 10Vrms (for ≤10kHz crystal); 5Vrms (for ≥10kHz crystal)

**Power-On Reset Logic Unit (284C13C/15 Only)**

The 284C13C/15 has the enhanced feature of a Power-on Reset Circuit. During the power-up sequence, the open-drain gate of the on-chip power-on reset circuit drives the **RESET pin** to '0' for 25 to 75 nsec after the power supply passes through approx. 2.2V. After the termination of the 'Power-on Reset' cycle, the open-drain gate of the on-chip Power-on Reset circuit stops to drive the **RESET** pin. It is required to have external pull-up resistor on the **RESET** pin.

If it receives a **RESET** signal from outside the power-on sequence and while the Reset Output Enable bit in Misc Control Register is cleared to '0', it will drive the **RESET** pin for 5-cycle clock cycles from the falling edge of the external **RESET** input. Otherwise, the **RESET** pin must be kept in the high state for a period of at least 3 system clock cycles.

If there is a power-on reset cycle outside of this device, the device will power up in the state with OPEN DRAIN type outputs and pulldown resistors because **RESET** signal is driven low for the period mentioned above during the power-on sequence. If the external Power-on Reset circuit has pull-up type drivers and they drive the **RESET** pin to '0' during this period, it may cause a malfunction. In particular, when using 284C13C/15 in the 284013C/15 socket, modification may be required for the external reset circuit.

**Wait State Generator Unit (284C13C/15 Only)**

The 284C13C/15 has the enhanced feature of a Wait State Generator circuit. This is capable of generating WAIT signals to the CPU internally. The status of the External WAIT input line is sampled after the intrinsic or software wait state has been completed. This ensures that the wait state is inactivated on Internal Delay Chain Wait (for this cycle, insertion of a wait state is not simple).

The Wait State Control Register can be programmed to generate multiple wait states during different CPU cycles as follows.

- **Memory Wait and Opcode Wait**: The Wait State Generator can put 0 to 3 wait states in memory accesses. Additionally, one added wait state can be inserted during the IMI (Opcode fetch) cycle, because IMI cycle's timing requirement is lighter than memory Read/Write cycles. It generates wait states to the Memory Accesses in a specified address range, which is programmed in the Memory Wait Boundary Register.
- **I/O Wait**: The Wait State generator can put 0, 2, 4 or 6 wait states in I/O accesses. Regardless of the programming in this field, no I/O wait states are inserted for accesses to external peripherals.

**Interrupt Vector Wait**: During Interrupt acknowledge cycle, the Wait State Generator can insert one wait state after IMI goes active, to extend the time between IMI going low to vector fetch by CPU. It allows a slow vector response device.

**Interrupt Dima Chain Wait and RETI sequence extension**: During Interrupt acknowledge cycle, the Wait State Generator can insert 2, 3, 4 or 6 wait states between any cycle going to Dima fetch cycle to the external interrupt acknowledge cycle. This is to control the number of wait states inserted during a cycle going to RETI fetch cycle. If so programmed, the wait state is inserted at the point that RETI cycle is executed. This allows a longer delay cycle. Also, this field controls the number of wait states inserted during RETI, fetch cycle. If so programmed, an extra 0 or 2 wait states during Interrupt Acknowledge cycle, Wait State Generator also inserts wait states during RETI fetch cycle. The sequence is generated with 2-cycle fetch cycles (On-Cycle EHD followed by 4E0). It inserts 2 or 4 wait states, respectively, if 0-cycle followed by 4E0 is not 40h. One wait state if the following 40h is not 40h.

**Chip Select Signals (284C13C/15 Only)**

The 284C13C/15 has an enhanced feature of adding two chip select signals (CS0, CS1) pins. Both signals are original I C bus pins (IC7 on the 284013C/15). The boundary value for each Chip Select signal is 4 bits wide, and compare with A15-A12 of the address. Each Chip Select Signal goes active when:

\[
\text{CS0: (D3-D0 of CS0) > A15-A12 0 \ b}
\]

\[
\text{CS1: (D7-D4 of CS1) A15-A12 2 \ b}
\]

Where CS0 is the common chip Select Boundary Register.

**I/O address assignment**

The Z84C13C/15 has 16-bit I/O addresses. The I/O addresses are listed in Table 1. They are fully decoded from 16-bit and 8-bit addresses. The Z84C13C/15 has 16-bit I/O addresses. They are fully decoded from 16-bit and 8-bit addresses. The Z84C13C/15 has 16-bit I/O addresses. They are fully decoded from 16-bit and 8-bit addresses. The Z84C13C/15 has 16-bit I/O addresses. They are fully decoded from 16-bit and 8-bit addresses. The Z84C13C/15 has 16-bit I/O addresses. They are fully decoded from 16-bit and 8-bit addresses.
### Table 1: I/O Control Register Address

<table>
<thead>
<tr>
<th>Address</th>
<th>Device</th>
<th>Channel</th>
<th>Register</th>
</tr>
</thead>
<tbody>
<tr>
<td>D0</td>
<td>CTC</td>
<td>Ch 0</td>
<td>Control Register</td>
</tr>
<tr>
<td>D1</td>
<td>CTC</td>
<td>Ch 1</td>
<td>Control Register</td>
</tr>
<tr>
<td>D2</td>
<td>CTC</td>
<td>Ch 2</td>
<td>Control Register</td>
</tr>
<tr>
<td>D3</td>
<td>CTC</td>
<td>Ch 3</td>
<td>Control Register</td>
</tr>
<tr>
<td>D4</td>
<td>SIO</td>
<td>Ch A</td>
<td>Data Register</td>
</tr>
<tr>
<td>D5</td>
<td>SIO</td>
<td>Ch A</td>
<td>Data Register</td>
</tr>
<tr>
<td>D6</td>
<td>SIO</td>
<td>Ch B</td>
<td>Data Register</td>
</tr>
<tr>
<td>D7</td>
<td>SIO</td>
<td>Ch B</td>
<td>Data Register</td>
</tr>
<tr>
<td>D8</td>
<td>PCD</td>
<td>Port A</td>
<td>Data Register (Not with Z84x13)</td>
</tr>
<tr>
<td>D9</td>
<td>PCD</td>
<td>Port A</td>
<td>Command Register (Not with Z84x13)</td>
</tr>
<tr>
<td>D10</td>
<td>PCD</td>
<td>Port B</td>
<td>Data Register (Not with Z84x13)</td>
</tr>
<tr>
<td>D11</td>
<td>PCD</td>
<td>Port B</td>
<td>Command Register (Not with Z84x13)</td>
</tr>
<tr>
<td>D12</td>
<td>Watchdog Timer</td>
<td>Port A</td>
<td>Master Register (WDT/MR)</td>
</tr>
<tr>
<td>D13</td>
<td>Watchdog Timer</td>
<td>Port B</td>
<td>Control Register (WDTCR)</td>
</tr>
<tr>
<td>D14</td>
<td>Watchdog Timer</td>
<td>Port B</td>
<td>Control Register (WDT/MR)</td>
</tr>
<tr>
<td>D15</td>
<td>Watchdog Timer</td>
<td>Port B</td>
<td>Control Register (WDTCR)</td>
</tr>
<tr>
<td>D16</td>
<td>System Control Register Pointer (SCP)</td>
<td>(Not with Z8401/010)</td>
<td>System Control Data Port (SCDP) (Not with Z8401/010)</td>
</tr>
<tr>
<td>D17</td>
<td>Through SCP and SCDP</td>
<td>Control Register 01 - Wait State Control Register (WSCR)</td>
<td>Control Register 01 - Memory Wait state Boundary Register (MWBKR)</td>
</tr>
<tr>
<td>D18</td>
<td>Through SCP and SCDP</td>
<td>Control Register 02 - Chip Select/Boundary Register (CSBR)</td>
<td>Control Register 02 - Misc. Control Register (MCR)</td>
</tr>
</tbody>
</table>

### PIO Registers

For more detailed information, please refer to the PIO Technical Manual. These registers are not in the Z84x13.

**Interrupt Vector Word**

The PIO logic unit is designed to work with the Z80 CPU in interrupt mode. The interrupt word must be programmed if interrupts are used. Bit D0 must be a zero (Figure 11).

**Mode Control Word**

Selects the port operating mode. This word is required and is written at any time (Figure 12).

**PIO Mode Control Word**

When Mode 3 is selected, the Mode Control Word is followed by the I/O Register Control Word. This word configures the I/O register, which determines which port lines are inputs or outputs. A "1" indicates input while a "0" indicates output. This word is required when in Mode 3 (Figure 13).

**Interrupt Control Word**

In Mode 3 operation, handshake signals are not used. Interrupts are generated as a logic function of the input signal levels. The Interrupt Control Word sets the logic conditions and the logic levels required for generating an interrupt. Two logic conditions or functions are available: ANY (all input bits change to the active level, an interrupt is triggered), OR (if any one of the input bits change to the active logic level, an interrupt is triggered). The user can program which input bits are to be considered as part of this logic function. Bit D0 sets the logic function, bit D1 sets the logic level, and bit D4 specifies a mask control word to follow (Figure 14).

**Figure 12. PIO Mode Control Word**

**Figure 13. I/O Register Control Word**

Interrupt Disable Word

This word can be used to enable or disable a port's interrupts without changing the rest of the port's interrupt conditions (Figure 15).
Figure 16. Internet Disable Word

CTC CONTROL REGISTERS

For more detailed information, refer to the CTC Technical Manual.

Channel Control Word

This word sets the operating modes and parameters as described below. Bit DD is a "1" to indicate that this is a Control Word (Figure 17).

Figure 17. CTC Channel Control Word

Bit D6, Mode Bit. This bit selects either Timer Mode or Counter Mode.

Bit D5, Precursor Factor. This bit selects the precursor factor for use in the timer mode. Either divide-by-1 or divide-by-256 is available.

Bit D4, Clock/Trigger Edge Select. This bit selects the active edge of the C/I/TRG input pulses.

Bit D3, Timer Trigger. This bit selects the trigger mode for timer operation. Either automatic or external trigger may be selected.

Bit D2, Time Constant. This bit indicates that the next word programmed is time constant data for the downcounter.

Bit D1, Software Reset. Writing 1 to this bit indicates a software reset operation, which stops counting activity until another time constant word is written.

Figure 18. CTC Time Constant Word

Time Constant Word

Before a channel starts counting, it must receive a time constant word. The time constant value is anywhere between 1 and 256, with 00 being accepted as a count of 256 (Figure 18).

Figure 19. CTC Interrupt Vector Word

Interrupt Vector Word

If one or more of the CTC channels have Interrupt enabled, then the Interrupt Vector Word must be programmed. Only the lowest significant bits of this word are programmed, and bit DD must be "0." Bits D2-D1 are automatically modified by the CTC channels which it responds with an interrupt vector (Figure 19).

Write Registers. The SIO channel B contains eight write registers which channel A contains only seven that are programmed to configure the operating modes characteristics of each channel. With the exception of WR0, programming the write registers is a two step operation. The first operation is a pointer written to WR0 which points to the selected register. The second operation is the actual control word that is written into the register to configure the SIO channel (Figure 21).
Figure 21. SIO Write Registers

WATCH DOG CONTROL REGISTERS

There are two registers to control Watch Dog Timer operation. These are the Watch Dog Timer Master Register (WDTMR; IO Address F8h) and the Watch Dog Command Register (WDTCR; IO Address F9h). The Watch Dog Time Logic has a "double key" structure to prevent the WDT disabling error, which may lead to the WDT operation to stop due to program runaway. Programming the WDT follows this procedure. Also, these registers program the power-down mode of operation. The "Second key" is needed when timing off the Watch Dog Timer.

Enabling the WDT. This is enabled by setting the WDT Enable bit (bit 0 of WDTMR) to "1" and the WDT Periodic field (DS30:WDT) to the desired time period. These command bits are in the Watch Dog Timer Master Register (WDTMR; IO Address F8h).

Disabling the WDT. This is disabled by clearing WDT Enable bit in WDTMR to "0" followed by writing "11" to the WDT Command Register (WDTCR; IO Address F9h).
Clearing the WDT. The WDT can be cleared by writing "MBN" into the WDTCH.

Watch Dog Timer Master Register (WDTMR, I/O address F3H). This register controls the activity of the Watch Dog Timer and selects power-down mode of operation (Figure 22).

Bit D4-D3, HALT mode (HALTM). This two bit field specifies one of four power-down modes. To change this field, write "DBY" to the WDT command register, followed by a write to this register. For detailed descriptions of this field, please refer to the section "Mode of operations". Upon Power-on Reset, this field is set to 11, which specifies "RUN mode."

00 - IDLE 1 Mode
01 - IDLE 0 Mode
10 - STOP0 Mode
11 - RUN Mode

Bit D2-D0. Reserved. These three bits are reserved and should always be programmed as '011'. A read to these bits returns '011'.

Watch Dog Timer Command Register (WDTCR, I/O address F4H). In conjunction with the WDTMR, this register works as a "Second key" for the Watch Dog Timer. This register is write only (Figure 23).

Write 81h after clearing WDE to 0 - Disable WDT. Write 4Eh - Clear WDT. Write 4Dh followed by a write to HALTM - Change Power-down mode.

Interrupt Priority Register (NTPR, I/O address F4H)

This register (write only) is provided to determine the priority for the GTO, SIG and the PIO (Figure 24).

System Control Register Pointer (SCRP, I/O address F5H)

This register stores the pointer to access System Control Registers (WCR, MBWR, CSBR and MCR). This register is Read/Write and it holds the pointer value until modified. Upon Power-on Reset, all bits are cleared to zero. The pointer value, other than 00h to 0Ch is reserved and not written. Upon Power-on Reset, this register is set to "00h" (Figure 25).

System Control Data Port (SCDP, I/O address F6H)

This register is to access WCR, MBWR, CSBR and MCR (Figure 26).
For fifteen M1 cycles from Power-on Reset, bits 7-6 are set to "11". They clear to "00" on the trailing edge of the 16th M1 signal unless programmed.

Bit 5: Interrupt Vector Wait. When this bit is set to one, the wait state generator inserts one wait state after the ICOR signal goes active during the Interrupt acknowledge cycle. This gives more time for the vector read cycle. While this bit is cleared to zero, no wait state is inserted (standard timing). For fifteen M1 cycles from Power-on Reset, this bit is set to "1", then cleared to "0" on the trailing edge of the 16th M1 signal, unless programmed.

Bit 4: Opcode Fetch Extension. If this bit is set to "1", one additional wait state is inserted during the op-code fetch cycle in addition to the number of wait states programmed in the Memory Wait field. For fifteen M1 cycles from Power-on Reset, this bit is set to "1", then cleared to "0" on the trailing edge of the 16th M1 signal, unless programmed.

Bit 3-2: Memory Wait States. This 2-bit field specifies the number of wait states to be inserted during memory Read/Write transactions.

99 - No Wait states
01 - 1 Wait state
10 - 2 Wait states
11 - 3 Wait states

For fifteen M1 cycles from Power-on Reset, these bits are set to "11", then cleared to "00" on the trailing edge of the 16th M1 signal, unless programmed.

Bit 1-0: IO Wait States. This 2-bit field specifies the number of wait states to be inserted during IO transactions.

00 - No Wait states
01 - 1 Wait state
10 - 2 Wait states
11 - 3 Wait states

For fifteen M1 cycles from Power-on Reset, these bits are set to "11", then cleared to "00" on the trailing edge of the 16th M1 signal, unless programmed. For the accesses to the on-chip IO registers, no wait states are inserted regardless of the programming of this field.

Interrupt Acknowledge

00 - No Wait states
01 - 2 Wait states
10 - 4 Wait states
11 - 6 Wait states

Memory Wait Boundary Register (MWRB, Control Register CTH)

This register specifies the address range to insert memory wait states. When accessed, memory addresses are within this range, the Memory Wait State generator inserts Memory Wait States specified in the Memory Wait field of MWR (Figure 28).

Chip Select Boundary Register (CSBR, Control Register 03H)

This register specifies the addresses range for each chip select signal. When accessed, memory addresses are within this range, chip select signals are active (Figure 29).

MCR (Read/Write)

30

<table>
<thead>
<tr>
<th>MCR (Read/Write)</th>
<th>D/A Disable</th>
<th>D/A Enable</th>
<th>A/Z Disable</th>
<th>A/Z Enable</th>
<th>C/A Disable</th>
<th>C/A Enable</th>
<th>EOP Disable</th>
<th>EOP Enable</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output on Power-on Reset</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

EOP: End of Program

D/A: Data Access

A/Z: Address/Zoom

C/A: Chip Access

Figure 29. Chip Select Boundary Register

D7-D4, JCS1 Boundary Address. These bits specify the boundary address range for JCS1. The JCS1 is asserted if the address lines A15-12 have an address value greater than or equal to the programmed value for JCS1, and less than or equal to the programmed value in these two bits.

JCS0: JCS0 Boundary Address. These bits specify the boundary address range for JCS0. JCS0 is asserted if the address lines A15-12 have an address value less than or equal to the programmed boundary value. The JCS0 enable bit in the MCR must be set to 1. Upon Power-on reset, these bits come up as all '1's so that JCS0 is asserted for all addresses.

Chip Select signals are active for the address range:

JCS0: (D3-D0 of CSBR) ≥ A15-A12 > (D3-D0 of CSBR)
JCS1: (D7-D4 of CSBR) ≥ A15-A12 > (D3-D0 of CSBR)

This register is set to "00001111b" on Power-on Reset, which specifies the address range for JCS0 for '0000' to 'FFFFH' (all Memory location) and JCS1 'undefined.'

Mac Control Register (MCR, Control Register 03H)

This register specifies miscellaneous options on this device (Figure 30).

The register has the following fields:

- D/A Enable: 1 = Enable, 0 = Disable
- A/Z Enable: 1 = Enable, 0 = Disable
- C/A Enable: 1 = Enable, 0 = Disable
- EOP Enable: 1 = Enable, 0 = Disable
- D/A Disable: 1 = Disable, 0 = Enable
- A/Z Disable: 1 = Disable, 0 = Enable
- C/A Disable: 1 = Disable, 0 = Enable
- EOP Disable: 1 = Disable, 0 = Enable
- Output on Power-on Reset: 1 = Active, 0 = Inactive
Table 2. Power-down Modes

<table>
<thead>
<tr>
<th>Operation Mode</th>
<th>WDTMR</th>
<th>Bit D4</th>
<th>Bit D3</th>
<th>Description at HALT State</th>
</tr>
</thead>
<tbody>
<tr>
<td>RUN Mode</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>The CPU continues operation and continuously supplies a clock to the outside.</td>
</tr>
<tr>
<td>IDLE1 Mode</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>The Internal oscillator operation is continued. Clock output (CLKOUT) as well as internal clock to the CPU, PIO, SID, CTIC and the Watch Dog Timer is stopped at &quot;0&quot; level of T4 state in the halt instruction operation code fetch cycle.</td>
</tr>
<tr>
<td>IDLE2 Mode</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>The internal oscillator and the CTIC operation continues and supplies clock to the outside on the CLKOUT pin continuously. But the internal clock to the CPU, PIO, SID and the Watch Dog Timer is stopped at &quot;0&quot; level of T4 state in the halt instruction operation code fetch cycle.</td>
</tr>
<tr>
<td>STOP Mode</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>All operations of the internal oscillator, clock (CLK) output, internal clock to the CPU, PIO, CTIC, SID and the Watch Dog Timer are stopped at &quot;0&quot; level of T4 state in the halt instruction operation code fetch cycle.</td>
</tr>
</tbody>
</table>

Table 3. Device status in Halt state

<table>
<thead>
<tr>
<th>Mode</th>
<th>CTC</th>
<th>CPU</th>
<th>PIO</th>
<th>SID</th>
<th>WDT</th>
<th>CLKOUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>IDLE1</td>
<td>0</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>IDLE2</td>
<td>0</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>O</td>
</tr>
<tr>
<td>STOP</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>RUN</td>
<td>O</td>
<td>O</td>
<td>O</td>
<td>O</td>
<td>O</td>
<td>O</td>
</tr>
</tbody>
</table>

D: Operating
X: Stop

TIMING

Basic Timing
The basic timing is explained here with emphasis placed on the halt function relative to the clock generator. The following items are identical to those for the Z84C300. Refer to the data sheet for the Z84C300.

- Operation code fetch cycle
- Memory Read/Write operation
- Input/Output operation
- Bus request/acknowledge operation
- Maskable interrupt request operation
- Non-Maskable interrupt request operation
- Reset Operation

Operation When HALT Instruction is Executed
- The CPU fetches an halt instruction in the operation code fetch cycle. HALT goes active (Low) in sync with the falling edge of T4 state before the peripheral LSIs and CPU stops the operation. After this, the system clock generation differs depending upon the operation mode (RUN Mode, IDLE1 Mode or STOP Mode). If the internal system clock is running, the CPU continues to execute NOP instruction even in the halt state.

RUN Mode (HALT = 11). Shown in Figure 31 is the basic timing when the halt instruction is executed in the RUN Mode.
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