GPC® 15A
General Purpose Controller Z84C15

TECHNICAL MANUAL

Single Euro size 100x160mm with interface to ABACO® industrial BUS; 84C15 CPU with 20 MHz crystal; up to 512K EPROM or 256K FLASH EPROM and up to 128K SRAM; through FGDOS the memory that exceeds 64K is managed as RAM/ROM disk; serial EEPROM up to 8K; up to 12 way Dip Switch and configuration jumper readable by software; activity LEDs, placed on the front side, driven through software; 2 RS 232 serial lines, one configurable in RS 422, RS 485 or Current Loop, software selectable baud rate, up to 38.4 KBAud; 40 I/O TTL lines, set via software: 24 managed by PPI 82C55 and 16 managed by PIO; four 8 bits timer counters I/O connector; optional backed SRAM with optional Real Time Clock able to up date day, month, year, week day, seconds, minutes and hours; Watch Dogs resettable by software and displayed through LEDs: single power supply +5Vdc 180 mA; wide range of base software and development tools that allow card use with only a standard PC, connected through serial line. Among these: FGDOS 15A; PASCAL 80; CBZ 80; NSB8; RSD 15A; HI TECH C 80; GET 80; DDS MICROC 85; NO ICE Z80; etc.
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For specific information on the components mounted on the card, please refer to the Data Book of the builder or second sources.

SYMBOLS DESCRIPTION

In the manual could appear the following symbols:

⚠️ Attention: Generic danger
⚠️Attention: High voltage

Trade Marks

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Other Product and Company names listed, are trade marks of their respective companies.
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INTRODUCTION

The use of these devices has turned - IN EXCLUSIVE WAY - to specialized personnel.

The purpose of this handbook is to give the necessary information to the cognizant and sure use of the products. They are the result of a continual and systematic elaboration of data and technical tests saved and validated from the manufacturer, related to the inside modes of certainty and quality of the information.

The reported data are destined- IN EXCLUSIVE WAY- to specialized users, that can interact with the devices in safety conditions for the persons, for the machine and for the enviroment, impersonating an elementary diagnostic of breakdowns and of malfunction conditions by performing simple functional verify operations , in the height respect of the actual safety and health norms.

The informations for the installation, the assemblage, the dismantlement, the handling, the adjustment, the reparation and the contingent accessories, devices etc. installation are destined - and then executable - always and in exclusive way from specialized warned and educated personnel, or directly from the TECHNICAL AUTHORIZED ASSISTANCE, in the height respect of the manufacturer recommendations and the actual safety and health norms.

The devices can't be used outside a box. The user must always insert the cards in a container that respect the actual safety normative. The protection of this container is not threshold to the only atmospheric agents, but specially to mechanic, electric, magnetic, etc. ones.

To be on good terms with the products, is necessary guarantee legibility and conservation of the manual, also for future references. In case of deterioration or more easily for technical updates, consult the AUTHORIZED TECHNICAL ASSISTANCE directly.

To prevent problems during card utilization, it is a good practice to read carefully all the informations of this manual. After this reading, the user can use the general index and the alphabetical index, respectly at the begining and at the end of the manual, to find information in a faster and more easy way.

CARD VERSION

The present handbook is reported to the GPC® 15A card release 250694 and later. The validity of the bring informations is subordinate to the number of the card release. The user must always verify the correct correspondence among the two denotations. On the card the release number is present in more points both board printed diagram (serigraph) and printed circuit (for example near socket IC23 on the card edge on the component side and near connector K1 on the card edge on the solder side).
GENERAL INFORMATIONS

The GPC® 15A card is a powerful control and managing card in the 100x160mm standard single Europa size. It relies on the powerful Industrial ABACO® BUS and exploits the numerous intelligent and non intelligent peripherals, available on this BUS.

The GPC® 15A is based on the powerful and diffuse CPU 84C15 Zilog, therefore being code compatible with the famous Z80, and it has considerable hardware resources available on board. Its modularity and the remarkable hardware resources allow this card to be easily used even in complex applications. Programming and exploiting the resources of this module is extremely easy thanks to FGDOS romated operative system. This latter supports high level languages such as BASIC, PASCAL, C compilers and so on; it drives the memory resources as ROM/RAM disk allowing an immediate use of these devices at high level. In addition to that the GPC® 15A allows a direct management of LCD or Fluorescent Displays, matrix keyboard, parallel printer and PCMCIA RAM cards. The FGDOS affords truly notable develop and debug facilities, and allows to program directly on board a FLASH with the user program. The GPC® 15A is equipped with a series of standard ABACO® connectors allowing immediate use of the many BLOCK I/O interface, or enabling a simple and inexpensive connections to equipment made by the user, or by third parties.

- Single Euro size 100x160mm with interface to Industrial ABACO® BUS.
- 84C15 CPU with 20 MHz crystal.
- Up to 512K EPROM or 256K FLASH EPROM and up to 128K SRAM. Through FGDOS the memory that exceeds 64K is managed as RAM/ROM disk. It is possible deleting and re-programming the on board FLASH, automatically, with the user programm.
- Serial EEPROM up to 8K.
- 4 or 12 way Dip Switch and configuration jumper readable by software.
- Activity LEDs, placed on the front side, driven through software.
- 2 RS 232 serial lines, one configurable in RS 422, RS 485 or Current Loop, software selectable baud rate up to 38.4 KBaud
- 40 I/O TTL lines, set via software: 24 managed by PPI 82C55 and 16 managed by PIO.
- Four 8 bits timer counters on I/O connector.
- Optional backed SRAM and Real Time Clock able to up date day, month, year, week day, seconds, minutes and hours.
- Watch Dogs reersettable by software and display through LED.
- Single power supply +5Vdc, 180 mA.
- Wide range of base software and development tools that allow card use with only a standard PC, connected through serial line. Among these: FGDOS 150; PASCAL 80; CBZ 80; NSB8; RSD 150; HI TECH C 80; GET 80; DDS MICROC 85; NO ICE Z80; etc.
**SIO**

Microprocessor peripheral device that manages two lines for serial communication. It can be used to connect to external systems capable to support RS 232, RS 422, RS 485 and Current loop electric protocols. Simply by programming four registers allocated in the microprocessor I/O addressing space, the User can set the baud rate, stop bits number, length of character, parity and handshake of each serial line.

**TIMER COUNTER**

It is a microprocessor peripheral device that manages four 8 bit timers counters. Each channel can be set with a different prescaler and with a different operating mode (timer with external trigger, counter of rising edge or falling edge, etc.), including eventual interrupt generation. CTC is connected to the external electronics by eight digital signals and it is completely driven by software programming four registers allocated in microprocessor I/O addressing space, by a specific control logic.

**PIO TTL I/O LINES**

It is a microprocessor peripheral device that manages 16 TTL I/O lines divided in two 8 bit parallel ports. The lines direction is software settable at bit level and interrupts can be generated. In this way an external status can obtain CPU control in any condition, with a fast response time. The PIO is completely driven by software programming four registers allocated in microprocessor I/O addressing space, by a specific control logic.

**REAL TIME CLOCK**

The optional backed SRAM module instalalble on IC7 can also have a Real Time Clock capable of a completely autonomous management of hours, minutes, seconds, day of month, month, year and day of week. The device is completely software programmable through 8 registers mapped in the CPU I/O.

**MEMORY MANAGEMENT UNIT**

A specific MMU section has been designed to manage in a practical and efficient way the memory configurations that the GPC® 15A board can assume. The use is provided with a 64K work area, which can be easily allocated anywhere in the 640K maximum memory space.
CPU

The **GPC® 15A** uses the powerfull microprocessors 84C15 produced by ZILOG. This 8 bit microprocessor is code compatible with standard Z80 CPU and it has an extended instruction set, fast execution time, fast data handling and an efficient vectorized interrupt management.

Some of the most important 84C15 features are its internal peripheral devices, as below described:

- 16 I/O lines programmable at bit level, capable to generate interrupts (PIO);
- four 8 bit timers counters, with programmable prescaler (CTC);
- 2 synchronous or asynchronous serial lines, provided of hardware handshake signals (SIO);
- watch dog timer;
- wait state generator;
- programmable clock frequency;
- interrupt controller;
- idle mode or power down mode.

For further information, please refer to specific documentation of the manufacturing company, or to appendix B of this manual.

SERIAL COMMUNICATION

The serial communication lines are completely software configurable for protocol and speed (from 300 to 38400 Baud); simply by programming the microprocessor SIO and the on board baud rate generator, the User can set the Baud Rate, stop bits number, length of character, parity and handshake of each serial line. For further information about these programmable sections, please refer to chapter "BAUD RATE GENERATOR" and to appendix B of this manual.

One of the two serial lines is always buffered with RS 232 electric protocol, while the second one is hardware configurable in fact connecting some jumpers, the User can select the electric standard interface between RS 232, RS 422, RS 485 and Current Loop; for RS 422-485 the transmitter activation and the line direction can be set by software. The chapter "SERIAL COMMUNICATION SELECTION" contains a detailed description of available hardware configurations.

Normally the card is provided with two RS 232 interfaces and a different configuration must be specified when ordering.

ABACO® BUS

One of the most important features of **GPC® 15A** is its possibility to be interfaced to industrial **ABACO® BUS**. Thanks to its standard **ABACO® BUS** connector, the card can be connected to some of the numerous **grifo®** boards, both intelligent and not. For example the User can directly use cards for analog signals acquisition (A/D), cards for analog signals generation (D/A), cards for digital I/O signals management, cards with timers and counters, cards for temperature controls, etc. Through mother boards like **ABB 03** and **ABB 05** it is also possible to manage serie 3 and 4 boards, which are provided with **ABACO® I/O BUS**. So, **GPC® 15A** becomes the right component for each industrial automation systems, in fact **ABACO® BUS** makes the card easily expandable with the best price/performance ratio.
FIGURE 1: BLOCK DIAGRAM
CLOCK DEVICES

On GPC® 15A there are two separate circuits with crystal to generate the clock signal for the microprocessor (20 MHz) and the timing signal for baud rate generator section (4.9152 MHz). The choice of using two circuits and as many separated crystals, has the advantage to change the microprocessor working speed (when best performances are required) without additional changes in communication software or firmware. The best time performances are always obtained both for execution time and serial communication, fulfilling the User necessity.

CONTROL LOGIC

The addresses of all peripheral device's registers and of memory devices on GPC® 15A are assigned through a specific control logic that allocates all these devices in the microprocessor addressing space.
For further information please refer to chapter "ADDRESSES AND MAPS" of this manual.

MEMORY DEVICES

On the card can be mounted up to 656K of memory divided with a maximum of 512K Byte EPROM or 256K Byte FLASH EPROM, 128K Byte SRAM, an optional backed SRAM module up to 8K Byte and 8K Byte serial EEPROM. The memory configuration must be chosen considering the application to realize or the specific requirements of the User. Normally the card is provided with 128K RAM and 512 bytes of serial EEPROM, all different configurations must be specified by the User, at the moment of the order. By means of the serial EEPROM and the backed SRAM module, memory can keep datas also in absence of power supply. The addressing of memory devices is controlled by a specific on-board control logic, that provides to allocate the devices in the microprocessor adress space. For further informations about memory configuration, sockets description and jumpers connection, please refer to chapter "HARDWARE", "PERIPHERIAL DEVICES SOFTWARE DESCRIPTION" and to the paragraph "MEMORY SELECTION".

WATCH DOG SECTIONS

GPC® 15A is provided with two separated Watch Dog circuits that can reset the card at programmable time intervals, if not retriggered. Watch dog circuits are used when the User want to exit from endless loops or to reset anomalous conditions not estimated by application program. There is a monostable section, inside the microprocessor, with programmable intervention time and a monostable/astable section, outside the microprocessor, with 700 ms fixed intervention time. By software the User can perform a complete management of the devoces, using specific registers allocated in microprocessor I/O addressing space.
The external watch dog intervention time can be modified in response to a specific User request, by modifications of proper RC components; if this modification is necessary, please contact grifo®.
**PPI 82C55 TTL I/O LINES**

It manages 24 TTL I/O lines divided in three 8 bit parallel ports. The lines direction is software settable at byte level. These I/O lines allow the possibility to connect several devices (for example: User interfaces) even when the handshake is completely software driven. The PPI 82C55 is completely driven by software programming four registers allocated in microprocessor I/O addressing space, by a specific control logic.

**BUZZER**

On **GPC® 15A** there is a circuit to emit a fixed sound, based on a capacitive buzzer. This circuit can be enabled and disabled by software by the control logic and it can be used to manage alarm, sound feedback, etc.

For further informations about the above described devices, please refer to the manufacturer documentations or to appendix B of this manual.
TECHNICAL FEATURES

GENERAL FEATURES

On board resources: 24 TTL programmable Input/Output TTL (PPI 82C55)
16 Input/Output (PIO)
4 eight bits TTL Timer Counter (CTC)
1 RS 232 bidirectional line
1 RS 232, RS 422, RS 485 or Current Loop bidirectional line
1 CPU internal Watch Dog
1 external Watch Dog
1 Real Time Clock (RTC)
1 Buzzer
1 eight dips Dip Switch
1 four dips Dip Switch
Industrial ABACO® BUS

Addressable memory: IC 18: EPROM from 128K x 8 to 512K x 8
FLASH EPROM from 128K x 8 to 256K x 8
IC 13: SRAM 128K x 8
IC 34: serial EEPROM from 256 byte to 8192 byte
IC 7: backed SRAM module from 2K x 8 to 8K x 8

CPU: ZILOG 84C15

CPU quartz frequence: 20 MHz

Baud Rate generator frequence: 4.9152 MHz

Watch Dog intervent time: 700 msec calibrated through an RC network

PHYSICAL FEATURES

Size: (W x H x D): EUROPE format : 100 x 160 x 15 mm

Weight: 190 g (basic configuration)

Connectors: K1: 64 pins DIN 41612 M 90 degreeses A+C type C
CN1: 10 pins low profile 90 degreeses M
CN2: 20 pins low profile 90 degreeses M
CN3: 10 pins low profile vertical M
CN4: 16 pins low profile vertical M
CN5: 26 pins low profile vertical M
Temperature range: from 0 to 70 Centigrad degrees

Relative humidity: 20% up to 90% (without condense)

**ELECTRIC FEATURES**

Power supply: +5 Vcc

Consumption on 5 Vdc:
- 150 mA in basic configuration
- 175 mA in full configuration (all options mounted)

**RS422, 485 termination network:**
- line termination= 120Ω
INSTALLATION

In this chapter there are the information for a right installation and correct use of the card. The user can find the location and functions of each connectors, jumpers and some explanatory diagrams.

CONNECTIONS

The GPC®15A board has 8 connectors that can be linkeded to other devices or directly to the field, according to system requirements. In this paragraph there are connectors pin out, a short signals description (including the signals direction), connectors location (see figure 22) and some electrical diagrams that show the on board circuit of each connector.

CN1 - CONNECTOR FOR TIMER COUNTER I/O

CN1 is a 10 pins, male, 90°, low profile connector with 2.54 mm pitch. On CN1 connector are available the input and output signals of each channels of the on board CTC timers counters. all CN1 signals follow TTL standard.

![Figure 2: CN1 - Connector for Timer Counters I/O](image)

<table>
<thead>
<tr>
<th>Pin</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1, 2</td>
<td>CLK0, T0</td>
</tr>
<tr>
<td>3, 4</td>
<td>CLK1, T1</td>
</tr>
<tr>
<td>5, 6</td>
<td>CLK2, T2</td>
</tr>
<tr>
<td>7, 8</td>
<td>CLK3, T3</td>
</tr>
<tr>
<td>9, 10</td>
<td>GND</td>
</tr>
<tr>
<td></td>
<td>+5 Vdc</td>
</tr>
<tr>
<td></td>
<td>ZC0</td>
</tr>
<tr>
<td></td>
<td>ZC1</td>
</tr>
<tr>
<td></td>
<td>ZC2</td>
</tr>
<tr>
<td></td>
<td>ZC3</td>
</tr>
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</table>

Signals description:

- **CLKn, Tn** = I - Clock, Trigger signal of CTC channel n
- **ZCn** = O - Zero Count Timer signal of CTC channel n
- **+5 Vdc** = O - Line connected to +5 Vdc
- **GND** = - Ground signal
**FIGURE 3: CTC CONNECTION DIAGRAM**
CN2 - CONNECTOR FOR PPI 82C55 PORT A AND C

CN2 is a 20 pins, male, vertical, low profile connector with 2.54 mm pitch.
On CN4 connector are available PPI 82C55 port A and C signals that equal to 16 I/O digital lines.
Any parameter of this device (like signals direction, data management mode, etc.) is completely software definable by programming the device itself. All signals are at TTL level and follow the standard pinout I/O ABACO® pin-out.

|          | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | +5 Vdc | 19 | 20 | N.C. |
|----------|---|---|---|---|---|---|---|---|---|----|----|----|----|----|----|----|----|-----|-----|-----|-----|
| PPI PA.1 |   |   |   |   |   |   |   |   |   |    |    |    |    |    |    |    |    |     |     |     |     |
| PPI PA.3 |   |   |   |   |   |   |   |   |   |    |    |    |    |    |    |    |    |     |     |     |     |
| PPI PA.5 |   |   |   |   |   |   |   |   |   |    |    |    |    |    |    |    |    |     |     |     |     |
| PPI PA.7 |   |   |   |   |   |   |   |   |   |    |    |    |    |    |    |    |    |     |     |     |     |
| PPI PC.6 |   |   |   |   |   |   |   |   |   |    |    |    |    |    |    |    |    |     |     |     |     |
| PPI PC.4 |   |   |   |   |   |   |   |   |   |    |    |    |    |    |    |    |    |     |     |     |     |
| PPI PC.2 |   |   |   |   |   |   |   |   |   |    |    |    |    |    |    |    |    |     |     |     |     |
| PPI PC.0 |   |   |   |   |   |   |   |   |   |    |    |    |    |    |    |    |    |     |     |     |     |
| GND      |   |   |   |   |   |   |   |   |   |    |    |    |    |    |    |    |    |     |     |     |     |
| N.C.     |   |   |   |   |   |   |   |   |   |    |    |    |    |    |    |    |    |     |     |     |     |

**Figure 4: CN2 - Connector for PPI 82C55 port A and C**

Signals description:

- **PPI PA.n** = I/O - PPI 82C55 port A digital line n
- **PPI PC.n** = I/O - PPI 82C55 port C digital line n
- **+5 Vdc** = O - Line connected to +5 Vdc power supply
- **GND** = - Ground signal
- **N.C.** = - Not connected
**Figure 5: PPI 82C55 Connection Diagram**
DSW2 - SOCKET FOR PPI 82C55 PORT B

DSW2 is a 16 pins socket with 2.54 pitch. By disconnecting the octal dip switch from DSW2 the PPI 82C55 port B can be used to manage eight TTL digital input output lines. The connection of the obtained 8 I/O lines with external electronics must be performed with proper flat cable DIL connector.

<table>
<thead>
<tr>
<th>PPI PB.0</th>
<th>PPI PB.1</th>
<th>PPI PB.2</th>
<th>PPI PB.3</th>
<th>PPI PB.4</th>
<th>PPI PB.5</th>
<th>PPI PB.6</th>
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</tr>
</tbody>
</table>

**Figure 6: DSW2 - Socket for PPI 82C55 Port B**

Signals description:

- **PPI PB.n** = I/O - PPI 82C55 port B digital line n
- **GND** = - Ground signal
CN3 - CONNECTOR FOR RS 422, RS 485 AND CURRENT LOOP

CN3 is a 10 pins, vertical, male connector with 2.54mm pitch. This connector carries all the signals of RS 422, RS 485 and Current Loop serial line B. Signals location on this connector has been designed to reduce problems due to interference; all the signals follow the CCITT normatives for each of the communication standards used. Please remark that the Current Loop serial line is passive.

Signals description:

RXB- RS422 = I - RS 422 serial line B Receive Data Negative signal
RXB+RS422 = I - RS 422 serial line B Receive Data Positive signal
TXB- RS422 = O - RS 422 serial line B Transmit Data Negative signal
TXB+ RS422 = O - RS 422 serial line B Transmit Data Positive signal
RXTXB- RS485 = I/O - RS 485 serial line B Receive Transmit Data Negative signal
RXTXB+ RS485 = I/O - RS 485 serial line B Transmit Data Positive signal
RXB- C.L. = I - Current Loop serial line B Receive Data Negative signal
RXB+ C.L. = I - Current Loop serial line B Receive Data Positive signal
TXB- C.L. = O - Current Loop serial line B Transmit Data Negative signal
TXB+ C.L. = O - Current Loop serial line B Transmit Data Positive signal
+5 Vdc = I - Power supply signal+5 Vcc
GND = - Ground signal
CN4 - RS 232 SERIAL LINES AND TIMER COUNTER CONNECTOR

CN4 is a 16 pins, male, 90°, low profile connector with 2.54 mm pitch.
Through CN7 it is possible to connect the RS 232 serial lines and the timer counters T0, T1 and T2 to the external world. SIO and CTC are CPU internal devices. To manage the serial lines the User needs to connect specific jumpers in the proper positions and program specific CPU internal registers.
The signals on this connector are at TTL level and RS 232 signals follow the CCITT specifications; signals location on this connector has been designed to reduce problems due to interference.

![Figure 8: CN4 - RS 232 serial lines and Timer Counter connector](image)

**Signals description:**

- **RXA, B RS232** = I - RS 232 serial line A, B Receive Data signal
- **TXA, B RS232** = O - RS 232 serial line A, B Transmit Data signal
- **CTS A, B RS232** = I - RS 232 serial line A, B Clear To Send signal
- **RTS A, B RS232** = O - RS 232 serial line A, B Request To Send signal
- **CLK, Tn** = I - TTL level CTC n-th counter Clock Trigger
- **ZCn** = O - TTL level CTC n-th counter Clock Trigger Zero Count
Figure 9: RS 422, RS 485 and Current Loop Connection Diagram
**Figure 10: RS 232 Point-to-Point Connection Example**

<table>
<thead>
<tr>
<th>CN4 GPC®15A</th>
<th>External Systems</th>
</tr>
</thead>
<tbody>
<tr>
<td>9 RXA RS232, TX</td>
<td></td>
</tr>
<tr>
<td>10 TXA RS232, RX</td>
<td></td>
</tr>
<tr>
<td>7 CTSA RS232, RTS</td>
<td></td>
</tr>
<tr>
<td>8 RTSA RS232, CTS</td>
<td></td>
</tr>
<tr>
<td>2 GND</td>
<td>GND</td>
</tr>
</tbody>
</table>

**Figure 11: RS 422 Point-to-Point Connection Example**

<table>
<thead>
<tr>
<th>CN3 GPC®15A</th>
<th>External System</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 RXB- RS422 TX -</td>
<td></td>
</tr>
<tr>
<td>2 RXB+ RS422 TX +</td>
<td></td>
</tr>
<tr>
<td>3 TXB- RS422 RX -</td>
<td></td>
</tr>
<tr>
<td>4 TXB+ RS422 RX +</td>
<td></td>
</tr>
<tr>
<td>9 GND</td>
<td>GND</td>
</tr>
</tbody>
</table>

**Figure 12: RS 485 Point-to-Point Connection Example**

<table>
<thead>
<tr>
<th>CN3 GPC®15A</th>
<th>External System</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 RXTXB- RS485 TX / RX -</td>
<td></td>
</tr>
<tr>
<td>2 RXTXB+ RS485 TX / RX +</td>
<td></td>
</tr>
<tr>
<td>9 GND</td>
<td>GND</td>
</tr>
</tbody>
</table>
Please remark that in a RS 485 network two forcing resistors (3.3 kΩ) must be connected across the net and two termination resistors (120 Ω) must be placed at its extremas, respectevely near the Master unit and the Slave unit at the greatest distance from the Master.

Forcing and terminating circuitry is installed on GPC® 15A board. It can be enabled or disabled through specific jumers, as explained later.

For further informations please refr to TEXAS INSTRUMENTS Data-Book , "RS 422 and RS 485 Interface Circuits", the introduction about RS 422-485.
FIGURE 14: 4 WIRES CURRENT LOOP POINT-TO-POINT CONNECTION EXAMPLE

FIGURE 15: 2 WIRES CURRENT LOOP POINT-TO-POINT CONNECTION EXAMPLE
Possible Current Loop connections are two: 2 wires and 4 wires. These connections are shown in figures 14 and 15 where it is possible to see the voltage for $V_{CL}$ and the resistances for current limitation ($R$). The supply voltage varies in compliance with the number of connected devices and voltage drop on the connection cable.

The choice of the values for these components must be done considering that:
- circulation of a 20 mA current must be guaranteed;
- potential drop on each transmitter is about 2,35 V with a 20 mA current;
- potential drop on each receiver is about 2,52 V with a 20 mA current;
- in case of short circuit each transmitter must dissipate at most 125 mW;
- in case of short circuit each receiver must dissipate at most 90 mW.

For further info please refer to HEWLETT-PACKARD Data Book, (HCPL 4100 and 4200 devices).
CN5 - CONNECTOR FOR MICROPROCESSOR PIO

CN5 is a 26 pins, male, vertical, low profile connector with 2.54 pitch. On CN5 are available the two 8 bits parallel ports and handshake lines, equal to 16 + 4 I/O digital lines; all these signals follow TTL standard.

**Figure 17: CN5 - Connector for Microprocessor PIO**

Signals description:

- **PIO PA.n** = I/O - Digital line n of PIO port A
- **PIO PB.n** = I/O - Digital line n of PIO port B
- **RDY A, B** = O - Ready signal of port A, B
- **/STB A, B** = I - Strobe signal of port A, B
- **+5 Vdc** = O - Lines connected to +5Vdc power supply
- **GND** = Ground signal
- **N.C.** = Not connected
FIGURE 18: PIO CONNECTION DIAGRAM
**K1 - CONNECTOR FOR ABACO® BUS**

K1 is a 64 pins, male, 90°, DIN 41612 connector with 2.54 pitch. On K1 are available all the industrial ABACO® BUS signals and it can be used for connections to many other peripheral cards. In the table below there are the standard pin outs both for 8 bits and 16 bits CPU and the signal connected on **GPC® 15A**. All signals follow TTL standard.

<table>
<thead>
<tr>
<th>A 16 bit BUS</th>
<th>A 8 bit BUS</th>
<th>A GPC 15A</th>
<th>PIN</th>
<th>C GPC 15A</th>
<th>C 8 bit BUS</th>
<th>C 16 bit BUS</th>
</tr>
</thead>
<tbody>
<tr>
<td>GND</td>
<td>GND</td>
<td>GND</td>
<td>1</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
</tr>
<tr>
<td>+5 Vdc</td>
<td>+5 Vdc</td>
<td>+5 Vdc</td>
<td>2</td>
<td>+5 Vdc</td>
<td>+5 Vdc</td>
<td>+5 Vdc</td>
</tr>
<tr>
<td>D0</td>
<td>D0</td>
<td>D0</td>
<td>3</td>
<td>N.C.</td>
<td>D8</td>
<td></td>
</tr>
<tr>
<td>D1</td>
<td>D1</td>
<td>D1</td>
<td>4</td>
<td>N.C.</td>
<td>D9</td>
<td></td>
</tr>
<tr>
<td>D2</td>
<td>D2</td>
<td>D2</td>
<td>5</td>
<td>N.C.</td>
<td>D10</td>
<td></td>
</tr>
<tr>
<td>D3</td>
<td>D3</td>
<td>D3</td>
<td>6</td>
<td>/INT</td>
<td>/INT</td>
<td>/INT</td>
</tr>
<tr>
<td>D4</td>
<td>D4</td>
<td>D4</td>
<td>7</td>
<td>/NMI</td>
<td>/NMI</td>
<td>/NMI</td>
</tr>
<tr>
<td>D5</td>
<td>D5</td>
<td>D5</td>
<td>8</td>
<td>N.C.</td>
<td>D11</td>
<td></td>
</tr>
<tr>
<td>D6</td>
<td>D6</td>
<td>D6</td>
<td>9</td>
<td>N.C.</td>
<td>/MREQ</td>
<td>/MREQ</td>
</tr>
<tr>
<td>D7</td>
<td>D7</td>
<td>D7</td>
<td>10</td>
<td>/IORQ</td>
<td>/IORQ</td>
<td>/IORQ</td>
</tr>
<tr>
<td>A0</td>
<td>A0</td>
<td>A0</td>
<td>11</td>
<td>/RD</td>
<td>/RD</td>
<td>/RDLDS</td>
</tr>
<tr>
<td>A1</td>
<td>A1</td>
<td>A1</td>
<td>12</td>
<td>/WR</td>
<td>/WR</td>
<td>/WRLDS</td>
</tr>
<tr>
<td>A2</td>
<td>A2</td>
<td>A2</td>
<td>13</td>
<td>N.C.</td>
<td>/BUSAK</td>
<td>D12</td>
</tr>
<tr>
<td>A3</td>
<td>A3</td>
<td>A3</td>
<td>14</td>
<td>/WAIT</td>
<td>/WAIT</td>
<td>/WAIT</td>
</tr>
<tr>
<td>A4</td>
<td>A4</td>
<td>A4</td>
<td>15</td>
<td>N.C.</td>
<td>/BUSRQ</td>
<td>D13</td>
</tr>
<tr>
<td>A5</td>
<td>A5</td>
<td>A5</td>
<td>16</td>
<td>/RESET</td>
<td>/RESET</td>
<td>/RESET</td>
</tr>
<tr>
<td>A6</td>
<td>A6</td>
<td>A6</td>
<td>17</td>
<td>N.C.</td>
<td>/M1</td>
<td>/IACK</td>
</tr>
<tr>
<td>A7</td>
<td>A7</td>
<td>A7</td>
<td>18</td>
<td>N.C.</td>
<td>/RFSH</td>
<td>D14</td>
</tr>
<tr>
<td>A8</td>
<td>A8</td>
<td>N.C.</td>
<td>19</td>
<td>N.C.</td>
<td>/MEMDIS</td>
<td>/MEMDIS</td>
</tr>
<tr>
<td>A9</td>
<td>A9</td>
<td>N.C.</td>
<td>20</td>
<td>N.C.</td>
<td>VDUSEL</td>
<td>A22</td>
</tr>
<tr>
<td>A10</td>
<td>A10</td>
<td>N.C.</td>
<td>21</td>
<td>N.C.</td>
<td>/IEI</td>
<td>D15</td>
</tr>
<tr>
<td>A11</td>
<td>A11</td>
<td>N.C.</td>
<td>22</td>
<td>N.C.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>A12</td>
<td>A12</td>
<td>N.C.</td>
<td>23</td>
<td>N.C.</td>
<td>CLK</td>
<td>CLK</td>
</tr>
<tr>
<td>A13</td>
<td>A13</td>
<td>N.C.</td>
<td>24</td>
<td>N.C.</td>
<td>/RUDS</td>
<td></td>
</tr>
<tr>
<td>A14</td>
<td>A14</td>
<td>N.C.</td>
<td>25</td>
<td>N.C.</td>
<td>/WRUDS</td>
<td></td>
</tr>
<tr>
<td>A15</td>
<td>A15</td>
<td>N.C.</td>
<td>26</td>
<td>N.C.</td>
<td>A21</td>
<td></td>
</tr>
<tr>
<td>A16</td>
<td>N.C.</td>
<td></td>
<td>27</td>
<td>N.C.</td>
<td>A20</td>
<td></td>
</tr>
<tr>
<td>A17</td>
<td>N.C.</td>
<td></td>
<td>28</td>
<td>N.C.</td>
<td>A19</td>
<td></td>
</tr>
<tr>
<td>+12 Vdc</td>
<td>+12 Vdc</td>
<td>N.C.</td>
<td>30</td>
<td>N.C.</td>
<td>-12 Vdc</td>
<td>-12 Vdc</td>
</tr>
<tr>
<td>+5 Vdc</td>
<td>+5 Vdc</td>
<td>+5 Vdc</td>
<td>31</td>
<td>+5 Vdc</td>
<td>+5 Vdc</td>
<td>+5 Vdc</td>
</tr>
<tr>
<td>GND</td>
<td>GND</td>
<td>GND</td>
<td>32</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
</tr>
</tbody>
</table>

**Figure 19: K1 - ABACO® BUS connector**
Signals description:

8 bits CPU

A0-A15 = O - Address BUS
D0-D7 = I/O - Data BUS
INT = I - Interrupt request
NMI = I - Non Maskable Interrupt
HALT = O - Halt state
MREQ = O - Memory Request
IORQ = O - Input Output Request
RD = O - Read cycle status
WR = O - Write cycle status
BUSAK = O - BUS Acknowledge
WAIT = I - Wait
BUSRQ = I - BUS Request
RESET = O - Reset
M1 = O - Machine cycle one
RFSH = O - Refresh for dynamic RAM
MEMDIS = I - Memory Display
VDUSEL = O - VDU Selection
IEI = I - Interrupt Enable Input
CLK = O - System clock
R.B. = I - Reset button
+5 Vdc = I - Power supply at +5 Vdc
+12 Vdc = I - Power supply at +12 Vdc
-12 Vdc = I - Power supply at -12 Vdc
GND = - Ground signal

16 bits CPU

A16-A22 = O - Address BUS
D8-D15 = I/O - Data BUS
RD UDS = O - Read Upper Data Strobe
WR UDS = O - Write Upper Data Strobe
IACK = O - Interrupt Acknowledge
RD LDS = O - Read Lower Data Strobe
WR LDS = O - Write Lower Data Strobe

N.B.
Directionality indications as above stated are referred to a master (CPU o GPC®) board and have been kept untouched to avoid ambiguity in case of multi-boards systems.
I/O CONNECTION

To prevent possible connecting problems between GPC® 15A and the external systems, the user has to read carefully the information of the previous paragraphs and he must follow these instructions:

- For RS 232, RS 422, Current Loop or RS 485 communication signals the User must follow the standard rules of these protocols.

- For all TTL signals the user must follow the rules of this electric standard. The connected digital signal must be always referred to card digital ground (GND). For TTL signals, the 0 Vdc level corresponds to logic state "0", while 5Vdc level corresponds to logic state "1".

VISUAL FEEDBACK

GPC® 15A board is provided with seven LEDs to signal status conditions, as described in the following table:

<table>
<thead>
<tr>
<th>LED</th>
<th>COLOUR</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>LD1</td>
<td>Yellow</td>
<td>It is activated when J6 is in position 2-3, corresponding to high level on SYNCB signal, and it denotes DEBUG mode.</td>
</tr>
<tr>
<td>LD2</td>
<td>Green</td>
<td>It is activated when J6 is in position 1-2, corresponding to low level on SYNCB signal, and it denotes RUN mode.</td>
</tr>
<tr>
<td>LD3</td>
<td>Red</td>
<td>It is activated when the microprocessor is in HALT status.</td>
</tr>
<tr>
<td>LD4, LD5</td>
<td>Green</td>
<td>Activity LEDs driven by software.</td>
</tr>
<tr>
<td>LD7</td>
<td>Red</td>
<td>It signals activation of external Watch Dog circuitry.</td>
</tr>
<tr>
<td>LD8</td>
<td>Red</td>
<td>It signals activation of on board reset circuitry.</td>
</tr>
</tbody>
</table>

**FIGURE 20: VISUAL FEEDBACK TABLE**

The main purpose of these LEDs is to give a visual indication of the board status, making easier the operations of system working verify. To easily locate these LEDs on the board, please refer to figure 22.
DIGITAL I/O INTERFACES

Through CN2 and CN5 (I/O Abaco® standard connector) the GPC® 15A card can be connected to all of the numerous grifo® boards featuring the same standard pin out. Installation of these interface is very easy; in fact only a 20 pins flat cable (code FLT.20+20) or a 26 pins GPC®-side and 20 pins interface-side flat cable (code FLT.26+20) is required, while the software management of these interfaces is as easy; in fact most of the software packages available for GPC® 15A card are provided with the necessary procedures. Remarkable modules are:

- **QTP 16P, QTP 24P, KDL x24, KDF 224, DEB 01**, etc. that solve all the local operator interfacing problems. These modules are provided with all the resources needed to obtain a high-level human-machine interface (they feature alphanumeric displays, matrix keyboard and visualization LEDs) at a short distance from GPC® 150 card. The available software drivers allow to manage the operator interface resources directly through the high-level instructions for console management.

- **IAC 01, DEB 01**: it is an interface for CENTRONICS parallel printer that can be connected with a standard printer cable. The printer is managed by software through the high-level instructions of the selected programming language (LPRINT for BASIC, PRINTF for C, etc.).

- **MCI 64**: it a large mass memory support that can directly manage the PCMCIA memory cards (RAM, FLASH, ROM, etc.) in their available sizes. About software the developed drivers provide a complete file system interfacing allowing to access the informations stored in the memory card directly through the high-level file management instructions.

- **RBO xx, TBO xx, XBI xx, OBI xx**: these are buffer interfaces for I/O TTL signals. With these modules the TTL input signals are converted in NPN or PNP optoisolated inputs and the TTL output signals are converted in relays or transistor optoisolated outputs.

For more informations refer to "EXTERNAL CARDS" chapter and the software tools documentation.

ON BOARD INPUT

GPC® 15A card is provided of twelve dip switches (four on DSW1 and eight on DSW2), that can be read by software, normally used for system configuration (operating mode selection, card number programmation inside a network system, firmware configuration, etc.). Reading the Dip Switch registers by software, the User obtain a negated combination, in fact "ON" position corresponds to 0 logic state and "OFF" position corresponds to 1 logic state. Only four of the twelve dip switches are always available on the card, in fact DSW2, connected to PPI 82C55 port B, is mounted on socket and it can be replaced by a proper flat cable DIL connector. The DSW1 and PDB registers are allocated in the microprocessor addressing space by the control logic as described in the paragraph "I/O ADDRESSES". To recognize dip switches location on GPC® 15A, please refer to figure 22.
JUMPERS

On GPC® 15A there are eleven jumpers for card configuration. Connecting these jumpers, the user can define for example the memory type and size, the peripheral devices functionality and so on. Below there is the jumpers list, location and function:

<table>
<thead>
<tr>
<th>JUMPERS</th>
<th>PIN N°</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>J1</td>
<td>2</td>
<td>Connect s /RESET signal to ABACO® BUS</td>
</tr>
<tr>
<td>J2</td>
<td>3</td>
<td>Selects IC 7 size between 2 or 8 KByte</td>
</tr>
<tr>
<td>J3</td>
<td>3</td>
<td>Configures IC 18 for EPROM or FLASH EPROM</td>
</tr>
<tr>
<td>J4</td>
<td>3</td>
<td>Selects external Watch Dog circuitry operating mode</td>
</tr>
<tr>
<td>J5</td>
<td>4</td>
<td>Configures serial line B hardware interface between RS 232, RS 422, RS 485 and Current Loop</td>
</tr>
<tr>
<td>J6</td>
<td>3</td>
<td>Defines handshake SYNCB signal status, to select RUN or DEBUG mode</td>
</tr>
<tr>
<td>J7, J11</td>
<td>2</td>
<td>Connect termination resistors to RS 422-485 receveing line</td>
</tr>
<tr>
<td>J8</td>
<td>3</td>
<td>Selects receiveing driver for RS 422-485 serial line</td>
</tr>
<tr>
<td>J9</td>
<td>4</td>
<td>Selects connection of /RESET circuitry</td>
</tr>
<tr>
<td>J10</td>
<td>5</td>
<td>Selects direction and operating modes for serial line B in RS 422-485</td>
</tr>
</tbody>
</table>

**FIGURE 21: JUMPERS SUMMARIZING TABLE**

The following tables describe all the right connections of GPC® 15A jumpers with their relative functions. To recognize these valid connections, please refer to the board printed diagram (serigraph) or to figure 30 of this manual, where the pins numeration is listed; for recognizing jumpers location, please refer to figure 25.

The "*" used in the following tables, denotes the default connection, or on the other hand the connection set up at the end of testing phase, that is the configuration the User receives.
Figure 22: Jumpers Location

- BZ1
- DSW1
- K1
- IC13 SRAM
- IC18 EPROM
- LD1 ÷ 3
- CN3
- LD4 ÷ 8
- CN4
- CN1
- CN2
- CN5

**GPC® 15A Rel. 5.20**
2 PINS JUMPERS

<table>
<thead>
<tr>
<th>JUMPERS</th>
<th>CONNECTION</th>
<th>FUNCTION</th>
<th>DEF.</th>
</tr>
</thead>
<tbody>
<tr>
<td>J1</td>
<td>not connected</td>
<td>The card /RESET signal is not connected to <strong>ABACO® BUS.</strong></td>
<td></td>
</tr>
<tr>
<td></td>
<td>connected</td>
<td>The card /RESET signal is connected to <strong>ABACO® BUS.</strong></td>
<td></td>
</tr>
<tr>
<td>J7, J11</td>
<td>not connected</td>
<td>The termination resistor is not connected to RS 422-485 receiving line.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>connected</td>
<td>The termination resistor is connected to RS 422-485 receiving line.</td>
<td></td>
</tr>
</tbody>
</table>

**Figure 23: 2 PINS JUMPERS table**

3 PINS JUMPERS

<table>
<thead>
<tr>
<th>JUMPERS</th>
<th>CONNECTION</th>
<th>FUNCTION</th>
<th>DEF.</th>
</tr>
</thead>
<tbody>
<tr>
<td>J2</td>
<td>position 1-2</td>
<td>Configures IC 7 for 2 KByte backed SRAM.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>position 2-3</td>
<td>Configures IC 7 for 8 KByte backed SRAM.</td>
<td></td>
</tr>
<tr>
<td>J3</td>
<td>position 1-2</td>
<td>Configures IC 18 for FLASH EPROM.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>position 2-3</td>
<td>Configures IC 18 for EPROM.</td>
<td></td>
</tr>
<tr>
<td>J4</td>
<td>position 1-2</td>
<td>Selects astable mode for external Watch Dog circuit.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>position 2-3</td>
<td>Selects monostable mode for external Watch Dog circuit.</td>
<td></td>
</tr>
<tr>
<td>J6</td>
<td>position 1-2</td>
<td>Connects SIO SYNCB signal to GND; LD2 is activated and RUN mode is selected.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>position 2-3</td>
<td>Connects SIO SYNCB signal to +5 Vdc; LD1 is activated and DEBUG mode is selected.</td>
<td></td>
</tr>
<tr>
<td>J8</td>
<td>position 1-2</td>
<td>Selects IC 27 driver for RS 422-485 receiving.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>position 2-3</td>
<td>Selects IC 28 driver for RS 422-485 receiving.</td>
<td></td>
</tr>
</tbody>
</table>

**Figure 24: 3 PINS JUMPERS table**
**FIGURE 25: JUMPERS LOCATION**
### 4 PINS JUMPER

<table>
<thead>
<tr>
<th>JUMPERS</th>
<th>CONNECTION</th>
<th>FUNCTION</th>
<th>DEF.</th>
</tr>
</thead>
<tbody>
<tr>
<td>J5</td>
<td>position 1-2</td>
<td>Configures serial line B for RS 232 communication.</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>position 2-3</td>
<td>Configures serial line B for Current Loop communication.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>position 2-4</td>
<td>Configures serial line B for RS 422, RS 485 communication.</td>
<td></td>
</tr>
<tr>
<td>J9</td>
<td>position 1-2</td>
<td>Connects the on board reset circuitry to /R.B. signal of ABACO® BUS. Card is reset only by external devices (i.e. reset button of mother board).</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>position 2-3</td>
<td>Connects the on board reset circuitry to external Watch Dog circuit.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>position 2-4</td>
<td>Connects the on board reset circuitry to internal Watch Dog circuit</td>
<td></td>
</tr>
</tbody>
</table>

**Figure 26: 4 pins jumper table**

### 5 PINS JUMPER

<table>
<thead>
<tr>
<th>JUMPERS</th>
<th>CONNECTION</th>
<th>FUNCTION</th>
<th>DEF.</th>
</tr>
</thead>
<tbody>
<tr>
<td>J10</td>
<td>position 1-2 &amp; 3-4</td>
<td>Select RS 485 serial communication (2 wires).</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>position 2-3 &amp; 4-5</td>
<td>Select RS 422 serial communication (4 wires).</td>
<td></td>
</tr>
</tbody>
</table>

**Figure 27: 5 pins jumper table**

The "*" used in the following tables, denotes the default connection, or on the other hand the connection set up at the end of testing phase, that is the configuration the User receives.
RESET AND WATCH DOG

On **GPC® 15A** there are two separated Watch Dog circuits that are really efficient and easy to use. The most important features of the external Watch Dog circuitry are:

- astable mode;
- intervention time fixed at 700 ms (modifiable by hardware);
- enable function by hardware;
- retrigger by software;

Jumper J4 selects the operating mode of external watch dog circuit between monostable (when intervention time is elapsed the circuit become active and it stays active as far as a reset or power on happens) and astable (when intervention time is elapsed the circuit become active, it stays active till the end of reset time and after it is again deactivated).

In astable mode when intervention time is elapsed the circuit becomes active, it stays active till the end of reset time (7 msec) and after it is again deactivated. The external Watch Dog intervent is signaled by the lighting of LED LD8.

The most important features of the CPU internal Watch Dog circuitry are:

- monostable mode;
- intervention time programmable by software;
- enable function by software and hardware;
- retrigger by software;

Jumper J9 selects the reset source and at the same time it defines the Watch Dog circuits connection; its available connections don't allow contemporaneously connection of both Watch Dog circuits.

In monostable mode when intervention time is elapsed the circuit becomes active and it stays active as far as a reset or power on happens.

In response to a /RESET signal activation and successive deactivation the board restarts the execution of the program stored at address 0000H on IC13 (EPROM or FLASH EPROM).

Please remark that /RESET signal generated by **GPC® 15A** the board is connected also to pin 16C of K1 connector. Other reset sources, in addition to the Watch Dog circuits, are: CPU internal peripherals and reset contact (R.T., pin 29C of connector K1).

About retrigger operation of internal and external Watch Dog circuits, please refer to paragraph "WATCH DOG" in chapter "PERIPHERAL DEVICES SOFTWARE DESCRIPTION" and to appendix B of this manual.
SERIAL COMMUNICATION SELECTION

Serial line A can be buffered only as RS 232 while serial line B can be buffered in RS 232, RS 422, RS 485 or Current Loop. By hardware can be selected which one of these electric standards is used, through jumpers connection (as described in the previous tables) and drivers installation. By software the serial line can be programmed to operate with all the standard physical protocols, in fact the bits per character, parity, stop bits and baud rates can be decided by setting opportunies CPU internal registers. In the following paragraphs there are all the informations on serial communication configurations.

Some devices needed for RS 422, RS 485 and Current Loop configurations are not mounted on the board in standard configuration; this is why each fist non-standard (non-RS 232) serial configuration for line B must be always performed by grifo® technicians. This far the User can change in autonomy the configuration following the informations below:

- SERIAL LINE B IN RS 232 (default configuration)

<table>
<thead>
<tr>
<th>IC24</th>
<th>IC25</th>
<th>IC27</th>
<th>IC28</th>
<th>IC31</th>
</tr>
</thead>
<tbody>
<tr>
<td>don't care</td>
<td>don't care</td>
<td>don't care</td>
<td>don't care</td>
<td>driver MAX 202</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>J5</th>
<th>J8</th>
<th>J10</th>
<th>J7, J11</th>
</tr>
</thead>
<tbody>
<tr>
<td>position 1-2</td>
<td>don't care</td>
<td>don't care</td>
<td>don't care</td>
</tr>
</tbody>
</table>

- SERIAL LINE B IN CURRENT LOOP (option .CLOOP)

<table>
<thead>
<tr>
<th>IC24</th>
<th>IC25</th>
<th>IC27</th>
<th>IC28</th>
<th>IC31</th>
</tr>
</thead>
<tbody>
<tr>
<td>HCPL 4200</td>
<td>HCPL 4100</td>
<td>no device</td>
<td>no device</td>
<td>no device</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>J5</th>
<th>J8</th>
<th>J10</th>
<th>J7, J11</th>
</tr>
</thead>
<tbody>
<tr>
<td>position 2-3</td>
<td>don't care</td>
<td>don't care</td>
<td>don't care</td>
</tr>
</tbody>
</table>

Please remark that Current Loop serial interface is passive, so it must be connected an active Current Loop serial line, that is a line provided with its own power supply. Current Loop interface can be employed to make both point-to-point and multi-point connections through a 2-wires or a 4-wires connection.

- SERIAL LINE B IN RS 422 (option .RS 422)

<table>
<thead>
<tr>
<th>IC24</th>
<th>IC25</th>
<th>IC27</th>
<th>IC28</th>
<th>IC31</th>
</tr>
</thead>
<tbody>
<tr>
<td>HCPL 4200</td>
<td>HCPL 4100</td>
<td>SN 75176 or MAX 483</td>
<td>SN 75176 or MAX 483</td>
<td>no device</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>J5</th>
<th>J8</th>
<th>J10</th>
<th>J7, J11</th>
</tr>
</thead>
<tbody>
<tr>
<td>position 2-4</td>
<td>position 1-2</td>
<td>position 2-3 and 4-5</td>
<td>(*1)</td>
</tr>
</tbody>
</table>

Status of signal /RTSB, which is software managed, allows to enable or disable the transmitter as follows:

- /RTSB = low level = logic state 0 -> transmitter enabled
- /RTSB = high level = logic state 1 -> transmitter disabled

In point-to-point connections, signal /RTSB can be always kept low (transmitter always enabled), while in multi-point connections transmitter must be enabled only when a transmission is requested.
FIGURE 28: SERIAL COMMUNICATION DRIVERS LOCATION
- SERIAL LINE B IN RS 485 (option .RS 485)

<table>
<thead>
<tr>
<th>Configuration</th>
<th>IC</th>
</tr>
</thead>
<tbody>
<tr>
<td>J5 = position 2-4</td>
<td>IC24 = no device</td>
</tr>
<tr>
<td>J8 = position 1-2</td>
<td>IC25 = no device</td>
</tr>
<tr>
<td>J10 = position 2-3 and 4-5</td>
<td>IC27 = SN 75176 or MAX 483</td>
</tr>
<tr>
<td>J7, J11 = (*1)</td>
<td>IC28 = no device</td>
</tr>
<tr>
<td></td>
<td>IC31 = no device</td>
</tr>
</tbody>
</table>

In this modality the signals to use are pins 1 and 2 of connector CN3, that become transmission or reception lines according to the status of signal /RTSB, managed by software, as follows:

/RTSB = low level = logic state 0 -> transmitter enabled
/RTSB = high level = logic state 1 -> transmitter disabled

This kind of serial communication can be used for multi-point connections, in addition it is possible to listen to own transmission, so the User is allowed to verify the success of transmission. In fact, any conflict on the line can be recognized by testing the received character after each transmission.

(*1) If using the RS 422 or RS 485 serial line, it is possible to connect the terminating circuit on the line by using J7 and J11. This circuit must be always connected in case of point-to-point connections, while in case of multi-point connections it must be connected only in the farthest boards, that is on the edges of the communication line.

When a reset or a power on occurs, signal /RTSB is kept to a logic level high, so in one of these two cases driver RS 485 is receiving or RS 422 driver is disabled, avoiding eventual conflicts in communication.

For further informations about serial communication please refer to the examples of figures 10÷16 and to appendix B of this manual.

CONFIGURATION INPUTS

GPC® 15A is provided with a 4 pins Dip Switch (DSW1), an 8 pins Dip Switch (DSW2) and jumper (J6), the jumper selects the RUN/DEBUG modality, typically used for system configuration and software readable. Most common applications for these devices are working conditions settings or firmware parameters input, etc.

Please remark that Dip Switch DSW2 is installed on a socket and is connected to digital signals of PPI 82C55 port B. These signals are available to the User simply removing the Dip Switch and connecting to socket DSW2 through a proper flat cable DIL connector.

Configuration inputs read modalities can be found in the chapter "PERIPHERAL DEVICES SOFTWARE DESCRIPTION", while to easily locate them on the board please refer to figures 22.
INTERRUPTS

A remarkable feature of **GPC® 15A** card is the powerful interrupt management. Here follows a short description of which devices can generate interrupts and their modalities; for further informations about interrupts management please refer to the microprocessor data sheet or to the appendix B of this manual.

- **ABACO® BUS**
  - Generates a CPU /NMI through K1 connector /NMI signal.
  - Generates normal /INT, without regard for the daisy chain priority, through K1 connector /INT signal.

- **CPU peripherals**
  - CPU internal sections CTC, SIO, PIO generate normal or vectored /INT, respecting the daisy chain priority.

The daisy chain on the **GPC® 15A** board is made only of SIO, PIO and CTC and can be software programmed through one of the microprocessor internam registers. This way the User can always respond promptly and efficienly to any external event, also deciding the priority to assign to the several event sources.

For further informations please refer to appendix B of this manual.

MEMORY SELECTION

On **GPC® 15A** can be mounted up to 656K bytes of memory divided in several configurations, as described in the following table:

<table>
<thead>
<tr>
<th>IC</th>
<th>DEVICE</th>
<th>SIZE</th>
<th>JUMPERS CONFIGURATIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>18</td>
<td>EPROM</td>
<td>128K Byte</td>
<td>J3 on position 2-3</td>
</tr>
<tr>
<td></td>
<td>EPROM</td>
<td>256K Byte</td>
<td>J3 on position 2-3</td>
</tr>
<tr>
<td></td>
<td>EPROM</td>
<td>512K Byte</td>
<td>J3 on position 2-3</td>
</tr>
<tr>
<td></td>
<td>FLASH EPROM</td>
<td>128K Byte</td>
<td>J3 on position 1-2</td>
</tr>
<tr>
<td></td>
<td>FLASH EPROM</td>
<td>256K Byte</td>
<td>J3 on position 1-2</td>
</tr>
<tr>
<td>13</td>
<td>SRAM</td>
<td>128K Byte</td>
<td>-</td>
</tr>
<tr>
<td>7</td>
<td>SRAM+RTC</td>
<td>2K Byte</td>
<td>J2 on position 1-2</td>
</tr>
<tr>
<td></td>
<td>SRAM+RTC</td>
<td>8K Byte</td>
<td>J2 on position 2-3</td>
</tr>
<tr>
<td>34</td>
<td>EEPROM</td>
<td>256÷8K Byte</td>
<td>-</td>
</tr>
</tbody>
</table>

**Figure 29: Memory selection table**
All the above described devices must feature a JEDEC compliant pin out except for the serial EEPROM installed on IC34 that must be requested to grifo® in the ordering phase. To determine the name of the memory devices that can be mounted, please refer to the manufacturer documentation.

GPC® 15A is delivered in its default configuration, this means 128K SRAM on IC13 and 512 bytes serial EEPROM on IC34; any different memory configuration can be mounted by the User in autonomy or requested to grifo® in the order. Below are reported the order codes for the several optional memory configurations:

<table>
<thead>
<tr>
<th>Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>.EE08</td>
<td>1K serial EEPROM</td>
</tr>
<tr>
<td>.EE16</td>
<td>2K serial EEPROM</td>
</tr>
<tr>
<td>.EE64</td>
<td>8K serial EEPROM</td>
</tr>
<tr>
<td>.128KMOD</td>
<td>128K backed work SRAM</td>
</tr>
<tr>
<td>.2KMOD</td>
<td>2K backed SRAM</td>
</tr>
<tr>
<td>.8KMOD</td>
<td>8K backed SRAM</td>
</tr>
<tr>
<td>.2KRTC</td>
<td>2K backed SRAM plus RTC</td>
</tr>
<tr>
<td>.8KRTC</td>
<td>8K backed SRAM plus RTC</td>
</tr>
</tbody>
</table>

For further information about memory options and their cost please contact grifo®, while to easily locate the memory devices on the board please refer to figure 22.
FIGURE 30: COMPONENTS MAP
SOFTWARE DESCRIPTION

A wide selection of software development tools can be obtained, allowing use of the module as a system for its own development, both in assembler and in other high level languages; in this way the User can easily develop all the requested application programs in a very short time. Generally all software packages available for the mounted microprocessor, or for the Z80 family, can be used:

GET 80
It is a complete program with Editor, Communication driver, and Mass Memory management for all Z80 family cards. This program, developed by grifo®, allows to operate in the best conditions when GDOS, FGDOS or xGDOS MCI software tools are used; GET 80 is supplied when one of these tools is ordered and it is personalized with name and general data of the customer. A useful list of pull down menus and the possibility of using mouse, make program use very comfortable. GET 80 program can be executed both on MS-DOS system and on MACINTOSH computers too, through SOFT-PC program. It is supplied on MS-DOS 3”1/2 floppy disk with the documentation on GDOS 80 manual.

GDOS 15A
It is a complete development Tool for GPC® 15A card. It is supplied together with GET 80 program to allow an easy and immediate use of this powerful development system. GDOS is divided in two different structures: the first one works on PC maintaining serial communication with the second one. The second structure is on EPROM, it works on board of the card and it is an efficient operating system that executes many low level functions and, at the same time, it allows high level language use. The combination of the said structures results in a complete machine, in fact the card uses PC resources (like floppy disk, hard disk, printer, keyboard, monitor, etc.) as its own peripheral devices. This resulting “virtual machine” performs operation in a transparent way for the User, so this latter can operate with the same modality of standard PC languages. It is really interesting the compatibility of GDOS with all CP/M program and languages; so, if the User has experience, knowledge or developed applications with CP/M, he can use immediately GDOS, without any changes. Moreover, GDOS can manage all memory devices exceeding 64K Bytes as RAM disk and ROM disk. The on board RAM devices can directly be used performing data read and write operations with the confortable file formats. This software tools is supplied on EPROM with MS-DOS GET 80 floppy disk, some examples, utilities and the operating system documentation.

FGDOS 15A
It is really similar to GDOS, but it can program and erase the on board FLASH EPROM with the application program developed from the User. In this way the external EPROM programmer is not necessary to store definitely the program and it is possible to modify or to add code directly on the installed machine, through a portable PC. This software tools is supplied on FLASH EPROM with MS-DOS GET 80 floppy disk, some examples, utilities and the operating system documentation.

NOICE
It is a PC hosted debugger consists of a target specific DOS program, NOICExxx.EXE, and a target resident monitor program. The two programs communicate via RS 232. NOICE includes: source level debug; a disassembler; a file viewer; memory display and editing; a virtually unlimited number of breakpoints; hardware free single step; definition of symbols; the ability to record and play back files of commands; on line help.
xGDOS MCI 15A
It is a version of GDOS or FGDOS software tools, capable of PCMCIA Memory Card management. Using MCI 64 card, the GDOS operating system manages memory cards as RAM disk or ROM disk. All applications with data acquisition and data logging can be realized with high level languages that manage data on files, with a fast development time and without any software complication. This software tool is supplied on EPROM or FLASH EPROM with MS-DOS GET 80 floppy disk, some examples, utilities and the operating system documentation.

CBZ-80
Is is a Basic Compiler that generates a really compact and fast code. It must work together with any GDOS version and it can exceed the 64K memory limits of Z80 family microprocessors through CHAIN modality. More than one application program can be saved in RAM and/or ROM disks and subsequently executed. In conjunction to the powerful GET 80 Editor the CBZ 80 program becomes a comfortable and really efficient development system for any kind of application program. This program is supplied ad ROM DISK file in GDOS EPROM or FLASH EPROM and on MS-DOS floppy disk with some examples and manual.

PASCAL 80
It is an efficient and complete PASCAL Compiler for Z80 family cards, with features similar to Release 3.0 of Borland Turbo PASCAL. It must work together with any GDOS version and it can exceed the 64K memory limits of Z80 family microprocessors through OVERLAY modality. More than one application program can be saved in RAM and/or ROM disks and subsequently executed. The terminal emulation of GET 80 program support the typical full screen PASCAL Editor, including the attributes management.
This program is supplied as ROM DISK file in GDOS EPROM or FLASH EPROM and on MS-DOS floppy disk with some example and manual.

RSD 15A
This software tools is a Remote Symbolic Debugger with two operating mode. The first one is a monitor debugger modality with software emulation on P.C.; the second is a remote monitor debugger modality that execute code directly on the card. Through serial communication the User can: down load an HEX file and associated symbol table, debug code in symbolic mode, execute code in step to step mode or in real time mode, set breakpoint, dump and modify memory and registers, etc. RSD software tool supports both Z80 and Z180 instruction sets. Really interesting is the program execution management, in fact many hardware and software breakpoint are supported. RSD can be used together with assembler tools, like ZASM 80, and C Compiler CC 80.
It is supplied on EPROM and on MS-DOS floppy disk with technical manual.

ZASM 80
It is a macro cross assembler that operates on any PC with MS-DOS operating system. It supports both Z80 and Z180 instruction sets. The generated code can be debugged on PC, through software simulation, or directly on target card, through remote modality, using RSD software tools. ZASM 80 is compatible with C Compiler CC 80 of which it assemble the compilation result.
It is supplied on MS-DOS floppy disk with technical manual.
CC 80
It is a complete C Compiler with ANSI/ISO standard, provided of floating point procedure, that can generate code for Z80 and Z180 family microprocessors. It works together with cross assembler ZASM 80 and Symbolic Debugger RSD.
It is supplied on MS-DOS floppy disk with technical manual.

HI TECH C 80
Professional C Cross Compiler of Hi-Tech Software Inc. This Compiler is terribly fast and it generates a small quantity of code. This result is due to advanced techniques in optimizing the generated code based on Artificial Intelligence techniques which allow to get a very compact and very fast code. The package includes: IDE, Compiler, Code optimizer, Assembler, Linker, Remote Debugger and so on. This tool is Full ANSI/ISO Standard and Full Library Source Code. Once the porting of the Remote-Debugger module is done, this tool allows the user the software debugging directly on the hardware that he is experimenting. This type of specialization of the Remote-Debugger is available from now ant it is supplied with all grifo® CPU cards’. This software package is on 3” 1/2 diskettes under MS-DOS format along with user manual. This version supports these following CPUs: Z80, Z180, 84C011, 84C11, 84C013, 80C13, 84C015, 84C15, 64180, NCS800, Z181, Z182.

DDS MICRO C 85
Low cost cross compiler for C source program. It is a powerful software tool that includes editor, C compiler (integer), assembler, optimizer, linker, library, and remote debugger, in one easy to use integrated development environment. There are also included the library sources and many utilities programs.
ADDRESSES AND MAPS

In this chapter are reported all information about card use, related to hardware and software. For example, the registers addresses and the memory allocation are described below.

ON BOARD RESOURCES ALLOCATION

The card devices addresses are managed by a specific control logic, realized with programmable logic devices. This control logic allocates SRAM, EPROM and peripheral devices in a comfortable way for the User.

The control logic is able to manage separately Input/Output peripherals and on board memory. CPU 84C15 is capable to address directly 64K Byte of memory and 256 I/O addresses, the control logic provides on board memory and peripheral devices allocation inside the 656K Byte address space. The maps management is completely driven by software through the MMU circuit programming: the used memory can be selected and divided in 32K Byte size segments. About I/O maps the control logic avoids every conflicts problems between CPU internal and external peripherals.

Summarizing the control logic allocates:

- ABACO® BUS
- Up to 512K Byte of EPROM or 256K FLASH EPROM installed on IC18
- Up to 128K Byte of SRAM installed on IC13
- Up to 8K Byte of serial EEPROM, installed on IC34
- Up to 8K Byte of backed SRAM, installed on IC7
- SIO
- CTC
- PIO
- RTC
- Buzzer
- Baud rate generator
- Memory Management Unit circuitry
- Configuration Dip Switch DSW1 and DSW2
- Activity LEDs
- Watch Dog circuits

The addresses of all these devices are described in the following paragraphs and can't be set with different values. If some different specific maps are required, please contact directly grifo®.
ABACO® BUS ADDRESSES

The GPC® 15A control logic defines ABACO® BUS addresses and only these addresses must be used to manages correctly the BUS. As described in figures 34 and 35, only the addresses from 30H to DFH are available for ABACO® BUS. Any I/O operations at each one of these addresses enables the /IORQ signal and the other control signals of K1 connector and the I/O operations is performed on the connected peripheral cards.

MEMORIES MAPPING

The total 656K Byte of memory supported by the card are divided this way:

- Up to 512K Byte of EPROM or 256K Byte of FLASH EPROM allocated in the memory space
- Up to 128K Byte of SRAM allocated in the memory space
- Up to 8K Byte of backed SRAM allocated in the I/O space
- Up to 8K Byte of serial EEPROM allocated in the I/O space

GPC® 15A can directly manage at most 64K bytes of memory that is the microprocessor logic addressable space. On the board this logic space can be divided in two 32K Byte pages: both SRAM and EPROM can be installed on the low page, while only SRAM can be installed on the high page. MMU circuitry, driven through a simple software management, takes care to divide the addressable space in 32K Byte pages and to make them available directly into the CPU addressing space. It is possible to address indirectly a memory area much greater than the area normally accessible by the CPU just programming the MEM register. Here follow two figures that show the possible memory devices configurations, for further informations please refer to the paragraph "MEMORY MANAGEMENT UNIT", while to easily locate the memory devices refer to figure 22.

Some software packages, like GDOS and FGDOS, are capable to manage in autonomy the MMU circuitry to make address in the CPU addressable memory area all the available memory without bothering the User.

When a power on or a reset occur, R/E signal is set to 0, so the board starts executing the code located at the logical address 0000H of page 0 on EPROM or FLASH EPROM installed IC18.
**Figure 32: Memory Mapping with R/E=0**

- **0000H** to **FFFFH**: Pages 0 to 15
- **8000H**: Page 0
- **7FFFH**: Pages 1 and 0
- **FFFH**: Page 0
Figure 33: Memory mapping with R/E=1
I/O ADDRESSES

The on board control logic manages the allocation of all the peripheral devices registers in the microprocessor I/O space, that is 256 bytes long. Next table shows names, addresses, meanings and directions of peripheral device registers (including the internal microprocessor ones).

<table>
<thead>
<tr>
<th>DEVICE</th>
<th>REG.</th>
<th>ADDRESS</th>
<th>R/W</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>IC7 RAM + RTC</td>
<td>B0</td>
<td>00H</td>
<td>R/W</td>
<td>1st byte of data block</td>
</tr>
<tr>
<td></td>
<td>B1</td>
<td>01H</td>
<td>R/W</td>
<td>2nd byte of data block</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>B15</td>
<td>0FH</td>
<td>R/W</td>
<td></td>
</tr>
<tr>
<td>CTC</td>
<td>RC0</td>
<td>10H</td>
<td>R/W</td>
<td>Counter 0 status and data register</td>
</tr>
<tr>
<td></td>
<td>RC1</td>
<td>11H</td>
<td>R/W</td>
<td>Counter 1 status and data register</td>
</tr>
<tr>
<td></td>
<td>RC2</td>
<td>12H</td>
<td>R/W</td>
<td>Counter 2 status and data register</td>
</tr>
<tr>
<td></td>
<td>RC3</td>
<td>13H</td>
<td>R/W</td>
<td>Counter 3 status and data register</td>
</tr>
<tr>
<td>PPI 82C55</td>
<td>PDA</td>
<td>14H</td>
<td>R/W</td>
<td>Port A data register</td>
</tr>
<tr>
<td></td>
<td>PDB</td>
<td>15H</td>
<td>R/W</td>
<td>Port B data register</td>
</tr>
<tr>
<td></td>
<td>PDC</td>
<td>16H</td>
<td>R/W</td>
<td>Port C data register</td>
</tr>
<tr>
<td></td>
<td>CNT</td>
<td>17H</td>
<td>R/W</td>
<td>Status and command register</td>
</tr>
<tr>
<td>SIO</td>
<td>RDA</td>
<td>18H</td>
<td>R/W</td>
<td>Serial line A data register</td>
</tr>
<tr>
<td></td>
<td>RSA</td>
<td>19H</td>
<td>R/W</td>
<td>Serial line A status register</td>
</tr>
<tr>
<td></td>
<td>RDB</td>
<td>1AH</td>
<td>R/W</td>
<td>Serial line B data register</td>
</tr>
<tr>
<td></td>
<td>RSB</td>
<td>1BH</td>
<td>R/W</td>
<td>Serial line B status register</td>
</tr>
<tr>
<td>PIO</td>
<td>PAD</td>
<td>1CH</td>
<td>R/W</td>
<td>Port A data register</td>
</tr>
<tr>
<td></td>
<td>PAS</td>
<td>1DH</td>
<td>W</td>
<td>Port A control register</td>
</tr>
<tr>
<td></td>
<td>PBD</td>
<td>1EH</td>
<td>R/W</td>
<td>Port B data register</td>
</tr>
<tr>
<td></td>
<td>PBS</td>
<td>1FH</td>
<td>W</td>
<td>Port B control register</td>
</tr>
</tbody>
</table>

**Figure 34: I/O addresses table - Part 1**
For a detailed description of the registers function, please refer to next chapter "PERIPHERAL DEVICES SOFTWARE DESCRIPTION".

**FIGURE 35: I/O ADDRESSES TABLE - PART 2**

<table>
<thead>
<tr>
<th>DEVICE</th>
<th>REG.</th>
<th>ADDRESS</th>
<th>R/W</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>B.R.G.</td>
<td>BAUD</td>
<td>25H</td>
<td>R/W</td>
<td>Two serial lines baud rate management register</td>
</tr>
<tr>
<td>EXT. W.D.</td>
<td>RWD</td>
<td>25H</td>
<td>R</td>
<td>External watch dog retrigger register</td>
</tr>
<tr>
<td>I/O RAM</td>
<td>MEMIO</td>
<td>26H</td>
<td>R/W</td>
<td>IC 7 addresses management register</td>
</tr>
<tr>
<td>MEM. ADDRESS</td>
<td>MEM</td>
<td>27H</td>
<td>R/W</td>
<td>Memory devices addresses management register</td>
</tr>
<tr>
<td>ACT. LED</td>
<td>LED</td>
<td>25H</td>
<td>W</td>
<td>Activity LEDs management register</td>
</tr>
<tr>
<td>BUZZER</td>
<td>BUZ</td>
<td>27H</td>
<td>W</td>
<td>Buzzer management register</td>
</tr>
<tr>
<td>DSW1</td>
<td>DSW1</td>
<td>27H</td>
<td>R</td>
<td>DSW1 acquisition register</td>
</tr>
<tr>
<td>ABACO® BUS</td>
<td>I/O BUS</td>
<td>30H:DFH</td>
<td>R/W</td>
<td>I/O addresses for ABACO® BUS</td>
</tr>
<tr>
<td>INTERNAL REGISTER</td>
<td>SCR</td>
<td>EEH</td>
<td>R/W</td>
<td>Register for microprocessor control register pointer</td>
</tr>
<tr>
<td></td>
<td>SCDP</td>
<td>EFH</td>
<td>R/W</td>
<td>Register for microprocessor control data port</td>
</tr>
<tr>
<td>INTERNAL W.D.</td>
<td>WDTMR</td>
<td>F0H</td>
<td>R/W</td>
<td>Internal watch dog programmation register</td>
</tr>
<tr>
<td></td>
<td>WDTCR</td>
<td>F1H</td>
<td>W</td>
<td>Internal watch dog enable register</td>
</tr>
<tr>
<td>INTERRUPT</td>
<td>INTPR</td>
<td>F4H</td>
<td>W</td>
<td>Interrupt priority setting register</td>
</tr>
</tbody>
</table>
PERIPHERAL DEVICES SOFTWARE DESCRIPTION

In the previous paragraphs are described the external registers addresses, while in this one there is a specific description of registers meaning and function (please refer to I/O addresses table, for the registers names and addresses values). For a more detailed description of the devices, please refer to manufacturing company documentation; for microprocessor internal peripheral devices, not described in this paragraph, refer to appendix B. In the following paragraphs the D7÷D0 and .0÷7 indications denote the eight bits of the combination used in I/O operations.

MEMORY MANAGEMENT UNIT

An efficient MMU circuitry takes care to allocate in the CPU addressing space all the memory devices that can be installed on GPC® 15A. This section can be programmed through the MEM register, which is allocated in the I/O addressing space. The bits of MEM register have the following meaning:

MEM: Meaning of bits

| MEM.7  | R/E: SRAM (D7=1) or EPROM/FLASH EPROM (D7=0) selector, for the low page (0000H÷7FFFH) of the CPU addressing space |
| MEM.6  | BUZ (please refer to the paragraph "BUZZER") |
| MEM.5  | A18 x IC18 |
| MEM.4  | A17 x IC18 |
| MEM.3  | A16 x IC18 and /A16 x IC13 |
| MEM.2  | A15 x IC18 |
| MEM.1  | /A15 x IC13 |
| MEM.0  | A12 x IC7 (please refer to the paragraph "BACKED SRAM+RTC") |

Bit D7, named R/E, selects the memory device allocated in the low page ((0000H÷7FFFH) of microprocessor logical memory space:

- R/E = 0 -> IC 18 EPROM, FLASH EPROM
- R/E = 1 -> IC 13 SRAM

Bits D1÷D5 selects the page of IC 13 SRAM or IC 18 EPROM, FLASH EPROM that must be used and allocated always in the low page. Finally bit D0 defines the backed SRAM+RTC address, allocated in microprocessor I/O space.

The described settings are performed by an output operation at the address of register MEM, while by an input operation at the same address, a portion of MMU status is obtained. More precisely only bits D0÷D3 of the input data coincide with MEM bits and the most significative nibble (D4÷D7) coincides with DSW1 status.

When a reset or a Power On occur all the bits of MEM register are reset (all bits 0); this means to program the MMU section where the low 32K Bytes page consists of page 0 EPROM or FLASH EPROM installed on IC10 and the high 32K Bytes page consists of page 0 SRAM installed on IC8. Please refer to the following table, also remembering figures 32 and 33, for an overview of all the possible MMU section configurations.

"X" means non significant bit, that is that bit can be "1" or "0" without influencing the setting there described.
### FIGURE 36: POSSIBLE MMU SECTION CONFIGURATIONS TABLE

<table>
<thead>
<tr>
<th>32K LOW PAGE</th>
<th>32K HIGH PAGE</th>
<th>MEM D7-D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0: IC 18 EPROM or FLASH</td>
<td>0: IC 13 RAM</td>
<td>0X0000XXB = 00</td>
</tr>
<tr>
<td>1: IC 18 EPROM or FLASH</td>
<td>0: IC 13 RAM</td>
<td>0X0001XXB = 04</td>
</tr>
<tr>
<td>2: IC 18 EPROM or FLASH</td>
<td>0: IC 13 RAM</td>
<td>0X0010XXB = 08</td>
</tr>
<tr>
<td>3: IC 18 EPROM or FLASH</td>
<td>0: IC 13 RAM</td>
<td>0X0011XXB = 0C</td>
</tr>
<tr>
<td>4: IC 18 EPROM or FLASH</td>
<td>0: IC 13 RAM</td>
<td>0X0100XXB = 10</td>
</tr>
<tr>
<td>5: IC 18 EPROM or FLASH</td>
<td>0: IC 13 RAM</td>
<td>0X0101XXB = 14</td>
</tr>
<tr>
<td>6: IC 18 EPROM or FLASH</td>
<td>0: IC 13 RAM</td>
<td>0X0110XXB = 18</td>
</tr>
<tr>
<td>7: IC 18 EPROM or FLASH</td>
<td>0: IC 13 RAM</td>
<td>0X0111XXB = 1C</td>
</tr>
<tr>
<td>8: IC 18 EPROM</td>
<td>0: IC 13 RAM</td>
<td>0X1000XXB = 20</td>
</tr>
<tr>
<td>9: IC 18 EPROM</td>
<td>0: IC 13 RAM</td>
<td>0X1001XXB = 24</td>
</tr>
<tr>
<td>10: IC 18 EPROM</td>
<td>0: IC 13 RAM</td>
<td>0X1010XXB = 28</td>
</tr>
<tr>
<td>11: IC 18 EPROM</td>
<td>0: IC 13 RAM</td>
<td>0X1011XXB = 2C</td>
</tr>
<tr>
<td>12: IC 18 EPROM</td>
<td>0: IC 13 RAM</td>
<td>0X1100XXB = 30</td>
</tr>
<tr>
<td>13: IC 18 EPROM</td>
<td>0: IC 13 RAM</td>
<td>0X1101XXB = 34</td>
</tr>
<tr>
<td>14: IC 18 EPROM</td>
<td>0: IC 13 RAM</td>
<td>0X1110XXB = 38</td>
</tr>
<tr>
<td>15: IC 18 EPROM</td>
<td>0: IC 13 RAM</td>
<td>0X1111XXB = 3C</td>
</tr>
<tr>
<td>0: IC 13 RAM</td>
<td>0: IC 13 RAM</td>
<td>1XXX1X1XB = 8A</td>
</tr>
<tr>
<td>1: IC 13 RAM</td>
<td>0: IC 13 RAM</td>
<td>1XXX1X0XB = 88</td>
</tr>
<tr>
<td>2: IC 13 RAM</td>
<td>0: IC 13 RAM</td>
<td>1XXX0X1XB = 82</td>
</tr>
<tr>
<td>3: IC 13 RAM</td>
<td>0: IC 13 RAM</td>
<td>1XXX0X0XB = 80</td>
</tr>
</tbody>
</table>
EXTERNAL WATCH DOG

Retrigger operation of GPC® 15A external Watch Dog circuit is performed with a simple input operation at the address of register RWD. To avoid external Watch Dog activation it is indispensable to perform retrigger operations at regular time periods and the duration of these periods must be smaller than intervention time. If retrigger doesn't happen as before described and jumper J4 is connected, when intervention time is elapsed, the card is reset. By default the intervention time is about 700 ms.

SERIAL EEPROM

For informations about the management of serial EEPROM module installed on IC34, please refer to the documentation of the software package used to program the board. This technical manual reports no further informations about the serial EEPROM management because this activity employs a very deep knowledge of the device itself. For this, its complete management is affordable through the high level instructions of the software package being used.

Please remark that the first 32 bytes (0÷31) are reserved so the User should avoid to modify their value. Control logic allows serial EEPROM software management through DTRA and DTRB SIO signals, these are the connections:

\[
\begin{align*}
DTRB & \rightarrow \text{DATA signal} \quad \text{(SDA)} \\
DTRA & \rightarrow \text{CLOCK signal} \quad \text{(SCL)}
\end{align*}
\]

Known the serial EEPROM management circuitry hardware implementation, please remark that signals A0,A1,A2 of this device’s slave address are all set to logic 0. Bit logic status 0 corresponds to low logic status (≈0V) of the corresponding signal, while bit logic status 1 corresponds to low logic status (≈0V).

For further informations about SIO signals management modalities please refer to proper technical documentation of appendix B of this manual.

CONFIGURATION INPUTS

GPC® 15A is provided with 9 software acquirable User settable configuration inputs divided as follows.

Dip Switch DSW1 can be acquired by software, performing a simple input operation from the address of DSW1 register. This is the correspondence between Dip Switch signals and DSW1 bits:

\[
\begin{align*}
\text{DSW1.7} & \rightarrow \text{Dip Switch 1.4} \\
\text{DSW1.6} & \rightarrow \text{Dip Switch 1.3} \\
\text{DSW1.5} & \rightarrow \text{Dip Switch 1.2} \\
\text{DSW1.4} & \rightarrow \text{Dip Switch 1.1} \\
\text{DSW1.4} & \rightarrow \text{A16 x IC18 and } /\text{A16 x IC13 (see paragraph “MMU”)} \\
\text{DSW1.4} & \rightarrow \text{A15 x IC 18 (see paragraph “MMU”)} \\
\text{DSW1.4} & \rightarrow /\text{A15 x IC 13 (see paragraph “MMU”)} \\
\text{DSW1.4} & \rightarrow \text{A12 x IC 7 (see paragraph “MMU”)}
\end{align*}
\]
Only the most significant nibble is used to read the Dip Switch. The signals are in complemented logic, this means that a dip ON gives a logic status 0 on the corresponding bit, while a dip OFF gives a logic status 1.

Configuration jumper \textbf{J6} is connected to /SYNCB SIO signal. Jumper \textbf{J7} connected in position 1-2 gives logic status 0, while connection in position 2-3 gives logic status 1. For further informations about the acquisition of /SYNCB signal status, please refer to the proper technical documentation of appendix B of this manual. Jumper \textbf{J6} (RUN/DEBUG) works as selector of RUN modality (position 1-2) or DEBUG modality (position 2-3). This feature is used by some of \textbf{grifo®} software packages.

For more informations about how to acquire the status of DSW2, which is connected to the digital lines of PPI 82C55 PORT B, please refer to the paragraph about this latter.

\textbf{ACTIVITY LEDS}

On board control logic allows the management of two activity LEDs, called LD4 and LD5, through the LED register:

\begin{itemize}
  \item LED.7 \textarrow \text{set LD4 status}
  \item LED.3 \textarrow \text{set LD5 status}
\end{itemize}

The LED can be lit performing an output operation to the register \textbf{LED} with the corresponding bit set to logical 1. Of course, the LED can be turned off through the same output operation with the corresponding bit reset to logical 0.

Please remark that register LED has the same allocation address of register BAUD, so every write operation to the bits of this register must consider the effects on the other device.

Register LED is reset (all bits 0) when a reset or a power on occurs, so after one of such events LEDs are turned off.

\textbf{BUZZER}

Buzzer is activated by performing an output operation with bit D6=1 at the address of register BUZ; vice versa buzzer is disabled by performing the same operation with bit D6=0.

Please remark that register BUZ has the same allocation address of register MEM, so every write operation to the bits of this register must consider the effects on the other device.

BUZ register is reset (all bits to 0) after Reset or power on, maintaining disabled the buzzer circuit.
SIO
For further informations please refer to technical documentation on appendix B of this manual.

PIO
For further informations please refer to technical documentation on appendix B of this manual.

CTC
For further informations please refer to technical documentation on appendix B of this manual.

INTERNAL WATCH DOG
For further informations please refer to technical documentation on appendix B of this manual.

BACKED SRAM+RTC
On **GPC® 15A** there is a socket (IC 7) for a 2K or 8K bytes backed SRAM module; the backed SRAM can also include a complete Real Time Clock section. In this paragraph is described the software management of these devices.
The addressable space of IC 7 device varies from 2K to 8K bytes and it is allocated in microprocessor I/O space that is 256 bytes long. For this reason the device is divided in many blocks (or pages), each one 16 bytes long. The data are read or wrote performing first a block selection operation and after an input or output operation at the addresses of these block bytes. The number of blocks varies according to module size:

- 2K module -> 128 blocks
- 8K module -> 512 blocks

and the block selection is performed by programmation of the proper register **MEMIO**, allocated in I/O space. The bits meanings of this register are:

- **MEMIO.7** -> A11 x IC 7
- **MEMIO.6** -> A10 x IC 7
- **MEMIO.5** -> A9 x IC 7
- **MEMIO.4** -> A8 x IC 7
- **MEMIO.3** -> A7 x IC 7
- **MEMIO.2** -> A6 x IC 7
- **MEMIO.1** -> A5 x IC 7
- **MEMIO.0** -> A4 x IC 7

Axx signals select the block number used on IC 7 module, in fact they coincide with device addresses.
MEMIO register can be used both for output (block selection) and input (selected block acquisition) operations and it is reset (all bits to 0) after a reset or power on.
The last devices address (A12 x IC 7) that must be used for block selection is managed by MEM register, as described in paragraph “MEMORY MANAGEMENT UNIT”.

For example, if the User has to write the byte AAH to the address 0700H of IC 7 device, the following operations must be executed:

1) Reset D0 bit of register MEM, by executing an output operation at the address of this register. Example: OUT 27H,00H

2) Select block number 70H = set byte 70H in MEMIO register, by executing an output operation at the address of this register. Example: OUT 26H,70H

3) Write byte AAH to the first byte of selected block, by executing an output operation at the address of this register. Example: OUT 00H,AAH

When the IC 7 module is a backed SRAM + RTC device, eight internal registers must be used to set and acquire time and data. These registers always are the last eight addresses of the device size, as described in the following table:

<table>
<thead>
<tr>
<th>REGISTRO</th>
<th>INDIRIZZO 2K</th>
<th>INDIRIZZO 8K</th>
</tr>
</thead>
<tbody>
<tr>
<td>CNT</td>
<td>07F8H</td>
<td>1FF8H</td>
</tr>
<tr>
<td>SEC</td>
<td>07F9H</td>
<td>1FF9H</td>
</tr>
<tr>
<td>MIN</td>
<td>07FAH</td>
<td>1FFAH</td>
</tr>
<tr>
<td>ORE</td>
<td>07FBH</td>
<td>1FFBH</td>
</tr>
<tr>
<td>SETT</td>
<td>07FCH</td>
<td>1FFCH</td>
</tr>
<tr>
<td>GIO</td>
<td>07FDH</td>
<td>1FFDH</td>
</tr>
<tr>
<td>MES</td>
<td>07FEH</td>
<td>1FFEH</td>
</tr>
<tr>
<td>ANN</td>
<td>07FFH</td>
<td>1FFFH</td>
</tr>
</tbody>
</table>

**Figure 37: SRAM+RTC registers addresses table**

With these registers the backed RTC can be read (acquisition of actual time and date), wrote (programmation of new time and date), started, stopped, etc. by using simple and fast I/O operations.
YEAR = Y7 Y6 Y5 Y4 Y3 Y2 Y1 Y0
where: Y7÷Y0 = BCD year value (00-99)

MONTH = 0 0 0 M4 M3 M2 M1 M0
where: M4÷M0 = BCD month value (01-12)

DAY = 0 0 D5 D4 D3 D2 D1 D0
where: D5÷D0 = BCD day of the month value (01-31)

WEEK = 0 FT 0 0 0 W2 W1 W0
where: W2 W1 W0 = Day of the week value:
  0 0 1 = Sunday
  0 1 0 = Monday
  0 1 1 = Tuesday
  1 0 0 = Wednesday
  1 0 1 = Thursday
  1 1 0 = Friday
  1 1 1 = Saturday
FT = Counter frequency test

HOUR = KS 0 H5 H4 H3 H2 H1 H0
where: KS = RTC counter start
  H5÷H0 = BCD hour value (00-23)

MINUTE = 0 M6 M5 M4 M3 M2 M1 M0
where: M6÷M0 = BCD minutes value (00-59)

SECOND = ST S6 S5 S4 S3 S2 S1 S0
where: S6÷S0 = BCD seconds value (00-59)
  ST = RTC counter stop

CONTROL= W R S C4 C3 C2 C1 C0
dove: W = Write operation selection
  R = Read operation selection
  S = Sign bit of compensation combination
  C4÷C0 = compensation combination

Here follows a short explanation about the meaning of the bits:

Bit R - Read operation selection

Setting bit R to "1" inhibites the Real Time Clock registers update, to prevent partial reads if the read operation should occur during the update.
Resetting bit R to "0" restores the normal operations.
Setting R to "1" when an update has already started doesn't stop the update itself.
Bit W - Write operation selection

Like it happens for bit R, setting bit W to "1" inhibites the Real Time Clock registers update, to allow the User to write the new values in the register bank. The new values are copied to the internal counters only when bit W is reset to "0", restoring all normal operations. Bits KS, FT and all other bits signed with a "0" must be kept to "0".

Bit S and bits C4÷C0 - Signed compensation combination

Thermal drifts in the clock counting can be compensated up to ±63.07 ppm (Parts per Million) along a 64 minutes compensation cycle by loading opportune values in the bits S and C4÷C0. Bits C4÷C0 indicate the entity of the compensation in steps of 2.034 ppm, being C0 the least significant bit, it is possible to input a correction from 0 to 31 steps, which means a maximum compensation of 31*2.034=63.07 ppm. When sign bit S is set to "1" indicates a positive correction (the clock is longer), else the correction is negative (the clock is shorter). This capability should compensate the maximum thermal drift of the internal quartz.
For example, shold the quartz oscillate at exactly 32768 Hz, setting to "1" all bits C4÷C0 wouls represent 5.35 seconds per month.

Bit FT - Counter frequency test

The least significant bit of SEC register will toggle exactly 512 times per second if the quartz oscillates exactly at 32768 Hz when bit FT is set to "1". Any deviation of the toggle frequence reflects perfectly the drift of the quartz oscillation frequence. For example, a deviation of +10 ppm of the internal quartz frequence could be compensated setting the bits S and C4÷C0 to -5 (S=0 and C4÷C0=00101).
During the test chip select and addresses must be well-stable.

Bits ST and KS - Counter Stop and Kick Start

To stop the internal oscillator and so optimize th internal battery duration just set bit ST to "1". For more safety, restarting the clock involves the manipulation of another bit called KS, "Kick Start". This is the procedure to restart the clock:

1) Set bit W to "1"
2) Reset bit ST to "0"
3) Set bit KS to "1"
4) Reset bit W to "0"
5) Wait 2 seconds
6) Set bit W to "1"
7) Reset bit KS to "0" - This is essential to optomize the duration of the battery
8) Set the desired time and date
9) Reset bit W to "0"

For further information about RTC use, please refer to manufacturing company documentation.
BAUD RATE GENERATOR

The baud rate generator section generates the right frequency signals that are used by SIO to obtain standard baud rates on its serial communication lines. The available baud rates range from 300 baud to 38.4K baud with six intermediary values and they are programmable by software. The baud rate managements is performed by input and output operations at the address of register BAUD and the bits meanings of this register are:

\[
\text{BAUD} = \text{LD4 BB2 BB1 BB0 LD5 BA2 BA1 BA0}
\]

where:

- \(\text{LD4}\) = LD4 activity LED management
- \(\text{BB2 BB1 BB0}\) = Select serial line B baud rate
  - 0 0 0 = Set baud rate at 300 baud
  - 0 1 0 = Set baud rate at 600 baud
  - 0 1 1 = Set baud rate at 1200 baud
  - 1 0 0 = Set baud rate at 2400 baud
  - 1 0 1 = Set baud rate at 4800 baud
  - 1 1 0 = Set baud rate at 9600 baud
  - 1 1 1 = Set baud rate at 19200 baud
- \(\text{BA2 BA1 BA0}\) = Select serial line A baud rate
  - 0 0 0 = Set baud rate at 300 baud
  - 0 0 1 = Set baud rate at 600 baud
  - 0 1 0 = Set baud rate at 1200 baud
  - 0 1 1 = Set baud rate at 2400 baud
  - 1 0 0 = Set baud rate at 4800 baud
  - 1 0 1 = Set baud rate at 9600 baud
  - 1 1 0 = Set baud rate at 19200 baud
  - 1 1 1 = Set baud rate at 38400 baud
- \(\text{LD5}\) = LD5 activity LED management

The User sets the desired baud rate on both serial lines by an output operation on register BAUD and he acquires the programmed baud rates by an input operation on the same register. The possibility to acquire the programmed baud rates of both serial lines is really interesting when some completely separated procedures manage at the same time serial communications. For example, the software can change serial line A baud rate with no modifications on serial line B baud rate, etc. BAUD register is reset (all bits to 0) after reset or power on, setting baud rate at 300 baud on both serial lines.
PPI 82C55

This external peripheral device is managed through 4 registers: one status register (CNT) and three data registers (PDA, PDB, PDC). The data registers are available both for input operation (to obtain signal status) and for output operation (to set signal status) with the correspondence described in figure 34. The PPI 82C55 can work in three different modes:

MODE 0 = it provides two 8 bits bidirectional ports (A,B) and two 4 bits bidirectional ports (C LOW, C HIGH); output signals are latched and input signals are not latched; no handshake signals are provided.

MODE 1 = it provides two 12 bits ports (A+C LOW and B+C HIGH) where ports A and B are used as 8 I/O lines and port C are used as 4 handshake lines. Both inputs and outputs are latched.

MODE 2 = it provides a 13 bits port (A+C3 ÷ 7) where port A is used as 8 I/O lines and the 5 bits of port C are used as handshake, and a 11 bits port (B+C0 ÷ 2) where port B is used as 8 I/O lines and the 3 bits of port C are used as handshakes. Both inputs and outputs are latched.

The device is programmed writing an 8 bits word in the status register CNT, with the following bits meaning:

CNT = SF  M1  M2  A  CH  M3  B  CL

where:
SF = mode Set Flag: if actived (1) the device is enabled for standard I/O operation
M1  M2 = mode selection:
0  0 = mode 0
0  1 = mode 1
1  X = mode 2
A = port A direction: 1=input; 0=output
CH = port C HIGH direction: 1=input; 0=output
M3 = mode selection: 1=mode 1; 0=mode 0
B = port B direction: 1=input; 0=output
CL = port C LOW direction: 1=input; 0=output

After Reset or power on PPI 82C55 is programmed in mode 0 with all three ports in input; in this way any connection of PPI 82C55 signals can be used without conflict problems.
EXTERNAL CARDS

GPC® 15A can be connected to a wide range of block modules and operator interface system produced by grifo®, or to many system of other companies. The on board resources can be expanded with a simple connection to the numerous peripheral grifo® boards, both intelligent and not, thanks to its standard ABACO® BUS connector. Even cards with ABACO® I/O BUS can be connected, by using the proper mother boards. Hereunder some of these cards are briefly described; ask the detailed information directly to grifo®, if required.

**KDL X24 - KDF 224**
Keyboard Display LCD 2,4 rows 24 keys
Interface with Fluorescent or LCD display, LEDs backlit, 20x2 or 20x4 characters; up to 24 keys matrix keyboard connector. It is directly driven by a 20 pins ABACO® I/O standard connector; High level languages supported; standard pinout for telephone keyboard.

**QTP 24 - QTP 24P**
Quick Terminal Panel 24 keys with Parallel interface
Intelligent user panel equipped with Fluorescent or LCD display, LEDs backlit, 20x2 or 20x4 characters; RS 232, RS 422, RS 485 or current loop serial line; serial E2 for set up and message. Possibility of re-naming keys, LEDs and panel name by inserting label with new name into the proper slot; 24 Keys and 16 LEDs with blinking attribute and buzzer manageable by software; built in power supply; RTC option, reader of magnetic badge and relay. The QTP 24P is low cost no intelligent (passive) version. It is directly driven from 16 TTL I/O lines; high level languages supported.

**QTP G28**
Quick Terminal Panel - LCD Graphic, 28 keys
LCD display 240x128 pixels, CFC backlit; Optocoupled RS 232 line and additional RS 232/422/485/C. L. line; CAN line controller; E2 for set up; RTC and RAM lithium backed; primary graphic object; possibility of re-naming keys, LEDs and panel name; 28 keys and 16 LEDs with blinking attribute and buzzer manageable by software; Buzzer; built-in power supply; reader of magnetic badge and relay option.

**ABB 03**
ABACO® Block BUS 3 slots
3 slots ABACO® mother board; 4 TE pitch connectors; ABACO® I/O BUS connector; screw terminal for power supply; connection for DIN C type and Ω rails.

**ABB 05**
ABACO® Block BUS 5 slots
5 slots ABACO® mother board with power supply. Double power supply built in; 5Vdc 2,5A section for powering the on board logic; second section at 24Vdc 400mA galvanically coupled, for the optocoupled input lines. Auxiliary connector for ABACO® I/O BUS. Connection for DIN Ω rails.

**MCI 64**
Memory Cards Interfaces 64 MBytes
Interfacing card for managing 68 pins PCMCIA memory cards, it is directly driven from any ABACO® I/O standard connector; High level languages GDOS supported.
Figure 38: Possible connections diagram

- ANY I/O TYPE
- CI/O R16
- RKD LT
- LAD 15
- IPC 52

- POWER SUPPLY +5Vdc ONLY

ANY MOTHERBOARD TYPE WITH ABACO® BUS

16 DIGITAL TTL INPUT/OUTPUT
- to XBI-01, OBI-01, RBO-08 etc.
- RELAY
- TRANSISTOR COUPLED

ANY CPU TYPE
- GPC® 552
- GPC® 15R

Serial Line
- RS 232, RS 422, RS 485, Current Loop

PC like or Macintosh

ANY I/O TYPE
- 16 DIGITAL TTL INPUT/OUTPUT
- to XBI-01, OBI-01, RBO-08 etc.
- OPTO RELAY
- TRANSISTOR COUPLED

4 Counters or 4 Timers

Any Memory Card

Opto Relay

16 DIGITAL TTL INPUT/OUTPUT

Power Supply +5Vdc ONLY

QTP 24 etc.

OR connect to MEMORY CARD

PrINTER
IAC 01
Interface Adapter Centronics
Interface between ABACO® standard I/O 20 pins connector and D 25 pins connector with Centronics standard pin out.

IBC 01
Interface Block Comunication
Conversion card for serial communication, 2 RS 232 lines; 1 RS 422–485 line; 1 optical fibre line; selectable DTE/DCE interface; quick connection for DIN 46277-1 and 3 rails.

OBI N8 - OBI P8
Opto BLOCK Input NPN-PNP
Interface between 8 NPN, PNP optocoupled and displayed input lines, with screw terminal and ABACO® standard I/O 20 pins connector; power supply section; connection for DIN Ω rails.

TBO 01 - TBO 08
Transistor BLOCK Output
Interface for ABACO® standard I/O 20 pins connector; 16 or 8 transistor output lines 45 Vdc 3 A open collector; screw terminal; optocoupled and displayed lines; connection for DIN 247277-1 and 3 rails.

RBO 08 - RBO 16
Relé BLOCK Output
Interface for ABACO® standard I/O 20 pins connector; 8 or 16 displayed Relays 3A with MOV; screw terminal; connection for DIN Ctype and Ω rails.

FBC 20 - FBC 120
Flat Block Contact 20 vie
Interfaccia tra 2 o 1 connettori a perforazione di isolante (scatolino da 20 vie maschi) e la filatura da campo (morsettiere a rapida estrazione). Attacco rapido per guide tipo DIN 46277-1 e 3.

DEB 01
Didactic Experimental Board
Supporting card for 16 TTL I/O lines use. It includes: 16 keys, 16 LEDs, 4 digits, 16 keys matrix keyboard, Centronics printer interface, LCD display and fluorescent display interface, GPC® 68 I/O connector, field connection with screw terminal.

IAL 42
Interface Adapter LCD
Interface between 16 I/O TTL available on I/O ABACO® standard connector and 14 pins lowprofile male connector featuring standard pin-out for fluorescent LCD displays management.

XBI 01
miXed BLOCK Input Output
Interface for ABACO® standard I/O 20 pins connector; 8 transistor output lines 45 Vdc 3A; 8 input lines; screw terminal; optocoupled and displayed I/O lines; connection for DIN 247277-1 and 3 rails.
XBI R4 - XBI T4
miXed BLOCK Input-Output
Interface for ABACO® standard I/O 20 pins connector; 4 Relays 3A with MOV or 4 optocoupled Transistors 3A open collectors; 4 input lines optocoupled; screw terminal; connection for DIN Ctype and Ω rails.

CI/O R16
16 Coupled Input Output with relays
16 optocoupled inputs with low frequency filter; standard rate +24 Vdc input voltage; 16 microrelays 1 A output lines; 24 Vac noise suppressor, type MOV; I/O displayed through LEDs.

IPC 52
Intelligent Peripheral Controller, 24 analogic input
This intelligent peripheral card acquires 24 independent analogic input lines: 8 PT 100 or PT 1000 sensors, 8 J,K,S,T termocouples, 8 analog input ±2Vdc or 4÷20mA; 16 bits + sign A/D section; 0.1 °C resolution; 32K RAM for local data logging; buzzer; 16 TTL I/O lines; 5 or 8 conversion per second; facility of networking up to 127 IPC 52 cards using serial line. BUS interfacing or through RS 232, RS 422, RS 485 or current loop line. Only 5Vdc power supply.

DAC 16
Digital to Analog Converter 16 bits
2 Digital to Analog converter, 16 bits galvanically insulated; programmed data displayed; ± 10 Vdc output; gain and offset setting; 8 bit Bus; standard addressing.

RKD LT
Remote Keyboard Display controller
Video terminal able to manage many different graphic LCD or alphanumeric fluorescent LCD or displays; matrix keyboard input; BUS or serial interfacing; 1 RS 232 line; additional RS 232, RS 422-485 or Current Loop line; serial EEPROM for set-up; primary graphic object; LEDs driving; Buzzer.

UCC A2
UART Communication Cards, 2 lines
2 Independent RS 232, RS 422, RS 485 or Current Loop lines. Each line: 3 characters buffer; Asyroncommuncation from 50 to 115K baud. Parity, bit stop and data length is software programmable.

PCI 01
Peripheral Coupled 32 Inputs
32 optocoupled input lines displayed through LEDs with Pi-Greek filter; standard rate 24 Vdc input voltage; 8/16 bits Bus extended addressing.

JMS 34
Jumbo Multifunction Support for Axis control
Generic peripheral axis control card. 3 optocoupled acquisition channels, with 16 bits bidirectional counter, for incremental encoder. 4 12bits ±10Vdc D/A channels. 8 Opto-in; 8 NPN Opto-output 40Vdc 500 mA. All I/O lines displayed with LEDs.
BIBLIOGRAPHY

Here follows a list of manuals that can be a source of further information about the devices installed on **GPC® 15A**.

TEXAS INSTRUMENTS Manual: *The TTL Data Book - SN54/74 Families*
Manuale TEXAS INSTRUMENTS Manual: *RS-422 and RS-485 Interface Circuits*
Manuale TEXAS INSTRUMENTS Manual: *Linear Circuits Data Book - Volume 1 and 3*

SGS-THOMSON Data Book: *MEMORIES - Data Book*
SGS-THOMSON Data Book: *INDUSTRY STANDARD LINEAR ICs - Data Book*

NEC Manual: *Microprocessors and Peripherals - Volume 3*
NEC Manual: *Memory Products*

AMD Manual: *Flash Memory Products*

MAXIM Manual: *New Releases Data Book - Volume IV*
MAXIM Manual: *New Releases Data Book - Volume V*

XICOR Manual: *Data Book*


Please connect to the manufacturers' websites to get the latest version of all manuals and data sheets.
This chapter shows the electric diagram of the most frequently used interfaces for GPC® 15A. Every one of these interfaces can be made by the User in autonomy, while only few of them are grifo® standard boards and can be ordered.

**Figure A1: IAC 01 Electric Diagram**
Figure A3: QTP 16P electric diagram
Figure A4: QTP 24P Electric Diagram - Part 1
Figure A5: QTP 24P electric diagram - part 2
FIGURE A6: SPA 01 ELECTRIC DIAGRAM
APPENDIX B: ON BOARD COMPONENTS DESCRIPTION

CPU Z84C15

Z84013/015
Z84C13/Z84C15
IPC INTELLIGENT PERIPHERAL CONTROLLER

FEATURES

- Z84C00 Z80 CPU with Z84C30 CTC, Z84C4X SIO, CGC, Watch Dog Timer (WDT). In addition, Z84C15 and Z84015 have Z84C20 PIO.
- High speed operation 6, 10 MHz
- 16 MHz operation for Z84C15 only.
- Low power consumption in four operation modes:
  - 4.1 mA Typ. (Run mode)
  - 6 mA Typ. (Idle1 mode)
  - 80 µA Typ. (Idle2 mode)
  - 0.5 µA Typ. (Stop mode)
- Wide operational voltage range (5V ± 10%)
- TTL/CMOS compatible.
- Z84013 features:
  - Z84000 Z80 CPU
  - On-chip two channel SIO (Z80 SIO)
  - On-chip four channel Counter Timer Controller (Z80 CTC)
  - Built-in Clock Generator Controller (CGC).
- Built-in Watch Dog Timer (WDT).
- Noise filter to CLR/TRG inputs of the CTC.
- 84-pin PLCC package.

Z84015 features:
- All Z84013 features, plus on-chip two 8-bit ports (Z80 P1O) and 100-pin QFP package.

Z84C13/Z84C15 enhancements to Z84013/Z84015:
- Power-on reset.
- Addition of two chip select pins.
- 32-bit CRC for Channel A of SIO.
- Wait state generator.
- Simplified EV mode selection.
- Schmitt trigger inputs to transmit and receive clocks of the SIO.
- Crystal divide-by-one mode.
- 100-pin QFP (Z84C15 only)

GENERAL DESCRIPTION

The Intelligent Peripheral Controller (IPC) is a series of highly superintegrated devices with four versions. The Z84C13 and the Z84C15 are upward compatible versions of the Z84013 and the Z84015. The Z84015 is a CMOS 8-bit microprocessor integrated with the CTC, SIO, CGC, WDT and the PIO into a single 100-pin Quad Flat Pack (QFP) package. The Z84013 is the Z84015 without PIO, and is housed in a 84-pin PLCC package. The Z84C13 is the Z84013 with enhancements and the Z84C15 is the Z84015 with enhancements. These high-end superintegrated intelligent peripheral controllers are targeted for a broad range of applications ranging from error correcting modems to enhancement/cost reductions of existing hardware using Z80-based discrete peripherals. Figures 1 and 2 show the difference between the Z84013/015 and the Z84C13/Z84C15.

Hereinafter, use the word IPC on the description covering all versions (Z84C13/Z84C15 and Z84013/Z84015). Use Z84C13/15 on the description that applies only to the Z84C13 and Z84C15, and use Z84013/015 on the description that applies only to the Z84013 and Z84015.
Figure 4. Z84015/Z84C15 Pin-out Assignments

PIN DEFINITIONS

The pin assignment for each device is shown in Figure 3 and 4. Following is the description on each pin. For the description and the pin number, it stated as "x13" or "x16", that applies to both Z84C13(Z84013) or Z84C15(Z84015). Otherwise, G13 for Z84C13, G16 for Z84015, 013 for Z84013 and O16 for Z84016.

CPU SIGNALS

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Input/Output, 3-State</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>A0-A15</td>
<td>16-1(x13), 6-1, 100-91(x15)</td>
<td>IO</td>
<td>16-bit address bus. Specified I/O and memory addresses to be accessed. During the refresh period, addresses for refreshing are output. The bus is an input when the external master is accessing the on-chip peripherals.</td>
</tr>
<tr>
<td>D0-D7</td>
<td>63-76(x13), 88-62(x15)</td>
<td>IO</td>
<td>8-bit bidirectional data bus. When the on-chip CPU is accessing on-chip peripherals, these lines are set to output and hold the data to/from on-chip peripherals.</td>
</tr>
<tr>
<td>JRD</td>
<td>30(x13), 14(x15)</td>
<td>IO</td>
<td>Read signal. CPU read signal for accessing data from memory or I/O devices. When an external master is accessing the on-chip peripherals, it is an input signal.</td>
</tr>
<tr>
<td>MR</td>
<td>20(x13), 13(x15)</td>
<td>IO</td>
<td>Write signal. This signal is output when data, to be stored in a specified memory or peripheral LSI, is put on the MPU data bus. When an external master is accessing the on-chip peripherals, it is an input signal.</td>
</tr>
<tr>
<td>MREQ</td>
<td>23(x13), 17(x15)</td>
<td>IO, 3-State</td>
<td>Memory request signal. When an effective address for memory access is on the address bus, “0” is output. When an external master is accessing the on-chip peripherals, it is an input signal.</td>
</tr>
<tr>
<td>IRQQ</td>
<td>21(x13), 15(x15)</td>
<td>IO</td>
<td>I/O request signal. When addresses for I/O are on the lower 8 bits (A7-A0) of the address bus in the I/O operation, “0” is output. In addition, the IRQQ signal is output with the M1 signal at the time of interrupt acknowledge cycle to inform peripheral LSI of the state of the interrupt response vector when put on the data bus. When an external master is accessing the on-chip peripherals, it is an input signal.</td>
</tr>
<tr>
<td>M1</td>
<td>17(x13), 80(x15)</td>
<td>IO</td>
<td>Machine cycle &quot;11&quot;, MREQ and &quot;0&quot; are output together in the operation code fetch cycle. M1 is output for every opcode fetch when a two byte opcode is executed. In the maskable interrupt acknowledge cycle, this signal is output together with IRQQ. It is 3-stated in EV mode.</td>
</tr>
</tbody>
</table>
### CPU SIGNALS (Continued)

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Input/Output, State</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>A/FSH</td>
<td>26(13), 7(15)</td>
<td>Out, 3-State</td>
<td>The refresh signal. When the dynamic memory refresh address is on the low order byte of the address bus, A/FSH is active along with M/REQ signal. This pin is 3-state in 3-State mode.</td>
</tr>
<tr>
<td>JNT</td>
<td>23(x-3), 19(x-15)</td>
<td>Open drain</td>
<td>Maskable interrupt request signal. Interrupt is generated by peripheral LSI. The signal is accepted if the interrupt enable (I/REQ) is set to &quot;1.&quot; The JNT signal of on-chip peripheral is internally wired - OFF without pull-up resistors and requires external pull-up. Also, interrupts from on-chip peripheral go out from this pin.</td>
</tr>
<tr>
<td>JNII</td>
<td>56(x-3), 63(x-15)</td>
<td>In</td>
<td>Non-maskable interrupt request signal. This interrupt request has a higher priority than the maskable interrupt request and does not rely upon the state of the interrupt enable (I/REQ).</td>
</tr>
<tr>
<td>HALT</td>
<td>31(x-13), 81(x-15)</td>
<td>Out, 3-State</td>
<td>Halt signal. Indicates that the CPU has executed a HALT instruction. This signal is 3-state in 3-State mode.</td>
</tr>
<tr>
<td>BUSREQ</td>
<td>18(x-13), 120(x-15)</td>
<td>In</td>
<td>BUS request signal. BUSREQ requests placement of the address bus, data bus, M/REQ, I/REQ, RD and WR signals into the high impedance state. BUSREQ is normally wired OFF and a pull-up resistor is externally connected.</td>
</tr>
<tr>
<td>BUSACK</td>
<td>23(x-13), 12(x-15)</td>
<td>Out (G3(G16), Out3-State (C19/C16))</td>
<td>Bus Acknowledge signal. In response to BUSREQ signal, BUSACK informs a peripheral LSI that the address bus, data bus, M/REQ, I/REQ, RD and WR signals have been placed in the high impedance state.</td>
</tr>
</tbody>
</table>

**Note:** For the Z84C150/154, the BUSACK signal will be enabled during 3-State mode. For the Z84C163/15/14, BUSACK will be 3-state during 3-State mode.

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Input/Output, State</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>A/RF</td>
<td>55(x-13), 70(x-15)</td>
<td>Out</td>
<td>1-bit auxiliary address bus. Output is the same as I/ALT (A7) of the address bus. However, during a refresh cycle, this pin outputs the address which is the most significant bit of the 8-bit refresh address signal linked to the low order 7 bits of the address bus.</td>
</tr>
</tbody>
</table>

### CTC SIGNALS

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Input/Output, State</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLK/TRG0 - CLK/TRG3</td>
<td>75-79(x-13), 81-88(x-15)</td>
<td>In</td>
<td>External clock/trigger input. These four CLK/TRG pins correspond to four Counter/Timer Channels. In the counter modes, each active edge will cause the down-counter to decrement by one. In timer modes, an active edge will start the timer. It is program selectable whether the active edge is rising or falling.</td>
</tr>
<tr>
<td>ZC/TOO - ZC/TO3</td>
<td>68-7(x-13), 74-77(x-15)</td>
<td>Out</td>
<td>Zero count/timer out signal. In either timer or counter mode, pulses are output when the down-counter has reached zero.</td>
</tr>
</tbody>
</table>

### SIO SIGNALS

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Input/Output, State</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>M/RDYA</td>
<td>32-52(x-13), 32-52(x-15)</td>
<td>Out</td>
<td>Wake/Ready signal A and Wake/Ready signal B. Used as WAIT or READY depending upon SIO programming. When programmed as WAIT they go active at &quot;1&quot;, alerting the CPU that addressed memory or I/O devices are not ready by requesting the CPU to wait. When programmed as READY, they are active at &quot;0&quot; which determines when a peripheral device associated with a DMA pin is for read/write data.</td>
</tr>
<tr>
<td>M/RDYY</td>
<td>32-52(x-13), 32-52(x-15)</td>
<td>Out</td>
<td>Wake/Ready signal A and Wake/Ready signal B. Used as WAIT or READY depending upon SIO programming. When programmed as WAIT they go active at &quot;1&quot;, alerting the CPU that addressed memory or I/O devices are not ready by requesting the CPU to wait. When programmed as READY, they are active at &quot;0&quot; which determines when a peripheral device associated with a DMA pin is for read/write data.</td>
</tr>
<tr>
<td>S/MODA, S/MODB</td>
<td>32-52(x-13), 32-52(x-15)</td>
<td>In/Output</td>
<td>Synchronous signals in asynchronous receive mode, they act as A/CTS and I/CDS. In external sync mode, these signals act as inputs. In internal sync mode, they act as outputs.</td>
</tr>
<tr>
<td>S/SCI, S/CIOB</td>
<td>34-52(x-13), 32-52(x-15)</td>
<td>In</td>
<td>Serial receive data signal</td>
</tr>
</tbody>
</table>
## SIO SIGNALS (Continued)

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Input/Output, 3-State</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>/RCA, /RCB</td>
<td>35,51(x13), 35,49(x15)</td>
<td>In</td>
<td>Receive clock signal. In the asynchronous mode, the receive clocks can be 1, 15, 32, or 64 times the data transfer rate.</td>
</tr>
<tr>
<td>/TCA, /TCB</td>
<td>35,50(x13), 35,48(x15)</td>
<td>In</td>
<td>Transmitter clock signal. In the asynchronous mode, the transmitter clocks can be 1, 15, 32, or 64 times the data transfer rate.</td>
</tr>
<tr>
<td>TXD, TXDB</td>
<td>37,49(x13), 37,47(x15)</td>
<td>Out</td>
<td>Serial transmit data signal.</td>
</tr>
<tr>
<td>RXRA, RXR8</td>
<td>38,48(x13), 38,46(x15)</td>
<td>Out</td>
<td>Data terminal ready signal. When ready, these signals go active to enable the terminal transmitter. When not ready, these signals go inactive to disable the terminal transmitter.</td>
</tr>
<tr>
<td>RTS, RTSB</td>
<td>39,47(x13), 37,45(x15)</td>
<td>Out</td>
<td>Request to send signal. “0” when transmitting serial data. They are active when enabling the receiver to transmit data.</td>
</tr>
<tr>
<td>CTS, CTSB</td>
<td>40,46(x13), 38,44(x15)</td>
<td>In</td>
<td>Clear to send signal. When “0”, after transmitting these signals the modem is ready to receive serial data. When ready, these signals go active to enable data transfer from the terminal.</td>
</tr>
<tr>
<td>DCD, DCDB</td>
<td>41,45(x13), 38,43(x15)</td>
<td>In</td>
<td>Data carrier detect signal. When “0”, serial data can be received. These signals are active to enable receivers to transmit.</td>
</tr>
</tbody>
</table>

## SYSTEM CONTROL SIGNALS

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Input/Output, 3-State</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>IEI</td>
<td>60(x13), 71(x15)</td>
<td>In</td>
<td>Interrupt enable input signal. IEl is used with the IEO to form a priority daisy chain when there is more than one interrupt-driven peripheral.</td>
</tr>
<tr>
<td>IEO</td>
<td>59(x13), 71(x15)</td>
<td>Out</td>
<td>The interrupt enable output signal in the daisy chain interrupt control. IEO controls the interrupt of external peripherals. IEO is active when IEl is “1” and the CPU is not servicing an interrupt from the on-chip peripherals.</td>
</tr>
<tr>
<td>J/CSO</td>
<td>42(x13), 40(x15)</td>
<td>Out</td>
<td>Chip Select 0. Used to access external memory or I/O devices. This pin has been assigned to “CS” pin on Z84012. This signal is decoded only from A15-A12 without control signals. Refer to “Functional Description” on-chip select signals for further explanation.</td>
</tr>
</tbody>
</table>

## SYSTEM CONTROL SIGNALS (Continued)

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Input/Output, 3-State</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>AC5</td>
<td>40(x13), 42(x15)</td>
<td>Out</td>
<td>Chip Select 1. Used to access external memory or I/O devices. This pin has been assigned to “CT” pin on Z84013. This signal is decoded only from A15-A12 without control signals. Refer to “Functional Description” on-chip select signals for further explanation.</td>
</tr>
<tr>
<td>/WOTOUT</td>
<td>61(x13), 73(x15)</td>
<td>Out</td>
<td>Watchdog Timer Output signal. Output pulse width depends on the externally connected pin.</td>
</tr>
<tr>
<td>/RESET</td>
<td>28(x13), 5(x15)</td>
<td>In</td>
<td>Input (I2C, I2C Open Drain (C13/C15)</td>
</tr>
</tbody>
</table>

Note: For the Z84012/Z84013, the /RESET must be kept in active state for a period of at least three system clock cycles.

Note: For the Z8412/Z8413, during the power-up sequence, the /RESET becomes an Open drain output and the Z8412/C15 will drive this pin to “0” for 25 to 75 ms, after the power supply passes through supply’s LRV and then returns to input. It receives the /RESET signal after power on sequence. If it does not receive /RESET pin for 15 processor clock cycles depending on the status of Reset Input Output (RI) in the Reset Logic. If this Reset output is observed, it must be kept in active state for a period of at least three system clock cycles. Note: When using Z8412/C15 in Z84710/C15 socket, modification may be noted on the internal circuit since this pin is “pull-up input” pin on the Z84012. Also, the /RESET pin does not have internal pull-up resistors and therefore requires external pull-ups. For more details on the device, please refer to “Functional Description.”

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Input/Output, 3-State</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>XTAL1</td>
<td>69(x13), 67(x15)</td>
<td>In</td>
<td>Crystal oscillator connecting terminal. A parallel resonant crystal is recommended. If external clock source is used as an input to the OSC unit, supply clock goes into this terminal. If external clock is supplied by CLKIN pin (without OSC unit), this terminal must be connected to “0” or “1.”</td>
</tr>
<tr>
<td>XTAL2</td>
<td>68(x13), 66(x15)</td>
<td>Out</td>
<td>Crystal oscillator connecting terminal,</td>
</tr>
<tr>
<td>CLKIN</td>
<td>67(x13), 69(x15)</td>
<td>In</td>
<td>Single-phase System Clock Input.</td>
</tr>
<tr>
<td>CLKOUT</td>
<td>66(x13), 68(x15)</td>
<td>Out</td>
<td>Single-phase clock output from on-chip Clock Generator/Controller.</td>
</tr>
<tr>
<td>EV</td>
<td>67(x13), 69(x15)</td>
<td>In</td>
<td>Evaluator signal. When “1” is applied to this pin, PIC is put in Evaluation mode.</td>
</tr>
</tbody>
</table>

Note: For the Z84012, together with /RESET, the EV pin contains the Halt mode evaluation logic. When the signal becomes active, the states of INT0, INT1, and INT2 change to pull-up. When using Z84012 with external clock, the CPU is automatically disconnected after one machine cycle is executed with the INT0 pin “1” and the /RESET input signal “1”. It enables the transitions from the other CPUs (for ROM). Upon receiving RUMPED/AC5, I2C, /RESET, INT0 and INT1 any change in input and EV changes its value when the /RESET or AC5 is NOT 5 seconds or it should be disconnected by an external connected circuit. For details, please refer to “Functional Description” on EV mode.
### SYSTEM CONTROL SIGNALS (Continued)

**Note:** For the Z8413C15, to access on-chip connectors from the CPU such as, ICE CPU, the CPU is electrically disconnected. Address A15-A0, IMEM, CMP, and WM are charged to input 1. If changes its direction. NMI, MAVT, and NRST are put into the high impedance state when the UV pin is set to 0. Also, BUSCHK is 0 voltage. For details, please refer to "Functional Description" on UV mode.

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Input/Output, 3-State</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>ICT</td>
<td>42, 64(013), 40, 62(015), Not with C13/C15</td>
<td>Out</td>
<td>Test pin. Used in the open state.</td>
</tr>
<tr>
<td>NC</td>
<td>24, 27, 67, 68(013), flat with x15</td>
<td></td>
<td>Not connected.</td>
</tr>
<tr>
<td>VCC</td>
<td>43, 84(013), 41, 39(015)</td>
<td>Power Supply</td>
<td>+5 V Volts</td>
</tr>
<tr>
<td>VSS</td>
<td>22, 63(013), 18, 64(015)</td>
<td>Power Supply</td>
<td>0 V Volts</td>
</tr>
</tbody>
</table>

**PIO SIGNALS** (for the Z84x15 only)

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Input/Output, 3-State</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>/ASTB</td>
<td>51(015)</td>
<td>In</td>
<td>Port A strobe pulse from a peripheral device. This signal is used as the handshake between Port A and external circuits. The meaning of this signal depends on the mode of operation selected for Port A (see &quot;PIO Basic Timing&quot;).</td>
</tr>
<tr>
<td>/STB</td>
<td>51(015)</td>
<td>In</td>
<td>Port B strobe pulse from a peripheral device. This signal is used as the handshake between Port B and external circuits. The meaning of this signal is the same as /ASTB, except when Port A is in mode 2 (see &quot;PIO Basic Timing&quot;).</td>
</tr>
<tr>
<td>/RDY</td>
<td>20(015)</td>
<td>Out</td>
<td>Register A ready signal. Used as the handshake between Port A and external circuits. The meaning of this signal depends on the mode of operation selected for Port A (see &quot;PIO Basic Timing&quot;).</td>
</tr>
<tr>
<td>/BRDY</td>
<td>62(015)</td>
<td>Out</td>
<td>Register B ready signal. Used as the handshake between Port B and external circuits. The meaning of this signal is the same as /RDY, except when Port A is in mode 2 (see &quot;PIO Basic Timing&quot;).</td>
</tr>
<tr>
<td>PA7-PA0</td>
<td>20-25(015)</td>
<td>IO, 3-State</td>
<td>Port A data signals. Used for data transfer between Port A and external circuits.</td>
</tr>
<tr>
<td>PB7-PB0</td>
<td>53-60(015)</td>
<td>IO, 3-State</td>
<td>Port B data signals. Used for transfer between Port B and external circuits.</td>
</tr>
</tbody>
</table>

The following pins have different functions between 013/015 and C13/C15

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin # X13</th>
<th>Pin # X15</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>RESET</td>
<td>29</td>
<td>9</td>
<td>Functionality is different.</td>
</tr>
<tr>
<td>WAIT</td>
<td>15</td>
<td>15</td>
<td>Functionality is different.</td>
</tr>
<tr>
<td>EV</td>
<td>55</td>
<td>57</td>
<td>Functionality is different.</td>
</tr>
<tr>
<td>AVDOUT</td>
<td>61</td>
<td>75</td>
<td>Push-pull output on Z84120/015. Open drain on Z8413/15C15</td>
</tr>
<tr>
<td>ICT</td>
<td>45, 40</td>
<td>45, 40</td>
<td>(Test pin) on Z8413/15C15.</td>
</tr>
<tr>
<td>TxC, TxCB, RxA and RxB</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>/N8N4/C4</td>
<td>21</td>
<td>12</td>
<td>In EV mode, state on 3-state on Z8413/15C15. If remaining active on Z84120/015.</td>
</tr>
</tbody>
</table>

**FUNCTIONAL DESCRIPTION**

Figure 5(a) shows the functional block diagram of the Z8413/015 and Figure 5(b) shows the functional block diagram of the Z8413C15. As described earlier, the only difference between the Z84x13 and the Z84x15 is the PIO not being available on the Z84x13.

- **Functionally, the only SIGPIO (not available in Z84x13), CTC, and the Z80 CPU are the same as the derivatives of the same device.** Therefore, for detailed description of each individual unit, refer to the Product Specification Technical Manual of each individual product.
- **The following subsections describe each individual functional unit of the Z8413/015.**

**Z8413C01 Logic Unit**

This unit provides the capabilities and pins of the Z80 CPU (32-bit) with Z80 CPU. Other than existing software, it also has the pin called "MFE" to extend the DMA refresh address to 32-bits. Refer to "Z8413C01 CPU with Z80 CPU".

**Z8413C01 Parallel I/O/Output Logic Unit (Z84x15 Only)**

This logic unit provides both TTL and CMOS-compatible interfaces between peripheral devices and a CPU through the use of two 8-bit parallel ports (Figure 6). The CPU configures the logic interface to be a wide range of peripheral devices with the external logic. Typical devices that are compatible with this interface are keyboards, printers, and EPROM/FAL, PARAGraphs, etc.

| Parallel ports (designated Port A and Port B) are byte wide and completely compatible with the Z6812/01, 812. These two ports have several modes of operation: input, output, bi-directional, or bit control mode. Each port has two handshake signals (RDY and STB) which are used to control data transfers. The RDY (ready) indicates that the port is ready for data transfer, while the STB (strobe) is used to start the data transfer. Each of the ports can be programmed to interrupt the CPU upon the occurrence of specified state conditions, and generate an interrupt vector when the CPU responds. For more information on the operation of this portion of the logic, please refer to the Z8413C01 PIO Product Specification and Technical Manual. |

Z8413C01 Counter/Timer Logic Unit

This logic unit provides the user with four individual 8-bit Counter/Timer Channels that are compatible with the Z8413 CTC (Figure 7). The Counter/Timers can be programmed by the CPU for a broad range of counting and timing applications. Typical applications include event counting, interval, and interval counting, and serial baud rate clock generation.

Each of the Counter/Timer Channels, designated Channels 0-3, have an 8-bit prescaler (when used in timer mode) and an 8-bit counter to provide a wide range of count resolution. Each of the channels has its own Clock/Frequency input to quantize the counting process and an output to indicate zero crossing timeframes. With only one internal vector programmed into the logic unit, each channel can generate a unique interrupt vector in response to the interrupt acknowledge cycle.
28HC4x Serial I/O Logic Unit

The logic unit provides the user with two separate multi-protocol serial I/O channels that are completely compatible with the 28HC4x SIO. Their basic functions as serial-to-parallel and parallel-to-serial converters can be programmed by a CPU for a broad range of serial communications applications. Each channel, designated Channel A and Channel B, is capable of supporting all common synchronous and asynchronous protocols (Manchester, Biwire, and SDLC/DLC, byte or bit oriented - Figure 8).

28HC13/13C15 Only. As an enhancement to the 28HC13/13C15, the 28HC13/13C15 can handle a 32-bit CRC on Channel A and Schmitt-trigger inputs on the TXC and RXC pins of both channels.
Watch Dog Timer (WDT) Logic Unit

This logic unit has been superimposed into the GPC. It detects an operation error, caused by the program runaway, and returns to normal operation. Figure 8 shows the block diagram of the WDT. Upon Power-On Reset (POR), the WDT is not enabled. If WRO is not required, the WDT is connected to the reset circuit, which enables the system clock initially. The WRO pin is the system clock input. The user can connect the WDT to the WRO pin to realize the WDT function. The WRO pin is connected to the system clock, and the WRO output is a pulse that is synchronized with the system clock.

WDT Output (WRO). When the WRO is used, the "0" level signal is output from the WRO pin after a certain period of time after the WRO pin is driven to "1". The output pulse width is determined by the time constant of the RC circuit connected to the WRO pin.

- The WRO pin is connected to the reset pin. The "0" level pulse is generated by the system clock cycle.
- The WRO pin is connected to a pin other than the reset pin. The "0" level pulse is generated by the system clock cycle.

Figure 8. WRO Block Diagram

CGC Logic Unit. The CGC has a clock generator control unit. This unit is identical to the one with the Z80C16 and the Z84C16S, and supports time-out operation. The output from this unit is on the pin called CLKOUT, and it is not connected to the system clock internally. The CLKOUT pin is the input clock pin. The user can connect the CGC to the CLKOUT pin to realize the CGC function. The CGC unit allows the crystal oscillation on the external clock pin (XTAL1, XTAL2) or the external clock input on the XTAL1 pin. It has clock divide-by-two circuits and generates a half-speed clock.

Z84C16S Only. If the system clock is provided on the CLKIN pin, the clock output is also provided on the CLKOUT pin. The clock output is synchronized with the system clock. When the external clock is provided, the CGC unit is selected. If the external clock is provided on the CLKIN pin, the XTAL1 pin is not used (set to "0" or "1") to avoid metastable conditions to minimize power consumption.

Z84C16C15. Clock output is the same, or half, of the external frequency.

System Clock Generation

The system clock can be generated by an external oscillator circuit. The required clock frequency can be generated by an external oscillator circuit. The oscillator circuit can be connected to the XTAL1 and XTAL2 pins. The oscillator circuit can be connected to the XTAL1 and XTAL2 pins. The oscillator circuit can be connected to the XTAL1 and XTAL2 pins. The oscillator circuit can be connected to the XTAL1 and XTAL2 pins. The oscillator circuit can be connected to the XTAL1 and XTAL2 pins. The oscillator circuit can be connected to the XTAL1 and XTAL2 pins. The oscillator circuit can be connected to the XTAL1 and XTAL2 pins.

Figure 9. Block Diagram of Watch Dog Timer

Figure 10. Circuit Configuration For Crystal
Recommended characteristics of the crystal and the values for the capacitor are as follows (the values will change with crystal frequency).  

- **Type of crystal:** Fundamental, parallel type crystal (AT cut is recommended).
- **Frequency tolerance:** Application dependent.
- **C1, Load capacitance:** Approximately 20pf (acceptable range is 25-35pf).
- **Rs, Equivalent series resistance:** ≤ 150 ohms.
- **Driver load:** 100mA (for 10MHz crystal); 50mA (for ≥ 10MHz crystal).

\[ C_0 = f_{osc} + f \]

**Power-On Reset Logic Unit (2B4C13/15 Only)**  
The 2B4C13/15 has the enhanced feature of a Power-On Reset Circuit. During the power-up sequence of the open-drain gate of the on-chip power-on reset circuit drives the \text{RESET pin} to “0” for 25 to 75 ms after the power supply passes through 3V. After the termination of the Power-On Reset cycle, the open-drain gate of the on-chip Power-On Reset circuit stops to drive the \text{RESET pin}. It is required to have external pull-up resistor on the \text{RESET pin}.

If it receives \text{RESET Input} from outside after the power-on sequence and while the Reset Output Enable bit in Misc Control Register is cleared to “0”, it will drive the \text{RESET pin} for 16 processor clock cycles from the falling edge of the external \text{RESET Input}. Otherwise, the \text{RESIN} pin is kept in the active state for a period of at least 3 system clock cycles.

If there are power-on reset circuitry outside of this device, the device should have a pull-up resistor on the \text{RESET pin} to prevent resetting because \text{RESET signal} is driven low for the period mentioned above during the Power-On sequence. If the external Power-On reset circuit has pull-up type drivers and they drive the \text{RESET pin} to “1”, the power-supply may cause damage. In particular, when using 2B4C13/15 in the 2B4013/15 socket, modification may be required on the external reset circuit.

**Wait State Generator Unit (2B4C19/15 Only)**  
The 2B4C13/15 has an enhanced feature of adding two chip select pins (\text{CSS0, CSS1}) pins. Both signals are originally I^2C test pins (CT) on the 2B4013/15. The boundary value for each Chip Select Signal is 4 bits wide, and compare with A15-A12 of the address. Each Chip Select Signal goes active when:

\[ \text{CSS0} = \{ \text{DD0 (CSS0)} \} \land \text{A15-A12} \land \text{CSS1} = \{ \text{DD1 (CSS1)} \} \land \text{A15-A12} \land \text{CSS0} \]  

\( \text{CSS0} = \text{CSS} \) identifies the Chip Select Boundary Register.

**I/O address assignment**  
The I/O of address is assigned to external devices. The registers to control external devices are included to the 2B4013/15, and not assigned on 2B4C13/15.

**Programming**  
I/O address assignment:

The I/O is on-chip peripherals’ I/O addresses are listed in Table 1. They are fully described from AT-2 to AT-7 and have no image. The registers with 2B4C13/15 located at IO Ad-
Table 1. I/O Control Register Addresses

<table>
<thead>
<tr>
<th>Address</th>
<th>Device</th>
<th>Channel</th>
<th>Register</th>
</tr>
</thead>
<tbody>
<tr>
<td>1Ch</td>
<td>CTC</td>
<td>Ch 0</td>
<td>Control Register</td>
</tr>
<tr>
<td>11h</td>
<td>CTC</td>
<td>Ch 1</td>
<td>Control Register</td>
</tr>
<tr>
<td>12h</td>
<td>CTC</td>
<td>Ch 2</td>
<td>Control Register</td>
</tr>
<tr>
<td>13h</td>
<td>CTC</td>
<td>Ch 3</td>
<td>Control Register</td>
</tr>
<tr>
<td>18h</td>
<td>SIO</td>
<td>Ch A</td>
<td>Data Register</td>
</tr>
<tr>
<td>19h</td>
<td>SIO</td>
<td>Ch A</td>
<td>Data Register</td>
</tr>
<tr>
<td>1Ah</td>
<td>SIO</td>
<td>Ch B</td>
<td>Data Register</td>
</tr>
<tr>
<td>1Bh</td>
<td>SIO</td>
<td>Ch B</td>
<td>Data Register</td>
</tr>
<tr>
<td>1Ch</td>
<td>PIO</td>
<td>Port A</td>
<td>Data Register (Not with Z84x13)</td>
</tr>
<tr>
<td>1Dh</td>
<td>PIO</td>
<td>Port A</td>
<td>Command Register (Not with Z84x13)</td>
</tr>
<tr>
<td>1Eh</td>
<td>PIO</td>
<td>Port A</td>
<td>Command Register (Not with Z84x13)</td>
</tr>
<tr>
<td>1Fh</td>
<td>PIO</td>
<td>Port B</td>
<td>Data Register (Not with Z84x13)</td>
</tr>
<tr>
<td>20h</td>
<td>Watch-Dog Timer</td>
<td>Port B</td>
<td>Command Register (Not with Z84x13)</td>
</tr>
<tr>
<td>21h</td>
<td>Watch-Dog Timer</td>
<td>Port B</td>
<td>Master Register (WDTMR)</td>
</tr>
<tr>
<td>22h</td>
<td>Watch-Dog Timer</td>
<td>Port B</td>
<td>Control Register (WDTCR)</td>
</tr>
<tr>
<td>23h</td>
<td>Watch-Dog Timer</td>
<td>Port B</td>
<td>Master Register (WDTMR)</td>
</tr>
<tr>
<td>24h</td>
<td>Watch-Dog Timer</td>
<td>Port B</td>
<td>Control Register (WDTCR)</td>
</tr>
<tr>
<td>25h</td>
<td>Watch-Dog Timer</td>
<td>Port B</td>
<td>Master Register (WDTMR)</td>
</tr>
<tr>
<td>26h</td>
<td>Watch-Dog Timer</td>
<td>Port B</td>
<td>Control Register (WDTCR)</td>
</tr>
<tr>
<td>27h</td>
<td>Watch-Dog Timer</td>
<td>Port B</td>
<td>Master Register (WDTMR)</td>
</tr>
<tr>
<td>28h</td>
<td>Watch-Dog Timer</td>
<td>Port B</td>
<td>Control Register (WDTCR)</td>
</tr>
<tr>
<td>29h</td>
<td>Watch-Dog Timer</td>
<td>Port B</td>
<td>Master Register (WDTMR)</td>
</tr>
<tr>
<td>2Ah</td>
<td>Watch-Dog Timer</td>
<td>Port B</td>
<td>Control Register (WDTCR)</td>
</tr>
<tr>
<td>2Bh</td>
<td>Watch-Dog Timer</td>
<td>Port B</td>
<td>Master Register (WDTMR)</td>
</tr>
<tr>
<td>2Ch</td>
<td>Watch-Dog Timer</td>
<td>Port B</td>
<td>Control Register (WDTCR)</td>
</tr>
</tbody>
</table>

PIO Registers

For more detailed information, please refer to the PIO Technical Manual. These registers are not in the Z84x13.

Interrupt Vector Word

The PIO logic unit is designed to work with the Z80 CPU in interrupt Mode 1. The interrupt word must be programmed if interrupts are used. Bit D0 must be a zero (Figure 11).

Mode Control Word

Selects the port operating mode. The word is required and is written at any time (Figure 12).

Figure 12. PIO Mode Control Word

VO Register Control Word

When Mode 0 is selected, the Mode Control Word is followed by the VO Register Control Word. This word configures the VO register, which defines which ports lines are inputs or outputs. A "1" indicates input while a "0" indicates output. This word is required when in Mode 0 (Figure 13).

Figure 13. VO Register Control Word

Interrupt Control Word

In Mode 3 operation, handshake signals are not used. Interrupts are generated as a logic function of the input signal levels. The Interrupt Control Word sets the logic conditions and the logic levels required for generating an interrupt. Two logic conditions or functions are available: AND (if all input bits change to the active logic level, an interrupt is triggered), OR (if any one of the input bits change to the active logic level, an interrupt is triggered). The user can program which input bits are to be considered as part of this logic function. Bit D3 sets the logic function, bit D2 sets the logic level, and bit D4 specifies a mask control word to follow (Figure 14).

Figure 14. Interrupt Control Word

Interrupt Disable Word

This word can be used to enable or disable a port's interrupts without changing the rest of the port's interrupt conditions (Figure 15).

Figure 15. Mask Control Word
### CTC CONTROL REGISTERS

For more detailed information, refer to the CTC Technical Manual.

**Channel Control Word**

This word sets the operating modes and parameters as described below. Bit 00 is a "1" to indicate that this is a Control Word (Figure 17).

#### Bit D6: Mode Bit

This bit selects either Timer Mode or Counter Mode.

- **0**: Timer Mode
- **1**: Counter Mode

#### Bit D5: Precise Factor

This bit selects the precise factor for use in the timer mode. Either divide-by-16 or divide-by-256 is available.

#### Bit D4: Clock/Trigger Edge Select

This bit selects the active edge of the OCR/TO input pulse.

#### Bit D3: Timer Trigger

This bit selects the trigger mode for timer operation. Either automatic or external trigger may be selected.

#### Bit D2: Time Constant

This bit indicates that the next word programmed is time constant data for the counter.

#### Bit D1: Software Reset

Writing a 1 to this bit indicates a software reset operation, which stops counting activities until another time constant word is written.

**Time Constant Word**

Before a channel starts counting, it must receive a time constant word. The time constant value is anywhere between 1 and 256, with 0 being accepted as a count of 256 (Figure 18).

#### Figure 17. CTC Channel Control Word

```
<table>
<thead>
<tr>
<th>Bit</th>
<th>0</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
</tr>
</thead>
<tbody>
<tr>
<td>D7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>D6</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>D5</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>D4</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>D3</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>D2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>D1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>D0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
```

*Bit 00 Only*

#### Figure 18. CTC Time Constant Word

```
<table>
<thead>
<tr>
<th>Bit</th>
<th>0</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
</tr>
</thead>
<tbody>
<tr>
<td>D7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>D6</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>D5</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>D4</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>D3</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>D2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>D1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>D0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
```

*Time value only*

#### Interrupt Vector Word

If one or more of the CTC channels have Interrupt enabled, then the Interrupt Vector Word must be programmed. Only the lowest significant bits of this word are programmed, and bit 00 must be "0". Bits D2-D1 are automatically modified by the CTC channels which it responds with an interrupt vector (Figure 19).

#### Figure 19. CTC Interrupt Vector Word

```
<table>
<thead>
<tr>
<th>Bit</th>
<th>0</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
</tr>
</thead>
<tbody>
<tr>
<td>D7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>D6</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>D5</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>D4</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>D3</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>D2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>D1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>D0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
```

*Reads data for eight Parallel/Serial programmed*

*Used in special receive condition mode

### SIO REGISTERS

For more detailed information, refer to the SIO Technical Manual.

#### Read Registers

The SIO channel B contains three read registers while channel A contains only two that are read to contain status information. To read the contents of a register (rather than IRQ), the program must first write a pointer to VPO in exactly the same manner as a write operation. The next I/O read cycle will place the contents of the selected read registers onto the data bus (Figure 20a, b, c).

#### Write Registers

The SIO Channel B contains eight write registers while Channel A contains only seven that are programmed to configure the operating mode characteristics of each channel. With the exception of WR0, programming the write registers is a two-step operation. The first operation is a pointer written to WR0 which points to the selected register. The second operation is the actual control word that is written into the register to configure the SIO channel (Figure 21).
**Watch Dog Control Registers**

There are two registers to control Watch Dog Timer operations. These are Watch Dog Timer Master Register (WDTMR, IO Address F0h) and the WDT Command Register (WDTCR, IO Address F1h). Watch Dog Timer Logic has a "double-key" structure to prevent the WDT disabling error, which may lead to the WDT operation to stop due to program runaway. Programming the WDT following this procedure. Also, these registers program the power-down mode of operation. The "Second key" is needed when turning off the Watch Dog Timer.

Enabling the WDT. The WDT is enabled by setting the WDT Enable bit (D7:WDTEN) to "1" and the WDT Periodic field (DS:01:WDTP) to the desired time period. These command bits are in the Watch Dog Timer Master Register (WDTMR, IO Address F0h).

Disabling the WDT. The WDT is disabled by clearing WDT Enable bit (WDTEN) in the WDTMR to "0" followed by writing "01h" to the WDT Command Register (WDTMR, IO Address F1h).

**Figure 21. SIO Write Registers**

- **Register 1**:
  - Rx Enable
  - Sync Character Load Enable
  - Address Search Mode (SDLC)
  - Rx OCP Enable
  - Extra Host Mode
  - Auto Enable
  - Write Ready Function
  - Write Ready Enable
  - Di or special condition

- **Register 2**: (External B Only)
  - Rx Enable
  - Sync Character Load Enable
  - Address Search Mode (SDLC)
  - Rx OCP Enable
  - Extra Host Mode
  - Auto Enable

- **Register 3**: (External B Only)
  - Rx Enable
  - Sync Character Load Enable
  - Address Search Mode (SDLC)
  - Rx OCP Enable
  - Extra Host Mode
  - Auto Enable

- **Register 4**: (Party Enable /Party Event/Out)
  - Tx GPO Enable
  - RTS
  - SDLC Mode 10
  - Tx Enable
  - Send Break

- **Register 5**: (Party Enable)
  - Tx GPO Enable
  - RTS
  - SDLC Mode 10
  - Tx Enable
  - Send Break

* For SDLC 1 must be programmed to "01111110" for flag recognition
Clearing the WDT. The WDT can be cleared by writing "00B" to the WDTCH.

Watch Dog Timer Master Register (WDTMR, I/O address F0H). This register controls the activities of the Watch Dog Timer and selects power-down mode of operation (Figure 22).

Bit D7. Watch Dog Timer Enable (WDET). This bit controls the activities of the Watch Dog Timer. The WDT can be enabled by setting the bit to '1'. To disable WDT, write '0' to this bit followed by writing '01B' to the WDT Command Register. Watch Dog Timer will not generate any interrupt when the WDTMR is enabled. When enabled, WDTMD will be automatically cleared to its initial value of 11B.

Bit D0-D5. WDT Periodic clock (WDTP). These bits determine the expiration period. Upon Power-on reset, this field sets to 11B.

Bit D4-D5. HALT mode (HALTM). This two-bit field specifies one of four power-down modes. To change this field, write '01B' to the WDT command register, followed by a write to this register. For detailed descriptions of this field, please refer to the section "Mode of operations." Upon Power-on Reset, this field is set to 11B, which specifies "RUN mode."

00 - IDLE 1 Mode
01 - IDLE 2 Mode
10 - STOP Mode
11 - RUN Mode

Bit D2-D6. Reserved. These three bits are reserved and should always be programmed as '011'. A read to these bits returns '111'.

Watch Dog Timer Command Register (WDTCR, I/O address F1H). In conjunction with the WDTMR, this register works as a "Second key" to the Watch Dog Timer. This register is writable only (Figure 23).

Write 01B after clearing WDT to '0'. Disable WDT. Write 45B - Clear WDT. Write 01B followed by a write to HALTM - Change Power-down mode.

InterruptPriority Register (NTPR, I/O address F4H)

This register (write only) is provided to determine the interrupt priority for the GTO, SIG and the PIC (Figure 24).

<table>
<thead>
<tr>
<th>0</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>01</td>
<td>02</td>
<td>03</td>
<td>04</td>
</tr>
<tr>
<td>05</td>
<td>06</td>
<td>07</td>
<td>08</td>
<td>09</td>
</tr>
<tr>
<td>10</td>
<td>11</td>
<td>12</td>
<td>13</td>
<td>14</td>
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<tr>
<td>15</td>
<td>16</td>
<td>17</td>
<td>18</td>
<td>19</td>
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<tr>
<td>20</td>
<td>21</td>
<td>22</td>
<td>23</td>
<td>24</td>
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<td>25</td>
<td>26</td>
<td>27</td>
<td>28</td>
<td>29</td>
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<td>30</td>
<td>31</td>
<td>32</td>
<td>33</td>
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<td>41</td>
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<td>45</td>
<td>46</td>
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<td>48</td>
<td>49</td>
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<td>51</td>
<td>52</td>
<td>53</td>
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<td>58</td>
<td>59</td>
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<tr>
<td>60</td>
<td>61</td>
<td>62</td>
<td>63</td>
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<tr>
<td>65</td>
<td>66</td>
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<td>68</td>
<td>69</td>
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<tr>
<td>70</td>
<td>71</td>
<td>72</td>
<td>73</td>
<td>74</td>
</tr>
<tr>
<td>75</td>
<td>76</td>
<td>77</td>
<td>78</td>
<td>79</td>
</tr>
</tbody>
</table>

Bit D7-D3. Unused

Bit D2-D6. This field specifies the order of the interrupt priority. Upon Power-on Reset, this field is set to '0000'.

Bit D0-D1. Reserved

System Control Data Port (SCDP, I/O address E0H)

System Control Data Port Register

System Control Data Port Register (SCDP, I/O address E0H)

This register is to access WCR, MBWR, CSBR and WCR (Figure 25).

System Control Data Port Register

System Control Data Port Register (SCDP, I/O address E0H)

This register is to access WCR, MBWR, CSBR and WCR (Figure 26).

Wall State Control Register (WCR, Control Register 00H)

This register can be accessed through SCDP with the power-on value 02H in SCDP (Figure 27). To maintain compatibility with the Z84C13C15, the Z84C13C15 inserts the maximum number of wait states (set 8 bytes of this register to write) for 16MHz system clock operation. It automatically clears the contents of this register (move to no wait state insertion) on the falling edge of the 16MHz clock unless it has programmed a value. If automatic wait state insertion is enabled, the wall state is programmed for wait state periods. A read to WCR during this period will return 0FH, unless programmed.
### Wait State Control Register

This register has the following fields:

- **Interrupt Acknowledge (IACK):**
  - 00: No Wait states
  - 01: 2 Wait states
  - 10: 4 Wait states
  - 11: 6 Wait states

- **RetI cycle:**
  - 00: No Wait states
  - 01: 1 Wait states
  - 10: 2 Wait states
  - 11: 3 Wait states

- **Interrupt Daisy Chain Wait:**
  - 00: No Wait states
  - 01: 1 Wait states
  - 10: 2 Wait states
  - 11: 4 Wait states

For fifteen M1 cycles from Power-on Reset, bits 7-6 are set to "11." They clear to "00" on the trailing edge of the 16th M1 signal unless programmed.

- **Bit 5, Interrupt Vector Wait:**
  - When this bit is set to one, the wait state generator inserts one wait state after the IORQ signal goes active during the Interrupt acknowledge cycle. This gives more time for the vectors read cycle. While this bit is cleared to zero, no wait state is inserted (standard timing). For fifteen M1 cycles from Power-on Reset, this bit is set to "11," then cleared to "00" on the trailing edge of the 16th M1 signal, unless programmed.

- **Bit 4, Opcode Fetch Extension:**
  - If this bit is set to "1," one additional wait state is inserted during the Opcode fetch cycle in addition to the number of wait states programmed in the Memory Wait field. For fifteen M1 cycles from Power-on Reset, this bit is set to "11," then cleared to "00" on the trailing edge of the 16th M1 signal, unless programmed.

- **Bit 3-2, Memory Wait Status:**
  - This 2-bit field specifies the number of wait states to be inserted during memory READ/ WRITE transactions.

  - 00: No Wait states
  - 01: 1 Wait states
  - 10: 2 Wait states
  - 11: 3 Wait states

For fifteen M1 cycles from Power-on Reset, these bits are set to "11," then cleared to "00" on the trailing edge of the 16th M1 signal, unless programmed.

- **Bit 1-0, I/O Wait Status:**
  - This 2-bit field specifies the number of wait states to be inserted during I/O transactions.

  - 00: No Wait states
  - 01: 1 Wait states
  - 10: 2 Wait states
  - 11: 3 Wait states

For fifteen M1 cycles from Power-on Reset, these bits are set to "11," then cleared to "00" on the trailing edge of the 16th M1 signal, unless programmed. For the accesses to the on-chip I/O registers, no wait states are inserted regardless of the programming of this field.

### Memory Wait Boundary Register (MWBR, Control Register 01h)

This register specifies the address range to insert memory wait states. When accessed memory addresses are within this range, the Memory Wait State generator inserts Memory Wait States specified in the Memory Wait field of the NOR (Figure 28).

### Chip Select Boundary Register (CSBR, Control Register 02h)

This register specifies the address range for each chip select signal. When accessed memory addresses are within this range, chip select signals are active (Figure 29).

### Misc Control Register (MCR, Control Register 03h)

This register specifies miscellaneous options on this device (Figure 30).

---

**Figure 27. Wait State Control Register**

**Figure 28. Memory Wait Boundary Register**

**Figure 29. Chip Select Boundary Register**

**Figure 30. Misc Control Register**
Table 2. Power-down Modes

<table>
<thead>
<tr>
<th>Operation Mode</th>
<th>WDTMR Bit D4</th>
<th>Bit D3</th>
<th>Description at HALT State</th>
</tr>
</thead>
<tbody>
<tr>
<td>RUN Mode</td>
<td>1</td>
<td>1</td>
<td>The I/O continues the operation and continuously supplies a clock to the outside.</td>
</tr>
<tr>
<td>IDLE1 Mode</td>
<td>0</td>
<td>0</td>
<td>The internal oscillator operation is continued. Clock output (CLKOUT) as well as internal clock to the CPU, PIO, SIO, CTC and the Watch Dog Timer is stopped at &quot;0&quot; level of T4 state in the halt instruction operation code fetch cycle.</td>
</tr>
<tr>
<td>IDLE2 Mode</td>
<td>0</td>
<td>1</td>
<td>The internal oscillator and the CTC operation continues and supplies clock to the outside on the CLKOUT pin continuously. But the internal clock to the CPU, PIO, SIO and the Watch Dog Timer is stopped at &quot;0&quot; level of T4 state in the halt instruction operation code fetch cycle.</td>
</tr>
<tr>
<td>STOP Mode</td>
<td>1</td>
<td>0</td>
<td>All operations of the internal oscillator, clock (CLK) output, internal clock to CPU, PIO, CTC, SIO and the Watch Dog Timer are stopped at &quot;0&quot; level of T4 state in the halt instruction operation code fetch cycle.</td>
</tr>
</tbody>
</table>

Table 3. Device status in Hal state

<table>
<thead>
<tr>
<th>Mode</th>
<th>CTC</th>
<th>CPU</th>
<th>PIO</th>
<th>SIO</th>
<th>WDT</th>
<th>CLKOUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>IDLE1</td>
<td>O</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>IDLE2</td>
<td>O</td>
<td>O</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>O</td>
</tr>
<tr>
<td>STOP</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>RUN</td>
<td>O</td>
<td>O</td>
<td>O</td>
<td>O</td>
<td>O</td>
<td>O</td>
</tr>
</tbody>
</table>

Operation When HALT Instruction is Executed: When the CPU fetches a halt instruction in the operation code fetch cycle, (HALT goes active Low) in sync with the falling edge of T4 state before the peripheral LSIs and CPU stops the operation. After this, the system clock generation differs depending upon the operation mode (RUN Mode, IDLE1 Mode or STOP Mode). If the internal system clock is running, the CPU continues to execute NOP instruction even in the HALT state.

RUN Mode (HALT = 1): Shown in Figure 31 the basic timing when the halt instruction is executed in RUN Mode.

TIMING

Basic Timing

The basic timing is explained here with emphasis placed on the halt function relative to the clock generator. The following terms are identical to those for the Z80400. Refer to the data sheet for the Z80400.

- Operation code fetch cycle
- Memory Read/Write operation
- Input/Output operation
- Bus request/acknowledge operation
- Maskable interrupt request operation
- Non-Maskable interrupt request operation
- Reset Operation

Figure 31. Timing of RUN Mode

(at HALT Instruction Command Execution)
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