GPC® 154
General Purpose Controller 84C15

TECHNICAL MANUAL
**GPC® 154**

*General Purpose Controller 84C15*

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**CPU 84C15** with **20 MHz** clock rate; **2 RS 232** serial lines one of which settable in RS 422 or RS 485(SIO); one 8 bit timer counter (CTC); 16 software manageable TTL I/O lines (PIO); 1 watch dog; 512K EPROM or FLASH EPROM; 512K RAM; Real Time Clock; serial EEPROM; 2 LEDs available for user indications; **ABACO® I/O BUS** interface; **back up** circuit for **32K RAM**, through on-board **LITHIUM** battery; designed for low consumptions; 100x50 mm size; format **DIN 46277-1** and **3 rails** compliant.
IMPORTANT

Although all the information contained herein have been carefully verified, grifo® assumes no responsibility for errors that might appear in this document, or for damage to things or persons resulting from technical errors, omission and improper use of this manual and of the related software and hardware.

grifo® reserves the right to change the contents and form of this document, as well as the features and specification of its products at any time, without prior notice, to obtain always the best product.

For specific informations on the components mounted on the card, please refer to the Data Book of the builder or second sources.

SYMBOLS DESCRIPTION

In the manual could appear the following symbols:

⚠️ Attention: Generic danger

⚠️ ⚡ Attention: High voltage

Trade Marks

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INTRODUCTION

The use of these devices has turned - IN EXCLUSIVE WAY - to specialized personnel.

The purpose of this handbook is to give the necessary information to the cognizant and sure use of the products. They are the result of a continual and systematic elaboration of data and technical tests saved and validated from the manufacturer, related to the inside modes of certainty and quality of the information.

The reported data are destined- IN EXCLUSIVE WAY- to specialized users, that can interact with the devices in safety conditions for the persons, for the machine and for the environment, impersonating an elementary diagnostic of breakdowns and of malfunction conditions by performing simple functional verify operations, in the height respect of the actual safety and health norms.

The informations for the installation, the assemblage, the dismantlement, the handling, the adjustment, the reparation and the contingent accessories, devices etc. installation are destined - and then executable - always and in exclusive way from specialized warned and educated personnel, or directly from the TECHNICAL AUTHORIZED ASSISTANCE, in the height respect of the manufacturer recommendations and the actual safety and health norms.

The devices can't be used outside a box. The user must always insert the cards in a container that respect the actual safety normative. The protection of this container is not threshold to the only atmospheric agents, but specially to mechanic, electric, magnetic, etc. ones.

To be on good terms with the products, is necessary guarantee legibility and conservation of the manual, also for future references. In case of deterioration or more easily for technical updates, consult the AUTHORIZED TECHNICAL ASSISTANCE directly.

To prevent problems during card utilization, it is a good practice to read carefully all the informations of this manual. After this reading, the user can use the general index and the alphabetical index, respectly at the begining and at the end of the manual, to find information in a faster and more easy way.

CARD VERSION

The present handbook is reported to the GPC® 154 card release 100997 and later. The validity of the bring informations is subordinate to the number of the card release. The user must always verify the correct correspondence among the two denotations. On the card the release number is present in more points both board printed diagram (serigraph) and printed circuit (for example near the microprocessor on the component side).
GENERAL FEATURES

GPC® 154 board is a powerful control low cost module capable of operating in stand alone mode or as an intelligent peripheral, and/or remoted, in a wider telecontrol or acquisition network. It is part of the CPU Serie 4, in BLOCK format, as low as 100x50 mm size. The GPC® 154 module can be secured in a plastic mount for connection to Omega rails DIN 46277-1 and DIN 46277-3, thereby dispensing with the need of a rack and allowing a less costly mounting direct to the electrical control panel. Thanks to this small size, the GPC® 154 put into the same plastic rails that contains the peripheral I/O, i.e ZBR 168, forms an unique BLOCK element. The GPC® 154 can also be mounted as a macro CPU module on a peripheral card of the end user, in Piggy Back (stack through) mode. The powerful and easy-to-use ROM-based FGDOS Operating System makes easy to program the board and to take advantage of its many resources. FGDOS supports high level languages like BASIC, PASCAL, C and so on, places at user's disposal all the memory resources as ROM/RAM Disks, allowing an immediate high-level use of these devices, manages PCMCIA RAM Cards through the MCI 64 board and on-board serial EEPROMs directly. In addition, FGDOS manages directly LCDs, fluorescent displays and a matrix keyboard. The KDL-224 serie boards allow an immediate use of these devices management features, while the QTP24P Operator Panel represents a valid low-cost solution to integrate display and keyboard in a single object. This Panel, offered in open frame version, has the same esthetics of QTP24 but can be controlled directly by GPC® 154 because it is designed to work without an on-board controller. FGDOS can also write the user program in a FLASH memory without need of external hardware.

This card it is also equipped with a serie of helpful ABACO® standard pin out connectors. Thanks to these connectors it is very easy to be interfaced to the field by using BLOCK I/O modules or adopting any user's card duly designed for this purpose.

For getting a quick prototype, cards such as SPA 03 and SPA 04 on which it is possible to mount the GPC® 324 in Piggy Back mode, are used. The presence on board of the ABACO® I/O BUS connector, allows to drive directly I/O cards as: ZBR 84, ZBR 168, ZBR 246, ZBR 324, ZBT 84, ZBT 168, ZBT 246, ZBT 324 and so on, and through ABB 03, ABB 05 it is possible to manage all the peripheral cards available on Abaco® BUS.

- Intelligent Modul of the Abaco® BLOCK serie, 100x50 mm size
- Optional plastic mount for connection to DIN 46277-1 and DIN 46277-3 Ω rails
- CPU Z84C15, with 20 MHz crystal
- Up to 512K of EPROM or FLASH and up to 512K of RAM. Through FGDOS memory exceeding 64K is available as RAM/ROM Disk. The user program can delete and reprogram the on-board FLASH memory without need of external hardware
- Back-up circuit for RAM, through on-board and external LITHIUM battery
- INT generation capable Real Time Clock
- Up to 8K of serial EEPROM and RUN/DEBUG Mode Jumper
- 16 TTL I/O lines, software bit-settable managed by the internal PIO
- 1 or 2 user available CTC channel capable of impulse count
- 2 RS232 serial lines, one of which settable as RS422 or RS485
- Double software settable Baud rate generator, up to 38.400 Baud
- Hardware excludable Watch-Dog circuit
- Abaco® I/O BUS 26 pins expansion connector
- One I/O Abaco® 20 pins connector
- Low-Power Halt Mode, Idle Mode, Stop Mode
- Only one 5 Vdc, 110 mA external power supply
- On-board logic protected against transients by TransZorb™
- Wide range of development software available: Remote Symbolic Debugger, Macro Assembler, GET 80, BASIC Compiler, FORTH, Compilatore C, HTC-80, Lisp, Compilatore PASCAL, etc.

Here follows a description of the board's functional blocks. To easily locate these block and to check their interconnections please refer to figure 1.

**ON-BOARD CPU**

The GPC® 154 board is designed to use the ZILOG Z84C15 microprocessor. It is an 8 bit, Z80 code compatible CPU provided with a wide instruction set (158), high speed in instructions execution and data manipulation, an efficient vectorized interrupt management. Mostly important is the presence of these devices inside the microprocessor:

- 16 bit-settable INT- generation capable I/O lines (PIO);
- Four 8 bit Timer Counter, with programmable prescaler (CTC);
- 2 asynchronous or synchronous serial lines provided with handshake signals (SIO);
- Watch Dog Timer;
- Wait state generator;
- Programmable Clock frequency;
- Interrupt controller;
- Idle Mode and Stop Mode to minimize the consumptions.

For further informations please refer to manufacturer documentation or Appendix B in this manual.

**MEMORY DEVICES**

On the card can be mounted up to 1032K of memory divided with a maximum of 512K Byte EPROM or FLASH EPROM, 512K Byte RAM an 8K Byte serial EEPROM. The memory configuration must be chosen considering the application to realize or the specific requirements of the user. Normally the card is provided with 128K RAM and 512 bytes of serial EEPROM, all different configurations must be specified from the user, at the moment of the order. By means of the on-board back-up circuit and the external battery, memory can keep data also in absence of power supply. The addressing of memory devices is controlled by a specific on-board control logic, that provides to allocate the devices in the microprocessor address space. For further informations about memory configuration, sockets description and jumpers connection, please refer to chapter "HARDWARE", "PERIPHERAL DEVICES SOFTWARE DESCRIPTION" and to the paragraph "MEMORY SELECTION".

**DIGITAL I/O LINES**

The Z84C15 CPU incorporates a PIO which manages two 8 bits wide parallel ports providing in all16 TTL I/O lines each one settable as direction. The lines are connected to an ABACO® I/O standard connector and are capable to generate interrupts. Taking advantage of this feature means to be able to interrupt the CPU when a particular condition occurs and promptly manage the situation. A specific control logic allows the complete programming of the internal PIO by using four registers mapped in the CPU I/O space.
SERIAL COMMUNICATION

The serial communication lines are completely software configurable and independent for protocol and speed (from 150 to 38400 Baud). These settings are made by programming the Z84C15 inside SIO and the Baaaud rate generation section, implemented through CTC, Timer 2 for serial A and Timer 3 for serial B, so for further informations please refer to the manufacturer documentation or to appendix B of this manual. By hardware it is possible to select the physical communication protocol through a set of comfortable jumpers. One serial line is always buffered in RS 232, while the other serial line can be buffered in RS 232, RS 485 or RS 422; for this last case it is also possible to select between Full Duplex or Half Duplex communication mode.

CONTROL LOGIC

The addresses of all peripheral device's registers and of memory devices on GPC® 154 are assigned from a specific control logic that allocates all these devices in the microprocessor addressing space. For further information please refer to chapter "ADDRESSES AND MAPS" of this manual.

MEMORY MANAGEMENT UNIT

A specific MMU section has been designed to manage in a practical and efficient way the memory configurations that the GPC® 154 board can assume. The use is provided with a 64K work area, which can be easily allocated anywhere in the 1024K maximum memory space.

ABACO® I/O BUS

One of the most important features of GPC® 154 is its possibility to be interfaced to industrial ABACO® I/O BUS. Thanks to its standard ABACO® I/O BUS connector, the card can be connected to some of the numerous grifo® boards, both intelligent and not. For example the user can directly use cards for analog signals acquisition (A/D like ABC 04 or ABB 08), cards for analog signals generation (D/A), cards for digital I/O signals management, cards with timers and counters, cards for temperature controls, etc. also custom boards designed to satisfy specific needs of the end user. Using ABB 03 or ABB 05 mother boards it is possible manage all the BUS ABACO® single EURO cards. So GPC® 154 becomes the right component for each industrial automation system, in fact ABACO® I/O BUS makes the card easily expandable with the best price/performance ratio.

REAL TIME CLOCK

GPC® 154 has installed on-board a Real Time Clock capable of a completely autonomous management of hours, minutes, seconds, day of month, month, year and day of week. The device is completely software programmable by 16 registers mapped in the CPU I/O space and is supplied by a back-up circuitry which warrants the validity of its data in any operating condition. In addition RTC section is capable to generate periodic interrupts, for example to wake the CPU away from halt, idle or stop conditions.
FIGURE 1: BLOCK DIAGRAM

- CPU 84c15
- DRIVERS: RS232, RS232, RS422-485
- CN3A SERIAL LINE A
- CN3B SERIAL LINE B
- IC8 SERIAL EEPROM
- CN2 EXTERNAL LITHIUM
- SIO
- PIO
- CTC
- 16 I/O LINES CTC CHANNEL 1 CN5
- ABACO® I/O BUS CN1
- IC7 RTC
- IC6 RAM
- IC3 EPROM FLASH
- CONTROL LOGIC
- 3V LITHIUM ON BOARD
WATCH DOG

GPC® 154 is provided with a watch dog circuit that can be used to exit from endless loops or to reset anomalous conditions not estimated by the application program. There is a monostable section inside the microprocessor with programmable intervention time which can also be used to generate periodic interrupts acting on an opportune jumper. The Watch Dog is completely software manageable by a set of registers mapped on the CPU addressing space and grants to the system an extremely high safety rank.

POWER SUPPLY

The only power supply voltage needed by the board is +5 Vdc which must be provided by pin 25 (GND) and 26 (+5Vdc) on CN1. The board takes advantage of componentistic and circuit choices intended to reduce the consumption and noise sensitivity, including the feature, for some microcontrollers, to work in power down and idle mode. We also would want to remark that a TransZorb™ circuitry is present to protect the board against voltage peaks.

COUNTER TIMER

The on-board CTC section consists of the CTC device included inside the microprocessor. This device provides four 8-bit independent and software programmable channels, it can operate as timer or counter, capable of interrupt generation, with prescaler trigger etc. by acting upon 4 registers mapped into the I/O space. Channels 2 and 3 are used as baud rate generators for the serial lines while channels 0 and 1 are available to the user, in particular channel 0 as timer and channel 1, connected also to the connector CN5, as timer or counter.

RESET CONTACT

P1 reset contact of the GPC® 154 board allows the user to reset the board and restarting it in a general clearing condition. The main purpose of this contact is to come out of infinite loop conditions, useful especially during debug or to grant a particular initial state. Please see figure 21 for an easy localization of this contact.

CLOCK

The GPC® 154 has an on-board circuit that generates the CPU clock frequency (19.660 MHz) and, through a CTC channel, also the Baud Rate frequency is generated, up to a maximum of 38400 Baud.
TECHNICAL FEATURES

GENERAL FEATURES

On board resources:
- 16 TTL programmable input/output (PIO)
- 4 TTL 8 bits timer counter (CTC)
- 1 RS 232 serial input/output (SIO)
- 1 RS 232 or RS 422-485 serial input/output (SIO)
- 1 reset contact (P1)
- 2 software manageable LEDs
- 1 monostable software watch dog
- 1 real time clock (RTC)
- 1 ABACO® I/O BUS interface

Addressable memory:
- IC 3: EPROM from 128K x 8 to 512K x 8
- FLASH EPROM from 128K x 8 to 512K x 8
- IC 6: RAM from 128K x 8 to 512K x 8
- IC 8: Serial EEPROM from 256 byte to 8K byte

CPU:
- ZILOG 84C15

Clock frequence:
- 19.660 MHz

Watch dog intervent time:
- 6÷419 msec

PHYSICAL FEATURES

Size (W x H x D):
- 100x 50x25 mm (without plastic container)
- 110x 60x60 mm (with plastic container)

Weight:
- 70 g (without plastic container)
- 110 g (with plastic container)

Connectors:
- CN1: 26 pins low profile vertical M
- CN2: 2 pins low profile vertical M
- CN3A: 6 pins plug
- CN3B: 6 pins plug
- CN5: 20 pins low profile vertical M

Temperature range:
- from 0 to 50 Centigrad degrees

Relative humidity:
- 20% up to 90% (without condense)
ELECTRIC FEATURES

Power supply: 5 Vdc ±5% (through CN1)

Consumption on 5 Vdc: 115 mA

Back up external battery: 3,6÷5 Vdc

Back up current: 15 µA

RS422-485 termination network: line termination 120Ω
pull-up on positive 3,3KΩ
pull-down on negative 3,3KΩ
In this chapter there are the information for a right installation and correct use of the card. The user can find the location and functions of each connectors, jumpers and some explanatory diagrams.

CONNECTIONS

The GPC®154 module has 4 connectors that can be linkeded to other devices or directly to the field, according to system requirements. In this paragraph there are connectors pin out, a short signals description (including the signals direction) and connectors location (see figure 14).

CN2 - BACK UP EXTERNAL BATTERY CONNECTOR

CN2 is a 2 pins, vertical, male connector with 2,54mm pitch. Through CN2 the user can connect an external battery for RAM and RTC back up when the power supply is switched off (for further information please refer to chapter "BACK UP").

Signals description:

<table>
<thead>
<tr>
<th>Signal</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>+Vbat</td>
<td>Back up external battery positive pin</td>
</tr>
<tr>
<td>GND</td>
<td>Back up external battery negative pin</td>
</tr>
</tbody>
</table>
CN3A - SERIAL LINE A CONNECTOR

CN3A is a 6 pins, female PLUG connector for serial communication. Placing of the signal has been designed to reduce interference and electrical noise and to simplify connections with other systems, while the electric protocol follows the CCITT normative.

![CN3A - Serial Line A Connector Diagram]

**Figure 3: CN3A - Serial Line A Connector**

Signals description:

- **RxDA RS 232** = I - RS 232 Receive Data on serial line A.
- **TxDA RS 232** = O - RS 232 Transmit Data on serial line A.
- **CTSA RS 232** = I - RS 232 Clear To Send on serial line A.
- **RTSA RS 232** = O - RS 232 Request To Send on serial line A.
- **+5 Vdc/GND** = - +5 Vdc power supply or ground signal
- **GND** = Ground signal
**Figure 4: Serial Communication Diagram**

- **RS 422**
- **RS 485**
- **RS 232**
- **CTC 2**
- **CTC**
- **CTC 3**
- **LINE A**
- **LINE B**
- **BAUD RATE LINE B**
- **BAUD RATE LINE A**
- **C N 3 A**
- **C N 3 B**
CN3B is a 6 pins, female PLUG connector for serial RS 232, RS 422, RS 485 communication. Placing of the signal has been designed to reduce interference and electrical noise and to simplify connections with other systems, while the electric protocol follows the CCITT normative.

![CN3B Connector Diagram]

**FIGURE 5: CN3B - SERIAL LINE B CONNECTOR**

Signals description:

- **RXB- RS 422-485** = I - Receive Data Negative: negative line for RS 422-485 serial differential receive on serial line B.
- **RXB+ RS 422-485** = I - Receive Data Positive: positive line for RS 422-485 serial differential receive on serial line B.
- **TXB- RS 422** = O - Transmit Data Negative: negative line for RS 422-485 serial differential transmit on serial line B.
- **TXB+ RS 422** = O - Transmit Data Positive: positive line for RS 422-485 serial differential transmit on serial line B.
- **RxDB RS 232 / TXDB RS 232** = I - RS 232 Receive Data on serial line B.
- **TxDB RS 232** = O - RS 232 Transmit Data on serial line B.
- **CTSB RS 232** = I - RS 232 Clear To Send on serial line B.
- **RTSB RS 232** = O - RS 232 Request To Send on serial line B.
- **+5 Vdc/GND** = - +5 Vdc power supply or ground signal
- **GND** = Ground signal

**NOTE:** CTS and RTS handshake signals must be connected, that is, it is not possible for physical reasons to acquire for certain by software their status if they are not connected to another serial transmission system.
FIGURE 6: RS 232 POINT TO POINT CONNECTION EXAMPLE

FIGURE 7: RS 422 POINT TO POINT CONNECTION EXAMPLE

FIGURE 8: RS 485 POINT TO POINT CONNECTION EXAMPLE
Figure 9: RS 485 network connection example
CN1 - ABACO® I/O BUS CONNECTOR

CN1 is a 26 pins, male, vertical, low profile connector with 2,54mm pitch. Through CN1 the card can be connected to some of the numerous grifo® boards, both intelligent and not. All this connector signals are at TTL level.

![Diagram of CN1 - ABACO® I/O BUS CONNECTOR](image)

**Signals description:**

- **A0-A7** = O - Address BUS.
- **D0-D7** = I/O - Data BUS.
- **/INT** = I - Interrupt request (open collector type).
- **/NMI** = I - Non maskable interrupt.
- **/IORQ** = O - Input output request.
- **/RD** = O - Read cycle status.
- **/WR** = O - Write cycle status.
- **/RESET** = O - Reset.
- **+5 Vdc** = I/O - +5 Vdc power supply.
- **GND** = I/O - Ground signal.
- **N.C.** = - Not connected.
CN5 - PIO AND CTC 1 I/O CONNECTOR

CN5 is a 20 pins low profile vertical male connectors, 2.54 mm pitch. Through CN5 the two 8 bits parallel ports of the on board programmable input/output (PIO) peripheral can be connected to the external world. The signals of the first CTC channel are also present.
All signals are at TTL level and follow the standard I/O Abaco® pin-out.

**FIGURE 11: CN5 - PIO AND CTC 1 I/O CONNECTOR**

Signals description:

- PIO PA.n = I/O - n-th digital signal of PIO port A
- PIO PB.n = I/O - n-th digital signal of PIO port A
- CLK/TR1 = I - Clock Trigger of CTC channel 1
- ZC/TO1 = O - Zero Count Timer Out of CTC counter 1
- +5 Vdc = O - +5 Vcc power supply
- GND = - Ground signal
- N.C. = - Not connected
FIGURE 12: DIGITAL I/O SIGNALS CONNECTION DIAGRAM
DIGITAL I/O INTERFACES

Through CN5 (I/O Abaco® standard connector) the GPC® 154 card can be connected to all of the numerous grifo® boards featuring the same standard pin out. Installation of these interface is very easy; in fact only a 20 pins flat cable is required, while the software management of these interfaces is as easy; in fact most of the software packages available for GPC® 154 card are provided with the necessary procedures. These latter ones are "software drivers" that are added to the programming language and allow to use directly high-level instructions with all their power.

Remarkable modules are:

- **QTP 24P, KDL x24, KDF 224, DEB 01**, etc. that solve all the local operator interfacing problems. These modules are provided with all the resources needed to obtain a high-level human-machine interface (they feature alphanumeric displays, matrix keyboard and visualization LEDs) at a short distance from GPC® 154 card. The available software drivers allow to manage the operator interface resources directly through the high-level instructions for console management.

- **MCI 64**: it a large mass memory support that can directly manage the PCMCIA memory cards RAM, FLASH, ROM, etc.) in their available sizes. About software the developed drivers provide a complete file system interfacing allowing to access the informations stored in the memory card directly through the high-level file management instructions.

- **IAC 01, DEB 01**: it is an interface for CENTRONICS parallel printer that can be connected with a standard printer cable. The printer is managed by software through the high level instructions of the selected programming language (LPRINT for BASIC, PRINTF for C, etc.).

- **RBO xx, TBO xx, XBI xx, OBI xx**: these are buffer interfaces for I/O TTL signals. With these modules the the TTL input signals are converted in NPN or PNP optoisolated inputs and the TTL output signals are converted in relays or transistor optoisolated outputs.

For further informations please refer to "EXTERNAL CARDS" chapter and the software tools documentation.

VISUAL SIGNALATIONS

GPC® 154 board is provided with two LEDs in order to signal to the user some internal status conditions, as described in the following table:

<table>
<thead>
<tr>
<th>LEDs</th>
<th>COLOUR</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>LD1</td>
<td>Green</td>
<td>Signals the connection of J7 in 1-2 position, leading /SYNCB to status &quot;low&quot;, meaning RUN mode</td>
</tr>
<tr>
<td>LD2</td>
<td>Yellow</td>
<td>Signals the connection of J7 in 2-3 position, leading /SYNCB to status &quot;high&quot;, meaning DEBUG mode</td>
</tr>
</tbody>
</table>

**Figure 13: Visual signalations table**

The main purpose of this LED is to provide the user a visual indication of the board status, making easier the operations to verify the correct working of the system. To easily locate the LED on the board please see figure 17.
Figure 14: LEDs, Connectors, etc. Location
I/O CONNECTION

To prevent possible connecting problems between GPC® 154 and the external systems, the user has to read carefully the information of the previous paragraphs and he must follow these instructions:

- For RS 232, RS 422 and RS485 communication signals the user must follow the standard rules of these protocols.
- For all TTL signals the user must follow the rules of this electric standard. The connected digital signal must be always referred to card digital ground. For TTL signals, the 0 Vdc level corresponds to logic state "0", while 5Vdc level corresponds to logic state "1".

JUMPERS

On GPC® 154 there are 13 jumpers for card configuration. Connecting these jumpers, the user can define for example the memory type and size, the peripheral devices functionality and so on. Below there is the jumpers list, location and function:

<table>
<thead>
<tr>
<th>JUMPERS</th>
<th>PINS</th>
<th>MEANING</th>
</tr>
</thead>
<tbody>
<tr>
<td>J3</td>
<td>4</td>
<td>Selects connection of watch dog, /INT and reset</td>
</tr>
<tr>
<td>J4</td>
<td>3</td>
<td>Selects memory device size for IC4</td>
</tr>
<tr>
<td>J5</td>
<td>2</td>
<td>Connects the real time clock interrupt section</td>
</tr>
<tr>
<td>J6</td>
<td>2</td>
<td>Sets the handshake /DCDB signal status used employed as generic User input</td>
</tr>
<tr>
<td>J7</td>
<td>3</td>
<td>Sets the handshake SYNCB signal status, to select between RUN or DEBUG mode</td>
</tr>
<tr>
<td>J8</td>
<td>5</td>
<td>Selects memory device size for IC3</td>
</tr>
<tr>
<td>JS1, JS2</td>
<td>2</td>
<td>Connect the termination and forcing resistor to the reception signal in RS 422, RS 485</td>
</tr>
<tr>
<td>JS3</td>
<td>3</td>
<td>Selects the connection for pin 1 of CN3A</td>
</tr>
<tr>
<td>JS4</td>
<td>3</td>
<td>Selects the connection for pin 1 of CN3B</td>
</tr>
<tr>
<td>JS11</td>
<td>2</td>
<td>Sets the handshake /CTSB signal status</td>
</tr>
<tr>
<td>JS14</td>
<td>2</td>
<td>Connects the on board lithium battery BT1 to the back up circuitry</td>
</tr>
<tr>
<td>JS15</td>
<td>5</td>
<td>Selects the communication type for serial line B between RS 422 and RS 485</td>
</tr>
</tbody>
</table>

**Figure 15: Jumpers summarizing table**

The following tables describe all the right connections of GPC® 154 jumpers with their relative functions. To recognize these valid connections, please refer to the board printed diagram (serigraph) or to figure 17 of this manual, where the pins numeration is listed; for recognizing jumpers location, please refer to figure 19.
FIGURE 16: CARD PHOTO

FIGURE 17: COMPONENTS MAP (COMPONENT SIDE AND SOLDER SIDE)
### 2 PINS JUMPERS

<table>
<thead>
<tr>
<th>JUMPER</th>
<th>CONNECTION</th>
<th>MEANING</th>
<th>DEF.</th>
</tr>
</thead>
<tbody>
<tr>
<td>J5</td>
<td>not connected</td>
<td>It does not connect the CPU /INT interrupt signal to the Real Time Clock section</td>
<td></td>
</tr>
<tr>
<td></td>
<td>connected</td>
<td>It connects the CPU /INT interrupt signal to the Real Time Clock section</td>
<td>*</td>
</tr>
<tr>
<td>J6</td>
<td>not connected</td>
<td>It connects SIO /DCDB signal to +Vcc, setting a logic state &quot;1&quot;</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>connected</td>
<td>It connects SIO /DCDB signal to GND, setting a logic state &quot;0&quot;</td>
<td></td>
</tr>
<tr>
<td>JS1</td>
<td>not connected</td>
<td>Matching with JS2, it does not connect the forcing and termination circuitry to serial line B in RS 422-485</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>connected</td>
<td>Matching with JS2, it connects the forcing and termination circuitry to serial line B in RS 422-485</td>
<td></td>
</tr>
<tr>
<td>JS2</td>
<td>not connected</td>
<td>Matching with JS1, it does not connect the forcing and termination circuitry to serial line B in RS 422-485</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>connected</td>
<td>Matching with JS1, it connects the forcing and termination circuitry to serial line B in RS 422-485</td>
<td></td>
</tr>
<tr>
<td>JS11</td>
<td>not connected</td>
<td>It does not change /CTSB signal.</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>connected</td>
<td>Connects SIO /CTSB signal to GND, setting a logic state &quot;0&quot; when IC10 is not installed.</td>
<td></td>
</tr>
<tr>
<td>JS14</td>
<td>not connected</td>
<td>It does not connect the on board battery BT1 to the back up circuitry.</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>connected</td>
<td>It connects the on board battery BT1 to the back up circuitry.</td>
<td></td>
</tr>
</tbody>
</table>

**Figure 18: 2 pins jumpers table**

The "*" used in the following tables, denotes the default connection, or on the other hand the connection set up at the end of testing phase, that is the configuration the User receives.
FIGURE 19: JUMPERS LOCATION
3 PINS JUMPERS

<table>
<thead>
<tr>
<th>JUMPERS</th>
<th>CONNECTION</th>
<th>MEANING</th>
<th>DEF.</th>
</tr>
</thead>
<tbody>
<tr>
<td>J4</td>
<td>position 1-2</td>
<td>Sets IC 6 for 128K Byte RAM</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>position 2-3</td>
<td>Sets IC 6 for 512K Byte RAM</td>
<td></td>
</tr>
<tr>
<td>J7</td>
<td>position 1-2</td>
<td>Connects SIO /SYNCB signal to GND, activating LD1 and selecting RUN mode</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>position 2-3</td>
<td>Connects SIO /SYNCB signal to +5 Vcc, activating LD2 and selecting DEBUG mode</td>
<td></td>
</tr>
<tr>
<td>JS3</td>
<td>position 1-2</td>
<td>Connects pin 1 of CN3A to GND</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>position 2-3</td>
<td>Connects pin 1 of CN3A to +5 Vcc</td>
<td></td>
</tr>
<tr>
<td>JS4</td>
<td>position 1-2</td>
<td>Connects pin 1 of CN3B to GND</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>position 2-3</td>
<td>Connects pin 1 of CN3B to +5 Vcc</td>
<td></td>
</tr>
</tbody>
</table>

**Figure 20: 3 pins jumpers table**

4 AND 5 PINS JUMPERS

<table>
<thead>
<tr>
<th>JUMPER</th>
<th>CONNECTION</th>
<th>MEANING</th>
<th>DEF.</th>
</tr>
</thead>
<tbody>
<tr>
<td>J3</td>
<td>position 1-2</td>
<td>Connects the internal watch dog circuitry to the CPU /INT signal</td>
<td></td>
</tr>
<tr>
<td></td>
<td>position 2-3</td>
<td>Connects the internal watch dog circuitry to the reset network</td>
<td></td>
</tr>
<tr>
<td></td>
<td>position 3-4</td>
<td>Manual reset, must not keep connected</td>
<td></td>
</tr>
<tr>
<td>J8</td>
<td>position 1-2 and 3-4</td>
<td>Sets IC3 for EPROM</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>position 2-3 and 4-5</td>
<td>Sets IC3 for FLASH EPROM</td>
<td></td>
</tr>
<tr>
<td>JS15</td>
<td>position 1-2 and 3-4</td>
<td>Enables RS 485 (2 wires half duplex) on serial line B</td>
<td></td>
</tr>
<tr>
<td></td>
<td>position 2-3 and 4-5</td>
<td>Enables RS 485 (4 wires full or half duplex) on serial line B</td>
<td></td>
</tr>
</tbody>
</table>

**Figure 21: 4 and 5 pins jumpers table**

The "*" used in the following tables, denotes the default connection, or on the other hand the connection set up at the end of testing phase, that is the configuration the User receives.
BACK UP

GPC® 154 has an on-board lithium battery BT1 for the back up of RAM and RTC content when power supply is switched off. Jumper JS14 connects physically the battery so it can be disconnected to save its duration whenever back-up is not needed. By CN2 connector it is possible to connect an external battery: configuration of jumper JS14 does not affect the working of this battery and it can replace BT1 completely. Please refer to the paragraph “ELECTRIC FEATURES” to choose the type of the external back-up battery, to easily locate see figure 17.

SERIAL COMMUNICATION SELECTION

Serial line A can be buffered only as RS 232 while serial line B can be buffered in RS 232, RS 422 or RS 485. By hardware can be selected which one of these electric standards is used, through jumpers connection (as described in the previous tables) and drivers installation. By software the serial line can be programmed to operate with all the standard physical protocols, in fact the bits per character, parity, stop bits and baud rates can be decided by setting opportunes CPU internal registers. In the following paragraphs there are all the informations on serial communication configurations; please note that jumpers which are not mentioned below do not affect the serial communication whatever their configuration is.

- RS 232 SERIAL LINE B
  MAX 202 serial driver must be installed on IC10, while on IC11, IC12, no driver must be installed.

- RS 485 SERIAL LINE B
  SN75176 serial driver must be installed on IC12, while no driver must be installed on IC 10 and IC11. Jumper JS15 must be connected in position 1-2 and 3-4. With /RTSB signal, the user can select by software the line direction, pins 4 and 5 of CN3B become transmission or reception lines, according the status of /RTSB signal (0=low=transmission, 1=high=reception). This kind of serial communication can be used for multi-point connections, in addition it is possible to listen to own transmission, so the user is allowed to verify the success of transmission. In fact, any conflict on the line can be recognized by testing the received character after each transmission.

- RS 422 SERIAL LINE
  SN75176 serial drivers must be installed on IC11 and IC12 while no driver must be installed on IC10. Jumper JS15 must be connected in position 2-3 and 4-5. /RTSB signal can be kept always low (active transmitter) for point-to-point connections, while for multi-point connections the transmitter must be activated only before the transmission (/RTSB =0=low=transmitter activated and vice versa). If using the RS 422-485 serial line, it is possible to connect the terminating and forcing circuit on the line by using JS1 and JS2, it is also needed to connect J11 to enable /CTSB. This circuit must be always connected in case of point-to-point connections, while in case of multi-point connections it must be connected only in the farthest boards, that is on the edges of the communication line. To easily locate of jumpers and serial drivers please refer to appendix A.
MEMORY SELECTION

On GPC® 154 can be mounted up to 1032K bytes of memory divided in several configurations, as described in the following table:

<table>
<thead>
<tr>
<th>IC</th>
<th>DEVICE</th>
<th>SIZE</th>
<th>CONNECTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>EPROM</td>
<td>128K÷512KByte</td>
<td>J8 in position 1-2 and 3-4</td>
</tr>
<tr>
<td></td>
<td>FLASH EPROM</td>
<td>128K÷512KByte</td>
<td>J8 in position 2-3 and 4-5</td>
</tr>
<tr>
<td>6</td>
<td>RAM</td>
<td>128K Byte</td>
<td>J4 in position 1-2</td>
</tr>
<tr>
<td></td>
<td>RAM</td>
<td>512K Byte</td>
<td>J4 in position 2-3</td>
</tr>
<tr>
<td>8</td>
<td>EEPROM</td>
<td>256÷8K Byte</td>
<td></td>
</tr>
</tbody>
</table>

**Figure 22: Memory selection table**

All the above described devices must feature a JEDEC compliant pin out except for the serial EEPROM installed on IC 8 that must be requested to grifo® in the ordering phase. To determin the name of the memory devices that can be mounted, please refer to the manufacturer documentation. To easily locate the memory devices on the board please refer to figure 17.

INTERRUPTS

A remarkable feature of GPC® 154 card is the powerful interrupt management. Here follows a short description of which devices can generate interrupts and their modalities; for further informations about interrupts management please refer to the microprocessor data sheet or to the appendix B of this manual.

- **ABACO® I/O BUS** -> Generates normal /INT and /NMI, without regard for the daisy chain priority.
- **SIO** -> Generates normal or vectored /INT, respecting the daisy chain priority.
- **PIO** -> Generates normal or vectored /INT, respecting the daisy chain priority.
- **CTC** -> Generates normal or vectored /INT, respecting the daisy chain priority.
- **Internal Watch dog** -> Generates normal /INT if J3 is connected in position 1-2, without regard for the daisy chain priority.
- **Real Time Clock RTC**-> Generates normal /INT, without regard for the daisy chain priority.

The daisy chain on the GPC® 154 board is made only of SIO, PIO and CTC and can be software programmed through one of the microprocessor internal registers. This way the User can always respond promptly and efficiently to any external event, also deciding the priority to assign to the several event sources.
RESET AND WATCH DOG

GPC® 154 board is provided with a watch dog circuitry very efficient and easy to manage. Its specifications are:

— microprocessor inside circuitry;
— monostable working mode;
— software programmable intervent time;
— software and hardware abilitation;
— software retrigger;

Please remark that, in monostable working mode, when the intervent time is expired, the watch dog circuitry activates until the next Power On or reset.

Also, amongst the several GPC® 154/RESET sources, in addition to the eventual watch dog, there are always the jumper J3 connected in position 3-4 and the power good circuitry.
SOFTWARE DESCRIPTION

A wide selection of software development tools can be obtained, allowing use of the module as a system for its own development, both in assembler and in other high level languages; in this way the User can easily develop all the requested application programs in a very short time. Generally all software packages available for the mounted microprocessor, or for the Z80 family, can be used:

GET 80
It is a complete program with Editor, Communication driver, and Mass Memory management for all Z80 family cards. This program, developed by grifo®, allows to operate in the best conditions when GDOS, FGDOS or xGDOS MCI software tools are used; GET 80 is supplied when one of these tools is ordered and it is personalized with name and general data of the customer. A useful list of pull down menus and the possibility of using mouse, make program use very comfortable. GET 80 program can be executed both on MS-DOS system and on MACINTOSH computers too, through SOFT-PC program. It is supplied on MS-DOS 3”1/2 floppy disk with the documentation on GDOS 80 manual.

GDOS 154
It is a complete development Tool for GPC® 154 card. It is supplied together with GET 80 program to allow an easy and immediate use of this powerful development system. GDOS is divided in two different structures : the first one works on PC maintaining serial communication with the second one. The second structure is on EPROM, it works on board of the card and it is an efficient operating system that executes many low level functions and, at the same time, it allows high level language use. The combination of the said structures results in a complete machine, in fact the card uses PC resources (like floppy disk, hard disk, printer, keyboard, monitor, etc.) as its own peripheral devices. This resulting “virtual machine” performs operation in a transparent way for the User, so this latter can operate with the same modality of standard PC languages. It is really interesting the compatibility of GDOS with all CP/M program and languages; so, if the User has experience, knowledge or developed applications with CP/M, he can use immediately GDOS, without any changes. Moreover, GDOS can manage all memory devices exceeding 64K Bytes as RAM disk and ROM disk. The on board RAM devices can directly be used performing data read and write operations with the confortable file formats.
This software tools is supplied on EPROM with MS-DOS GET 80 floppy disk, some examples, utilities and the operating system documentation.

FGDOS 154
It is really similar to GDOS, but it can program and erase the on board FLASH EPROM with the application program developed from the User. In this way the external EPROM programmer is not necessary to store definitely the program and it is possible to modify or to add code directly on the installed machine, through a portable PC.
This software tools is supplied on FLASH EPROM with MS-DOS GET 80 floppy disk, some examples, utilities and the operating system documentation.

NOICE
It is a PC hosted debugger consists of a target specific DOS program, NOICExxx.EXE, and a target resident monitor program. The two programs comunicate via RS 232. NOICE includes: source level debug; a disassembler; a file viewer; memory display and editing; a virtually unlimited number of breakpoints; hardware free single step; definition of symbols; the ability to record and play back files of commands; on line help.
xGDOS MCI 154
It is a version of GDOS or FGDIS software tools, capable of PCMCIA Memory Card management. Using MCI 64 card, the GDOS operating system manages memory cards as RAM disk or ROM disk. All applications with data acquisition and data logging can be realized with high level languages that manage data on files, with a fast development time and without any software complication. This software tool is supplied on EPROM or FLASH EPROM with MS-DOS GET 80 floppy disk, some examples, utilities and the operating system documentation.

CBZ-80
It is a Basic Compiler that generates a really compact and fast code. It must work together with any GDOS version and it can exceed the 64K memory limits of Z80 family microprocessors through CHAIN modality. More than one application program can be saved in RAM and/or ROM disks and subsequently executed. In conjunction to the powerful GET 80 Editor the CBZ 80 program becomes a comfortable and really efficient development system for any kind of application program. This program is supplied as ROM DISK file in GDOS EPROM or FLASH EPROM and on MS-DOS floppy disk with some exaples and manual.

PASCAL 80
It is an efficient and complete PASCAL Compiler for Z80 family cards, with features similar to Release 3.0 of Borland Turbo PASCAL. It must work together with any GDOS version and it can exceed the 64K memory limits of Z80 family microprocessors through OVERLAY modality. More than one application program can be saved in RAM and/or ROM disks and subsequently executed. The terminal emulation of GET 80 program support the typical full screen PASCAL Editor, including the attributes management. This program is supplied as ROM DISK file in GDOS EPROM or FLASH EPROM and on MS-DOS floppy disk with some exaples and manual.

RSD 154
This software tools is a Remote Symbolic Debugger with two operating mode. The first one is a monitor debugger modality with software emulation on P.C.; the second is a remote monitor debugger modality that execute code directly on the card. Trough serial communication the User can: download an HEX file and associated symbol table, debug code in symbolic mode, execute code in step to step mode or in real time mode, set breakpoint, dump and modify memory and registers, etc. RSD software tool supports both Z80 and Z180 instruction sets. Really interesting is the program execution management, in fact many hardware and software breakpoint are supported. RSD can be used together with assembler tools, like ZASM 80, and C Compiler CC 80. It is supplied on EPROM and on MS-DOS floppy disk with technical manual.

ZASM 80
It is a macro cross assempler that operates on any PC with MS-DOS operating system. It supports both Z80 and Z180 instruction sets. The generated code can be debugged on PC, through software simulation, or directly on target card, through remote modality, using RSD software tools. ZASM 80 is compatible with C Compiler CC 80 of which it assemble the compilation result. It is supplied on MS-DOS floppy disk with technical manual.
It is a complete **C Compiler** with ANSI/ISO standard, provided of floating point procedure, that can generate code for Z80 and Z180 family microprocessors. It works together with cross assembler **ZASM 80** and Symbolic Debugger **RSD**.

It is supplied on MS-DOS floppy disk with technical manual.

**HI TECH C 80**

Professional C Cross Compiler of Hi-Tech Software Inc. This Compiler is terribly fast and it generates a small quantity of code. This result is due to advanced techniques in optimizing the generated code based on Artificial Intelligence techniques which allow to get a very compact and very fast code. The package includes: IDE, Compiler, Code optimizer, Assembler, Linker, Remote Debugger and so on. This tool is Full ANSI/ISO Standard and Full Library Source Code. Once the porting of the Remote-Debugger module is done, this tool allows the user the software debugging directly on the hardware that he is experimenting. This type of specialization of the **Remote Debugger** is available from now ant it is supplied with all **grifo**® CPU cards. This software package is on 3” 1/2 diskettes under MS-DOS format along with user manual. This version supports these following CPUs: Z80, Z180, 84C011, 84C11, 84C013, 80C13, 84C015, 84C15, 64180, NCS800, Z181, Z182.

**DDS MICRO C 85**

Low cost ross compiler for C source program. It is a powerful software tool that includes editor, C compiler (integer), assembler, optimizer, linker, library, and remote debugger, in one easy to use integrated development environment. There are also included the library sources and many utilities programs.
ADDRESSES AND MAPS

INTRODUCTION

In this chapter are reported all information about card use, related to hardware and software. For example, the registers addresses and the memory allocation are described below.

ON BOARD RESOURCES ALLOCATION

The card devices addresses are managed by a specific control logic, realized with programmable logic devices. This control logic allocates RAM, EPROM and peripheral devices in a comfortable way for the user.

The control logic is able to manage separately Input/Output peripherals and on board memory. CPU 84C15 is capable to address directly 64K Byte of memory and 256 I/O addresses, the control logic provides on board memory and peripheral devices allocation inside the 1032K Byte address space.

The maps management is completely driven by software through the MMU circuit programmation: the used memory can be selected and divided in 32K Byte size segments. About I/O maps the control logic avoids every conflicts problems between CPU internal and external peripherals.

Summarizing the control logic allocates:

- **ABACO® I/O BUS**
  - Up to 512K Byte of EPROM or FLASH EPROM installed on IC 3
  - Up to 512K Byte of RAM installed on IC 6
  - Up to 8K Byte of serial EEPROM, installed on IC 8
- SIO
- CTC
- PIO
- MMU circuitry

The addresses of all these devices are described in the following paragraphs and can't be set with different values. If some different specific maps are required, please contact directly grifo®.
I/O ADDRESSES

The on board control logic manages the allocation of all the peripheral devices registers in the microprocessor I/O space, that is 256 bytes long. Next table shows names, addresses, meanings and directions of peripheral device registers (including the internal microprocessor ones).

<table>
<thead>
<tr>
<th>DEV.</th>
<th>REG.</th>
<th>ADD.</th>
<th>R/W</th>
<th>MEANING</th>
</tr>
</thead>
<tbody>
<tr>
<td>CTC</td>
<td>CTC0</td>
<td>10H</td>
<td>R/W</td>
<td>Data status register of channel 0</td>
</tr>
<tr>
<td></td>
<td>CTC1</td>
<td>11H</td>
<td>R/W</td>
<td>Data status register of channel 1</td>
</tr>
<tr>
<td></td>
<td>CTC2</td>
<td>12H</td>
<td>R/W</td>
<td>Data status register of channel 2</td>
</tr>
<tr>
<td></td>
<td>CTC3</td>
<td>13H</td>
<td>R/W</td>
<td>Data status register of channel 3</td>
</tr>
<tr>
<td>SIO</td>
<td>RDA</td>
<td>18H</td>
<td>R/W</td>
<td>Serial line A data register</td>
</tr>
<tr>
<td></td>
<td>RSA</td>
<td>19H</td>
<td>R/W</td>
<td>Serial line A status register</td>
</tr>
<tr>
<td></td>
<td>RDB</td>
<td>1AH</td>
<td>R/W</td>
<td>Serial line B data register</td>
</tr>
<tr>
<td></td>
<td>RSB</td>
<td>1BH</td>
<td>R/W</td>
<td>Serial line A status register</td>
</tr>
<tr>
<td>PIO</td>
<td>PAD</td>
<td>1CH</td>
<td>R/W</td>
<td>Port A data register</td>
</tr>
<tr>
<td></td>
<td>PAS</td>
<td>1DH</td>
<td>W</td>
<td>Port A control register</td>
</tr>
<tr>
<td></td>
<td>PBD</td>
<td>1EH</td>
<td>R/W</td>
<td>Port B data register</td>
</tr>
<tr>
<td></td>
<td>PBS</td>
<td>1FH</td>
<td>W</td>
<td>Port B control register</td>
</tr>
</tbody>
</table>

**Figure 23: I/O addresses table - Part 1**

For a detailed description of the registers function, please refer to next chapter "PERIPHERAL DEVICES SOFTWARE DESCRIPTION".
<table>
<thead>
<tr>
<th>DEV.</th>
<th>REG.</th>
<th>ADD.</th>
<th>R/W</th>
<th>MEANING</th>
</tr>
</thead>
<tbody>
<tr>
<td>Real Time</td>
<td>SEC1</td>
<td>20H</td>
<td>R/W</td>
<td>Units of seconds data register</td>
</tr>
<tr>
<td>Clock</td>
<td>SEC10</td>
<td>21H</td>
<td>R/W</td>
<td>Tens of seconds data register</td>
</tr>
<tr>
<td></td>
<td>MIN1</td>
<td>22H</td>
<td>R/W</td>
<td>Units of minutes data register</td>
</tr>
<tr>
<td></td>
<td>MIN10</td>
<td>23H</td>
<td>R/W</td>
<td>Tens of minutes data register</td>
</tr>
<tr>
<td></td>
<td>HOU1</td>
<td>24H</td>
<td>R/W</td>
<td>Units of hours data register</td>
</tr>
<tr>
<td></td>
<td>HOU10</td>
<td>25H</td>
<td>R/W</td>
<td>Tens of hours and AM/PM register</td>
</tr>
<tr>
<td></td>
<td>DAY1</td>
<td>26H</td>
<td>R/W</td>
<td>Units of day data register</td>
</tr>
<tr>
<td></td>
<td>DAY10</td>
<td>27H</td>
<td>R/W</td>
<td>Tens of day data register</td>
</tr>
<tr>
<td></td>
<td>MON1</td>
<td>28H</td>
<td>R/W</td>
<td>Units of month data register</td>
</tr>
<tr>
<td></td>
<td>MON10</td>
<td>29H</td>
<td>R/W</td>
<td>Tens of month data register</td>
</tr>
<tr>
<td></td>
<td>YEAI</td>
<td>2AH</td>
<td>R/W</td>
<td>Units of year data register</td>
</tr>
<tr>
<td></td>
<td>YEAI0</td>
<td>2BH</td>
<td>R/W</td>
<td>Tens of year data register</td>
</tr>
<tr>
<td></td>
<td>WEE</td>
<td>2CH</td>
<td>R/W</td>
<td>Day of week data register</td>
</tr>
<tr>
<td></td>
<td>REGD</td>
<td>2DH</td>
<td>R/W</td>
<td>D control register</td>
</tr>
<tr>
<td></td>
<td>REGE</td>
<td>2EH</td>
<td>R/W</td>
<td>E control register</td>
</tr>
<tr>
<td></td>
<td>REGF</td>
<td>2FH</td>
<td>R/W</td>
<td>F control register</td>
</tr>
<tr>
<td></td>
<td>.......</td>
<td>30H-3FH</td>
<td>R/W</td>
<td>Repetition of the above registers</td>
</tr>
</tbody>
</table>

| M.M.U.       | MEM  | 40H-5FH | W   | MMU circuitry setting register               |
| ABACO® I/O BUS| I/O BUS | 60H-DFH | R/W | ABACO® I/O BUS addresses                     |

<table>
<thead>
<tr>
<th>INTERN. REG.</th>
<th>SCRP</th>
<th>EEH</th>
<th>R/W</th>
<th>Microprocessor internal registers addressing register</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>SCDP</td>
<td>EFH</td>
<td>R/W</td>
<td>Microprocessor internal registers data register</td>
</tr>
</tbody>
</table>

| INTERN. W. D. | WDTMR | F0H | R/W | Internal watch dog programming register               |
|               | WDTMR | F1H | W   | Internal watch dog access register                    |

| INTERRU. | INTPR | F4H | W   | Interrupt priority setting register                   |

**Figure 24: I/O addresses table - Part 2**
MEMORIES MAPPING

The total 1032K Byte of memory supported by the card are divided this way:

Up to 512K Byte of EPROM or 512K Byte of FLASH EPROM allocated in the memory space
Up to 512K Byte of RAM allocated in the memory space
Up to 8K Byte of serial EEPROM allocated in the I/O space

GPC® 154 can directly manage no more than 64K bytes of memory that is the microprocessor logic addressable space. On the board this logic space can be divided in two 32K Byte pages: both RAM and EPROM can be installed on the low page, while only RAM can be installed on the high page.

MMU circuitry, driven through a simple software management, takes care to divide the addressable space in 32K Byte pages and to make them available directly into the CPU addressing space. It is possible to address indirectly a memory area much greater than the area normally accessible by the CPU just programming the MEM register. Here follow two figures that show the possible memory devices configurations, for further informations please refer to the paragraph "MEMORY MANAGEMENT UNIT", while to easily locate the memory deviced refer to figure 17.

Some software packages, like GDOS, are capable to manage in autonomy the MMU circuitry to make address in the CPU addressable memory area all the available memory without bothering the User.

**Figure 25: Memory Mapping with R/E=0**

![Diagram of memory mapping with R/E=0](image-url)
When a reset or a Power On occur the R/E signal is set to 0, so the board starts to execute the code stored at the logic address 0000H page 0 of EPROM installed on IC 3.

**ABACO® I/O BUS ADDRESSES**

The **GPC® 154** control logic defines **ABACO® I/O BUS addresses** and only these addresses must be used to manage correctly the BUS. As described in figure 24 "I/O ADDRESSES" table, only the addresses from 60H to DFH are available for **ABACO® I/O BUS**. Any I/O operations at each one of these addresses enables the /IORQ signal and the other control signals of CN1 connector.
PERIPHERAL DEVICES SOFTWARE DESCRIPTION

In the previous paragraphs are described the external registers addresses, while in this one there is a specific description of registers meaning and function (please refer to I/O addresses table, for the registers names and addresses values). For a more detailed description of the devices, please refer to manufacturing company documentation; for microprocessor internal peripheral devices, not described in this paragraph, refer to appendix B. In the following paragraphs the D7÷D0 indication denotes the eight bits of the combination used in I/O operations.

MEMORY MANAGEMENT UNIT

An efficient MMU circuitry takes care to allocate in the CPU addressing space all the memory devices that can be installed on GPC® 154. This section can be programmed through the MEM register, which is allocated in the I/O addressing space. The bits of MEM register have the following meaning:

MEM:

- D7  ->  not used
- D6  ->  not used
- D5  ->  R/E: selector for RAM (D5=1) or EPROM/FLASH EPROM (D5=0), in the CPU addressing space low page (0000H÷7FFFH)
- D4  ->  A18 x IC 3 and /A18 x IC 6
- D3  ->  A17 x IC 3 and /A17 x IC 6
- D2  ->  A16 x IC 3 and /A16 x IC 6
- D1  ->  A15 x IC 3
- D0  ->  /A15 x IC 6

Only bits D0÷D5 decide the RAM installed on IC 6 page or EPROM/FLASH EPROM installed on IC 3 page that must be addressed.

When a reset or a Power On occur all the bits of MEM register are reset (all bits 0); this means to program the MMU section where the low 32K Bytes page consists of page 0 EPROM/FLASH EPROM installed on IC 3 and the high 32K Bytes page consists of page 0 RAM installed on IC 6. Please refer to the following table, also remembering figures 25 and 26, for an overview of all the possible MMU section configurations.
**Figure 27: Possible MMU section configurations table**

"X" means non significant bit, that is that bit can be "1" or "0" without influencing the setting there described.

<table>
<thead>
<tr>
<th>32K LOW PAGE</th>
<th>32K HIGH PAGE</th>
<th>MEM REGISTER</th>
</tr>
</thead>
<tbody>
<tr>
<td>0: IC 3</td>
<td>0: IC 6</td>
<td>XX000000B = 00H</td>
</tr>
<tr>
<td>1: IC 3</td>
<td>0: IC 6</td>
<td>XX000010B = 02H</td>
</tr>
<tr>
<td>2: IC 3</td>
<td>0: IC 6</td>
<td>XX000100B = 04H</td>
</tr>
<tr>
<td>3: IC 3</td>
<td>0: IC 6</td>
<td>XX000110B = 06H</td>
</tr>
<tr>
<td>4: IC 3</td>
<td>0: IC 6</td>
<td>XX001000B = 08H</td>
</tr>
<tr>
<td>5: IC 3</td>
<td>0: IC 6</td>
<td>XX001010B = 0AH</td>
</tr>
<tr>
<td>6: IC 3</td>
<td>0: IC 6</td>
<td>XX001100B = 0CH</td>
</tr>
<tr>
<td>7: IC 3</td>
<td>0: IC 6</td>
<td>XX001110B = 0EH</td>
</tr>
<tr>
<td>8: IC 3</td>
<td>0: IC 6</td>
<td>XX010000B = 10H</td>
</tr>
<tr>
<td>9: IC 3</td>
<td>0: IC 6</td>
<td>XX010100B = 12H</td>
</tr>
<tr>
<td>10: IC 3</td>
<td>0: IC 6</td>
<td>XX010100B = 14H</td>
</tr>
<tr>
<td>11: IC 3</td>
<td>0: IC 6</td>
<td>XX011000B = 16H</td>
</tr>
<tr>
<td>12: IC 3</td>
<td>0: IC 6</td>
<td>XX011000B = 18H</td>
</tr>
<tr>
<td>13: IC 3</td>
<td>0: IC 6</td>
<td>XX011100B = 1AH</td>
</tr>
<tr>
<td>14: IC 3</td>
<td>0: IC 6</td>
<td>XX011100B = 1CH</td>
</tr>
<tr>
<td>15: IC 3</td>
<td>0: IC 6</td>
<td>XX1111X1B = 3DH</td>
</tr>
<tr>
<td>0: IC 6</td>
<td>0: IC 6</td>
<td>XX1111X0B = 3CH</td>
</tr>
<tr>
<td>1: IC 6</td>
<td>0: IC 6</td>
<td>XX1110X1B = 39H</td>
</tr>
<tr>
<td>2: IC 6</td>
<td>0: IC 6</td>
<td>XX1110X0B = 38H</td>
</tr>
<tr>
<td>3: IC 6</td>
<td>0: IC 6</td>
<td>XX1101X1B = 35H</td>
</tr>
<tr>
<td>4: IC 6</td>
<td>0: IC 6</td>
<td>XX1101X0B = 34H</td>
</tr>
<tr>
<td>5: IC 6</td>
<td>0: IC 6</td>
<td>XX1100X1B = 31H</td>
</tr>
<tr>
<td>6: IC 6</td>
<td>0: IC 6</td>
<td>XX1100X0B = 30H</td>
</tr>
<tr>
<td>7: IC 6</td>
<td>0: IC 6</td>
<td>XX1011X1B = 2DH</td>
</tr>
<tr>
<td>8: IC 6</td>
<td>0: IC 6</td>
<td>XX1011X0B = 2CH</td>
</tr>
<tr>
<td>9: IC 6</td>
<td>0: IC 6</td>
<td>XX1010X1B = 29H</td>
</tr>
<tr>
<td>10: IC 6</td>
<td>0: IC 6</td>
<td>XX1010X0B = 28H</td>
</tr>
<tr>
<td>11: IC 6</td>
<td>0: IC 6</td>
<td>XX1001X1B = 25H</td>
</tr>
<tr>
<td>12: IC 6</td>
<td>0: IC 6</td>
<td>XX1001X0B = 24H</td>
</tr>
<tr>
<td>13: IC 6</td>
<td>0: IC 6</td>
<td>XX1000X1B = 21H</td>
</tr>
<tr>
<td>14: IC 6</td>
<td>0: IC 6</td>
<td>XX1000X0B = 20H</td>
</tr>
<tr>
<td>15: IC 6</td>
<td>0: IC 6</td>
<td>XX1000X0B = 20H</td>
</tr>
</tbody>
</table>
BAUD RATE GENERATOR

The SIO frequencies generation section is capable to generate two separated baud rates that can vary in the range 150 Baud ÷ 38400 Baud, picking the seven most common used values. **GPC® 154** ccard allows to set the communication speeds performing a simple output instruction to the CTC2 and CTC3 I/O addresses. In fact timer counters 2 and 3 of microprocessor CTC section are used to generate the baud rate respectively for serial line A and B.

To make the CTC channels operate as baud rate generators it is essential to program them as described here:

- Give a channel reset command = output to CTCn control register the value 03H.
- Give a channel control word that: disables interrupt, selects timer mode, sets 16 for prescaler, selects a descending front, activates automatic trigger and loads a time constant = output to CTCn control register the value 05H.
- Load the time constant corresponding to the baud rate required = output to CTCn control register the value indicated by the following table.

<table>
<thead>
<tr>
<th>BAUD RATE</th>
<th>TIME CONSTANT</th>
</tr>
</thead>
<tbody>
<tr>
<td>150 Baud</td>
<td>00H</td>
</tr>
<tr>
<td>300 Baud</td>
<td>80H</td>
</tr>
<tr>
<td>600 Baud</td>
<td>40H</td>
</tr>
<tr>
<td>1200 Baud</td>
<td>20H</td>
</tr>
<tr>
<td>2400 Baud</td>
<td>10H</td>
</tr>
<tr>
<td>4800 Baud</td>
<td>08H</td>
</tr>
<tr>
<td>9600 Baud</td>
<td>04H</td>
</tr>
<tr>
<td>19200 Baud</td>
<td>02H</td>
</tr>
<tr>
<td>38400 Baud</td>
<td>01H</td>
</tr>
</tbody>
</table>

**Figure 28: Baud rate time constants table**

All CTC channels are disabled after a reset or a Power On, and so the baud rate generators.
For further informations please refer to the proper paragraph of Appendix B in this manual.

**SIO**

For further informations please refer to the proper paragraph of Appendix B in this manual.

**PIO**

For further informations please refer to the proper paragraph of Appendix B in this manual.

**CTC**

For further informations please refer to the proper paragraph of Appendix B in this manual.
INTERNAL WATCH DOG

For further informations please refer to the proper paragraph of Appendix B in this manual.

SERIAL EEPROM

For informations about the management of serial EEPROM module installed on IC 8, please refer to the documentation of the software package used to program the board. This technical manual reports no further informations about the serial EEPROM management because this activity employs a very deep knowledge of the device itself. For this, its complete management is affordable through the high level instructions of the software package being used.

REAL TIME CLOCK

This peripheral is allocated in 16 consecutives I/O addresses, 3 of which correspond to status registers while the remaining 13 are for datas. Data registers are used both for read operations (of the current time and date) and write operations (to initialize the time and date) just like the status registers which are used in write operations (to program the operative mode) and in read operations (to acquire the RTC status). Here follows a list of the RTC data registers’ meanings:

- **SEC1** - Units of seconds - 4 least significant bits of SEC1.3÷SEC1.0
- **SEC10** - Decines of seconds - 3 least significant bits of SEC10.2÷SEC10.0
- **MIN1** - Units of minutes - 4 least significant bits of MIN1.3÷MIN1.0
- **MIN10** - Decines of minutes - 3 least significant bits of MIN10.2÷MIN10.0
- **HOU1** - Units of hours - 4 least significant bits of HOU1.3÷HOU1.0
- **DAY1** - Units of day number - 4 least significant bits of DAY1.3÷DAY1.0
- **DAY10** - Decines of day number - 2 least significant bits of DAY10.1÷DAY10.0
- **MON1** - Units of month - 4 least significant bits of MON1.3÷MON1.0
- **MON10** - Decines of month - 1 least significant bit of MON10.0
- **YEA1** - Units of year - 4 least significant bits of YEA1.3÷YEA1.0
- **YEA10** - Decines of year - 4 least significant bits of YEA10.3÷YEA10.0
- **WEE** - Day of the week - 3 least significant bits of WEE.2÷WEE.0

The third bit of HOU10.2 indicates AM/PM

For this last register the three least significant bits mean:

<table>
<thead>
<tr>
<th>WEE.2</th>
<th>WEE.1</th>
<th>WEE.0</th>
<th>Day of the week</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Sunday</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Monday</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Tuesday</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>Wednesday</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Thursday</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>Friday</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>Saturday</td>
</tr>
</tbody>
</table>

For this manual, please refer to the proper paragraph of Appendix B in this manual.
The meaning of the three control registers is:

REG D = NU NU NU NU 30S IF B H

where:

NU = Not used.
30S = If high (1) it allows a 30 seconds correction of the time. Once set the RTC seconds are reset and the minutes increased, if the previous seconds was equal or greater than 30.
IF = It manages the RTC interrupt status. When read it shows the current interrupt status (1 active and vice versa), when reset to 0 it disables the RTC interrupt signal if the interrupt mode is selected.
B = Indicates whether R/W operations can be performed on the registers:
   1 -> operations are not permitted and vice versa.
H = If high (1) it stores the written time and date.

REG E = NU NU NU NU T1 T0 I M

where:

NU = Not used.
T1 T0 = Determines the duration of the internal counters interrupt cycle.
0 0 -> 1/64 second
0 1 -> 1 second
1 0 -> 1 minute
1 1 -> 1 hour
I = It defines the interrupt operating mode:
   1 -> it selects interrupt mode: when the selected duration elapses the interrupt is enabled and then disabled only with a reset of bit IF of control register D;
   0 -> it selects the standard mode: when the selected duration elapses the interrupt is enabled and then disabled only after 7.8 msec.
M = It mask the interrupt status:
   1 -> interrupt masked: the RTC interrupt signal is always disabled;
   0 -> interrupt not masked: the RTC interrupt signal reflects interrupt status.

REG F = NU NU NU NU T 24/12 S R

where:

NU = Not used.
T = It determines from which internal counter to take the counting signal:
   1 -> main counter (fast counter for test);
   0 -> 15th counter.
24/12 = It determines the hours counting mode:
   1 -> 0÷23;
   0 -> 1-12 with AM/PM.
S = If high (1) it stops the clock time counting until the next enabling (0).
R = If high (1) it resets all the internal counters.
EXTERNAL CARDS

GPC® 154 can be connected to a wide range of block modules and operator interface system produced by grifo®, or to many system of other companies. The on board resources can be expanded with a simple connection to the numerous peripheral grifo® boards, both intelligent and not, thanks to its standard ABACO® I/O BUS connector. Even single EURO cards with BUS ABACO® can be connected, by using the proper mother boards.

Hereunder some of these cards are briefly described; ask the detailed information directly to grifo®, if required.

KDL X24 - KDF 224

Keyboard Display LCD 2,4 rows 24 keys
Interface with Fluorescent or LCD display, LEDs backlit, 20x2 or 20x4 characters; up to 24 keys matrix keyboard connector. It is directly driven by a 20 pins ABACO® I/O standard connector; High level languages supported; standard pinout for telephone keyboard.

QTP 24 - QTP 24P

Quick Terminal Panel 24 keys with Parallel interface
Intelligent user panel equipped with Fluorescent or LCD display, LEDs backlit, 20x2 or 20x4 characters; RS 232, RS 422, RS 485 or current loop serial line; serial E2 for set up and message. Possibility of re-naming keys, LEDs and panel name by inserting label with new name into the proper slot; 24 Keys and 16 LEDs with blinking attribute and buzzer manageable by software; built in power supply; RTC option, reader of magnetic badge and relay. The QTP 24P is low cost no intelligent (passive) version. It is directly driven from 16 TTL I/O lines; high level languages supported.

QTP G28

Quick Terminal Panel - LCD Graphic, 28 keys
LCD display 240x128 pixels, CFC backlit; Optocoupled RS 232 line and additional RS 232/422/485/ C. L. line; CAN line controller; E2 for set up; RTC and RAM lithium backed; primary graphic object; possibility of re-naming keys, LEDs and panel name; 28 keys and 16 LEDs with blinking attribute and buzzer manageable by software; Buzzer; built-in power supply; reader of magnetic badge and relay option.

MCI 64

Memory Cards Interfaces 64 MBytes
Interfacing card for managing 68 pins PCMCIA memory cards, it is directly driven from any ABACO® I/O standard connector; High level languages GDOS supported.

IBC 01

Interface Block Communication
Conversion card for serial communication, 2 RS 232 lines; 1 RS 422-485 line; 1 optical fibre line; selectable DTE/DCE interface; quick connection for DIN 46277-1 and 3 rails.

IAC 01

Interface Adapter Centronics
Interface between ABACO® standard I/O 20 pins connector and D 25 pins connector with Centronics standard pin out.
OBI N8 - OBI P8
Opto BLOCK Input NPN-PNP
Interface between 8 NPN, PNP optocoupled and displayed input lines, with screw terminal and ABACO® standard I/O 20 pins connector; power supply section; connection for DIN Ω rails.

TBO 01 - TBO 08
Transistor BLOCK Output
Interface for ABACO® standard I/O 20 pins connector; 16 or 8 transistor output lines 45 Vdc 3 A open collector; screw terminal; optocoupled and displayed lines; connection for DIN 247277-1 and 3 rails.

RBO 08 - RBO 16
Relé BLOCK Output
Interface for ABACO® standard I/O 20 pins connector; 8 or 16 displayed Relays 3A with MOV; screw terminal; connection for DIN Ctype and Ω rails.

FBC 20 - FBC 120
Flat Block Contact 20 vie
Interfaccia tra 2 o 1 connettori a perforazione di isolante (scatolino da 20 vie maschi) e la filatura da campo (morsettiere a rapida estrazione). Attacco rapido per guide tipo DIN 46277-1 e 3.

DEB 01
Didactic Experimental Board
Supporting card for 16 TTL I/O lines use. It includes: 16 keys, 16 LEDs, 4 digits, 16 keys matrix keyboard, Centronics printer interface, LCD display and fluorescent display interface, GPC® 68 I/O connector, field connection with screw terminal.

IAL 42
Interface Adapter LCD
Interface between 16 I/O TTL available on I/O ABACO® standard connector and 14 pins low profile male connector featuring standard pin-out for fluorescent LCD displays management.

XBI 01
miXed BLOCK Input Output
Interface for ABACO® standard I/O 20 pins connector; 8 transistor output lines 45 Vdc 3A; 8 input lines; screw terminal; optocoupled and displayed I/O lines; connection for DIN 247277-1 and 3 rails.

XBI R4 - XBI T4
miXed BLOCK Input-Output
Interface for ABACO® standard I/O 20 pins connector; 4 Relays 3A with MOV or 4 optocoupled Transistors 3A open collectors; 4 input lines optocoupled; screw terminal; connection for DIN Ctype and Ω rails.

ABB 05
ABACO® Block BUS 5 slots
5 slots ABACO® mother board with power supply. Double power supply built in; 5Vdc 2,5A section for powering the on board logic; second section at 24Vdc 400mA galvanically coupled, for the optocoupled input lines. Auxiliary connector for ABACO® I/O BUS. Connection for DIN Ω rails.
ABB 03
ABACO® Block BUS 3 slots
3 slots ABACO® mother board; 4 TE pitch connectors; ABACO® I/O BUS connector; screw terminal for power supply; connection for DIN C type and Ω rails.

ZBR xxx
Zipped BLOCK Relays xx Input + xx Output
Peripheral cards family, relays outputs, equipped with housing for Ω rails mounting. Double power supply built in; 5Vdc section for powering the on board logic and an external CPU cards; second section, galvanically coupled, for the optocoupled input lines. All I/O lines are displayed by LEDs. Relays contacts are 3A and are MOV protected. All I/O connections are availables on quick terminal connectors. 1 connector interface to ABACO® I/O BUS. The ZBR serie represent the ideal complement for cards 3 and 4 type. The ZBR cards can be directly driven, through the PC parallel port, by using the PCC A26 low cost interface card. ZBR 324 -> 32 opto in, 24 relays; ZBR 246 -> 24 opto in, 16 relays; ZBR 168 -> 16 opto in, 8 relays; ZBR 84 -> 8 opto in, 4 relays.

ZBT xxx
Zipped BLOCK Transistors xx Input + xx Output
Peripheral cards family having optocoupled outputs and 3A transistor in open collector. Cards are equipped with housing for Ω rails mounting. Double power supply built in; 5Vdc section for powering the on board logic and an external CPU cards; second section, galvanically coupled, for the optocoupled input lines. All I/O lines are displayed by LEDs. All output transistors are equipped with protection against inductive loads. All I/O connections are availables on easy quick terminal connectors. Connector interface to ABACO® I/O BUS. The ZBT serie represent the ideal complement for cards 3 and 4 type. The ZBT cards can be directly driven, through the PC parallel port, by using the PCC A26 low cost interface card. ZBT 324 -> 32 opto in, 24 transistors; ZBT 246 -> 24 opto in, 16 transistors; ZBT 168 -> 16 opto in, 8 transistors; ZBT 84 -> 8 opto in, 4 transistors.

ETI 324
Encoder Timer I/O for Abaco® I/O BUS
Three timer counter driven by 82C54; bidirectional optocoupled encoder input; direction identifier; phases multiplier; 24 digital lines driven by 82C55 on two standard I/O Abaco® connectors; Abaco® I/O BUS interface; direct mounting for DIN 247277-1 and 3 rails.

CAN 14
Control Area Network, 1 channel, galvanically insulated
UART CAN SJA1000, 1 serial channels galvanically insulated, Abaco® I/O BUS interface 4 TYPE; direct mounting for DIN 247277-1 and 3 rails.

ADC 812
Analog to Digital Converter, 12 bits, multi-range
DAS (Data Acquisition System) multi-range 8 channels 12 bit A/D conversion lines; Track-Hold; 6µs conversion time; range ±10, ±5, +10, +5Vdc or 0÷20, 4÷20mA, Abaco® I/O BUS interface; direct mounting for DIN 247277-1 and 3 rails.

DAC 212
Digital to Analog Converter 12 bits, multi-range
Digital to Analog converter, multi-range 2 channels 12 bits ±10, +10 Vdc output, Abaco® I/O BUS interface; direct mounting for DIN 247277-1 and 3 rails.
BIBLIOGRAPHY

Here follows a list of manuals that can be a source of further information about the devices installed on GPC® 154.

Manual TEXAS INSTRUMENTS: The TTL Data Book - SN54/74 Families
Manual TEXAS INSTRUMENTS: RS-422 and RS-485 Interface Circuits
Manual NEC: Memory Products
Manual SGS-THOMSON: Programmable logic manual - GAL products
Manual MAXIM: New Releases Data Book - Volume V
Manual XICOR: Data Book
Manual ZILOG: Z80 Microprocessor Family
Figure 29: Available Connections Diagram
APPENDIX A: JUMPERS AND DRIVERS LOCATION

**FIGURE A1: MEMORY JUMPERS LOCATION**

**FIGURE A2: SERIAL COMMUNICATION JUMPERS LOCATION**
Serial A = RS 232
Serial B = RS 422

Serial A = RS 232
Serial B = RS 485

Serial A = RS 232
Serial B = RS 232

Figure A3: Serial Communication Drivers Location
APPENDIX B: ON BOARD COMPONENTS DESCRIPTION

PRODUCT SPECIFICATION

Z84013/015
Z84C13/Z84C15
IPC INTELLIGENT PERIPHERAL CONTROLLER

FEATURES

- Z84C00 80 CPU with Z84C20 CTC, Z84C4X SIO, CGC, Watch Dog Timer (WDT). In addition, Z84C15 and Z84015 have Z84C20 PIO.
- High speed operation 6, 10 MHz
- 16 MHz operation for Z84C15 only.
- Low power consumption in four operation modes:
  - 41 mA Typ, (Run mode)
  - 6 mA Typ, (Idle1 mode)
  - 50 μA Typ, (Idle2 mode)
  - 0.5 μA Typ, (Stop mode)
- Wide operational voltage range (5V±10%).
- TTL/CMOS compatible.
- Z84013 features:
  - Z84C00 Z80 CPU
  - On-chip two channel SIO (Z80 SIO).
  - On-chip four channel Counter Timer Controller (Z80 CTC).
  - Built-in Clock Generator Controller (CGC).
- Built-in Watch Dog Timer (WDT).
- Noise filter to CLK/TRG inputs of the CTC.
- 84-pin PLCC package.

Z84015 features:
- All Z84013 features, plus on-chip two 8-bit ports (Z80 PIO) and 100-pin QFP package.

Z84C13/Z84C15 enhancements to Z84013/Z84015:
- Power-on reset.
- Addition of two chip select pins.
- 32-bit CRC for Channel A of SIO.
- Wait state generator.
- Simplified EV mode selection.
- Schmitt-trigger inputs to transmit and receive clocks of the SIO.
- Crystal divide-by-one mode.
- 100-pin QFP (Z84C15 only)

GENERAL DESCRIPTION

The Intelligent Peripheral Controller (IPC) is a series of highly superintegrated devices with four versions. The Z84C13 and the Z84C15 are upward compatible versions of the Z84013 and the Z84015. The Z84013 is a CMOS 8-bit microprocessor integrated with the CTC, SIO, CGC, WDT and the PIO into a single 84-pin Quad Flat Pack (QFP) package. The Z84015 is the Z84013 without PIO, and it is housed in a 84-pin PLCC package. The Z84C13 is the Z84013 with enhancements and the Z84C15 is the Z84015 with enhancements. These high-end superintegrated intelligent peripheral controllers are targeted for a broad range of applications ranging from error correcting modules to enhancement/cock reductions of existing hardware using Z80-based discrete peripherals. Figures 1 and 2 show the difference between the Z84013/016 and the Z84C13/Z84C15.

Hereinafter, use the word IPC on the description covering all versions (Z84013/Z84C13 and Z84015/Z84C15). Use Z84C13/Z15 on the description that applies only to the Z84C13 and Z84C15, and use Z84013/015 on the description that applies only to the Z84013 and Z84015.
CPU SIGNALS

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Input/Output, 3-State</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>A0-A15</td>
<td>16-1(x13), 6-1, 100-01(x15)</td>
<td>I/O</td>
<td>16-bit address bus. Specifies I/O and memory addresses to be accessed. During the refresh period, addresses for refreshing are output. The bus is an input when the external master is accessing the on-chip peripherals.</td>
</tr>
<tr>
<td>D0-D7</td>
<td>83-76(x13), 80-82(x15)</td>
<td>I/O</td>
<td>8-bit bidirectional data bus. When the on-chip CPU is accessing on-chip peripherals, these lines are set to output and hold the data to/from on-chip peripherals.</td>
</tr>
<tr>
<td>RFD</td>
<td>30(x13), 14(x15)</td>
<td>I/O</td>
<td>Read signal. CPU read signal for accepting data from memory or I/O devices. When an external master is accessing the on-chip peripherals, it is an input signal.</td>
</tr>
<tr>
<td>WR</td>
<td>20(x13), 130(x15)</td>
<td>I/O</td>
<td>Write Signal. This signal is output when data, to be stored in a specified memory or peripheral LSI, is on the MPU data bus. When an external master is accessing the on-chip peripherals, it is an input signal.</td>
</tr>
<tr>
<td>MREQ</td>
<td>23(x13), 17(x15)</td>
<td>I/O, 3-State</td>
<td>Memory request signal. When an effective address for memory access is on the address bus, &quot;0&quot; is output. When an external master is accessing the on-chip peripherals, it is an output signal.</td>
</tr>
<tr>
<td>/IORQ</td>
<td>21(x13), 15(x15)</td>
<td>I/O</td>
<td>I/O request signal. When addresses for I/O are on the lower 8 bits (A7-A0) of the address bus in the I/O operation, &quot;0&quot; is output. In addition, the /IORQ signal is output with the M1 signal at the time of interrupt acknowledgment cycle to inform peripheral LSI of the state of the interrupt response vector when it is on the data bus. When an external master is accessing the on-chip peripherals, it is an output signal.</td>
</tr>
<tr>
<td>M1</td>
<td>17(x13), 6(x15)</td>
<td>I/O</td>
<td>Machine cycle &quot;1&quot;. MREQ and &quot;0&quot; are output together in the operation code fetch cycle. M1 is output for every opcode fetch when a two byte opcode is executed. In the maskable interrupt acknowledgment cycle, this signal is output together with /IORQ. It is 3-state in EV mode.</td>
</tr>
</tbody>
</table>

PIN DEFINITIONS

The pin assignment for each device is shown in Figures 3 and 4. Following is the description on each pin. For the description and the pin number, it stated as "x13" or "x15", that applies to both Z84C13/Z84C15 or Z84C15/Z84C15. Otherwise, C15 for Z84C13, C15 for Z84C15, 013 for Z84C13 and 015 for Z84C15.
### CPU SIGNALS (Continued)

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Input/Output, State</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>RFSH</td>
<td>26(x13), 7(x15)</td>
<td>Out, 3-State</td>
<td>The refresh signal. When the dynamic memory refresh address is on the low order byte of the address bus, RFSH is active along with MREQ signal. This pin is 3-state in CMOS mode.</td>
</tr>
<tr>
<td>INT</td>
<td>23(x13), 19(x15)</td>
<td>Open drain</td>
<td>Maskable Interrupt request signal. Interrupt is generated by peripheral LSI. The interrupt request is accepted if the interrupt enable pin is high (IP = 1). The INT signal of on-chip peripherals is internally wired OR without pull-up resistors and requires external pull-up. Also, interrupts from on-chip peripherals go out from this pin.</td>
</tr>
<tr>
<td>INH</td>
<td>56(x13), 65(x15)</td>
<td>IN</td>
<td>Non-maskable interrupt request signal. This interrupt request has a higher priority than the maskable interrupt request and does not rely upon the state of the interrupt enable (IP).</td>
</tr>
<tr>
<td>HALT</td>
<td>31(x13), 81(x15)</td>
<td>Out, 3-State</td>
<td>HALT signal. Indicates that the CPU has executed a HALT instruction. This signal is 3-state in CMOS mode.</td>
</tr>
<tr>
<td>BUSREQ</td>
<td>19(x13), 10(x15)</td>
<td>IN</td>
<td>BUS request signal. BUSREQ requests placement of the address bus, data bus, MREQ, /IORD, /IRD, and /MR signals into the high impedance state. BUSREQ is normally wired-off and a pull-up resistor is externally connected.</td>
</tr>
<tr>
<td>BUSACK</td>
<td>22(x13), 12(x15)</td>
<td>Out (G13/C16), Out3-State (C19/C16)</td>
<td>Bus Acknowledge signal. In response to BUSREQ signal, BUSACK informs the peripheral LSI that the address bus, data bus, MREQ, /IORD, /IRD, and /MR signals have been placed in the high impedance state. Note: For the 284013215, the BUSACK signal will be tri-state during CMOS mode. For the 284013215, the BUSACK will be 3-state during CMOS mode.</td>
</tr>
<tr>
<td>WAIT</td>
<td>18(x13), 11(x15)</td>
<td>IN (0D/C16), IN (0D/C16)</td>
<td>Wait signal. WAIT informs the CPU that specified memory or peripheral is not ready for data transfer. As long as WAIT signal is active, MPU is continuously kept in the wait state. Note: For the 284013215, the WAIT pin becomes an input to bring out on-chip wait-state generator during CMOS mode.</td>
</tr>
</tbody>
</table>

### CTC SIGNALS

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Input/Output, State</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>CL/KTRG</td>
<td>75-76(x13), 81-82(x15)</td>
<td>IN</td>
<td>External clock/timer input. These four CL/KTRG pins correspond to four Counter/Timers Channels. In the counter mode, each active edge will clear the downcounter to decrement by one. In timer mode, an active edge will start the timer. It is program selectable whether the active edge is rising or falling.</td>
</tr>
<tr>
<td>C/T00</td>
<td>68-71(x13), 74-77(x15)</td>
<td>Out</td>
<td>Zero counter output. In either timer or counter mode, pulses are output when the down-counter has reached zero.</td>
</tr>
</tbody>
</table>

### SIO SIGNALS

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Input/Output, State</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>M/RYA</td>
<td>32, 54(x13), 30, 52(x15)</td>
<td>Out</td>
<td>Wait/Ready signal A and Wait/Ready signal B. Used as WAIT or READY depending upon SIO programming. When programmed as WAIT they go active at &quot;0&quot;, selecting the CPU that addressed memory or I/O devices are not ready by requesting the CPU to wait. When programmed as READY, they are active at &quot;1&quot; which determines when a peripheral device associated with a DMA pin is free for read/write data.</td>
</tr>
<tr>
<td>M/RDYB</td>
<td>32, 54(x13), 30, 52(x15)</td>
<td>Out</td>
<td>Wait/Ready signal A and Wait/Ready signal B. Used as WAIT or READY depending upon SIO programming. When programmed as WAIT they go active at &quot;0&quot;, selecting the CPU that addressed memory or I/O devices are not ready by requesting the CPU to wait. When programmed as READY, they are active at &quot;1&quot; which determines when a peripheral device associated with a DMA pin is free for read/write data.</td>
</tr>
<tr>
<td>XGCA, XGDB</td>
<td>34, 52(x13), 32, 52(x15)</td>
<td>IN</td>
<td>Serial receive data signal</td>
</tr>
</tbody>
</table>
### SIO SIGNALS (Continued)

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Input/Output, 3-State</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>RWCA, RWCB</td>
<td>35,51(x13), 33,49(x15)</td>
<td>In</td>
<td>Receive clock signal. In the asynchronous mode, the receive clock can be 1, 16, 32, or 64 times the data transfer rate.</td>
</tr>
<tr>
<td>RWCA, RWCB</td>
<td>35,50(x13), 34,49(x15)</td>
<td>In</td>
<td>Transmitter clock signal. In the asynchronous mode, the transmitter clock can be 1, 16, 32, or 64 times the data transfer rate.</td>
</tr>
<tr>
<td>TXDA, TXDB</td>
<td>37,49(x13), 36,47(x15)</td>
<td>Out</td>
<td>Serial transmit data signal.</td>
</tr>
<tr>
<td>J7RA, J7RB</td>
<td>36,48(x13), 38,46(x15)</td>
<td>Out</td>
<td>Data terminal ready signal. When ready, these signals go active to enable the terminal transmitter. When not ready, they go inactive to disable the transfer from the terminal.</td>
</tr>
<tr>
<td>J7SA, J7SB</td>
<td>39,47(x13), 37,45(x15)</td>
<td>Out</td>
<td>Request to send signal. “0” when transmitting serial data. They are active when enabling receiver to transmit data.</td>
</tr>
<tr>
<td>J7SA, J7SB</td>
<td>40,46(x13), 36,44(x15)</td>
<td>In</td>
<td>Clear to send signal. When “0”, after transmitting these signals the modem is ready to receive serial data. When ready, these signals go active to enable terminal transmitter. When not ready, these signals go inactive to disable transfer from the terminal.</td>
</tr>
<tr>
<td>IDCDA, IDCDB</td>
<td>41,45(x13), 38,43(x15)</td>
<td>In</td>
<td>Data carrier detect signal. When “0”, serial data can be received. These signals are active to enable receivers to transmit.</td>
</tr>
</tbody>
</table>

### SYSTEM CONTROL SIGNALS

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Input/Output, 3-State</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>IE1</td>
<td>60(x13), 71(x15)</td>
<td>In</td>
<td>Interrupt enable input signal. IE1 is used with the IEO to form a priority daisy chain when there is more than one interrupt-driven peripheral.</td>
</tr>
<tr>
<td>IEO</td>
<td>59(x13), 71(x15)</td>
<td>Out</td>
<td>The interrupt enable output signal in the daisy chain interrupt control. IEO controls the interrupt of external peripherals. IEO is active when IE1 is “1” and the CPU is not servicing an interrupt from the on-chip peripherals.</td>
</tr>
<tr>
<td>J330 (C13/C15 only)</td>
<td>42(C13), 40(C15)</td>
<td>Out</td>
<td>Chip Select 0. Used to access external memory or I/O devices. This pin has been assigned to “C1” pin on Z8401/20. This signal is decoded only from A15-A12 without control signals. Refer to “Functional Description” on-chip select signals for further explanation.</td>
</tr>
</tbody>
</table>

### SYSTEM CONTROL SIGNALS (Continued)

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Input/Output, 3-State</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>JCS1</td>
<td>499(x13), 493(x15)</td>
<td>Out</td>
<td>Chip Select 1. Used to access external memory or I/O devices. This pin has been assigned to “CT” pin on Z8401/20. This signal is decoded only from A15-A12 without control signals. Refer to “Functional Description” on-chip select signals for further explanation.</td>
</tr>
<tr>
<td>M/R OUT</td>
<td>61(x13), 73(x15)</td>
<td>Out(3/15), Open Drain(C13/C15)</td>
<td>Watchdog Timer Output signal. Output pulse width depends on the externally connected pin.</td>
</tr>
<tr>
<td>J330 (C13/C15 only)</td>
<td>29(x13), 9(x15)</td>
<td>Input</td>
<td>Chip Select 1. Used to access external memory or I/O devices. This pin has been assigned to “C1” pin on Z8401/20. This signal is decoded only from A15-A12 without control signals. Refer to “Functional Description” on-chip select signals for further explanation.</td>
</tr>
</tbody>
</table>

Note: For the Z8401/20 (Z8402) and the Z8411/20 (Z8412) in the reset state, no pulse is output to the output pin. When the Z8402/12 is in an interrupt-driven mode, supply clock goes to the terminal. If external clock is supplied to CLKIN pin (without going through the Z8402/20 and the Z8412), terminal must be connected to “0” or “1”.
### SYSTEM CONTROL SIGNALS (Continued)

**Note:** For the 28413/15, to access on-chip resources from the CPU or on I/O, the CPU is electrically disconnected. A 15-4, JMDR, JFRD, JDDR, JDDR, and JDMR are charged to input D7-D0 changed in direction. If J7, JNALT, and JNRF are put into high impedance mode when the EV pin is set to "1", the BUSCH is in state. For details, please refer to "Functional Description" on EV mode.

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Input/Output, 3-State</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>ICT</td>
<td>42, 44(13), 46, 47(15), Not with C13/C15</td>
<td>Out</td>
<td>Test pin, used in the open state.</td>
</tr>
<tr>
<td>NC</td>
<td>24, 27, 67, 68(13), flat with x15</td>
<td></td>
<td>Not connected.</td>
</tr>
<tr>
<td>VCC</td>
<td>43, 84(x13), 41, 90(x15)</td>
<td>Power Supply</td>
<td>+5 Vols</td>
</tr>
<tr>
<td>VSS</td>
<td>22, 60(x13), 16, 64(x16)</td>
<td>Power Supply</td>
<td>0 Vols</td>
</tr>
</tbody>
</table>

### PIO SIGNALS (for the Z84x15 only)

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Input/Output, 3-State</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>/ASTB</td>
<td>81(x13)</td>
<td>In</td>
<td>Port A strobe pulse from a peripheral device. This signal is used as the handshake between Port A and external circuits. The meaning of this signal depends on the mode of operation selected for Port A (see &quot;PIO Basic Timing&quot;).</td>
</tr>
<tr>
<td>/ASTB</td>
<td>81(x15)</td>
<td>In</td>
<td>Port B strobe pulse from a peripheral device. This signal is used as the handshake between Port B and external circuits. The meaning of this signal is the same as /ASTB, except when Port A is in mode 2 (see &quot;PIO Basic Timing&quot;).</td>
</tr>
<tr>
<td>ARDY</td>
<td>20(x15)</td>
<td>Out</td>
<td>Register A ready signal. Used as the handshake between Port A and external circuits. The meaning of this signal depends on the mode of operation selected for Port A (see &quot;PIO Basic Timing&quot;).</td>
</tr>
<tr>
<td>BRDY</td>
<td>62(x15)</td>
<td>Out</td>
<td>Register B ready signal. Used as the handshake between Port B and external circuits. The meaning of this signal depends on the mode of operation selected for Port B (see &quot;PIO Basic Timing&quot;).</td>
</tr>
<tr>
<td>PA7-PAS</td>
<td>22-28(x15)</td>
<td>IO, 3-State</td>
<td>Port A data signals. Used for data transfer between Port A and external circuits.</td>
</tr>
<tr>
<td>PB7-PBD</td>
<td>53-60(x15)</td>
<td>IO, 3-State</td>
<td>Port B data signals. Used for data transfer between Port B and external circuits.</td>
</tr>
</tbody>
</table>

### FUNCTIONAL DESCRIPTION

The following pins have different functions between 013/015 and 131/C15

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin # X13</th>
<th>Pin # X15</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>RESET</td>
<td>21</td>
<td>9</td>
<td>Functionality is different.</td>
</tr>
<tr>
<td>WAIT</td>
<td>15</td>
<td>15</td>
<td>Functionality is different.</td>
</tr>
<tr>
<td>EV</td>
<td>55</td>
<td>57</td>
<td>Functionality is different.</td>
</tr>
<tr>
<td>EVSTOUT</td>
<td>61</td>
<td>73</td>
<td>Push-pull output on Z8413/15, Open drain on Z8413/C15</td>
</tr>
<tr>
<td>ICT</td>
<td>42, 42</td>
<td>42, 42</td>
<td>(Test pin) on Z8413/15, ICSV and ICS1 on Z8413/C15</td>
</tr>
<tr>
<td>TxCA, TxCB, RsCA, and RsCB</td>
<td>33, 36, 60, 51, 33, 34, 48, 49</td>
<td>In EV mode, 3-stated on Z8413/C15, remains active on Z8413/15</td>
<td></td>
</tr>
</tbody>
</table>

Figure 5(a) shows the functional block diagram of the Z8413/15 and Figure 5(b) shows the functional block diagram of the Z8413/C15. As described earlier, the only difference between the Z84x13 and the Z84x15 is the PIO not being available on the Z84x13.

Functionally, the only SIO/PIO not available on the Z8413/C15, ICSV, and the Z80 CPU are the same as the previous devices. Therefore, for detailed description of each individual unit, refer to the Product Specification/Technical Manual of each device.

The following subsections describe each individual functional unit of the IPC.

**Z84C0001 Logic Unit**

This CPU provides all the capabilities and pins of the Z80 CPU. This allows 100% software compatibility with existing Z80-based systems. In addition to the pin called "A97" to extend the DMA refresh addess to 16-bits, refer to "Z84C001 Z80 CPU with 16-Bit Product Specification/Technical Manual".

**Z84C20 Parallel Input/Output Logic Unit (Z84x15 Only)**

This logic unit provides both TTL- and CMOS-compatible interfaces between peripherals and a CPU through the use of two 8-bit parallel ports (Figure 6). The CPU configures the logic to interface to a wide range of peripheral devices with or without external logic. Typical devices that can be interfaced with the interface are keyboards, printers, and EPROM/PAL programmable logic devices.

The parallel ports (designated Port A and Port B) are byte wide and completely compatible with the Z84C20 PIO.

These two ports have several modes of operation: input, output, bidirectional, or bit control mode. Each port has two handshake signals (RDY and S15) which are used to control data transfers. The RDY (read) indicates that the port is ready to accept data when the Z84x (strobe) is input to the port that indicates when data transfer has occurred. Each of the ports can be programmed to interrupt the CPU upon the occurrence of specified status conditions, and generate an interrupt vector when the CPU responds to it. Additional information on the operation of the portion of the logic, please refer to the Z84C20 PIO Product Specification/Technical Manual.

**Z84C20 Counter/Timer Logic Unit**

This logic unit provides the user with four individual 8-bit Counter/Timer Channels that are compatible with the Z84C20 (Figure 7). The Counter/Timers can be programmed by the CPU for a broad range of counting and timing applications. Typical applications include event counting, interrupt, interval counting, and serial baud rate clock generation.

Each of the Counter/Timer Channels, designated Channels 0-3, have an 8-bit prescaler (when used in timer mode) and its own 8-bit counter to provide a wide range of count modes. Each of the Channels have their own Clock/Trigger inputs to input the counting process and an output to indicate zero crossing/timeout conditions. With only one internal vector generated into the logic unit, each channel can generate a unique interrupt vector in response to the interrupt acknowledge cycle.
Figure 6. PIO Block Diagram

28HC08 Serial I/O Logic Unit
This logic unit provides the user with two separate multi-protocol serial I/O channels that are completely compatible with the 28HC0x SIO. Their basic functions as serial-to-parallel and parallel-to-serial converters can be programmed by a CPU for a broad range of serial communications applications. Each channel, designated Channel A and Channel B, is capable of supporting all common asynchronous and synchronous protocols (Manchester, Bipolar, and SLCD/DLC, byte and bit oriented - Figure 8).

28HC12C15 Only. As an enhancement to the 28HC12C15, the 28HC12C15 can handle a 32-bit CRC on Channel A and Schmitt-trigger inputs on the IVC and RWC pins of both channels.
**Watch Dog Timer (WDT) Logic Unit**

This logic unit has been superintegrated into the IPC. It detects an operation error, caused by the program runaway, and returns to normal operation. Figure 8 shows the block diagram of the WDT. Upon Power-Off Reset, this unit is enabled. If WDT is not required, but WDTOUT is connected to a pin other than the RESET pin, it has to be disabled. During the power-down mode of operation (either IDLE or STOP), the Watch Dog Timer is disabled.

**WDT Output (WDTOUT pin):** When the WDT is used, the "0" level signal is output from the WDTOUT pin after a duration of time specified in the WDTP or in the WDTMR. The output pulse width is one of the following, depending on the WDTOUT pin connection:

- **The WDTOUT is connected to the RESET pin:** The "0" level is pulled for 5ms (System clock cycles).
- **The WDTOUT is connected to a pin other than the RESET pin:** The "0" level is held until the Watch Dog Timer is cleared by software, or read by the RESET pin.

**CGC Logic Unit:** The CGC has CGC (Clock Generator Controller) unit. This unit is identical to the one with the Z84D24 and the Z84QD24, and supports power-down modes of operation. The output from this unit is on the pin called CLKOUT, and is not connected to the system clock internally. The CLKIN pin is the system clock input. The user can connect CLKOUT to CLKIN to utilize the CGC unit or supply external clock from CLKIN pin. The CGC unit allows crystal input (XTAL1, XTAL2) or External Clock input on the XTAL1 pin. It has clock divide-by-two circuits and generates a half-speed clock to the input.

Z84D19S15: The power-down modes of the IPC vary depending upon whether the system clock is fed from the CGC unit (i.e., CLKOUT to CLKIN) or the external clock source on the CLKIN pin. They also have divide-by-one Mode. If the clock is supplied by the CGC unit, all of the modes in "halt" state are available. When external clock is provided on the CLKIN pin, XTAL1 is left open (tied to "0" or "1") to avoid meta-stable conditions to minimize power consumption.

**Z84D19S15** Only, if the system clock is provided on the CLKIN pin, none of the power-down mode (except RUN mode) is supported.

**Z84C13K15** Clock output is the same, or half, of the external frequency.

**Z84C13K15** Only, if the system clock is provided on the CLKIN pin, only the IDLE mode is applicable. In this mode, the Halted Instruction is executed, internal clock to the CGC is kept on "Continuous", but the clock to the other components (CPU, PIO, SIO and Watch Dog Timer) are stopped. The divided-by-two circuit of the CGC unit can be skipped by programming bit 4 of the WDTMR (see "Programming" section). Upon Power-on Reset, it comes up in divide by two mode.

**System Clock Generation**

The IPC has a built-in oscillator circuit and the required clock can be easily generated by connecting a crystal to the external terminals (XTAL1, XTAL2). Clock output is at the same frequency as half the speed of the crystal frequency. Example of oscillator connections are shown in Figure 10.
The Wait State Control Register can be programmed to generate multiple wait states during different CPU cycles listed as follows:

- Memory Wait and Opcode wait. The Wait State Generator can put 0 to 3 wait states in memory accesses. Additionally, one wait state can be inserted during an IMC (Opcode fetch) cycle, because IMC cycle timing requirements are tighter than memory Read/Write cycles. It generates wait states to the Memory Access in a specific address range, which is programmed in the Memory Wait Brancher Register.

- I/O Wait. The Wait State generator can put 0, 1, or 2 wait states in I/O accesses. Regardless of the programming of this field, no I/O wait states are inserted for accesses to another peripheral.

This interrupt vector Wait During Interrupt acknowledge cycle, the Wait State Generator can insert one wait state after the I/OQ pin goes active, to extend the time between the I/OQ pin going active and the CPU. It allows a slow vector response device.

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### Table 1. I/O Control Register Address

<table>
<thead>
<tr>
<th>Address</th>
<th>Device</th>
<th>Channel</th>
<th>Register</th>
</tr>
</thead>
<tbody>
<tr>
<td>19h</td>
<td>CTC</td>
<td>Ch 0</td>
<td>Control Register</td>
</tr>
<tr>
<td>11h</td>
<td>CTC</td>
<td>Ch 1</td>
<td>Control Register</td>
</tr>
<tr>
<td>13h</td>
<td>CTC</td>
<td>Ch 2</td>
<td>Control Register</td>
</tr>
<tr>
<td>15h</td>
<td>CTC</td>
<td>Ch 3</td>
<td>Control Register</td>
</tr>
<tr>
<td>19h</td>
<td>SIC</td>
<td>Ch A</td>
<td>Data Register</td>
</tr>
<tr>
<td>11h</td>
<td>SIC</td>
<td>Ch B</td>
<td>Data Register</td>
</tr>
<tr>
<td>13h</td>
<td>SIC</td>
<td>Ch C</td>
<td>Control Register</td>
</tr>
<tr>
<td>15h</td>
<td>PIC</td>
<td>Port A</td>
<td>Data Register (Not with Z84x13)</td>
</tr>
<tr>
<td>11h</td>
<td>PIC</td>
<td>Port B</td>
<td>Data Register (Not with Z84x13)</td>
</tr>
<tr>
<td>13h</td>
<td>PIC</td>
<td>Port C</td>
<td>Control Register (Not with Z84x13)</td>
</tr>
<tr>
<td>15h</td>
<td>Watch-Dog Timer</td>
<td>Watch-Dog timer</td>
<td>Master Register (WDTMR)</td>
</tr>
<tr>
<td>17h</td>
<td>Watch-Dog Timer</td>
<td>Watch-Dog timer</td>
<td>Control Register (WDTCTR)</td>
</tr>
<tr>
<td>3Bh</td>
<td>Systems Control Register Pointer (SCP) (Not with Z84015/3015)</td>
<td>Systems Control Data Port (SCDP) (Not with Z84015/3015)</td>
<td>Through SCP and SCP</td>
</tr>
<tr>
<td>15h</td>
<td>Control Register 00 - Wave State Control Register (WSCR)</td>
<td>Control Register 01 - Memory Wave State Boundary Register (MWBR)</td>
<td>Control Register 02 - Chip Select Boundary Register (CSBR)</td>
</tr>
<tr>
<td>17h</td>
<td>Control Register 03 - Misc. Control Register (MCR)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### PIO Registers

For more detailed information, please refer to the PIO Technical Manual. These registers are not in the Z84x13.

**Interrupt Vector Word**

The PIO logic unit is designed to work with the Z80 CPU; it must be programmed if interrupts are used. Bit D0 must be a zero (Figure 11).

![Figure 11. PIO Interrupt Vector Word](image)

**Mode Control Word**

When Mode 3 is selected, the Mode Control Word is followed by the I/O Register Control Word. This word configures the I/O register, which defines which ports lines a port is connected to. A '1' indicates output, a '0' indicates output. This word is required when in Mode 3 (Figure 12).

![Figure 12. PIO Mode Control Word](image)

**I/O Register Control Word**

This word sets the mask control register, thus allowing any unused bits to be masked off. If any bits are to be masked, then bit D4 of the Interrupt Control Word is set. When bit D4 of theInterrupt Control Word is set, then the next word programmed is the Mask Control Word. To mask an input bit, the corresponding Mask Control Word bit is a '1' (Figure 13).

![Figure 13. I/O Register Control Word](image)

**Interrupt Control Word**

In Mode 3 operation, handshake signals are not used. Interrupts are generated as a logic function of the input signal levels. The Interrupt Control Word sets the logic conditions and the logic levels required for generating an interrupt. Two logic conditions or functions are available: AND (if all input bits change to the active level, an interrupt is triggered), OR (if any one of the input bits change to the active logic level, an interrupt is triggered). The user can program which input bits are to be considered as part of this logic function. Bit D5 sets the logic function, bit D6 sets the logic level, and bit D4 specifies a mask control word to follow (Figure 14).

![Figure 14. Interrupt Control Word](image)

**Interrupt Disable Word**

This word can be used to enable or disable a port's interrupts without changing the rest of the port's interrupt conditions (Figure 15).

![Figure 15. Interrupt Disable Word](image)
CTC CONTROL REGISTERS

For more detailed information, refer to the CTC Technical Manual.

Channel Control Word

This word sets the operating modes and parameters as described below. Bit D0 is a **1** to indicate that this is a Control Word (Figure 17).

**Figure 17. CTC Channel Control Word**

- **Bit D7**: Interrupt Enable
- **Bit D6**: Mode Bit
- **Bit D5**: Precalcer Factor
- **Bit D4**: Clock/Trigger Edge Select
- **Bit D3**: Timer Trigger
- **Bit D2**: Time Constant
- **Bit D1**: Software Reset
- **Bit D0**: Value

Time Constant

Before a channel starts counting, it must receive a time constant word. The time constant value is anywhere between **1** and **255**, with **0** being accepted as a count of **256** (Figure 18).

**Figure 18. CTC Time Constant Word**

Interrupt Vector Word

If one or more of the CTC channels have Interrupt enabled, then the Interrupt Vector Word must be programmed. Only the most significant bits of this word are programmed, and bit D0 must be a **0**. Bits D2-D1 are automatically modified by the CTC channels which it responds with an interrupt vector (Figure 19).

**Figure 19. GTC Interrupt Vector Word**

**SIO REGISTERS**

For more detailed information, refer to the SIO Technical Manual.

Read Registers. The SIO channel B contains three read registers while channel A contains only two that are read to obtain status information. To read the contents of a register (rather than WR), the program must first write a pointer to WR in exactly the same manner as a write operation. The next 20 read cycle will place the contents of the selected read registers onto the data bus (Figure 20a, b, c).

**Figure 20a. SIO Read Register 0**

Write Registers. The SIO Channel B contains eight write registers while Channel A contains only seven that are programmed to configure the operating mode characteristics of each channel. With the exception of WR, programming the write registers is a two-step operation. The first operation is a pointer written to WR which points to the selected register. The second operation is the actual control word that is written into the register to configure the SIO channel (Figure 21).

**Figure 20b. SIO Read Register 1**

**Figure 20c. SIO Read Register 2**
**Watch Dog Control Registers**

There are two registers to control Watch Dog Timer operations: the Watch Dog Timer Master Register (WDTMR, I/O Address F0H) and the WDT Control Register (WDTCR, I/O Address F1H). Watch Dog Timer Logic has a "double key" structure to prevent the WDT disabling error, which may lead to the WDT operation to stop due to program runaway. Programming the WDT follows this procedure. Also, these registers program the power-down mode of operation. The "Second key" is needed when turning off the Watch Dog Timer.

Enabling the WDT: The WDT is enabled by setting the WDT Enable Bit (ST7_WRITE to "1") and the WDT Enable field (G3.D6吴DTF) to the desired time period. These command bits are in the Watch Dog Timer Master Register (WDTMR, I/O Address F0H).

Disabling the WDT: The WDT is disabled by clearing WDT Enable bit (WDTEnable) in the WDTMR to "0" followed by setting "0" to the WDT Command Register (WDTCR, I/O Address F1H).
Clearing the WDT. The WDT can be cleared by writing "0011" into the WDTOH.

Watch Dog Timer Master Register (WDTMR; I/O address F4H). This register controls the activities of the Watch Dog Timer and selects power-down mode of operation (Figure 22).

Bit 00, Idle Mode (HALTM). A two bit field specifies one of four power-down modes. To change this field, write "DBH" to the WDT command register, followed by a write to this register. For detailed description of this field, please refer to the section "Mode of Operation." Upon Power-on Reset, this field is set to 11, which specifies "RUN mode."

- 00: IDLE 1 Mode
- 01: IDLE 2 Mode
- 10: STOP Mode
- 11: RUN Mode

Bit 02. Reserved. These three bits are reserved and should always be programmed as "011." A read to these bits will always return "011."

Watch Dog Timer Command Register (WDTCR; I/O address F4H). In conjunction with the WDTMR, this register works as a "second key" for the Watch Dog Timer. This register is write only (Figure 23).

Write 8'h41 after clearing WDTOE to "0" - Disable WDT. Write 8'h51 followed by a write to HALTM - Change Power-down mode.

Bit 07. Watch Dog Timer Enable (WDT). This bit controls the activities of the Watch Dog Timer. The WDT can be enabled by setting the bit to "1." To disable the WDT, write "0" to this bit followed by writing "DBH" in the WDT Command Register. Watch Dog Timer logic has a "double-bit" structure to prevent the WDT disabling error, which may lead to the WDT operation to stop, due to program runaway. Upon Power-on reset, this bit is set to "1" and the WDT is enabled.

Bit 06-05. WD T Periodic field (WDT). This two bit field determines the desired time period. Upon Power-on reset, this field is set to "11."

Figures 24 and 25:

**Interrupt Priority Register (INTPR, I/O address F4H)**

This register (write only) is used to determine the interrupt priority for the CTC, SIO and the PIO (Figure 24).

**System Control Data Port (SCDP, I/O address E6H)**

This register is used to access the SIO. The SCDP is read/write and holds the 16-bit mode value after modification. When entering or leaving Power-on Reset, all bits are cleared to zero. The pointer value, rather than 00'h to 20'h is reserved and is not written. Upon Power-on Reset, this register is set to "00h" (Figure 25).

**System Control Data Port (SCDP, I/O address E6H)**

This register stores the pointer to access System Control Register (SCR, MWR, SRB, CBRR, and MST). This register is read/write and holds the 16-bit mode value after modification. When entering or leaving Power-on Reset, all bits are cleared to zero. The pointer value, rather than 00'h to 20'h is reserved and is not written. Upon Power-on Reset, this register is set to "00h" (Figure 25).

**REGISTERS FOR SYSTEM CONFIGURATION**

(The following registers are not available on Z8413015.)

There are four indirectly accessible registers to determine System configuration with the Z8413015. These indirectly accessible registers are: Wait State Control Register (WCR, Control Register 00h), Memory Wait Boundary Register (MWBR, Control Register 01h), Chip Select Boundary Register (CSBR, Control Register 02h) and Misc. Control Register (MCR, Control Register 03h). To access these registers, Z8413015 using "reduced register number to be accessed" to the System Control Register Pointer (SCRP).

2-93
This register has the following fields:

- Bit 1-5: Interrupt Daisy Chain Wait. This 2-bit field specifies the number of wait states to be inserted during an interrupt. Daisy Chain wait period of the Interrupt Acknowledge cycle, which is GPR followed by the setting period of 151, going active '0'. Also, this field controls the number of wait states inserted during the RETI (Return From Interrupt) cycle. If specified to insert 4 or 5 wait states during Interrupt Acknowledge cycle, the wait states generator also inserts wait states during the RETI return sequence. This sequence is formed with two op-code fetch cycles (Op-code is GPR followed by 43H). It inserts 1 wait state if op-code followed by 43H is NOT 43H, and inserts 2 if 2 wait states, respectively, if the following op-code is 43H.

- Bit 6: (Op) Wait states. This 1-bit field specifies the number of wait states to be inserted during I/O transactions.

- Bit 7-11: Wait states. These bits are set to '11'1', then cleared to '00' on the trailing edge of the 16th M1 signal, unless programmed.

- Bit 12-15: Memory Wait states. These four bits are used to specify the number of wait states to be inserted during memory Read/Write operations.

- Bit 16-19: Memory Wait states. These four bits are used to specify the number of wait states to be inserted during memory Read/Write operations.

- Bit 20: Chip Select signals are active for the address range:
  - IC50: (D3-D0 of CSB) ≥ A51-A12 ≥ A51-A12 ≥ (D3-D0 of CSB)

  This register is set to "xx111111b" on Power-on Reset, which specifies the address range of CSB for "0000h to FFFFh" (all Memory location). CS51 "unpowered."
**Table 2. Power-down Modes**

<table>
<thead>
<tr>
<th>Operation Mode</th>
<th>WDTRM Bit D4</th>
<th>WDTRM Bit D3</th>
<th>Description at HALT State</th>
</tr>
</thead>
<tbody>
<tr>
<td>RUN Mode</td>
<td>1</td>
<td>1</td>
<td>The CPU continues the operation and continuously supplies a clock to the outside.</td>
</tr>
<tr>
<td>IDLE1 Mode</td>
<td>0</td>
<td>0</td>
<td>The internal oscillator's operation is continued. Clock output (CLKOUT) as well as internal clock to the CPU, PIO, SIO, CTC, and the Watch Dog Timer is stopped at '0' level of T4 state in the halt instruction operation code fetch cycle.</td>
</tr>
<tr>
<td>IDLE2 Mode</td>
<td>0</td>
<td>1</td>
<td>The internal oscillator and the CTC operation continues and supplies clock to the outside on the CLKOUT pin continuously. But the internal clock to the CPU, PIO, SIO and the Watch Dog Timer is stopped at '0' level of T4 state in the halt instruction operation code fetch cycle.</td>
</tr>
<tr>
<td>STOP Mode</td>
<td>1</td>
<td>0</td>
<td>All operations of the internal oscillator, clock (CLK) output, internal clock to the CPU, PIO, CTC, SIO and the Watch Dog Timer are stopped at '0' level of T4 state in the halt instruction operation code fetch cycle.</td>
</tr>
</tbody>
</table>

**Table 3. Device status in HALT state**

<table>
<thead>
<tr>
<th>Mode</th>
<th>CPU</th>
<th>CTC</th>
<th>PIO</th>
<th>SIO</th>
<th>WDTRM</th>
<th>CLKOUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>IDLE1</td>
<td>O</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>IDLE2</td>
<td>O</td>
<td>X</td>
<td>O</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>STOP</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>RUN</td>
<td>X</td>
<td>X</td>
<td>O</td>
<td>SIO</td>
<td>WDTRM</td>
<td>X</td>
</tr>
</tbody>
</table>

**Timing**

**Basic Timing**

The timing is explained here with emphasis placed on the halt function relative to the clock generator. The following items are identical to those for the Z84C000. Refer to the data sheet for the Z84C000.

- Operation code fetch cycle
- Memory Read/Write operation
- Input/Output operation
- Bus request acknowledge operation
- Maskable interrupt request operation
- Non-Maskable interrupt request operation
- Reset Operation

Operation When HALT Instruction is Executed: When the CPU fetches a halt instruction in the operation code fetch cycle, HALT goes active (Low) in sync with the falling edge of T4 state before the peripheral LSI and CPU stops the operation. After this, the system clock generator differs depending upon the operation mode (RUN Mode, IDLE1 Mode or STOP Mode). If the internal system clock is running, the CPU continues to execute NOP instruction even in the halt state.

**Figure 31. Timing of RUN Mode**

(At HALT instruction Command execution)
APPENDIX C: CARD MECHANICAL MOUNTING

The GPC® 154 can be physically mounted in two different manner. The first is the piggy back mounting (stack trough mode) that use the three connectors CN1, CN5 for the interface with a user developed board. This connectors lead out of 7 mm on solder side and the user board must have proper female strip connectors (2,54 mm pitch) where the card can be plugged in, obtaining a single system.

The second mode expect a mounting inside a proper plastic container for a direct mounting on DIN 247277-1 and 3 Ω rails; if the card is used with some other peripheral cards (i.e. ZBR xxx or ZBT xxx), a single longer container can be used obtaining a single module. The described plastic container code is 414487 type RS/100 by Weidmuller and it can be ordered to grifo® as BLOCK 100.4T option. By selecting this mounting the electric connection between GPC® 154 and other peripheral cards is performed with a flat cable that must be really short and eventually can be ordered to grifo® as FLT 26+26 I/O.

In the following figures are described the module dimensions with the connector positions and some immages that illustrate the connection modes.

**Figure C1: Module dimension for Piggy-Back mounting**
FIGURE C2: PIGGY-BACK MOUNTING

FIGURE C3: WEIDMULLER RAIL MOUNTING
Title: PPI example
date: 16/11/1998
rel. 1.1
Page: 1 of 1

Figure D1: Expansion PPI Electric Diagram
Figure D2: SPA 03 Electric Diagram
FIGURE D3: QTP 16P ELECTRIC DIAGRAM
FIGURE D4: QTP 24P 1/2 ELECTRIC DIAGRAM
**Figure D5: QTP 24P 2/2 Electric Diagram**
**Figure D6: IAC 01 Electric Diagram**

**Title:** IAC 01

**Date:** 13-11-98

**Page:** 1 of 1

---

**CN2**
20 pin Low-Profile Male

**CN1**
25 pin D-Type Female

- **P1.0**
- **P0.0**
- **P0.1**
- **P0.2**
- **P0.3**
- **P0.4**
- **P0.5**
- **P0.6**
- **P0.7**
- **P1.5**
- **P1.7**
- **P1.4**
- **P1.6**
- **P1.1**
- **P1.2**
- **P1.3**
- **+5V**
- **GND**

- **C2** 100 nF
- **C1**
- **C3**
- **C4** 2.2 nF
- **C5**
- **C6** 2.2 nF
- **C7**
- **C8** 2.2 nF
- **C9**
- **C10** 2.2 nF
- **C11**

- **RR1** 4.7 KΩ 9+1
- **+5V**
- **22 μF 6.3V**
FIGURE D7: ABACO® I/O BUS - I/O ELECTRIC DIAGRAM

ABACO® I/O BUS
26 pin connector

Title: I/O example
Date: 28/04/1999
Rel. 1.2
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