GPC® 153
General Purpose Controller Z84C15

TECHNICAL MANUAL
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General Purpose Controller Z84C15

TECHNICAL MANUAL

Size 100x149 mm; optional container for DIN 46277-1 and 3 Ω rails; interface to BUS I/O Abaco®, CPU CMOS 84C15 with 20 MHz quartz; up to 512K EPROM or FLASH EPROM and up to 512K SRAM; RAM/ROM disk managed through FGDOS; serial EEPROM up to 8 KBytes; six pins dip Switch and two configuration jumpers software readable; 1 activity LED; 2 RS 232 one of which settable in RS 422, RS 485 or Current Loop with baud rate up to 115 KBAud; 16 TTL I/O signals; 4 timer counter; 8 A/D Converter lines, conversion time 6 μs, ranges 0÷5V, 0÷10V, ±5V or ±10V software configurable and ranges 0÷20 mA or 4÷20 mA hardware configurable, resolution up to 12 bits+sign, possibility to generate an INT at the end of the conversion; Real Time Clock capable to manage day, month, year, day of week, hours, minutes, seconds and to generate a periodical INT with software defineable period; Watch Dog software resettable visualized through LED; back up circuitry for SRAM and RTC with Lithium battery and connector for optional external battery; unique required supply voltage +5Vdc, 280 mA; wide range of software and development environments that allow to use the board through a normal PC, some remarkable packages are: FGDOS 153; PASCAL 80; CBZ 80; NSB8; RSD 153; HI TECH C 80; GET 80; DDS MICRO C 85; NO ICE Z80; etc.
IMPORTANT

Although all the information contained herein have been carefully verified, grifo® assumes no responsibility for errors that might appear in this document, or for damage to things or persons resulting from technical errors, omission and improper use of this manual and of the related software and hardware. grifo® reserves the right to change the contents and form of this document, as well as the features and specification of its products at any time, without prior notice, to obtain always the best product.

For specific informations on the components mounted on the card, please refer to the Data Book of the builder or second sources.

SYMBOLS DESCRIPTION

In the manual could appear the following symbols:

⚠️  Attention: Generic danger

⚡️  Attention: High voltage

Trade Marks

GPC®, grifo®: are trade marks of grifo®.

Other Product and Company names listed, are trade marks of their respective companies.
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INTRODUCTION

The use of these devices has turned - IN EXCLUSIVE WAY - to specialized personnel.

The purpose of this handbook is to give the necessary information to the cognizant and sure use of the products. They are the result of a continual and systematic elaboration of data and technical tests saved and validated from the manufacturer, related to the inside modes of certainty and quality of the information.

The reported data are destined- IN EXCLUSIVE WAY- to specialized users, that can interact with the devices in safety conditions for the persons, for the machine and for the enviroment, impersonating an elementary diagnostic of breakdowns and of malfunction conditions by performing simple functional verify operations , in the height respect of the actual safety and health norms.

The informations for the installation, the assemblage, the dismantlement, the handling, the adjustment, the reparation and the contingent accessories, devices etc. installation are destined - and then executable - always and in exclusive way from specialized warned and educated personnel, or directly from the TECHNICAL AUTHORIZED ASSISTANCE, in the height respect of the manufacturer recommendations and the actual safety and health norms.

The devices can't be used outside a box. The user must always insert the cards in a container that respect the actual safety normative. The protection of this container is not threshold to the only atmospheric agents, but specially to mechanic, electric, magnetic, etc. ones.

To be on good terms with the products, is necessary guarantee legibility and conservation of the manual, also for future references. In case of deterioration or more easily for technical updates, consult the AUTHORIZED TECHNICAL ASSISTANCE directly.

To prevent problems during card utilization, it is a good practice to read carefully all the informations of this manual. After this reading, the user can use the general index and the alphabetical index, respectly at the begining and at the end of the manual, to find information in a faster and more easy way.

CARD VERSION

The present handbook is reported to the GPC® 153 card release 180398 and later. The validity of the bring informations is subordinate to the number of the card release. The user must always verify the correct correspondence among the two denotations. On the card the release number is present in more points both board printed diagram (serigraph) and printed circuit (for example near battery BT1 and connector CN2 both on the component sideand on the solder side).
GPC® 153 is a powerful, low cost, controller module capable of operating in stand alone mode or as an intelligent peripheral, and/or remoted, in a wider telecontrol or acquisition network. The GPC® 153 board is secured in a plastic mount for connection to Omega rails DIN 46277-1 and DIN 46277-3, thereby dispensing with the need of rack and allowing a cheaper mounting direct to the electrical control panel. GPC® 153 board is provided with a set of Abaco® standard connectors, allowing the User to connect it to any of the BLOCK I/O module or to third parts or User made interfaces to the field.

The Abaco® I/O BUS connector allows to drive directly the ZBR 324÷ZBR 84 and ZBT 324÷ZBT 84 cards and through ABB 03, ABB 05 and so on, it is possible to run all peripheral cards available on Abaco® BUS. The powerful and easy-to-use ROM-based FGDOS Operating System makes easy to program the board and to take advantage of its many resources. FGDOS supports high level languages like BASIC, PASCAL, C and so on, places at user's disposal all the memory resources as ROM/RAM Disks, allowing an immediate high-level execution of these devices, manages PCMCIA RAM Cards through the MCI 64 board and on-board serial EEPROMs directly. In addiction, FGDOS manages directly LCDs, fluorescent displays and a matrix keyboard. The KDL-224 serie boards allow an immediate use of these devices management features, while the QTP24P Operator Panel represents a valid low-cost solution to integrate display and keyboard in a single object. This Panel, offered in open frame version, has the same esthetics of QTP24 but can be controlled directly by GPC® 153 because it is designed to work without an on-board controller. FGDOS can also write the user program in a FLASH memory without need of external hardware.

- Size 100x149 mm with interface to Industrial ABACO® I/O BUS.
- 84C15 CPU with 20 MHz crystal.
- Up to 512K EPROM or FLASH EPROM and up to 512K SRAM. Through FGDOS the memory that exceed 64K is managed as RAM/ROM disk. It is possible deleting and re-programming the on board FLASH, automatically, with the user programm.
- Serial EEPROM up to 8K.
- 6 way Dip Switch and two configuration jumpers readable by software.
- Activity LED driven through software.
- 2 RS 232 serial lines, one configurable in RS 422, RS 485 or Current Loop managed by the powerful SIO and software manageable baud rate generators, up to 115 KBAud
- 16 I/O TTL lines, bit-level set via software (PIO).
- Four 8 bits timer counters: 2 used ad baud rate generator and 2 on I/O connector.
- 8 A/D Converter multi range lines, 6 µs, Track & Hold, 5MHz bandwidth, 100Ksps sampling rate, software settable ranges are 0÷5 V, 0÷10 V, ±5 V, ±10 V or hardware settable ranges are 0÷20 mA or 4÷20 mA.
- Real Time Clock able to up date day, month, year, week day, seconds, minutes and hours. It can be programmed to issue an INT at intervals defined by software.
- Watch Dog resettable by software and display through LED.
- Back up circuit for SRAM and RTC provided of lithium battery and connector for external battery. The battery charge status can be acquired by software.
- One I/O Abaco® 20 pins connector
- One A/D Abaco® 20 pins connector
- On-board logic protected against transients by TransZorb™
- Low-Power Halt Mode, Idle Mode, Stop Mode.
- Single power supply +5Vdc, 280 mA.
- Wide range of base software and development tools that allow card use with only a standard PC, connected through serial line. Among these: FGDOS 153; PASCAL 80; CBZ 80; NSB8; RSD 153; HI TECH C 80; GET 80; DDS MICROC 85; NO ICE Z80; etc.

**SIO**

Microprocessor peripheral device that manages two lines for serial communication. It can be used to connect to external systems capable to support RS 232, RS 422, RS 485 and Current loop electric protocols. Simply by programming four registers allocated in the microprocessor I/O addressing space, the User can set the baud rate, stop bits number, length of character, parity and handshake of each serial line.

**TIMER COUNTER**

It is a microprocessor peripheral device that manages four 8 bit timers counters. Each channel can be set with a different prescaler and with a different operating mode (timer with external trigger, counter of rising edge or falling edge, etc.), including eventual interrupt generation. CTC is connected to the external electronics by two digital signals and it is completely driven by software programming four registers allocated in microprocessor I/O addressing space, by a specific control logic. Two channels out of four are used by the baud rate generator for the serial lines.

**PIO TTL I/O LINES**

It is a microprocessor peripheral device that manages 16 TTL I/O lines divided in two 8 bit parallel ports. The lines direction is software settable at bit level and interrupts can be generated. In this way an external status can obtain CPU control in any condition, with a fast response time. The PIO is completely driven by software programming four registers allocated in microprocessor I/O addressing space, by a specific control logic.

**REAL TIME CLOCK**

GPC® 153 has installed on-board a Real Time Clock capable of a completely autonomous management of hours, minutes, seconds, day of month, month, year and day of week. The device is completely software programmable by 16 registers mapped in the CPU I/O space and is supplied by a back-up circuitry which warrants the validity of its data in any operating condition. In addition RTC section is capable to generate periodic interrupts, for example to wake the CPU away from halt, idle or stop conditions.

**MEMORY MANAGEMENT UNIT**

A specific MMU section has been designed to manage in a practical and efficient way the memory configurations that the GPC® 153 board can assume. The use is provided with a 64K work area, which can be easily allocated anywhere in the 1024K maximum memory space.
CPU

The **GPC® 153** uses the powerfull microprocessors 84C15 produced by ZILOG. This 8 bit microprocessor is code compatible with standard Z80 CPU and it has an extended instruction set, fast execution time, fast data handling and an efficient vectorized interrupt management. Some of the most important 84C15 features are its internal peripheral devices, as below described:

- 16 I/O lines programmable at bit level, capable to generate interrupts (PIO);
- four 8 bit timers counters, with programmable prescaler (CTC);
- 2 synchronous or asynchronous serial lines, provided of hardware handshake signals (SIO);
- watch dog timer;
- wait state generator;
- programmable clock frequency;
- interrupt controller;
- idle mode or power down mode.

For further information, please refer to specific documentation of the manufacturing company, or to appendix B of this manual.

SERIAL COMMUNICATION

The serial communication lines are completely software configurable for protocol and speed (from 600 to 115200 Baud); simply by programming the microprocessor SIO and the on board baud rate generators, the User can set the baud rate, stop bits number, lenght of character, parity and handshake of each serial line. For further information about these programmable sections, please refer to chapter "BAUD RATE GENERATOR" and to appendix B of this manual.

One of the two serial lines is always buffered with RS 232 electric protocol, while the second one is hardware configurable in fact connecting some jumpers, the User can select the electric standard interface between RS 232, RS 422, RS 485 and Current Loop; for RS 422-485 the transmitter activation and the line direction can be set by software. The chapter "SERIAL COMMUNICATION SELECTION" contains a detailed description of available hardware configurations.

Normally the card is provided with two RS 232 interfaces and a different configuration must be specified when ordering.

**ABACO® I/O BUS**

One of the most important features of **GPC® 153** is its possibility to be interfaced to industrial **ABACO® I/O BUS**. Thanks to its standard **ABACO® I/O BUS** connector, the card can be connected to some of the numerous **grifo®** boards, both intelligent and not. For example the user can directly use cards for analog signals acquisition (A/D like **ABC 04** or **ABB 08**), cards for analog signals generation (D/A), cards for digital I/O signals management, cards with timers and counters, cards for temperature controls, etc. also custom boards designed to satisfy specific needs of the end user.

Using **ABB 03** or **ABB 05** mother boards it is possible manage all the BUS **ABACO® single EURO cards**. So **GPC® 154** becomes the right component for each industrial automation system, in fact **ABACO® I/O BUS** makes the card easily expandable with the best price/performance ratio.
**Figure 1: Block diagram**

- **CPU 84C15**
- **CTC**
- **SIO**
- **J6**
- **CN4** Power
- **CN1** 
  - ABACO® I/O Bus
- **CN2** Back Up
- **CN5** 16 I/O Lines
- **CN6** 8 A/D Lines
- **OPTIONAL POWER SUPPLY**
- **A/D MAX 197**
- **WATCH DOG Activity LED BUZZER**
- **DSW1**
- **IC17 EEPROM**
- **IC 5 EPROM**
- **IC4 SRAM**
- **IC3 RTC**
- **ON BOARD BATTERY**

- **DRIVERS**
  - RS232
  - RS422-485
  - CURRENT LOOP

- **+5 Vdc**
CLOCK DEVICES

On **GPC® 153** there are two separate circuits with crystal to generate the clock signal for the microprocessor (20 MHz) and the timing signal for baud rate generator section (1.8432 MHz). The choice of using two circuits and as many separated crystals, has the advantage to change the microprocessor working speed (when best performances are required) without additional changes in communication software or firmware. The best time performances are always obtained both for execution time and serial communication, fulfilling the User necessity.

CONTROL LOGIC

The addresses of all peripheral device's registers and of memory devices on **GPC® 153** are assigned through a specific control logic that allocates all these devices in the microprocessor addressing space.
For further information please refer to chapter "Addresses and Maps" of this manual.

MEMORY DEVICES

On the card can be mounted up to 1032K of memory divided with a maximum of 512K Byte EPROM or FLASH EPROM, 512K Byte SRAM, and 8K Byte serial EEPROM. The memory configuration must be chosen considering the application to realize or the specific requirements of the user. Normally the card is provided with 128K SRAM and 512 bytes of serial EEPROM, all different configurations must be specified from the user, at the moment of the order. By means of the on-board back-up circuit and the external battery, memory can keep datas also in absence of power supply. The addressing of memory devices is controlled by a specific on-board control logic, that provides to allocate the devices in the microprocessor address space. For further informations about memory configuration, sockets description and jumpers connection, please refer to chapter "Hardware", "Peripheral Devices Software Description" and to the paragraph "Memory Selection".

WATCH DOG SECTIONS

**GPC® 153** is provided with two separated Watch Dog circuits that can reset the card at programmable time intervals, if not retriggered. Watch dog circuits are used when the User want to exit from endless loops or to reset anomalous conditions not estimated by application program. There is a monostable section, inside the microprocessor, with programmable intervention time and a monostable/astable section, outside the microprocessor, with 1.5 s fixed intervention time. By software the User can perform a complete management of the devices, using specific registers allocated in microprocessor I/O addressing space.
A/D CONVERTER

The MAX 197, multi-range, 12-bit data-acquisition system (DAS) uses successive approximation and internal track/hold circuitry. Main features of this device are: resolution 12 bits in unipolar mode or 11 bits plus sign in bipolar mode; multi-range software configurable inputs, allowed ranges are
0 \div 5 \text{ V}, 0 \div 10 \text{ V}, \pm 5 \text{ V}, \pm 10 \text{ V}, \text{ by hardware it is possible to configure } 0 \div 20 \text{ mA and } 4 \div 20 \text{ mA ranges; conversion time per channel } 6 \mu \text{sec; sample rate per channel } 100 \text{ Ksps; easy software management; end-of-conversion interrupt generation.}
A/D Converter section is completely software driven, through the programming of two registers allocated in the CPU I/O space by the control logic. A/D Converter section is optional and must be explicitly requested in the order. 
The code to require A/D converter optional section in the order is .AD.

POWER SUPPLY

The GPC® 153 board can be optionally provided with the power supply section capable to generate the unique +5 Vdc voltage needed to supply the board. Should the supply section be absent, the +5Vdc voltage is the only one needed to supply the board, otherwise two different types of supply sections are available: linear supply section, which requires an alternate input voltage in the range 6\div 12 \text{ Vac; switching supply section, which requires an alternate input voltage in the range } 15\div 24 \text{ Vac (for further informations please refer to the paragraph “SUPPLY VOLTAGES”. The supply voltage can be supplied through proper standard connectors fast and easy to use. The power supply circuit is designed for reducing the consumption (the microprocessor power down and idle modes are available) and for increasing the electrical noise immunity. The type of supply cannot be changed by the User so it must be specified in the order.

RESET KEY

GPC® 153 board features a comfortable reset key that, when pushed, restarts the board from a general reset condition. The main purpose of this key is to exit from infinite loop conditions, useful especially during the debug phase or to warrant a special starting status.
BOARD CONFIGURATION

To make the board and the applications program developed for it easier to configure a 6 pins Dip Switch (DSW1) and two jumpers (J10 and J11) have been installed. One of the jumpers (J11) has the purpose to select the RUN/DEBUG modality and to configure the management software. The possibility to read by software the status of these devices allows the User the chance to manage several working conditions through an unique program without no need to employ more input signals (characteristic applications are: language selection, program parameter determination, working modalities selection, etc.).

For further informations about the above described devices, please refer to the manufacturer documentations or to appendix B of this manual.
**Figure 2: Card Photo**
TECHNICAL FEATURES

GENERAL FEATURES

On board resources:
16 Input/Output (PIO)
4 eight bits TTL Timer Counter (CTC)
1 RS 232 bidirectional line
1 RS 232, RS 422, RS 485 or Current Loop
1 CPU internal Watch Dog
1 external Watch Dog
1 Real Time Clock (RTC)
1 six dips Dip Switch
8 A/D Converter lines
1 Buzzer
1 power supply section

Industrial ABACO® I/O BUS

Addressable memory:
IC 5: EPROM from 128K x 8 to 512K x 8
FLASH EPROM from 128K x 8 to 512K x 8
IC 4: SRAM 128K x 8 or 512Kx8
IC 17: serial EEPROM from 256 byte to 8192 byte

CPU:
ZILOG 84C15

CPU frequency:
20 MHz

Baud Rate generator frequency:
1.8432 MHz

A/D Converter resolution:
12 bit + sign

A/D conversion time:
6 µsec

Watch Dog intervent time:
1500 msec through an RC network (external watch dog)

PHYSICAL FEATURES

Size (W x H x D):
100 x 149 x 25 mm (without container)
110 x 160 x 60 mm (with container for DIN rails)

Weight:
190 g (without container)
300 g (with container for DIN rails)

Connectors:
CN1: 26 pins low profile vertical M
CN2: 2 pins low profile vertical M
CN3A: 6 pins plug 90 degreeses F
CN3B: 6 pins plug 90 degreeses F
CN4: 2 pins quick extraction screw terminal M
CN5: 20 pins low profile vertical M
CN6: 20 pins low profile vertical M

Temperature range: from 0 to 70 Centigrade degrees
Relative humidity: 20% up to 90% (without condense)

ELECTRIC FEATURES

Power supply: +5 Vdc (without power supply section)
6÷12 Vac * (with linear power supply section)
15÷24 Vac (with switching power supply section)

Current consumption on 5 Vdc: 280 mA

On board back up battery: 3.0 Vdc; 1/2 AA

Current available on +5 Vdc for external loads: 120 mA * (switching power supply section)
720 mA * (linear power supply section)

External back up battery: 3.6÷5 Vdc

Back up current: 2 μA

Analog voltage inputs: 0÷5; 0÷10; ±5; ±10 Vdc (software settable)

Analog current inputs: 0÷20; 4÷20 mA (with conversion module)

Analog inputs impedance: 21 KΩ (unipolar mode)
16 KΩ (bipolar mode)

RS422, 485 termination network:
line termination = 120Ω
Pull-up on positive = 3.3KΩ
Pull-down on negative = 3.3KΩ

* Data here reported are referred to a 20 centigrade degreeses environmental temperature (for further informations please refer to the paragraph “SUPPLY VOLTAGES”).
INSTALLATION

In this chapter there are the information for a right installation and correct use of the card. The user can find the location and functions of each connectors, jumpers and some explanatory diagrams.

CONNECTIONS

The GPC®153 board has 6 connectors that can be linked to other devices or directly to the field, according to system requirements. In this paragraph there are connectors pin out, a short signals description (including the signals direction), connectors location (see figure 20) and some electrical diagrams that show the on board circuit of each connector.

CN 4 - POWER SUPPLY CONNECTOR

CN4 is a 2 pins screw terminal connector. The board supply voltage must be provided through this connector. When using the board without any power supply section, the +5 Vdc must be provided through pin 26 (+Vdc) and pin 25 (GND) of CN1.

Signals description:

\[
15\div24 \text{ Vac} / 6\div12 \text{ Vac} =
\]

- I - 15÷24 Vac power supply signals (switching supply section)
- I - 6÷12 Vac power supply signals (linear supply section)
CN1 - ABACO® I/O BUS CONNECTOR

CN1 is a 26 pins, male, vertical, low profile connector. Through CN1 the card can be connected to external expansion modules developed by the user or to the numerous grifo® boards, both intelligent and not. All this connector's signals are at TTL level and follow the ABACO® I/O BUS standard.

**Figure 4: CN1 - ABACO® I/O BUS CONNECTOR**

 Signals description;

- **A0-A7** = O - Address BUS.
- **D0-D7** = I/O - Data BUS.
- **/INT BUS** = I - Interrupt request (open collector type).
- **/NMI BUS** = I - Non maskable interrupt (open collector type).
- **/IORQ** = O - Input output request.
- **/RD** = O - Read cycle status.
- **/WR** = O - Write cycle status.
- **/RESET** = O - Reset.
- **+5 Vdc** = I/O - +5 Vdc power supply.
- **GND** = - Ground signal.
- **N.C.** = - Not connected.
CN3A - SERIAL LINE A CONNECTOR

CN3A is a 6 pins, female PLUG connector for serial communication. Placing of the signal has been designed to reduce interference and electrical noise and to simplify connections with other systems, while the electric protocol follows the CCITT normative.

**FIGURE 5: CN3A - SERIAL LINE A CONNECTOR**

Signals description:

<table>
<thead>
<tr>
<th>Signal</th>
<th>Code</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>RxD RS 232</td>
<td>I</td>
<td>Receive Data: RS 232 Receive Data signal</td>
</tr>
<tr>
<td>TxD RS 232</td>
<td>O</td>
<td>Transmit Data: RS 232 Transmit Data signal</td>
</tr>
<tr>
<td>CTSA RS 232</td>
<td>I</td>
<td>Clear To Send</td>
</tr>
<tr>
<td>RTSA RS 232</td>
<td>O</td>
<td>Request To Send</td>
</tr>
<tr>
<td>+5 Vdc/GND</td>
<td>I</td>
<td>+5 Vcc or ground signal</td>
</tr>
<tr>
<td>GND</td>
<td></td>
<td>Ground signal</td>
</tr>
</tbody>
</table>
FIGURE 6: SERIAL COMMUNICATION CONNECTION DIAGRAM
**Figure 7: RS 232 Point-to-Point Connection Example**

- CN6A/B GPC® 153
  - 4 CTS RS 232
  - 3 RTS RS 232
  - 2 TxD RS 232
  - 5 RxD RS 232
  - 6 GND

- External Systems
  - CTS
  - RTS
  - TxD
  - RxD
  - GND

**Figure 8: RS 422 Point-to-Point Connection Example**

- CN3B GPC® 153
  - 4 RXB- RS 422
  - 5 RXB+ RS 422
  - 3 TXB- RS 422
  - 2 TXB+ RS 422
  - 6 GND

- External System
  - TX -
  - TX +
  - RX -
  - RX +
  - GND

**Figure 9: RS 485 Point-to-Point Connection Example**

- CN3B GPC® 153
  - 4 RXTXB- RS 485
  - 5 RXTXB+ RS 485
  - 6 GND

- External System
  - TX / RX -
  - TX / RX +
  - GND
Please remark that in a RS 485 network two forcing resistors must be connected across the net and two termination resistors (120 Ω) must be placed at its extremis, respectively near the Master unit and the Slave unit at the greatest distance from the Master.

Forcing and terminating circuitry is installed on GPC® 153 board. It can be enabled or disabled through specific jumpers, as explained later.

For further informations please refer to TEXAS INSTRUMENTS Data-Book, "RS 422 and RS 485 Interface Circuits", the introduction about RS 422-485.
**Figure 11:** 4 wires Current Loop point-to-point connection example

**Figure 12:** 2 wires Current Loop point-to-point connection example
Possible Current Loop connections are two: 2 wires and 4 wires. These connections are shown in figures 11 and 12 where it is possible to see the voltage for VCL and the resistances for current limitation (R). The supply voltage varies in compliance with the number of connected devices and voltage drop on the connection cable.

The choice of the values for these components must be done considering that:
- circulation of a **20 mA** current must be guaranteed;
- potential drop on each transmitter is about **2.35 V** with a **20 mA** current;
- potential drop on each receiver is about **2.52 V** with a **20 mA** current;
- in case of shortcircuit each transmitter must dissipate at most **125 mW**;
- in case of shortcircuit each receiver must dissipate at most **90 mW**.

For further info please refer to HEWLETT-PACKARD Data Book, (HCPL 4100 and 4200 devices).
CN3B - SERIAL LINE B CONNECTOR

CN3B is a 6 pins, female PLUG connector for serial communication. Placing of the signal has been designed to reduce interference and electrical noise and to simplify connections with other systems, while the electric protocols follow the CCITT normative.

![Diagram of CN3B Connector]

Signals description:

- **RXTXB- RS 485** = I - Receive Data Negative: negative signal for RS 485 serial differential receive
- **RXTXB+ RS 485** = I - Receive Data Positive: positive signal for RS 485 serial differential receive
- **TXB- RS 422** = O - Transmit Data Negative: negative signal for RS 422 serial differential transmit
- **TXB+ RS 422** = O - Transmit Data Positive: positive signal for RS 422 serial differential transmit
- **RxDB RS 232** = I - Receive Data: RS 232 Receive Data signal
- **TxDB RS 232** = O - Transmit Data: RS 232 Transmit Data signal
- **RXB- C.L.** = I - Receive Data Negative: negative signal for Current Loop serial differential receive
- **RXB+ C.L.** = I - Receive Data Positive: positive signal for Current Loop serial differential receive
- **TXB- C.L.** = O - Transmit Data Negative: negative signal for Current Loop serial differential transmit

*Figure 14: CN3B - Serial Line B Connector*
**TXB+ C.L.** = O - Transmit Data Positive: positive signal for Current Loop serial differential transmit
**+5 Vdc/GND** = I  +5 Vdc or ground signal
**GND** = Ground signal

**CN2 - EXTERNAL BACK UP BATTERY CONNECTOR**

CN2 is a 2 pins, vertical, male connector with 2,54mm pitch. Through CN1 the user can connect an external battery for SRAM and RTC back up when the power supply is switched off (for further information please refer to chapter "BACK UP").

![CN2 Connector Diagram](image)

**Figure 15: CN2 - External back up battery connector**

Signals description:

**+Vbat** = I - External back up battery positive pin
**GND** = - External back up battery negative pin
CN5 - PIO I/O CONNECTOR

CN5 is a 20 pins, male, 90°, low profile connector with 2.54 mm pitch.  
On CN6 are available the two 8 bits parallel ports of CPU internal PIO that can be connected to the external world.  
All these signals follow TTL standard.

![CN5 - PIO I/O Connector Diagram]

**FIGURE 16: CN5 - PIO I/O CONNECTOR**

- **PIO PA.n** = I/O - CPU internal PIO port A n-th digital signal
- **PIO PB.n** = I/O - CPU internal PIO port A n-th digital signal
- **+5 Vdc** = O - Power supply signal +5 Vdc
- **GND** = - Ground signal
- **N.C.** = - Not Connected
FIGURE 17: PIO CONNECTION DIAGRAM
CN6 - A/D CONVERTER INPUTS CONNECTOR

CN6 is a 20 pins, male, 90°, low profile connector with 2.54 mm pitch. Through CN5 an external device can connect up to 8 analog inputs. These are low impedance lines directly connected to the on board A/D Converter and are provided with a capacitive filter. The inputs may vary in the ranges 0÷5 V, 0÷10 V, ±5 V or ±10 V or 0÷20 mA, 4÷20 mA. By installing an opportune conversion module it is possible to acquire 8 single ended channels as currents inputs in the ranges 0÷20 mA or 4÷20 mA. Signals location on this connector has been designed to reduce problems due to interference.

FIGURE 18: CN5 - A/D CONVERTER INPUTS CONNECTOR

Signals description:

CHn = I - Analog input signal connected to A/D Converter n-th channel
AGND = - Analog ground signal
+5 Vdc = O - Power supply signal +5 Vdc
GND = - Digital ground signal
N.C. = - Not Connected
Figure 19: A/D Converter input diagram
TRIMMERS AND CALIBRATION

On GPC® 153 is available a trimmer, named RV1, that calibrates the Vref voltage of the A/D Converter section. The GPC® 153 is subjected to a careful test that verifies and calibrates all the card sections. To easily locate the trimmer, please refer to figure 20. The calibration is executed in laboratory, with a controlled +20°C room temperature, following these steps:

- The A/D voltage reference (Vref) is calibrated through RV1 trimmer, by using a 5 digits precision multimeter, to a value of +4.096 Vdc, on test point TP1.

- The correspondence between the analog input signal and the combination read from A/D is verified. This check is performed with a reference signal connected to A/D inputs and testing that the A/D combination and the theoretical combination differ at maximum of the A/D section errors sum.

- The trimmer is blocked with paint.

The analog interfaces use high precision components that are selected during mounting phase to avoid complicate and long calibration procedures. After the calibration, the on board trimmer is blocked with paint to maintain calibration also in presence of mechanic stresses (vibrations, movements, delivery, etc.).

The user must not modify the card calibration, but if thermic drifts, time drifts and so on, make necessary a new calibration, the user must strictly follow the previous described procedure.

The circuitry that generates the reference voltage defines also the full range for all the 8 analog input channels; by software it is possible to define the range of the signals: 0÷5 V, 0÷10 V, ±5 V, ±10 V. It is also possible to define by hardware the ranges 0÷20 mA or 4÷20 mA.

The User must NOT intervent on the circuit that generates the reference voltage, however if this should be necessary (example: for time derives) then he/she must follow the above mentioned procedure.

To easily locate RV1 and TP1 please refer to figure 20.

TEST POINT

The board is provided with a test point called TP1, that allows to read, through a galvanically isolated multimeter, the reference voltage calibrated in laboratory and whose value is Vref=4.096 V. TP1 is made of two contacts:

```
pin +  ->  Vref
pin -  ->  GND
```

To easily locate the test point contacts please refer to figure 20, while for further informations about Vref signal please refer to the paragraph “TRIMMER AND CALIBRATION”.

Page 26
TYPE OF ANALOG INPUT SELECTION

GPC® 153 board can accept analog voltage and/or current inputs, as described in the previous paragraphs and chapters. The input type selection must be made during the order phase and is performed mounting a specific voltage-current conversion module (option code .8420) made by precision resistors. In detail:

- R48 -> channel 0
- R47 -> channel 1
- R46 -> channel 2
- R45 -> channel 3
- R44 -> channel 4
- R43 -> channel 5
- R42 -> channel 6
- R41 -> channel 7

Should the voltage-current conversion module not to be mounted (default case) the corresponding channel accepts a voltage input signal in the ranges 0÷5 V, 0÷10 V, ±5 V or ±10 V; otherwise a current input signal is accepted. In this latter case the input range must be set as 0÷5 V, so the value of the above mentioned resistors is obtained by the following spread:

$$ R = \frac{5 \text{ V}}{I_{\text{max}}} $$

Usually the voltage-current conversion modules are made using 248 Ω precision resistors, corresponding to 4÷20 mA or 0÷20 mA.

Any eventual configuration out of this standard shold be asked directly to grifo®.

To easily locate the voltage-current conversion module please refer to figure 20.

I/O CONNECTION

To prevent possible connecting problems between GPC® 153 and the external systems, the user has to read carefully the information of the previous paragraphs and he must follow these instructions:

- For RS 232, RS 422, Current Loop or RS 485 communication signals the User must follow the standard rules of these protocols.

- For all TTL signals the user must follow the rules of this electric standard. The connected digital signal must be always referred to card digital ground (GND). For TTL signals, the 0 Vdc level corresponds to logic state "0", while 5Vdc level corresponds to logic state "1".

- The analog inputs (A/D section) must be connected to low impedance signals in the following ranges: 0±5 V, 0±10 V, ±5 V or ±10 V according to selected voltage reference (Vref) or 0±20 mA or 4±20 mA if the conversion module is installed. Remember that the eight analog inputs available on CN6 are provided of filter capacitors that ensure an higher stability of the acquired signals, but reduce at the same time the bandwidth frequency. For further informations please refer to the paragraph “TYPE OF ANALOG INPUT SELECTION”.

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DIGITAL I/O INTERFACES

Through CN5 (I/O Abaco® standard connector) the GPC® 153 card can be connected to all of the numerous grifo® boards featuring the same standard pin out. Installation of these interface is very easy; in fact only a 20 pins flat cable (code FLT.20+20) is required, while the software management of these interfaces is as easy; in fact most of the software packages available for GPC® 153 card are provided with the necessary procedures. Remarkable modules are:

- **QTP 16P, QTP 24P, KDL x24, KDF 224, DEB 01**, etc. that solve all the local operator interfacing problems. These modules are provided with all the resources needed to obtain a high-level human-machine interface (they feature alphanumeric displays, matrix keyboard and visualization LEDs) at a short distance from GPC® 153 card. The available software drivers allow to manage the operator interface resources directly through the high-level instructions for console management.

- **IAC 01, DEB 01**: it is an interface for CENTRONICS parallel printer that can be connected with a standard printer cable. The printer is managed by software through the high level instructions of the selected programming language (LPRINT for BASIC, PRINTF for C, etc.).

- **MCI 64**: it a large mass memory support that can directly manage the PCMCIA memory cards (RAM, FLASH, ROM, etc.) in their available sizes. About software the developed drivers provide a complete file system interfacing allowing to access the informations stored in the memory card directly through the high-level file management instructions.

- **RBO xx, TBO xx, XBI xx, OBI xx**: these are buffer interfaces for I/O TTL signals. With these modules the TTL input signals are converted in NPN or PNP optoisolated inputs and the TTL output signals are converted in relays or transistor optoisolated outputs.

For more informations refer to "EXTERNAL CARDS" chapter and the software tools documentation.
FIGURE 20: CONNECTORS, MEMORIES, DIP SWITCH ETC. LOCATION
JUMPERS

On GPC® 153 there are 16 jumpers (4 are solder jumpers) for card configuration. Connecting these jumpers, the user can define for example the memory type and size, the peripheral devices functionality and so on. Below there is the jumpers list, location and function:

<table>
<thead>
<tr>
<th>JUMPERS</th>
<th>N. PIN</th>
<th>USE</th>
</tr>
</thead>
<tbody>
<tr>
<td>J1</td>
<td>2</td>
<td>Connects pin 26 of CN1 to +5 Vdc board's power supply</td>
</tr>
<tr>
<td>J2</td>
<td>3</td>
<td>Selects size of memory device on IC4</td>
</tr>
<tr>
<td>J3</td>
<td>3</td>
<td>Selects type of memory device on IC5</td>
</tr>
<tr>
<td>J4</td>
<td>3</td>
<td>Selects type of memory device on IC5</td>
</tr>
<tr>
<td>J5</td>
<td>2</td>
<td>Connects on board lithium battery BT1 to back up circuitry</td>
</tr>
<tr>
<td>J6</td>
<td>8</td>
<td>Defines CTC channels 2 and 3 and ABACO® I/O BUS interrupt signals connections</td>
</tr>
<tr>
<td>J7</td>
<td>2</td>
<td>Connects Real Time Clock interrupt signal</td>
</tr>
<tr>
<td>J8</td>
<td>4</td>
<td>Defines the connection of Watch Dog and reset circuitries</td>
</tr>
<tr>
<td>J9</td>
<td>2</td>
<td>Connects A/D Converter interrupt signal</td>
</tr>
<tr>
<td>J10</td>
<td>2</td>
<td>Determines the status of /DCDB handshake signal, used as generic User input</td>
</tr>
<tr>
<td>J11</td>
<td>3</td>
<td>Determines the status of /SYNCB handshake signal, used to select RUN or DEBUG modality</td>
</tr>
<tr>
<td>J12</td>
<td>5</td>
<td>Selects the communication type for serial line B between RS 422 and RS 485</td>
</tr>
<tr>
<td>JS1, JS2</td>
<td>2</td>
<td>Connect termination and forcing resistor network to reception signal in RS 422, RS 485</td>
</tr>
<tr>
<td>JS3</td>
<td>3</td>
<td>Selects the type of connection for pin 1 of CN6B</td>
</tr>
<tr>
<td>JS4</td>
<td>3</td>
<td>Selects the type of connection for pin 1 of CN6A</td>
</tr>
</tbody>
</table>

**Figure 21: JUMPERS summarizing table**

The following tables describe all the right connections of GPC® 153 jumpers with their relative functions. To recognize these valid connections, please refer to the board printed diagram (serigraph) or to figure 33 of this manual, where the pins numeration is listed; for recognizing jumpers location, please refer to figures 23 and 24.

The "*" used in the following tables, denotes the default connection, or on the other hand the connection set up at the end of testing phase, that is the configuration the User receives.
### 2 PINS JUMPERS

<table>
<thead>
<tr>
<th>JUMPERS</th>
<th>CONNECTION</th>
<th>USE</th>
<th>DEF.</th>
</tr>
</thead>
<tbody>
<tr>
<td>J1</td>
<td>not connected</td>
<td>Does not connect pin 26 of CN1 to +5 Vdc of board's power supply</td>
<td></td>
</tr>
<tr>
<td></td>
<td>connected</td>
<td>Connects pin 26 of CN1 to +5 Vdc of board's power supply</td>
<td>*</td>
</tr>
<tr>
<td>J5</td>
<td>not connected</td>
<td>Does not connect on board battery BT1 to the back up circuitry</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>connected</td>
<td>Connects on board battery BT1 to the back up circuitry</td>
<td></td>
</tr>
<tr>
<td>J7</td>
<td>not connected</td>
<td>Does not connect interrupt signal /INT of the CPU to Real Time Clock</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>connected</td>
<td>Connects interrupt signal /INT of the CPU to Real Time Clock</td>
<td></td>
</tr>
<tr>
<td>J9</td>
<td>not connected</td>
<td>Does not connect interrupt signal /INT of the CPU to A/D Converter</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>connected</td>
<td>Connects interrupt signal /INT of the CPU to A/D Converter</td>
<td></td>
</tr>
<tr>
<td>J10</td>
<td>not connected</td>
<td>Connects signal /DCDB of SIO to +5 Vdc, setting it in the logic state 1</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>connected</td>
<td>Connects signal /DCDB of SIO to GND, setting it in the logic state 0</td>
<td></td>
</tr>
<tr>
<td>JS1, JS2</td>
<td>not connected</td>
<td>Do not connect forcing and terminating circuitry for serial line B in RS 422-485</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>connected</td>
<td>Connect forcing and terminating circuitry for serial line B in RS 422-485</td>
<td></td>
</tr>
</tbody>
</table>

**Figure 22: 2 PINS JUMPERS table**

The "*" used in the following tables, denotes the default connection, or on the other hand the connection set up at the end of testing phase, that is the configuration the User receives.
Figure 23: Jumpers Location (Component Side)
**Figure 24: Jumpers Location (solder side)**
### 3 PINS JUMPERS

<table>
<thead>
<tr>
<th>JUMPERS</th>
<th>CONNECTION</th>
<th>USE</th>
<th>DEF.</th>
</tr>
</thead>
<tbody>
<tr>
<td>J2</td>
<td>position 1-2</td>
<td>Selects IC 4 for SRAM size 128K Byte</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>position 2-3</td>
<td>Selects IC 4 for SRAM size 512K Byte</td>
<td></td>
</tr>
<tr>
<td>J3</td>
<td>position 1-2</td>
<td>Selects IC 5 for EPROM</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>position 2-3</td>
<td>Selects IC 5 for FLASH EPROM</td>
<td></td>
</tr>
<tr>
<td>J4</td>
<td>position 1-2</td>
<td>Selects IC 5 for EPROM</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>position 2-3</td>
<td>Selects IC 5 for FLASH EPROM</td>
<td></td>
</tr>
<tr>
<td>J11</td>
<td>position 1-2</td>
<td>Connects signal /SYNCB of SIO to GND, turning LD9 on and selecting RUN modality</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>position 2-3</td>
<td>Connects signal /SYNCB of SIO to +5 Vdc, turning LD8 on and selecting DEBUG modality</td>
<td></td>
</tr>
<tr>
<td>JS3</td>
<td>position 1-2</td>
<td>Connects pin 1 of CN3B to GND</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>position 2-3</td>
<td>Connects pin 1 of CN3B to +5 Vdc</td>
<td></td>
</tr>
<tr>
<td>JS4</td>
<td>position 1-2</td>
<td>Connects pin 1 of CN3A to GND</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>position 2-3</td>
<td>Connects pin 1 of CN3A to +5 Vdc</td>
<td></td>
</tr>
</tbody>
</table>

**Figure 25: 3 pins jumpers table**

### 4 PINS JUMPER

<table>
<thead>
<tr>
<th>JUMPERS</th>
<th>CONNECTION</th>
<th>UTILIZZO</th>
<th>DEF.</th>
</tr>
</thead>
<tbody>
<tr>
<td>J8</td>
<td>not connected</td>
<td>Connects reset circuitry only to key P1</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>position 1-2</td>
<td>Connects internal Watch Dog circuitry to CPU /INT signal</td>
<td></td>
</tr>
<tr>
<td></td>
<td>position 2-3</td>
<td>Connects internal Watch Dog circuitry to reset circuitry</td>
<td></td>
</tr>
<tr>
<td></td>
<td>position 3-4</td>
<td>Connects external Watch Dog circuitry to reset circuitry</td>
<td></td>
</tr>
</tbody>
</table>

**Figure 26: 4 pins jumper table**
5 PINS JUMPER

<table>
<thead>
<tr>
<th>JUMPERS</th>
<th>CONNECTION</th>
<th>USE</th>
<th>DEF.</th>
</tr>
</thead>
<tbody>
<tr>
<td>J12</td>
<td>position 1-2</td>
<td>Enables RS 485 communication (2 wires half</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>and 3-4</td>
<td>duplex) on serial line B</td>
<td></td>
</tr>
<tr>
<td></td>
<td>position 2-3</td>
<td>Enables RS 422 communication (4 wires half</td>
<td></td>
</tr>
<tr>
<td></td>
<td>and 4-5</td>
<td>or full duplex) on serial line B</td>
<td></td>
</tr>
</tbody>
</table>

**FIGURA 27: 5 PINS JUMPER TABLE**

8 PINS JUMPER

<table>
<thead>
<tr>
<th>JUMPERS</th>
<th>CONNECTION</th>
<th>USE</th>
<th>DEF.</th>
</tr>
</thead>
<tbody>
<tr>
<td>J6</td>
<td>position 1-2</td>
<td>Connects signal /NMI BUS of ABACO® I/O BUS</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td></td>
<td>to signal /NMI of CPU</td>
<td></td>
</tr>
<tr>
<td></td>
<td>position 2-4</td>
<td>Connects CTC channel 3 signal (ZC/TO3) to</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>CPU /NMI signal</td>
<td></td>
</tr>
<tr>
<td></td>
<td>position 1-3</td>
<td>Connects signal /NMI BUS of ABACO® I/O BUS</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>to signal CLK/T3 of CTC</td>
<td></td>
</tr>
<tr>
<td></td>
<td>position 5-7</td>
<td>Connects signal /INT BUS of ABACO® I/O BUS</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>to signal CLK/T2 of CTC</td>
<td></td>
</tr>
<tr>
<td></td>
<td>position 7-8</td>
<td>Connects signal /INT BUS of ABACO® I/O BUS</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>to signal /INT of CPU</td>
<td></td>
</tr>
</tbody>
</table>

**FIGURA 28: 8 PINS JUMPER TABLE**

The "*" used in the following tables, denotes the default connection, or on the other hand the connection set up at the end of testing phase, that is the configuration the User receives.
JUMPER J6

Jumper J6 can also be used as a connector to reach CTC channels 2 and 3 and some interrupt signals. The following picture shows its pin out:

![Figure 29: JUMPERS J6](image)

Signals description:

<table>
<thead>
<tr>
<th>PIN</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>/INT BUS = O - Interrupt request from ABACO® I/O BUS</td>
</tr>
<tr>
<td>2</td>
<td>/NMI BUS = O - Non Maskable Interrupt request from ABACO® I/O BUS</td>
</tr>
<tr>
<td>3</td>
<td>/INT = I - Interrupt request from CPU.</td>
</tr>
<tr>
<td>4</td>
<td>/NMI = I - Non Maskable Interrupt from CPU.</td>
</tr>
<tr>
<td>5</td>
<td>CLK/T2 = I - n-th CTC Clock Trigger signal</td>
</tr>
<tr>
<td>6</td>
<td>ZC/T2 = O - n-th CTC’s counter Zero Count Timer Out</td>
</tr>
</tbody>
</table>

All signals available on connector J6 are TTL compliant and can be connected to compatible connectors.

Amongst the several possible connections of J6 as jumper, remarkably interesting are connections in position 1-2, 7-8 by which the ABACO® I/O BUS interrupt signals generate CPU /INT and /NMI and connections in position 1-3, 5-6 by which the same ABACO® I/O BUS interrupt signals are connected to CTC channels and can be counted. In particular, matching GPC® 153 with ZBT xxx and ZBR xxx boards, optocupled input signals can generate interrupts that can be quickly serviced by specific software procedures or the number of interrupts can be counted.

Channels 0 and 1 of CTC are internally connected to be used as baud rate generators respectively for serial line A and B; if the serial lines are not used the corresponding channels can be used by the application program but only in timer mode.

BACK UP

GPC® 153 has an on-board lithium battery BT1 for the back up of SRAM and RTC content when power supply is switched off. Jumper J5 connects physically the battery so it can be disconnected to save its duration whenever back up is not needed. Through CN2 connector it is possible to connect an external battery: configuration of jumper J5 does not affect the working of this battery and it can replace BT1 completely.

Please refer to the paragraph "ELECTRIC FEATURES" to choose the type of the external back up battery, to easily locate see figure 20.
RESET AND WATCH DOG

On GPC® 153 there are two separated Watch Dog circuits that are really efficient and easy to use. The most important features of the external Watch Dog circuitry are:

- astable mode;
- intervention time fixed at 1.5 s (modifiable by hardware);
- enable function by hardware;
- retrigger by software;

In astable mode when intervention time is elapsed the circuit becomes active, it stays active till the end of reset time and after it is again deactivated. The external Watch Dog intervent is signaled by the lighting of LED LD3.

The most important features of the CPU internal Watch Dog circuitry are:

- monostable mode;
- intervention time programmable by software;
- enable function by software and hardware;
- retrigger by software;

In monostable mode when intervention time is elapsed the circuit becomes active and it stays active as far as a reset or power on happens.

In response to a /RESET signal activation and successive deactivation the board restarts the execution of the program stored at address 0000H on IC5 (EPROM or FLASH EPROM).

Please remark that /RESET signal generated by GPC® 153 the board is connected also to pin 16C of K1 connector. Other reset sources, in addition to the Watch Dog circuits, are: CPU internal peripherals and reset contact P1.

About retrigger operation of internal and external watch dog circuits, please refer to paragraph "WATCH DOG" in chapter "PERIPHERAL DEVICES SOFTWARE DESCRIPTION" and to appendix B of this manual.

CONFIGURATION INPUTS

GPC® 153 is provided with an on board 6 pins Dip Switch (DSW1) and two jumpers (J10 andJ11), the jumper called J11 selects the RUN/DEBUG modality, typically used for system configuration and software readable. Most common applications for these devices are working conditions settings or firmware parameters input, etc.

Configuration inputs read modalities can be found in the chapter "PERIPHERAL DEVICES SOFTWARE DESCRIPTION", while to easily locate them on the board please refer to figures 20 and 23.
SERIAL COMMUNICATION SELECTION

Serial line A can be buffered only as RS 232 while serial line B can be buffered in RS 232, RS 422 or RS 485. By hardware can be selected which one of these electric standards is used, through jumpers connection (as described in the previous tables) and drivers installation. By software the serial line can be programmed to operate with all the standard physical protocols, in fact the bits per character, parity, stop bits and baud rates can be decided by setting opportunes CPU internal registers. In the following paragraphs there are all the informations on serial communication configurations. Some devices needed for RS 422, RS 485 and Current Loop configurations are not mounted on the board in standard configuration; this is why each fist non-standard (non-RS 232) serial configuration for line B must be always performed by grifo® technicians. This far the User can change in autonomy the configuration following the informations below:

- SERIAL LINE B IN RS 232 (default configuration)
  - IC25 = driver MAX 202
  - IC26 = no device
  - J12 = don’t care
  - IC28 = no device
  - JS1, JS2 = don’t care
  - IC27 = no device
  - IC29 = no device

- SERIAL LINE B IN CURRENT LOOP (option .CLOOP)
  - IC25 = driver MAX 202
  - IC26 = no device
  - J12 = don’t care
  - IC28 = no device
  - JS1, JS2 = not connected
  - IC27 = HCPL 4200
  - IC29 = HCPL 4100

Please remark that Current Loop serial interface is passive, so it must be connected an active Current Loop serial line, that is a line provided with its own power supply. Current Loop interface can be employed to make both point-to-point and multi-point connections through a 2-wires or a 4-wires connection.

- SERIAL LINE B IN RS 422 (option .RS 422)
  - IC25 = no device
  - IC26 = SN 75176 or MAX 483
  - J12 = position 2-3 and 4-5
  - IC28 = SN 75176 or MAX 483
  - JS1, JS2 = (*1)
  - IC27 = no device
  - IC29 = no device

Status of signal /RTSB, which is software managed, allows to enable or disable the transmitter as follows:

  /RTSB = low level = logic state 0 -> transmitter enabled
  /RTSB = high level = logic state 1 -> transmitter disabled

In point-to-point connections, signal /RTSB can be always kept low (transmitter always enabled), while in multi-point connections transmitter must be enabled only when a transmission is requested.
Serial B in RS 232

Serial B in Current Loop

Serial B in RS 422

Serial B in RS 485

**Figure 30: Serial Communication Drivers Location**
- **SERIAL LINE B IN RS 485 (option .RS 485)**

<table>
<thead>
<tr>
<th>IC</th>
<th>DEVICE</th>
<th>SIZE</th>
<th>JUMPERS POSITION</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>EPROM</td>
<td>128K Byte</td>
<td>J3 and J4 in position 1-2</td>
</tr>
<tr>
<td></td>
<td>EPROM</td>
<td>256K Byte</td>
<td>J3 and J4 in position 1-2</td>
</tr>
<tr>
<td></td>
<td>EPROM</td>
<td>512K Byte</td>
<td>J3 and J4 in position 1-2</td>
</tr>
<tr>
<td></td>
<td>FLASH EPROM</td>
<td>128K Byte</td>
<td>J3 and J4 in position 2-3</td>
</tr>
<tr>
<td></td>
<td>FLASH EPROM</td>
<td>512K Byte</td>
<td>J3 and J4 in position 2-3</td>
</tr>
<tr>
<td>4</td>
<td>SRAM</td>
<td>128K Byte</td>
<td>J2 in position 1-2</td>
</tr>
<tr>
<td></td>
<td>SRAM</td>
<td>512K Byte</td>
<td>J2 in position 2-3</td>
</tr>
<tr>
<td>17</td>
<td>EEPROM</td>
<td>256÷8K Byte</td>
<td>-</td>
</tr>
</tbody>
</table>

In this modality the signals to use are pins 4 and 5 of connector CN3, that become transmission or reception lines according to the status of signal /RTSB, managed by software, as follows:

  - /RTSB = low level = logic state 0 -> transmitter enabled
  - /RTSB = high level = logic state 1 -> transmitter disabled

This kind of serial communication can be used for multi-point connections, in addition it is possible to listen to own transmission, so the User is allowed to verify the success of transmission. In fact, any conflict on the line can be recognized by testing the received character after each transmission.

(*1) If using the RS 422 or RS 485 serial line, it is possible to connect the terminating and forcing circuit on the line by using JS1 and JS2. This circuit must be always connected in case of point-to-point connections, while in case of multi-point connections it must be connected only in the farthest boards, that is on the edges of the communication line.

When a reset or a power on occur, signal /RTSB is kept to a logic level high, so in one of these two cases driver RS 485 is receiving or RS 422 driver is disabled, avoiding eventual conflicts in communication.

For further informations about serial communication please refer to the examples of figures 7÷13 and to appendix B of this manual.

**MEMORY SELECTION**

On **GPC® 153** can be mounted up to 1032K bytes of memory divided in several configurations, as described in the following table:
All the above described devices must feature a JEDEC compliant pin out except for the serial EEPROM installed on IC17 that must be requested to grifo® in the ordering phase. To determine the name of the memory devices that can be mounted, please refer to the manufacturer documentation. GPC® 153 is delivered in its default configuration, this means 128K SRAM on IC4 and 512 bytes serial EEPROM on IC17; any different memory configuration can be mounted by the User in autonomy or requested to grifo® in the order. Below are reported the order codes for the several optional memory configurations:

- .512K -> 512K SRAM
- .EE08 -> 1K serial EEPROM
- .EE16 -> 2K serial EEPROM
- .EE64 -> 8K serial EEPROM

For further information about memory options and their cost please contact grifo®, while to easily locate the memory devices on the board please refer to figure 20.

VISUAL FEEDBACK

GPC® 153 board is provided with nine LEDs to signal status conditions, as described in this table:

<table>
<thead>
<tr>
<th>LED</th>
<th>COLOUR</th>
<th>MEANING</th>
</tr>
</thead>
<tbody>
<tr>
<td>LD1</td>
<td>Red</td>
<td>Indicates the activation of CPU /INT signal</td>
</tr>
<tr>
<td>LD2</td>
<td>Red</td>
<td>Indicates the presence of +5 Vdc power supply</td>
</tr>
<tr>
<td>LD3</td>
<td>Red</td>
<td>Indicates the activation of external Watch Dog</td>
</tr>
<tr>
<td>LD4</td>
<td>Green</td>
<td>Software managed activity LED</td>
</tr>
<tr>
<td>LD5</td>
<td>Red</td>
<td>Indicates that an external Watch Dog retrigger operation is in progress</td>
</tr>
<tr>
<td>LD6</td>
<td>Red</td>
<td>Indicates the activation of CPU /HALT signal</td>
</tr>
<tr>
<td>LD7</td>
<td>Red</td>
<td>Indicates the activation of on board reset circuitry</td>
</tr>
<tr>
<td>LD8</td>
<td>Yellow</td>
<td>Indicates that J11 is connected in position 2-3, corresponding to an high level of status /SYNCB, matched to DEBUG mode</td>
</tr>
<tr>
<td>LD9</td>
<td>Green</td>
<td>Indicates that J11 is connected in position 1-2, corresponding to a low level of status /SYNCB, matched to RUN mode</td>
</tr>
</tbody>
</table>

FIGURE 32: VISUAL FEEDBACK TABLE

The main purpose of these LEDs is to give a visual indication of the board status, making easier the operations of system verify. To easily locate these LEDs on the board, please refer to figure 20.
INTERRUPTS

A remarkable feature of **GPC® 153** card is the powerful interrupt management. Here follows a short description of which devices can generate interrupts and their modalities; for further informations about interrupts management please refer to the microprocessor data sheet or to the appendix B of this manual.

- **ABACO® I/O BUS** -> Generates a CPU /NMI if jumper J6 is in position 1-2.
  
  Generates normal /INT, without regard for the daisy chain priority, if jumper J6 is in position 7-8.

- **Real Time Clock** -> Generates normal /INT, without regard for the daisy chain priority, according to the connection of jumper J7.

- **A/D Converter** -> Generates normal /INT, without regard for the daisy chain priority, according to the connection of jumper J9.

- **Internal Watch dog** -> Generates normal /INT, without regard for the daisy chain priority, if jumper J8 is connected in position 1-2.

- **CPU peripherals** -> CPU internal sections CTC, SIO, PIO generate normal or vectored /INT, respecting the daisy chain priority.

The daisy chain on the **GPC® 153** board is made only of SIO, PIO and CTC and can be software programmed through one of the microprocessor internam registers. This way the User can always respond promptly and efficiently to any external event, also deciding the priority to assign to the several event sources.

For further informations please refer to appendix B of this manual.
POWER SUPPLY SELECTION

GPC® 153 board is provided with an efficient circuitry that solves in an efficient and comfortable way the problem of power supply in any employ condition. Here follows the list of the possible configurations for power supply section:

- No power supply section (default configuration):
  In this configuration the board must be supplied with a +5Vdc tension that can be provided through specific pins on connector CN3A, CN3B or CN1. Should the supply be provided through plug connectors CN3A or CN3B (for example in distributed systems where several boards are connected in a network and an unique cable carries both the signals and the supply), jumpers JS3 and JS4 must be properly configured.

- Linear power supply section (option ALIM.12):
  In this configuration the board must be supplied with a 6÷12 Vac tension, or the corresponding direct voltage, that must be provided on pins 1 and 2 of CN4. This kind of power supply section offers two options: normal linear, which requires 8÷12 Vac, and low leakage linear, which requires 6÷10 Vac.

- Switching power supply section (option .SW):
  In this configuration the board must be supplied with a 15÷24 Vac tension, or the corresponding direct voltage, that must be provided on pins 1 and 2 of CN4.

Regardless the type of supply section chosen, the GPC® 153 board is always provided with an efficient protection circuitry that protects the board against voltage peaks or noise. Please remark that the desired supply section must be explicitly specified in the order; in fact the choice implies a different hardware configuration that must be performed by the grifo® technical personnel.

Jumper J1 connects the positive terminal of the board's power supply to the ABACO® I/O BUS connector, so it must be not connected only when a GPC® 153 board provided with power supply section is connected to another board also provided with its own power supply section. By means to reduce the consumption the idle and stop modes can be invoked.

To do this, specific CPU registers must be properly programmed then the HALT instruction must be executed. To awake from such modes interrupt lines must be used. Referring to the “INTERRUPTS” paragraph, interrupt sources useful to awake the CPU are CTC, Real Time Clock, A/D Converter and ABACO® I/O BUS.

For further informations please refer to the paragraph “ELECTRIC FEATURES”.

GPC® 153 Rel. 5.10
SOFTWARE DESCRIPTION

A wide selection of software development tools can be obtained, allowing use of the module as a system for its own development, both in assembler and in other high level languages; in this way the User can easily develop all the requested application programs in a very short time. Generally all software packages available for the mounted microprocessor, or for the Z80 family, can be used:

GET 80
It is a complete program with Editor, Communication driver, and Mass Memory management for all Z80 family cards. This program, developed by grifo®, allows to operate in the best conditions when GDOS, FGDOS or xGDOS MCI software tools are used; GET 80 is supplied when one of these tools is ordered and it is personalized with name and general data of the customer. A useful list of pull down menus and the possibility of using mouse, make program use very comfortable. GET 80 program can be executed both on MS-DOS system and on MACINTOSH computers too, through SOFT-PC program. It is supplied on MS-DOS 3”1/2 floppy disk with the documentation on GDOS 80 manual.

GDOS 153
It is a complete development Tool for GPC® 153 card. It is supplied together with GET 80 program to allow an easy and immediate use of this powerful development system. GDOS is divided in two different structures: the first one works on PC maintaining serial communication with the second one. The second structure is on EPROM, it works on board of the card and it is an efficient operating system that executes many low level functions and, at the same time, it allows high level language use. The combination of the said structures results in a complete machine, in fact the card uses PC resources (like floppy disk, hard disk, printer, keyboard, monitor, etc.) as its own peripheral devices. This resulting “virtual machine” performs operation in a transparent way for the User, so this latter can operate with the same modality of standard PC languages. It is really interesting the compatibility of GDOS with all CP/M program and languages; so, if the User has experience, knowledge or developed applications with CP/M, he can use immediately GDOS, without any changes. Moreover, GDOS can manage all memory devices exceeding 64K Bytes as RAM disk and ROM disk. The on board RAM devices can directly be used performing data read and write operations with the confortable file formats. This software tools is supplied on EPROM with MS-DOS GET 80 floppy disk, some examples, utilities and the operating system documentation.

FGDOS 153
It is really similar to GDOS, but it can program and erase the on board FLASH EPROM with the application program developed from the User. In this way the external EPROM programmer is not necessary to store definitely the program and it is possible to modify or to add code directly on the installed machine, through a portable PC. This software tools is supplied on FLASH EPROM with MS-DOS GET 80 floppy disk, some examples, utilities and the operating system documentation.

NOICE
It is a PC hosted debugger consists of a target specific DOS program, NOICExxx.EXE, and a target resident monitor program. The two programs communicate via RS 232. NOICE includes: source level debug; a disassembler; a file viewer; memory display and editing; a virtually unlimited number of breakpoints; hardware free single step; definition of symbols; the ability to record and play back files of commands; on line help.
xGDOS MCI 153
It is a version of GDOS or FGDOS software tools, capable of PCMCIA Memory Card management. Using MCI 64 card, the GDOS operating system manages memory cards as RAM disk or ROM disk. All applications with data acquisition and data logging can be realized with high level languages that manage data on files, with a fast development time and without any software complication. This software tool is supplied on EPROM or FLASH EPROM with MS-DOS GET 80 floppy disk, some examples, utilities and the operating system documentation.

CBZ-80
It is a Basic Compiler that generates a really compact and fast code. It must work together with any GDOS version and it can exceed the 64K memory limits of Z80 family microprocessors through CHAIN modality. More than one application program can be saved in RAM and/or ROM disks and subsequently executed. In conjunction to the powerful GET 80 Editor the CBZ 80 program becomes a comfortable and really efficient development system for any kind of application program. This program is supplied ad ROM DISK file in GDOS EPROM or FLASH EPROM and on MS-DOS floppy disk with some exaples and manual.

PASCAL 80
It is an efficient and complete PASCAL Compiler for Z80 family cards, with features similar to Release 3.0 of Borland Turbo PASCAL. It must work together with any GDOS version and it can exceed the 64K memory limits of Z80 family microprocessors through OVERLAY modality. More than one application program can be saved in RAM and/or ROM disks and subsequently executed. The terminal emulation of GET 80 program support the typical full screen PASCAL Editor, including the attributes management. This program is supplied as ROM DISK file in GDOS EPROM or FLASH EPROM and on MS-DOS floppy disk with some example and manual.

RSD 153
This software tools is a Remote Symbolic Debugger with two operating mode. The first one is a monitor debugger modality with software emulation on P.C.; the second is a remote monitor debugger modality that execute code directly on the card. Through serial communication the User can: down load an HEX file and associated symbol table, debug code in symbolic mode, execute code in step to step mode or in real time mode, set breakpoint, dump and modify memory and registers, etc. RSD software tool supports both Z80 and Z180 instruction sets. Really interesting is the program execution management, in fact many hardware and software breakpoint are supported. RSD can be used together with assembler tools, like ZASM 80, and C Compiler CC 80. It is supplied on EPROM and on MS-DOS floppy disk with technical manual.

ZASM 80
It is a macro cross assempler that operates on any PC with MS-DOS operating system. It supports both Z80 and Z180 instruction sets. The generated code can be debugged on PC, through software simulation, or directly on target card, through remote modality, using RSD software tools. ZASM 80 is compatible with C Compiler CC 80 of which it assemble the compilation result. It is supplied on MS-DOS floppy disk with technical manual.
CC 80
It is a complete C Compiler with ANSI/ISO standard, provided of floating point procedure, that can generate code for Z80 and Z180 family microprocessors. It works together with cross assembler ZASM 80 and Symbolic Debugger RSD.
It is supplied on MS-DOS floppy disk with technical manual.

HI TECH C 80
Professional C Cross Compiler of Hi-Tech Software Inc. This Compiler is terribly fast and it generates a small quantity of code. This result is due to advanced techniques in optimizing the generated code based on Artificial Intelligence techniques which allow to get a very compact and very fast code. The package includes: IDE, Compiler, Code optimizer, Assembler, Linker, Remote Debugger and so on. This tool is Full ANSI/ISO Standard and Full Library Source Code. Once the porting of the Remote-Debugger module is done, this tool allows the user the software debugging directly on the hardware that he is experimenting. This type of specialization of the Remote-Debugger its available from now ant it is supplied with all grifo® CPU cards’. This software package is on 3” 1/2 diskettes under MS-DOS format along with user manual. This version supports these following CPUs: Z80, Z180, 84C011, 84C11, 84C013, 80C13, 84C015, 84C15, 64180, NCS800, Z181, Z182.

DDS MICRO C 85
Low cost ross compiler for C source program. It is a powerful software tool that includes editor, C compiler (integer), assembler, optimizer, linker, library, and remote debugger, in one easy to use integrated development environment. There are also included the library sources and many utilities programs.
FIGURE 33: COMPONENTS MAP
In this chapter are reported all information about card use, related to hardware and software. For example, the registers addresses and the memory allocation are described below.

**ON BOARD RESOURCES ALLOCATION**

The card devices addresses are managed by a specific control logic, realized with programmable logic devices. This control logic allocates SRAM, EPROM and peripheral devices in a comfortable way for the User.

The control logic is able to manage separately Input/Output peripherals and on board memory. CPU 84C15 is capable to address directly 64K Byte of memory and 256 I/O addresses, the control logic provides on board memory and peripheral devices allocation inside the 1036K Byte address space. The maps management is completely driven by software through the MMU circuit programming: the used memory can be selected and divided in 32K Byte size segments. About I/O maps the control logic avoids every conflicts problems between CPU internal and external peripherals.

Summarizing the control logic allocates:

- **ABACO® I/O BUS**
- Up to 512K Byte of EPROM or FLASH EPROM installed on IC5
- Up to 512K Byte of SRAM installed on IC4
- Up to 8K Byte of serial EEPROM, installed on IC17
- SIO
- CTC
- PIO
- RTC
- A/D Converter
- Memory Management Unit circuitry (MMU)
- Configuration Dip Switch DSW1 and jumpers J10, J11
- Activity LED
- Watch Dog circuits

The addresses of all these devices are described in the following paragraphs and can't be set with different values. If some different specific maps are required, please contact directly grifo®.
**I/O ADDRESSES**

The on board control logic manages the allocation of all the peripheral devices registers in the microprocessor I/O space, that is 256 bytes long. Next table shows names, addresses, meanings and directions of peripheral device registers (including the internal microprocessor ones).

<table>
<thead>
<tr>
<th>DEV.</th>
<th>REG.</th>
<th>ADD.</th>
<th>R/W</th>
<th>MEANING</th>
</tr>
</thead>
<tbody>
<tr>
<td>Real Time Clock</td>
<td>SEC1</td>
<td>00H</td>
<td>R/W</td>
<td>Units of seconds data register</td>
</tr>
<tr>
<td></td>
<td>SEC10</td>
<td>01H</td>
<td>R/W</td>
<td>Decines of seconds data register</td>
</tr>
<tr>
<td></td>
<td>MIN1</td>
<td>02H</td>
<td>R/W</td>
<td>Units of minutes data register</td>
</tr>
<tr>
<td></td>
<td>MIN10</td>
<td>03H</td>
<td>R/W</td>
<td>Decines of minutes data register</td>
</tr>
<tr>
<td></td>
<td>HOU1</td>
<td>04H</td>
<td>R/W</td>
<td>Units of hours data register</td>
</tr>
<tr>
<td></td>
<td>HOU10</td>
<td>05H</td>
<td>R/W</td>
<td>Decines of hours data register; AM/PM</td>
</tr>
<tr>
<td></td>
<td>DAY1</td>
<td>06H</td>
<td>R/W</td>
<td>Units of day data register</td>
</tr>
<tr>
<td></td>
<td>DAY10</td>
<td>07H</td>
<td>R/W</td>
<td>Decines of day data register</td>
</tr>
<tr>
<td></td>
<td>MON1</td>
<td>08H</td>
<td>R/W</td>
<td>Units of month data register</td>
</tr>
<tr>
<td></td>
<td>MON10</td>
<td>09H</td>
<td>R/W</td>
<td>Decines of month data register</td>
</tr>
<tr>
<td></td>
<td>YEA1</td>
<td>0AH</td>
<td>R/W</td>
<td>Units of year data register</td>
</tr>
<tr>
<td></td>
<td>YEA10</td>
<td>0BH</td>
<td>R/W</td>
<td>Decines of year data register</td>
</tr>
<tr>
<td></td>
<td>WEE</td>
<td>0CH</td>
<td>R/W</td>
<td>Day of week data register</td>
</tr>
<tr>
<td></td>
<td>REGD</td>
<td>0DH</td>
<td>R/W</td>
<td>D control and status register</td>
</tr>
<tr>
<td></td>
<td>REGE</td>
<td>0EH</td>
<td>R/W</td>
<td>E control and status register</td>
</tr>
<tr>
<td></td>
<td>REGF</td>
<td>0FH</td>
<td>R/W</td>
<td>F control and status register</td>
</tr>
<tr>
<td>CTC</td>
<td>CTC0</td>
<td>10H</td>
<td>R/W</td>
<td>Channel 0 data status register</td>
</tr>
<tr>
<td></td>
<td>CTC1</td>
<td>11H</td>
<td>R/W</td>
<td>Channel 1 data status register</td>
</tr>
<tr>
<td></td>
<td>CTC2</td>
<td>12H</td>
<td>R/W</td>
<td>Channel 2 data status register</td>
</tr>
<tr>
<td></td>
<td>CTC3</td>
<td>13H</td>
<td>R/W</td>
<td>Channel 3 data status register</td>
</tr>
</tbody>
</table>

**Figure 34: I/O addresses table - Part 1**
<table>
<thead>
<tr>
<th>DISP.</th>
<th>REG.</th>
<th>IND.</th>
<th>R/W</th>
<th>SIGNIFICATO</th>
</tr>
</thead>
<tbody>
<tr>
<td>A/D</td>
<td>ADCNT</td>
<td>14H</td>
<td>W</td>
<td>A/D converter control register</td>
</tr>
<tr>
<td></td>
<td>ADL</td>
<td>14H</td>
<td>R</td>
<td>A/D converter low data register</td>
</tr>
<tr>
<td></td>
<td>ADH</td>
<td>15H</td>
<td>R</td>
<td>A/D converter high data register</td>
</tr>
<tr>
<td>SIO</td>
<td>RDA</td>
<td>18H</td>
<td>R/W</td>
<td>Serial line A data register</td>
</tr>
<tr>
<td></td>
<td>RSA</td>
<td>19H</td>
<td>R/W</td>
<td>Serial line A status register</td>
</tr>
<tr>
<td></td>
<td>RDB</td>
<td>1AH</td>
<td>R/W</td>
<td>Serial line B data register</td>
</tr>
<tr>
<td></td>
<td>RSB</td>
<td>1BH</td>
<td>R/W</td>
<td>Serial line B status register</td>
</tr>
<tr>
<td>PIO</td>
<td>PAD</td>
<td>1CH</td>
<td>R/W</td>
<td>Port A data register</td>
</tr>
<tr>
<td></td>
<td>PAS</td>
<td>1DH</td>
<td>W</td>
<td>Port A control register</td>
</tr>
<tr>
<td></td>
<td>PBD</td>
<td>1EH</td>
<td>R/W</td>
<td>Port B data register</td>
</tr>
<tr>
<td></td>
<td>PBS</td>
<td>1FH</td>
<td>W</td>
<td>Port B control register</td>
</tr>
<tr>
<td>WD. EXT</td>
<td>RWD</td>
<td>E0H</td>
<td>R</td>
<td>External Watch Dog retrigger register</td>
</tr>
<tr>
<td>M.M.U.</td>
<td>MEM</td>
<td>16H</td>
<td>W</td>
<td>MMU settings register</td>
</tr>
<tr>
<td>LED ATT.</td>
<td>LD4</td>
<td>16H</td>
<td>W</td>
<td>Activity LED management register</td>
</tr>
<tr>
<td>BUZZER</td>
<td>BUZ</td>
<td>16H</td>
<td>W</td>
<td>Buzzer management register</td>
</tr>
<tr>
<td>DSW1</td>
<td>DSW1</td>
<td>17H</td>
<td>R</td>
<td>DSW1,LD4,Buzzer status read register</td>
</tr>
<tr>
<td>ABACO® I/O BUS</td>
<td>I/O BUS</td>
<td>20H:DFH F8H:FFH</td>
<td>R/W</td>
<td>ABACO® I/O BUS registers</td>
</tr>
<tr>
<td>INTERNAL REGISTER</td>
<td>SCRP</td>
<td>EEH</td>
<td>R/W</td>
<td>Microprocessor internal registers addressing register</td>
</tr>
<tr>
<td></td>
<td>SCDP</td>
<td>EFH</td>
<td>R/W</td>
<td>Microprocessor internal registers data register</td>
</tr>
<tr>
<td>INTERNAL W. D.</td>
<td>WDTMR</td>
<td>F0H</td>
<td>R/W</td>
<td>Internal Watch Dog programming register</td>
</tr>
<tr>
<td></td>
<td>WDTCR</td>
<td>F1H</td>
<td>W</td>
<td>Internal Watch Dog access register</td>
</tr>
<tr>
<td>INTER.</td>
<td>INTPR</td>
<td>F4H</td>
<td>W</td>
<td>Interrupt priority setting register</td>
</tr>
</tbody>
</table>

**Figure 35: I/O Addresses Table - Part 2**

For a detailed description of the registers function, please refer to next chapter "PERIPHERAL DEVICES SOFTWARE DESCRIPTION".
ABACO® I/O BUS ADDRESSES

The GPC® 153 control logic defines ABACO® I/O BUS addresses and only these addresses must be used to manage correctly the BUS. As described in figures 34 and 35, only the addresses from 20H to DFH and from F8H to FFH are available for ABACO® BUS. Any I/O operations at each one of these addresses enables the /IORQ signal and the other control signals of connector CN1.

MEMORIES MAPPING

The total 1032K Byte of memory supported by the card are divided this way:

- Up to 512K Byte of EPROM or 512K Byte of FLASH EPROM allocated in the memory space
- Up to 512K Byte of SRAM allocated in the memory space
- Up to 8K Byte of serial EEPROM allocated in the I/O space

GPC® 153 can directly manage at most 64K bytes of memory that is the microprocessor logic addressable space. On the board this logic space can be divided in two 32K Byte pages: both SRAM and EPROM can be installed on the low page, while only SRAM can be installed on the high page. MMU circuitry, driven through a simple software management, takes care to divide the addressable space in 32K Byte pages and to make them available directly into the CPU addressing space. It is possible to address indirectly a memory area much greater than the area normally accessible by the CPU just programming the MEM register. Here follow two figures that show the possible memory devices configurations, for further informations please refer to the paragraph "MEMORY MANAGEMENT UNIT", while to easily locate the memory devices refer to figure 20. Some software packages, like GDOS and FGDOS, are capable to manage in autonomy the MMU circuitry to make address in the CPU addressable memory area all the available memory without bothering the User.

When a power on or a reset occur, R/E signal is set to 0, so the board starts executing the code located at the logical address 0000H of page 0 on EPROM or FLASH EPROM installed IC5.
Figure 36: Memory mapping with R/E=0
FIGURE 37: MEMORY MAPPING WITH R/E=1
PERIPHERAL DEVICES SOFTWARE DESCRIPTION

In the previous paragraphs are described the external registers addresses, while in this one there is a specific description of registers meaning and function (please refer to I/O addresses table, for the registers names and addresses values). For a more detailed description of the devices, please refer to manufacturing company documentation; for microprocessor internal peripheral devices, not described in this paragraph, refer to appendix B. In the following paragraphs the $D_7$÷$D_0$ and $O_0$÷$O_7$ indications denote the eight bits of the combination used in I/O operations.

MEMORY MANAGEMENT UNIT

An efficient MMU circuitry takes care to allocate in the CPU addressing space all the memory devices that can be installed on GPC® 153. This section can be programmed through the MEM register, which is allocated in the I/O addressing space. The bits of MEM register have the following meaning:

MEM: Meaning of bits

<table>
<thead>
<tr>
<th>MEM.7</th>
<th>MEM.6</th>
<th>MEM.5</th>
<th>MEM.4</th>
<th>MEM.3</th>
<th>MEM.2</th>
<th>MEM.1</th>
<th>MEM.0</th>
</tr>
</thead>
<tbody>
<tr>
<td>BUZ</td>
<td>LD4</td>
<td>R/E: selector SRAM (MEM.5=1) or EPROM/FLASH EPROM (MEM.5=0), for the low page (0000H÷7FFFH) of CPU addressing space</td>
<td>A18 x IC5 and /A18 x IC4</td>
<td>A17 x IC5 and /A17 x IC4</td>
<td>A16 x IC5 and /A16 x IC4</td>
<td>A15 x IC5</td>
<td>/A15 x IC4</td>
</tr>
</tbody>
</table>

Only bits D0÷D5 define which page of SRAM installed IC4 or EPROM or FLASH EPROM installed on IC5 must be addressed.

When a reset or a Power On occur all the bits of MEM register are reset (all bits 0); this means to program the MMU section where the low 32K Bytes page consists of page 0 EPROM or FLASH EPROM installed on IC5 and the high 32K Bytes page consists of page 0 SRAM installed on IC4. Please refer to the following table, also remembering figures 36 and 37, for an overview of all the possible MMU section configurations.

"X" means non significant bit, that is that bit can be "1" or "0" without influencing the setting there described.
<table>
<thead>
<tr>
<th>PAGINA 32K LOW</th>
<th>PAGINA 32K HIGH</th>
<th>REGISTRO MEM</th>
</tr>
</thead>
<tbody>
<tr>
<td>0: IC 5</td>
<td>0: IC 4</td>
<td>XX000000B = 00H</td>
</tr>
<tr>
<td>1: IC 5</td>
<td>0: IC 4</td>
<td>XX000010B = 02H</td>
</tr>
<tr>
<td>2: IC 5</td>
<td>0: IC 4</td>
<td>XX000100B = 04H</td>
</tr>
<tr>
<td>3: IC 5</td>
<td>0: IC 4</td>
<td>XX000110B = 06H</td>
</tr>
<tr>
<td>4: IC 5</td>
<td>0: IC 4</td>
<td>XX001000B = 08H</td>
</tr>
<tr>
<td>5: IC 5</td>
<td>0: IC 4</td>
<td>XX001010B = 0AH</td>
</tr>
<tr>
<td>6: IC 5</td>
<td>0: IC 4</td>
<td>XX001100B = 0CH</td>
</tr>
<tr>
<td>7: IC 5</td>
<td>0: IC 4</td>
<td>XX011100B = 0EH</td>
</tr>
<tr>
<td>8: IC 5</td>
<td>0: IC 4</td>
<td>XX011100B = 10H</td>
</tr>
<tr>
<td>9: IC 5</td>
<td>0: IC 4</td>
<td>XX011100B = 12H</td>
</tr>
<tr>
<td>10: IC 5</td>
<td>0: IC 4</td>
<td>XX010100B = 14H</td>
</tr>
<tr>
<td>11: IC 5</td>
<td>0: IC 4</td>
<td>XX010110B = 16H</td>
</tr>
<tr>
<td>12: IC 5</td>
<td>0: IC 4</td>
<td>XX011100B = 18H</td>
</tr>
<tr>
<td>13: IC 5</td>
<td>0: IC 4</td>
<td>XX011100B = 1AH</td>
</tr>
<tr>
<td>14: IC 5</td>
<td>0: IC 4</td>
<td>XX011100B = 1CH</td>
</tr>
<tr>
<td>0: IC 4</td>
<td>0: IC 4</td>
<td>XX1111X1B = 3DH</td>
</tr>
<tr>
<td>1: IC 4</td>
<td>0: IC 4</td>
<td>XX1111X0B = 3CH</td>
</tr>
<tr>
<td>2: IC 4</td>
<td>0: IC 4</td>
<td>XX1110X1B = 39H</td>
</tr>
<tr>
<td>3: IC 4</td>
<td>0: IC 4</td>
<td>XX1110X0B = 38H</td>
</tr>
<tr>
<td>4: IC 4</td>
<td>0: IC 4</td>
<td>XX1101X1B = 35H</td>
</tr>
<tr>
<td>5: IC 4</td>
<td>0: IC 4</td>
<td>XX1101X0B = 34H</td>
</tr>
<tr>
<td>6: IC 4</td>
<td>0: IC 4</td>
<td>XX1100X1B = 31H</td>
</tr>
<tr>
<td>7: IC 4</td>
<td>0: IC 4</td>
<td>XX1100X0B = 30H</td>
</tr>
<tr>
<td>8: IC 4</td>
<td>0: IC 4</td>
<td>XX1011X1B = 2DH</td>
</tr>
<tr>
<td>9: IC 4</td>
<td>0: IC 4</td>
<td>XX1011X0B = 2CH</td>
</tr>
<tr>
<td>10: IC 4</td>
<td>0: IC 4</td>
<td>XX1010X1B = 29H</td>
</tr>
<tr>
<td>11: IC 4</td>
<td>0: IC 4</td>
<td>XX1010X0B = 28H</td>
</tr>
<tr>
<td>12: IC 4</td>
<td>0: IC 4</td>
<td>XX1001X1B = 25H</td>
</tr>
<tr>
<td>13: IC 4</td>
<td>0: IC 4</td>
<td>XX1001X0B = 24H</td>
</tr>
<tr>
<td>14: IC 4</td>
<td>0: IC 4</td>
<td>XX1000X1B = 21H</td>
</tr>
<tr>
<td>15: IC 4</td>
<td>0: IC 4</td>
<td>XX1000X0B = 20H</td>
</tr>
</tbody>
</table>

**FIGURE 38: POSSIBLE MMU SECTION CONFIGURATIONS TABLE**
A/D CONVERTER

A/D Converter section installed on **GPC®153** is based on DAS MAX 197. This device is managed through three registers, two readable and one writable as shown in figure 35, such registers are called ADCNT, ADL and ADH, they allow the User to perform all the operations proper of this section. Here follows the meaning of the registers and their use.

![Bit assignment image](image.png)

**ADCNT = PD1 PD0 ACQMOD RNG BIP A2 A1 A0**

This write register manages the DAS MAX 197 operations: a write instruction to its address will start the conversion from the specified channel range.

The meaning of the bits making the register is:

<table>
<thead>
<tr>
<th>Bit</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>PD1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>PD0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>ACQMOD</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>RNG</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>BIP</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>A2</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>A1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>A0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

- **PD1  PD0** = Set the working modality of A/D converter amongst the following:
  - 0 0 -> Use external clock in normal mode
  - 0 1 -> Use internal clock in normal mode *(DO NOT USE)*
  - 1 0 -> Standby Power-Down mode
  - 1 1 -> Full Power-Down mode

- **ACQMOD** = Controls the A/D internal Track-Hold working:
  - 0 -> Track-Hold of the channel specified by A0÷A2, remains active for 3 \(\mu\)sec then begins the conversion phase of the signal captured.
  - 1 -> Track-Hold of the channel specified by A0÷A2, is activated and remains active up to the next write to the control register, the data written will be equal to the previous one, but ACQMOD=0. By this modality the User can capture the signal to be converted for as long as he/She wishes.

- **RNG BIP** = Set the voltage range for the analog channel, specified by bit A0÷A2; this setting will affect only the conversion the device is going to perform, so it may vary from channel to channel and even on the same channel for different conversions:
  - 0 0 -> Range 0÷5 V
  - 1 0 -> Range 0÷10 V
  - 0 1 -> Range ±5 V
  - 1 1 -> Range ±10 V

- **A2 A1 A0** = Select the analog input channel where the Track-Hold operation and the next conversion of the signal captured will be performed:
  - 0 0 0 -> Channel 0
  - 0 0 1 -> Channel 1
  - 0 1 0 -> Channel 2
  - 0 1 1 -> Channel 3
  - 1 0 0 -> Channel 4
  - 1 0 1 -> Channel 5
  - 1 1 0 -> Channel 6
  - 1 1 1 -> Channel 7

**NOTE**

*Never use internal clock in normal mode*, because **GPC® 153** employs its own clock circuitry designed to optimize conversion time and noise immunity.
For example, writing 0BH into register ADCNT, the device will perform a conversion from line ADC3 connected to connector CN6, in the range ±5 V with automatic Track-Hold modality.

\[
\begin{array}{cccccccc}
\text{bit} & 7 & 6 & 5 & 4 & 3 & 2 & 1 & 0 \\
\text{ADL} &= C7 \ C6 \ C5 \ C4 \ C3 \ C2 \ C1 \ C0 \\
\end{array}
\]

This read only register allows to acquire the low byte of the last conversion performed by the A/D Converter; a read operation from this register will return bits 7÷0 of the last combination. Please remark that this register returns valid data only when a Track-Hold phase or a conversion are not in progress, that is only after the conversion has been completed.

\[
\begin{array}{cccccccc}
\text{bit} & 7 & 6 & 5 & 4 & 3 & 2 & 1 & 0 \\
\text{ADH} &= NU \ NU \ NU \ NU \ C11 \ C10 \ C9 \ C8 \\
\end{array}
\]

This read only register allows to acquire the high byte of the last conversion performed by the A/D Converter; a read operation from this register will return bits 11÷8 of the last combination. Please remark that this register returns valid data only when a Track-Hold phase or a conversion are not in progress, that is only after the conversion has been completed.

Bit D3=C11 will contain the twelveth bit of the combination in case the conversion ranges are unipolar (0÷5 V, 0÷10 V) or the sign of the combination (0 = positive, 1 = negative) in case the conversion ranges are bipolar (±5 V, ±10 V).

Here follows a short example that shows how to perform A/D conversion in several modalities using the hardware installed on GPC® 153:

**Polling conversion**
- Write to ADCNT register the data that specifies the desired conversion modalities (channel, range, Track-Hold, etc.).
- Wait for at least a conversion time (≥ 10 μsec).
- Read bits 8÷11 of the combination obtained from the conversion from register ADH.
- Read bits 0÷7 of the combination obtained from the conversion from register ADL.
- Elaborate the obtained combination

**Conversion in interrupt**
Main program must perform the following operations:
- Write to ADCNT register the data that specifies the desired conversion modalities (channel, range, Track-Hold, etc.).
- Elaborate the combination obtained from the interrupt handler routine

While the interrupt handler routine must contain:
- Read bits 8÷11 of the combination obtained from the conversion from register ADH.
- Read bits 0÷7 of the combination obtained from the conversion from register ADL.

**NOTE**
This latter conversion modality can be used only if the A/D section interrupt line is connected through jumper J9, as described in the previous chapter.
BUZZER

Buzzer is activated by performing a "write operation" with bit D7=1 at the address of register BUZ; vice versa buzzer is disabled by performing the same operation with bit D7=0. The remaining seven bits of BUZ register must be set according to the programmation of MMU and activity LED circuitry, in fact BUZ register is allocated at the same I/O address used by MEM and LD4 registers. The buzzer status can be acquired by software performing an input operation from register DSW1 and masking bit D7.

BUZ.7        -> buzzer management
DSW1.7        -> buzzer status acquisition

BUZ register is reset (all bits to 0) after Reset or power on, maintaining disabled the buzzer circuit.

REAL TIME CLOCK

This peripheral is allocated in 16 consecutives I/O addresses, 3 of which correspond to status registers while the remaining 13 are for datas. Data registers are used both for read operations (of the current time and date) and write operations (to initialize the time and date) just like the status registers which are used in write operations (to program the operative mode) and in read operations (to acquire the RTC status). Here follows a list of the RTC data registers' meanings:

SEC1 - Units of seconds - 4 least significant bits of SEC1.3÷SEC1.0
SEC10 - Decines of secondi - 3 least significant bits of SEC10.2÷SEC10.0
MIN1 - Units of minutes - 4 least significant bits of MIN1.3÷MIN1.0
MIN10 - Decines of minutes - 3 least significant bits of MIN10.2÷MIN10.0
HOU1 - Units of hours - 4 least significant bits of HOU1.3÷HOU1.0

The third bit of HOU10.2 indicates AM/PM

DAY1 - Units of day number - 4 least significant bits of DAY1.3÷DAY1.0
DAY10 - Decines of day number - 2 least significant bits of DAY10.1÷DAY10.0

MON1 - Units of month - 4 least significant bits of MON1.3÷MON1.0
MON10 - Decines of month - 1 least significant bit of MON10.0

YEA1 - Units of year - 4 least significant bits of YEA1.3÷YEA1.0
YEA10 - Decines of year - 4 least significant bits of YEA10.3÷YEA10.0

WEE - Day of the week - 3 least significant bits of WEE.2÷WEE.0

For this last register the three least significant bits mean:

<table>
<thead>
<tr>
<th>WEE.2</th>
<th>WEE.1</th>
<th>WEE.0</th>
<th>Day of the week</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Sunday</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Monday</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Tuesday</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>Wednesday</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Thursday</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>Friday</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>Saturday</td>
</tr>
</tbody>
</table>
The meaning of the three control registers is:

**REG D = NU NU NU NU 30S IF B H**

where:
- **NU** = Not used.
- **30S** = If high (1) it allows a 30 seconds correction of the time. Once set the RTC seconds are reset and the minutes increased, if the previous seconds was equal or greater than 30.
- **IF** = It manages the RTC interrupt status. When read it shows the current interrupt status (1 active and vice versa), when reset to 0 it disables the RTC interrupt signal if the interrupt mode is selected.
- **B** = Indicates whether R/W operations can be performed on the registers:
  - 1 -> operations are not permitted and vice versa.
- **H** = If high (1) it stores the written time and date.

**REG E = NU NU NU NU T1 T0 I M**

where:
- **NU** = Not used.
- **T1 T0** = Determines the duration of the internal counters interrupt cycle.
  - 0 0 -> 1/64 second
  - 0 1 -> 1 second
  - 1 0 -> 1 minute
  - 1 1 -> 1 hour
- **I** = It defines the interrupt operating mode:
  - 1 -> it selects interrupt mode: when the selected duration elapses the interrupt is enabled and then disabled only with a reset of bit IF of control register D;
  - 0 -> it selects the standard mode: when the selected duration elapses the interrupt is enabled and then disabled only after 7.8 msec.
- **M** = It masks the interrupt status:
  - 1 -> interrupt masked: the RTC interrupt signal is always disabled;
  - 0 -> interrupt not masked: the RTC interrupt signal reflects interrupt status.

**REG F = NU NU NU NU T 24/12 S R**

where:
- **NU** = Not used.
- **T** = It determines from which internal counter to take the counting signal:
  - 1 -> main counter (fast counter for test);
  - 0 -> 15th counter.
- **24/12** = It determines the hours counting mode:
  - 1 -> 0÷23;
  - 0 -> 1-12 with AM/PM.
- **S** = If high (1) it stops the clock time counting until the next enabling (0).
- **R** = If high (1) it resets all the internal counters.

After a reset or a power on occur, the RTC is not reinitialized, in order to warrant the conservation of its content, after such events, through the back up ciruircuitry.
CPU INTERNAL DEVICES

For further informations about CPU internal devices please refer to technical documentation on appendix B of this manual.

EXTERNAL WATCH DOG

Retrigger operation of GPC® 153 external Watch Dog circuit is performed with a simple input operation at the address of register RWD. To avoid external Watch Dog activation it is indispensable to perform retrigger operations at regular time periods and the duration of these periods must be smaller than intervention time. If retrigger doesn't happen as before described and jumper J8 is connected in position 3-4, when intervention time is elapsed, the card is reset. By default the intervention time is about 1.5 s and jumper J8 does NOT connect external Watch Dog to reset circuitry.

SERIAL EEPROM

For informations about the management of serial EEPROM module installed on IC17, please refer to the documentation of the software package used to program the board. This technical manual reports no further informations about the serial EEPROM management because this activity employs a very deep knowledge of the device itself. For this, its complete management is affordable through the high level instructions of the software package being used.

Please remark that the first 32 bytes (0÷31) are reserved so the User should avoid to modificate their value. Control logic allows serial EEPROM software management through /SYNCA, /DTRA and /DTRB SIO signals, these are the connections;

- /SYNCA -> DATA input signal (SDA)
- /DTRB -> DATA output signal (SDA)
- /DTRA -> CLOCK signal (SCL)

Known the serial EEPROM management circuitry hardware implementation, please remark that signals A0,A1,A2 of this device's slave address are all set to logic 0. Bit logic status 0 corresponds to low logic status (=0V) of the corresponding signal, while bit logic status 1 corresponds to low logic status (=0V).

For further informations about SIO signals management modalities please refer to proper technical documentation of appendix B of this manual.
ACTIVITY LED

On board control logic allows the management of an activity LED, called LD4, through LD4 and DSW1 registers:

\[\begin{align*}
    \text{LD4.6} & \rightarrow \text{set LD4 status} \\
    \text{DSW1.6} & \rightarrow \text{get LD4 stats}
\end{align*}\]

The LED can be lit performing an output operation to the allocation address of register LD4 with the corresponding bit (bit 6) set to logical 1. Of course, the LED can be turned off through the same output operation with the corresponding bit reset to logical 0.

The status of the activity LED can be acquired by software performing an input operation at the address of register DSW1 and extracting bit 6.

The remaining seven bits of BUZ register must be set according to the programming of MMU and buzzer circuitry, in fact BUZ register is allocated at the same I/O address used by MEM and BUZ registers.

Register LD4 is reset (all bits 0) when a reset or a power on occurs, so after one of such events the activity LED is turned off.

CONFIGURATION INPUTS

GPC® 153 is provided with 9 software acquirable User settable configuration inputs divided as follows.

Dip Switch DSW1 can be acquired by software, performing a simple input operation from the address of DSW1 register. This is the correspondence between Dip Switch signals and DSW1 bits:

\[\begin{align*}
    \text{DSW1.5} & \rightarrow \text{Dip Switch 6} \\
    \text{DSW1.4} & \rightarrow \text{Dip Switch 5} \\
    \text{DSW1.3} & \rightarrow \text{Dip Switch 4} \\
    \text{DSW1.2} & \rightarrow \text{Dip Switch 3} \\
    \text{DSW1.1} & \rightarrow \text{Dip Switch 2} \\
    \text{DSW1.0} & \rightarrow \text{Dip Switch 1}
\end{align*}\]

The signals are in complemented logic, this means that a dip ON gives a logic status 0 on the corresponding bit, while a dip OFF gives a logic status 1.

Please remark that Dip Switch status acquisition implies also external Watch Dog retrigger, because RWD register and DSW1 register are allocated at the same I/O address.

Configuration jumper J10 is connected to /DCDB SIO signal. Jumper J11 is connected to /SYNCB SIO signal.

Jumper J11 connected in position 1-2 gives logic status 0, while connection in position 2-3 gives logic status 1. For further informations about the acquisition of /SYNCB and /DCDB signals status, please refer to the proper technical documentation of appendix B of this manual.

Jumper J11 (RUN/DEBUG) works as selector of RUN modality (position 1-2) or DEBUG modality (position 2-3). This feature is used by some of grifo® software packages.
BAUD RATE GENERATOR

The SIO frequencies generation section is capable to generate two separated baud rates that can vary in the range 600 Baud ÷ 115200 Baud, picking the seven most common used values. GPC® 153 card allows to set the communication speeds performing a simple output instruction to the CTC0 and CTC1 I/O addresses. In fact timer counters 0 and 1 of microprocessor CTC section are used to generate the baud rate respectively for serial line A and B.

To make the CTC channels operate as baud rate generators it is essential to program them as follows:

- Give a channel reset command = output to CTCn control register the value 03H.
- Give a channel control word that: disables interrupt, selects timer mode, selects a descending front, and loads a time constant = output to CTCn control register the value 45H.
- Load the time constant corresponding to the baud rate required = output to CTCn control register the value indicated by the following table.

<table>
<thead>
<tr>
<th>BAUD RATE</th>
<th>TIME CONSTANT</th>
</tr>
</thead>
<tbody>
<tr>
<td>600 Baud</td>
<td>C0H</td>
</tr>
<tr>
<td>1200 Baud</td>
<td>60H</td>
</tr>
<tr>
<td>2400 Baud</td>
<td>30H</td>
</tr>
<tr>
<td>4800 Baud</td>
<td>18H</td>
</tr>
<tr>
<td>9600 Baud</td>
<td>0CH</td>
</tr>
<tr>
<td>19200 Baud</td>
<td>06H</td>
</tr>
<tr>
<td>38400 Baud</td>
<td>03H</td>
</tr>
<tr>
<td>57600 Baud</td>
<td>02H</td>
</tr>
<tr>
<td>115200 Baud</td>
<td>01H</td>
</tr>
</tbody>
</table>

**FIGURE 39: BAUD RATE TIME CONSTANTS TABLE**

All CTC channels are disabled after a reset or a Power On, and so the baud rate generators. For further informations please refer to the proper paragraph of Appendix B in this manual.
EXTERNAL CARDS

GPC® 153 can be connected to a wide range of block modules and operator interface system produced by grifo®, or to many system of other companies. The on board resources can be expanded with a simple connection to the numerous peripheral grifo® boards, both intelligent and not, thanks to its standard ABACO® BUS connector. Even cards with ABACO® I/O BUS can be connected, by using the proper mother boards. Hereunder some of these cards are briefly described; ask the detailed information directly to grifo®, if required.

KDL X24 - KDF 224

Keyboard Display LCD 2,4 rows 24 keys
Interface with Fluorescent or LCD display, LEDs backlit, 20x2 or 20x4 characters; up to 24 keys matrix keyboard connector. It is directly driven by a 20 pins ABACO® I/O standard connector; High level languages supported; standard pinout for telephone keyboard.

QTP 24 - QTP 24P

Quick Terminal Panel 24 keys with Parallel interface
Intelligent user panel equipped with Fluorescent or LCD display, LEDs backlit, 20x2 or 20x4 characters; RS 232, RS 422, RS 485 or current loop serial line; serial E2 for set up and message; Possibility of re-naming keys, LEDs and panel name by inserting label with new name into the proper slot; 24 Keys and 16 LEDs with blinking attribute and buzzer manageable by software; built in power supply; RTC option, reader of magnetic badge and relay. The QTP 24P is low cost no intelligent (passive) version. It is directly driven from 16 TTL I/O lines; high level languages supported.

QTP G28

Quick Terminal Panel - LCD Graphic, 28 keys
LCD display 240x128 pixels, CFC backlit; Optocoupled RS 232 line and additional RS 232/422/485/C. L. line; CAN line controller; E2 for set up; RTC and RAM lithium backed; primary graphic object; possibility of re-naming keys, LEDs and panel name; 28 keys and 16 LEDs with blinking attribute and buzzer manageable by software; buzzer; built-in power supply; reader of magnetic badge and relay option.

ABB 03

ABACO® Block BUS 3 slots
3 slots ABACO® mother board; 4 TE pitch connectors; ABACO® I/O BUS connector; screw terminal for power supply; connection for DIN C type and Ω rails.

ABB 05

ABACO® Block BUS 5 slots
5 slots ABACO® mother board with power supply. Double power supply built in; 5Vdc 2,5A section for powering the on board logic; second section at 24Vdc 400mA galvanically coupled, for the optocoupled input lines. Auxiliary connector for ABACO® I/O BUS. Connection for DIN Ω rails.

MCI 64

Memory Cards Interfaces 64 MBytes
Interfacing card for managing 68 pins PCMCIA memory cards, it is directly driven from any ABACO® I/O standard connector; High level languages GDOS supported.
IAC 01
Interface Adapter Centronics
Interface between ABACO® standard I/O 20 pins connector and D 25 pins connector with Centronics standard pin out.

IBC 01
Interface Block Communication
Conversion card for serial communication, 2 RS 232 lines; 1 RS 422–485 line; 1 optical fibre line; selectable DTE/DCE interface; quick connection for DIN 46277-1 and 3 rails.

OBI N8 - OBI P8
Opto BLOCK Input NPN-PNP
Interface between 8 NPN, PNP optocoupled and displayed input lines, with screw terminal and ABACO® standard I/O 20 pins connector; power supply section; connection for DIN Ω rails.

TBO 01 - TBO 08
Transistor BLOCK Output
Interface for ABACO® standard I/O 20 pins connector; 16 or 8 transistor output lines 45 Vdc 3 A open collector; screw terminal; optocoupled and displayed lines; connection for DIN 247277-1 and 3 rails.

RBO 08 - RBO 16
Relé BLOCK Output
Interface for ABACO® standard I/O 20 pins connector; 8 or 16 displayed Relays 3A with MOV; screw terminal; connection for DIN Ctype and Ω rails.

FBC 20 - FBC 120
Flat Block Contact 20 vie
Interfaccia tra 2 o 1 connettori a perforazione di isolante (scatolino da 20 vie maschi) e la filatura da campo (morsettiere a rapida estrazione). Attacco rapido per guide tipo DIN 46277-1 e 3.

DEB 01
Didactic Experimental Board
Supporting card for 16 TTL I/O lines use. It includes: 16 keys, 16 LEDs, 4 digits, 16 keys matrix keyboard, Centronics printer interface, LCD display and fluorescent display interface, GPC® 68 I/O connector, field connection with screw terminal.

IAL 42
Interface Adapter LCD
Interface between 16 I/O TTL available on I/O ABACO® standard connector and 14 pins lowprofile male connector featuring standard pin-out for fluorescent LCD displays management.

XBI 01
miXed BLOCK Input Output
Interface for ABACO® standard I/O 20 pins connector; 8 transistor output lines 45 Vdc 3A; 8 input lines; screw terminal; optocoupled and displayed I/O lines; connection for DIN 247277-1 and 3 rails.
OPTIMAL POWER SUPPLY
+5 or +12 Vdc
6÷12 Vac
15÷24 Vac (Switching)

ABACO® I/O BUS

ZBx series

ANY I/O TYPE
C/I/O R16-T16, etc.
IPC 52,
UAR 24, etc.

DIRECT CONNECTION
TO QTP 24P

GRAPHIC USER INTERFACE

DIGITAL TTL INPUT/OUTPUT
to XBI-01, OBI-01, RBO-08 etc....

12 Bits ANALOG INPUT.
VOLTAGE:
0÷5, 0÷10, ±5, ±10 V
CURRENT:
0÷20, 4÷20 mA

CURRENT to VOLTAGE
CONVERTER
with 8 A-V modules

EXTERNAL LITIUM
BATTERY for
Back up

Serial Line RS-232

PC like or
Macintosh

PLC

QTP G28

ABB 03 or ABB 05, etc.

DIRECT CONNECTION
TO QTP 24P

1 RS 232
OR
RS 422, 485,
Current Loop

SERIAL LINE
RS 232, RS 422, RS 485, Current Loop

OPTIONAL
POWER SUPPLY
+5 or +12 Vdc
6÷12 Vac
15÷24 Vac

ABB® I/O BUS

ABACO® BUS

EXTENDED RELAY
TRANS.
FORM COUPLED

PC like or
Macintosh

PLC

QTP G28

PLC

QTP G28

PC like or
Macintosh

PLC

QTP G28

FIGURE 40: POSSIBLE CONNECTIONS DIAGRAM
XBI R4 - XBI T4
miXed BLOCK Input-Output
Interface for ABACO® standard I/O 20 pins connector; 4 Relays 3A with MOV or 4 optocoupled Transistors 3A open collectors; 4 input lines optocoupled; screw terminal; connection for DIN Ctype and Ω rails.

CI/O R16
16 Coupled Input Output with relays
16 optocoupled inputs with low frequency filter; standard rate +24 Vdc input voltage; 16 microrelays 1 A output lines; 24 Vac noise suppressor, type MOV; I/O displayed through LEDs.

IPC 52
Intelligent Peripheral Controller, 24 analogic input
This intelligent peripheral card acquires 24 independent analogic input lines: 8 PT 100 or PT 1000 sensors, 8 J,K,S,T thermocouples, 8 analog input ±2Vdc or 4÷20mA; 16 bits + sign A/D section; 0.1 °C resolution; 32K RAM for local data logging; buzzer; 16 TTL I/O lines; 5 or 8 conversion per second; facility of networking up to 127 IPC 52 cards using serial line. BUS interfacing or through RS 232, RS 422, RS 485 or current loop line. Only 5Vdc power supply.

DAC 16
Digital to Analog Converter 16 bits
2 Digital to Analog converter, 16 bits galvanically insulated; programmed data displayed; ± 10 Vdc output; gain and offset setting; 8 bit Bus; standard addressing.

RKD LT
Remote Keyboard Display controller
Video terminal able to manage many different graphic LCD or alphanumeric fluorescent LCD or displays; matrix keyboard input; BUS or serial interfacing; 1 RS 232 line; additional RS 232, RS 422-485 or Current Loop line; serial EEPROM for set-up; primary graphic object; LEDs driving; Buzzer.

UCC A2
UART Communication Cards, 2 lines
2 Independent RS 232, RS 422, RS 485 or Current Loop lines. Each line: 3 characters buffer; Asynchronous communication from 50 to 115K baud. Parity, bit stop and data length is software programmable.

PCI 01
Peripheral Coupled 32 Inputs
32 optocoupled input lines displayed through LEDs with Pi-Greek filter; standard rate 24 Vdc input voltage; 8/16 bits Bus extended addressing.

JMS 34
Jumbo Multifunction Support for Axis control
Generic peripheral axis control card. 3 optocoupled acquisition channels, with 16 bits bidirectional counter, for incremental encoder. 4 12bits ±10Vdc D/A channels. 8 Opto-in; 8 NPN Opto-output 40Vdc 500 mA. All I/O lines displayed with LEDs.
BIBLIOGRAPHY

Here follows a list of manuals that can be a source of further information about the devices installed on GPC® 153.

TEXAS INSTRUMENTS manual: The TTL Data Book - SN54/74 Families
TEXAS INSTRUMENTS manual: RS-422 and RS-485 Interface Circuits
TEXAS INSTRUMENTS manual: Linear Circuits Data Book - Volumi 1 e 3

HEWLETT PACKARD manual: Optoelectronics Designer’s Catalog

NEC manual: Memory Products

SGS-THOMSON manual: Programmable Logic Manual GAL Products

MAXIM manual: New Releases Data Book - Volume IV
MAXIM manual: New Releases Data Book - Volume V

XICOR manual: Data Book


NATIONAL SEMICONDUCTOR manual: Linear Databook - Volume 1

SEIKO EPSON data sheet: RTC-62421 Real Time Clock module

Please connect to the manufacturers’ websites to get the latest version of all manuals and data sheets.
APPENDIX A: ELECTRIC DIAGRAMS

This chapter shows the electric diagram of the most frequently used interfaces for GPC® 153. Every one of these interfaces can be made by the User in autonomy, while only few of them are grifo® standard boards and can be ordered.

**Figure A1: IAC 01 Electric Diagram**
**Title:** KDL/F-2/424

**Date:** 22-07-1998

**Page:** 1 of 1

**Figure A2: KDx x24 Electric Diagram**

- **I/O 20 pins**
  - PA.7, PA.6, PA.5, PA.4, PA.3, PA.2, PA.1, PA.0
  - PC.2, PC.1, PC.0, PC.3, PC.4
  - CN3

- **VFD Futaba**
  - D7, D6, D5, D4, D3, D2, D1
  - CN5

- **LCD 20x2**
  - CN6

- **LCD 20x4**
  - CN4

- **Components:**
  - C1, C2, C3, C4, C5 (100nF, 22µF 6.3V Tantalium)
  - R1, R2, R3, R4, R5, R6, R7, R8, R9, RR1, RR2 (18kΩ, 47kΩ, 470kΩ, 2.2kΩ 9+1 SIP, 10kΩ trimmer)
  - IC1 (7407)
  - CN2, CN4 (2 pins mini male connector, 10 pins male strip)
  - CN3 (20 pins male low profile connector)
  - CN4 (LCD L214 (20x4), LCD VFD20x2, LCD L2012 (20x2))
  - IC1 (7407)
  - J1 (2 pins female jumper)

- **External Keyboard 4x6**
  - D0-D5
  - R0-R5

- **Notes:**
  - LCD20x2, LCD20x4, Futaba VFD
  - R1 = 0Ω, N.M., N.M.
  - R2 = N.M., 12Ω, N.M.
  - R3 = N.M., 12Ω, N.M.
  - R4 = 18Ω, 12Ω, N.M.
  - R5 = N.M., N.M., N.M.
  - R6 = 470Ω
  - R7 = 470Ω
  - R8 = 470Ω
  - R9 = 470Ω
  - RR1 = 22kΩ 9+1 SIP
  - RR2 = 22kΩ 9+1 SIP
  - RV1 = 10kΩ trimmer
  - C1 = 100µF
  - C2 = 22µF 6.3V Tantalium
  - C3 = 100µF
  - R8 = 100Ω
  - C5 = 22µF 6.3V Tantalium
  - CN1 = 2 pins mini male connector
  - CN2 = 20 pins female jumper
**FIGURE A3: QTP 16P ELECTRIC DIAGRAM**
FIGURE A4: QTP 24P ELECTRIC DIAGRAM - PART 1
Figure A5: QTP 24P Electric Diagram - Part 2
FIGURE A6: SPA 03 ELECTRIC DIAGRAM
Appendix B: On Board Components Description

CPU Z84C15

Product Specification

Z84013/015  
Z84C13/Z84C15

IPC Intelligent Peripheral Controller

Features

- Z84C00 Z80 CPU with Z84C30 CTC, Z84C4X SIO,  
  CGC, Watch Dog Timer (WDT). In addition, Z84C15  
  and Z84015 have Z84C20 PIO.

- High speed operation 6, 10 MHz

- 16 MHz operation for Z84C15 only.

- Low power consumption in four operation modes:
  - 41 mA Typ. (Run mode)
  - 6 mA Typ. (Idle1 mode)
  - 50 µA Typ. (Idle2 mode)
  - 0.5 µA Typ. (Stop mode)

- Wide operational voltage range (5V ± 10%)  
- TTL/CMOS compatible.

- Z84C00 features:
  - Z84000 Z80 CPU
  - On-chip two channel SIO (Z80 SIO)
  - On-chip four channel Counter Timer Controller  
    (Z80 CTC)
  - Built-in Clock Generator Controller (CGC).

- Built-in Watch Dog Timer (WDT).
- Noise filter to CLS/TRG inputs of the CTC.
- 84-pin PLCC package.

Z84C15 features:

- All Z84013 features, plus on-chip two 8-bit ports  
  (Z80 PIO) and 100-pin QFP package.

- Power-on reset.
- Addition of two chip select pins.
- 32-bit CRC for Channel A of SIO.
- Wait state generator.
- Simplified EV mode selection.
- Schmitt-trigger inputs to transmit and receive clocks  
  of the SIO.
- Crystal divide-by-one mode.
- 100-pin QFP (Z84C15 only)

Z84C13/Z84C15 enhancements to Z84013/Z84015:

2-69

General Description

The Intelligent Peripheral Controller (IPC) is a series of  
highly super-integrated devices with four versions. The  
Z84C13 and the Z84C15 are upward compatible versions  
of the Z84013 and the Z84015. The Z84013 is a CMOS  
8-bit microprocessor integrated with the CTC, SIO, CGC,  
WDT and the PIO into a single 100-pin Quad Flat Pack(QFP)  
package. The Z84013 is the Z84015 without PIO, and is  
housed in a 84-pin PLCC package. The Z84C13 is the  
Z84013 with enhancements and the Z84C15 is the Z84015  
with enhancements. These high-end super-integrated  
intelligent peripheral controllers are targeted for a broad  
range of applications ranging from error correcting mo-  
dems to enhancement/cost reductions of existing hard-  
ware using Z80-based discrete peripherals. Figures 1 and  
2 show the difference between the Z84013/015 and the  
Z84C13/Z84C15.

Hereinafter, use the word IPC on the description covering  
all versions (Z84C13/Z84C15 and Z84013/Z84015). Use  
Z84C13/C15 on the description that applies only to  
the Z84C13 and Z84C15, and use Z84013/015 on the descrip-  
tion that applies only to the Z84013 and Z84015.
### CPU SIGNALS

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Input/Output, 3-State</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>A0-A15</td>
<td>16-(x13), 6-1, 100-91(x15)</td>
<td>IO</td>
<td>16-bit address bus. Specifis I/O and memory addresses to be accessed. During the refresh period, addresses for refreshing are output. The bus is an input when the external master is accessing the on-chip peripherals.</td>
</tr>
<tr>
<td>D0-D7</td>
<td>63-76(x13), 88-11(x15)</td>
<td>IO</td>
<td>6-bit bidirectional data bus. When the on-chip CPU is accessing on-chip peripherals, these lines are set to output and hold the data to/from on-chip peripherals.</td>
</tr>
<tr>
<td>IRD</td>
<td>30(x13), 14(x15)</td>
<td>IO</td>
<td>Read signal. CPU read signal for addressing data from memory or I/O devices. When an external master is accessing the on-chip peripherals, it is an input signal.</td>
</tr>
<tr>
<td>WR</td>
<td>20(x13), 13(x15)</td>
<td>IO</td>
<td>Write signal. This signal is output when data, to be stored in a specified memory or peripheral LSI, is on the MPU data bus. When an external master is accessing the on-chip peripherals, it is an input signal.</td>
</tr>
<tr>
<td>MREQ</td>
<td>23(x13), 17(x15)</td>
<td>IO, 3-State</td>
<td>Memory request signal. When an effective address for memory access is on the address bus, &quot;0&quot; is output. When an external master is accessing the on-chip peripherals, it is an input signal.</td>
</tr>
<tr>
<td>IORQ</td>
<td>21(x13), 15(x15)</td>
<td>IO</td>
<td>I/O request signal. When addresses for I/O are on the lower 8 bits (A7-A0) of the address bus in the I/O operation, &quot;0&quot; is output. In addition, the IORQ signal is output with the M1 signal at the time of interrupt acknowledge cycle to inform peripheral LSI of the status of the interrupt response vector that is called on the data bus. When an external master is accessing the on-chip peripherals, it is an input signal.</td>
</tr>
<tr>
<td>M1</td>
<td>17(x13), 80(x15)</td>
<td>IO</td>
<td>Machine cycle *1&quot;, IORQ and &quot;0&quot; are output together in the operation code fetch cycle. M1 is output for every opcode fetch when a two byte opcode is executed. In the maskable interrupt acknowledge cycle, this signal is output together with IORQ. It is 3-stated in EV mode.</td>
</tr>
</tbody>
</table>

---

**Figure 4. Z84015/Z84C15 Pin-out Assignments**

**PIN DEFINITIONS**

The pin assignment for each device is shown in Figures 3 and 4. Following is the description on each pin. For the description and the pin number, it stated as "x13" or "x15", that applies to both Z84C13/2Z84013 or Z84C15/2Z84015. Otherwise, G13 for Z84C13, G15 for Z84015, 013 for Z84013 and 015 for Z84015.
### CPU SIGNALS (Continued)

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Input/Output, State</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>RFSH</td>
<td>26(x13), 7(x15)</td>
<td>Out, 3-State</td>
<td>The refresh signal. When the dynamic memory refresh address is on the low order byte of the address bus, RFSH is active along with MREQ signal. This pin is 3-stated in BV mode.</td>
</tr>
<tr>
<td>INT</td>
<td>53(x13), 19(x15)</td>
<td>Open drain</td>
<td>Maskable interrupt request signal. Interrupt is generated by peripheral LSI. The signal is accepted if the Interrupt enable Flip-Fop (IFF) is set to &quot;1&quot;. The INT signal of on-chip peripheral is internally wired OR without pull-up resistors and requires external pull-up. Also, interrupts from on-chip peripherals go out from this pin.</td>
</tr>
<tr>
<td>INH</td>
<td>56(x13), 60(x15)</td>
<td>In</td>
<td>Non-maskable interrupt request signal. This interrupt request has a higher priority than the maskable interrupt request and does not rely upon the state of the interrupt enable Flip-Fop (IFF).</td>
</tr>
<tr>
<td>HALT</td>
<td>31(x13), 81(x15)</td>
<td>Out, 3-State</td>
<td>Halt signal. Indicates that the CPU has executed a HALT instruction. This signal is 3-stated in BV mode.</td>
</tr>
<tr>
<td>BUSREQ</td>
<td>18(x13), 120(x15)</td>
<td>In</td>
<td>BUS request signal. BUSREQ requests placement of the address bus, data bus, MREQ, /IOR, /IRD and NWR into the high impedance state. BUSREQ is normally wired OR and a pull-up resistor is externally connected.</td>
</tr>
<tr>
<td>BUSACK</td>
<td>20(x13), 12(x15)</td>
<td>Out (8'1300), 0(x120) (C19/C16)</td>
<td>Bus Acknowledge signal. In response to BUSREQ signal, BUSACK informs a peripheral that the address bus, data bus, MREQ, /IOR, /IRD and NWR signals have been placed in the high impedance state.</td>
</tr>
</tbody>
</table>

**Note:** For the 28413015, the BUSACK signal will be 3-stated during BV mode. For the 28413015 the BUSACK will be gated during BV mode.

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Input/Output, State</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>ATRF</td>
<td>55(x13), 70(x15)</td>
<td>Out</td>
<td>1-bit auxiliary address bus. Output is the same as bus A7 (A7) of the address bus. However, during a refresh cycle, this pin outputs the address which is the most significant bit of the 8-bit refresh address signal linked to the low order 7 bits of the address bus.</td>
</tr>
</tbody>
</table>

### CTC SIGNALS

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Input/Output, State</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLK/TRG0 - CLK/TRG3</td>
<td>75-77(x13), 81-78(x16)</td>
<td>In</td>
<td>External clock trigger input. These four CLK/ TRG pins correspond to four Counter/Timer Channels. In the counter modes, each active edge will cause the down-counter to decrement by one. In timer modes, an active edge will start the timer. It is program selectable whether the active edge is rising or falling.</td>
</tr>
<tr>
<td>ZC/TOO - ZC/TO3</td>
<td>68-7(x13), 76-77(x15)</td>
<td>Out</td>
<td>Zero count/trigger out signals. In either timer or counter mode, pulses are output when the down-counter has reached zero.</td>
</tr>
</tbody>
</table>

### SIO SIGNALS

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Input/Output, State</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>WRDY A</td>
<td>32,54(x13), 30,52(x15)</td>
<td>Out</td>
<td>WrA/Ready Signal A. If WrA is high, the CPU waits for the Ready signal.</td>
</tr>
<tr>
<td>WRDY B</td>
<td>32,54(x13), 30,52(x15)</td>
<td>Out</td>
<td>WrB/Ready Signal B. If WrB is high, the CPU waits for the Ready signal.</td>
</tr>
</tbody>
</table>

**Note:** For the 28413015, the WAIT pin becomes an output to bring out on-chip wait state generator during the BV mode.
### SIO SIGNALS (Continued)

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Input/Output, 3-State</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>/RXCA, /RXCB</td>
<td>35,51(x13), 33,49(x15)</td>
<td>In</td>
<td>Receive clock signal. In the asynchronous mode, the receive clock can be 1, 15, 32, or 64 times the data transfer rate.</td>
</tr>
<tr>
<td>/TXCA, /TXCB</td>
<td>35,50(x13), 34,48(x15)</td>
<td>In</td>
<td>Transmitter clock signal. In the asynchronous mode, the transmitter clock can be 1, 15, 32, or 64 times the data transfer rate.</td>
</tr>
<tr>
<td>TDXA, TDXB</td>
<td>37,49(x13), 37,47(x15)</td>
<td>Out</td>
<td>Serial transmit data signal.</td>
</tr>
<tr>
<td>TDRA, TDRB</td>
<td>38,48(x13), 38,46(x15)</td>
<td>Out</td>
<td>Data terminal ready signal. When ready, these signals go active to enable the terminal transmitter. When not ready, they go inactive to disable the transfer from the terminal.</td>
</tr>
<tr>
<td>RTSA, RTSB</td>
<td>39,47(x13), 37,40(x15)</td>
<td>Out</td>
<td>Request to send signal. When &quot;0&quot;, sends data signals. When &quot;1&quot;, circulates the data.</td>
</tr>
<tr>
<td>CTS</td>
<td>40,46(x13), 36,44(x15)</td>
<td>In</td>
<td>Clear to send signal. When &quot;0&quot;, after transmitting these signals, the modem is ready to receive serial data. When ready, these signals go active to enable terminal transmitter. When ready, these signals go inactive to disable transfer from the terminal.</td>
</tr>
<tr>
<td>RXDA, RXDB</td>
<td>41,45(x13), 38,43(x15)</td>
<td>In</td>
<td>Data carrier detect signal. When &quot;0&quot;, serial data cannot be received. These signals are active to enable receivers to transmit.</td>
</tr>
</tbody>
</table>

### SYSTEM CONTROL SIGNALS

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Input/Output, 3-State</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>IEI</td>
<td>60(x13), 71(x15)</td>
<td>In</td>
<td>Interrupt enable input signal. IEI is used with the IEO to form a priority daisy chain where there is more than one interrupt driven peripheral.</td>
</tr>
<tr>
<td>IEO</td>
<td>59(x13), 71(x15)</td>
<td>Out</td>
<td>The interrupt enable output signal in the daisy chain interrupt control. IEO controls the interrupt of external peripherals. IEO is active when IE1 is &quot;1&quot; and the CPU is not servicing an interrupt from the on-chip peripherals.</td>
</tr>
<tr>
<td>JCO</td>
<td>42(C13), 40(C15)</td>
<td>Out</td>
<td>Chip Select 0. Used to access external memory or I/O devices. This pin has been assigned to &quot;CT&quot; pin on 28401-016. This signal is decoded only from A15-A12 without control signals. Refer to &quot;Functional Description&quot; on-chip select signals for further explanation.</td>
</tr>
</tbody>
</table>

### SYSTEM CONTROL SIGNALS (Continued)

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Input/Output, 3-State</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>ASE</td>
<td>40(x13), 42(x15)</td>
<td>Out</td>
<td>Chip Select 1. Used to access external memory or I/O devices. This pin has been assigned to &quot;CT&quot; pin on 28401-016. This signal is decoded only from A15-A12 without control signals. Refer to &quot;Functional Description&quot; on-chip select signals for further explanation.</td>
</tr>
<tr>
<td>WOOUT</td>
<td>64(x13), 73(x15)</td>
<td>Out</td>
<td>Watchdog Timer Output signal. Output pulse width depends on the externally connected pin.</td>
</tr>
<tr>
<td>RESET</td>
<td>28(x13), 9(x15)</td>
<td>In</td>
<td>Input(16), I/O (Open Drain) (C13/C15)</td>
</tr>
</tbody>
</table>

Note: For the 28401-016, the RESET must be kept in active state for a period of at least three system clock cycles.

Note: For the 28401-016, during the power-up sequence, the RESET becomes an Open drain output and the 28401-016 will drive the pin to "0" for 25 to 75 microsecond after the power supply passes through 8 volts and then returns to input. If it receives the RESET signal after power on sequence, it will drive the INT pin for 15 processor clock cycles depending on the status of Reset Output On Boot bit in Micro Computer Register. If the Reset output is observed, it must be kept in active state for a period of at least three system clock cycles. Note: For the 28401-016, in 28401-016, the only method of returning to the operational state is to drive INT low for 15 processor clock cycles. For more details on the device, please refer to "Functional Description."
SYSTEM CONTROL SIGNALS (Continued)

Note: For the 2634/13C15, in access to chip connectors from the CPU (e.g., ICE CPU3), the CPU is electrically disconnected; A15-A0, ADDR1-0, RD and WR are charged to input 5V. Ctrl signals are discussed. M1, M0, M3, M4 are the pull-up/push-down pins when the VCC pin is set to 1.5V. BUSCH 5 is static. For details, please refer to "Functional Description" on V0 mode.

Pin Name | Pin Number | Input/Output | Function
---|---|---|---
ICT | 42, 44(013, 40, 42(015), Not with C13C15) | Out | Test pin. Used in the open state.
NC | 34, 37, 67, 69(013), flat with x15 | Not connected.
VCC | 43, 84(x13, 41, 30(x15) | Power Supply | +5 Vols
VSS | 22, 63(x13), 18, 64(x15) | Power Supply | 0 Vols

PIO SIGNALS (for the Z84x15 only)

Pin Name | Pin Number | Input/Output | Function
---|---|---|---
/ASTB | 01(x15) | In | Port A strobe pulse from a peripheral device. This signal is used as the handshake between Port A and external circuits. The meaning of this signal depends on the mode of operation selected for Port A (see "PIO Basic Timing").
/STB | 01(x15) | In | Port B strobe pulse from a peripheral device. This signal is used as the handshake between Port B and external circuits. The meaning of this signal is the same as /ASTB, except when Port A is in mode 2 (see "PIO Basic Timing").
ARDY | 20(x15) | Out | Register A ready signal. Used as the handshake between Port A and external circuits. The meaning of this signal is the same as /ASTB (see "PIO Basic Timing").
BRDY | 62(x15) | Out | Register B ready signal. Used as the handshake between Port B and external circuits. The meaning of this signal is the same as /ASTB except when Port A is in mode 2 (see "PIO Basic Timing").
PA7-PAS | 22-29(x15) | IO, 3-State | Port A data signals. Used for data transfer between Port A and external circuits.
PB7-PB0 | 53-60(x15) | IO, 3-State | Port B data signals. Used for transfer between Port B and external circuits.

The following pins have different functions between 013/015 and C13/C15:

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin # X13</th>
<th>Pin # X15</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>RESET</td>
<td>22</td>
<td>9</td>
<td>Functionality is different.</td>
</tr>
<tr>
<td>WAIT</td>
<td>15</td>
<td>15</td>
<td>Functionality is different.</td>
</tr>
<tr>
<td>EV</td>
<td>55</td>
<td>57</td>
<td>Functionality is different.</td>
</tr>
<tr>
<td>NWDOUT</td>
<td>61</td>
<td>75</td>
<td>Push-pull output on Z8413015, Open drain on Z84 C13C15</td>
</tr>
<tr>
<td>ICT</td>
<td>45, 46</td>
<td>45, 46</td>
<td>(Test pin) on Z8413015, C25 and C21 on Z84C1315.</td>
</tr>
<tr>
<td>TxC, TxB, RXA and RXB</td>
<td>30, 36, 50, 51</td>
<td>35, 34, 38, 39</td>
<td>On Z84C1315, these signals have Schmitt-triggered inputs</td>
</tr>
</tbody>
</table>

In EV mode, 3-state on Z84C13/15/16 remains active on Z8413015.

FUNCTIONAL DESCRIPTION

Figure 5(a) shows the functional block diagram of the Z8413015 and Figure 5(b) shows the functional block diagram of the 2634/13C15. It describes section, the only difference between a Z8413 and the Z84x13 is that the Z84x15 is the PIO not being included in the Z84x13.

Functionally, the only SOClPIO (not available on Z8413), CTC, and the Z80 CPU are the same as the devices. Therefore, for detailed description of each individual unit, refer to the Product Specification and Technical Manual of each individual device.

The following sub-sections describe each individual functional unit of the PIC.

Z84C000/01 Logil Unit

This CPU provides all the capabilities and pins of the Z80 CPU with 280 software in addition, it has the pin called "ACK" to expand the DMA refresh address to 280. Refer to "Z84C0113015 CPU with C25 Product Specification".

Z84C20 Parallel Input/Output Logic Unit (Z84x15 Only)

This logic unit provides both TTL and CMOS compatible interfaces between peripheral devices and a CPU through the use of two 8-bit parallel ports (Figure 6). The CPU configures the logic interfaces to a wide range of peripheral devices. Typical devices with an external logic are keyboards, printers, and EPROM/PAL programmers.

The parallel ports (designated Port A and Port B) are byte wide and completely compatible with the Z84C010 PIO.

These two ports have several modes of operation: input, output, bidirectional, or bit control mode. Each port has two handshake signals (RDY and STB) which are used to control data transfers. The RDY (ready) indicates that the port is ready for data transfer. The STB (strobe) is input to the port that indicates when data transfer has occurred. Each of the ports can be programmed to interrupt the CPU upon the occurrence of specified status conditions, and generate an interrupt vector when the CPU responds. For more information on the operation of this portion of the logic, please refer to the Z84C20 Product Specification and Technical Manual.

Z84C30 Counter/Timer Logic Unit

This logic unit provides the user with four individual 8-bit Counter/Timer Channels that are compatible with the Z84C30 CTC (Figure 7). The Counter/Timer Channels can be programmed by the CPU for a wide range of counting and timing applications. Typical applications include event counting, interrupt processing, and serial baud rate clock generation.

Each of the Counter/Timer Channels, designated Channels 0-3, have an 8-bit prescaler (when used in timer mode) and to its own 8-bit counter to provide a wide range of count resolution. Each of the channels have their own Clock/Trigger input to quantify the counting process and an output to indicate zero crossing/timeout conditions. With only one interrupt vector programmed into the logic unit, each channel can generate a unique interrupt vector in response to the interrupt acknowledge cycle.
28HC4x Serial I/O Logic Unit

The logic unit provides the user with two asynchronous multi-protocol serial I/O channels that are completely compatible with the 28HC4x SIO. Their basic functions are serial-to-parallel and parallel-to-serial conversions can be programmed by a CPU for a broad range of serial communications applications. Each channel, dedicated Channel A and Channel B, is capable of supporting all common synchronous and asynchronous protocols (Manchester, BiIEEE, and SOCH/DLC, byte or bit oriented - Figure 8).

28HC13C16 Only. As an enhancement to the 28HC13C15, the 28HC13C16 can handle a 32-bit CRC on Channel A and Channel B, capable of handling CRC input on the TXC and RXC pins of both channels.
Watch Dog Timer (WDT) Logic Unit

This logic unit has been superimposed onto the IPC. It detects an operation error, caused by the program runaway, and returns to normal operation. Figure 8, shows the block diagram of the WDT. Upon power-on reset, this unit is enabled. If WDT is not required, but WDTOUT is connected to RESET or any other circuit, it has to be disabled.

During the power-down mode of operation (other than Idle), the Watch Dog Timer is halted.

WDT Output (WDTOUT pin): When the WDT is used, the 'O' level signal is output from the WDTOUT pin after a duration of time specified in the WDT or in the WDTMR. The output pulse width is one of the following, depending on the WDTOUT pin connection.

- The WDTOUT is connected to the RESET pin. The 'O' level is pulled for 0.02 ms (System clock cycles).
- The WDTOUT is connected to a pin other than the RESET pin. The 'O' level is held until the Watch Dog timer is cleared by software, or read by the RESET pin.

CGC Logic Unit: The CGC has three components: Clock Generator (CGC), Control (CGC), and Output (CGC). The CGC unit has the following functions: GPO, SPO, STPO, and Watch Dog Timer (WDT). The CGC unit also supports power-down modes of operation. The output from this unit is on the pin called CCLKOUT, which is connected to the system clock frequency. The CGC unit also includes a counter that is used for output control. The output from the CGC unit is on the pin called CCLKOUT. The user can connect CCLKOUT to CCLK to utilize the CGC unit or supply external clock (from CLKN pin).

The CGC unit allows four different clock sources: XTAL1, XTAL2, and External Clock. In the XTAL1 mode, it has clock output divided by two circuits and generates a half-speed clock to the input.

Z84015/C155: The power-down modes of the IPC vary depending upon whether the system clock is fed from the CGC unit or the external clock source on the CLKN pin. They also have divide-by-two mode. If the clock is supplied by the CGC unit, all of the modes in 'hall' state are available. When external clock is provided on the CLKN pin, XTAL1 is not open (led to 'O' or '1') to avoid meta-stable conditions to minimize power consumption.

Z84015/C155 Only: If the system clock is provided on the CLKN pin, none of the power-down mode (except RUN mode) is supported.

Z84C15/C155: Clock output is the same, or half, of the external frequency.

System Clock Generation

The IPC has a built-in oscillator circuit and the required clock can be easily generated by connecting a crystal to the external terminals (XTAL1, XTAL2). Clock output is the same frequency as half the speed of the crystal frequency. Example of oscillator connections are shown in Figure 10.
Recommended characteristics of the crystal and the values for the capacitor are as follows (the values will change with crystal frequency).

- **Type of crystal**: Fundamental, parallel type crystal
- **AT cut is recommended**.
- **Frequency tolerance**: Application dependent.

Other functional features (2B4C3/C15 Only)

- **Memory Wait and Opcode wait**: The Wait State Generator can insert 0, 2, or 4 wait states in memory accesses. Addionally, a single wait state can be inserted during an IMU (Opcode fetch) cycle, because IMU cycle timing requirements are different than memory Read/Wire cycles. It generates wait states in the Memory Access in a specified address range, which is programmed in the Memory Wait Boundary Register.
- **I/O Wait**: The Wait State generator can insert 0, 2, or 4 wait states in I/O accesses. Regardless of the programming in this field, no I/O wait states are inserted for accesses to external peripherals.

Clock Divide-by-One Option

- **Reset Output Disable**

- **32-bit CRC Generator/Checking**: This feature is programmed by Bit 2 of CRG. If the CRC is enabled, the Checksum/CRG and the 32-bit CRC Generator/Checking are used in the same cycle. If the CRC is disabled, the Checksum/CRG and the 32-bit CRC Generator/Checking are used in asynchronous modes. The polynomial to be used in this mode is the one for the protocols such as V.41, and is 03D = X8 + 2X5 + 2X2 + 1.

**Programming**

- **I/O address assignment**: The I/O address configuration of the 2B4C3/C15 is shown in Table 1. They are fully decoded from 0 to 255, and no I/O addresses are reserved for any other control purposes. The lower 8-bit address of the 2B4C3/C15 is connected to the external CPU.
Table 1. I/O Control Register Address

<table>
<thead>
<tr>
<th>Address</th>
<th>Device</th>
<th>Channel</th>
<th>Register</th>
</tr>
</thead>
<tbody>
<tr>
<td>16h</td>
<td>CTC</td>
<td>Ch 0</td>
<td>Control Register</td>
</tr>
<tr>
<td>11h</td>
<td>CTC</td>
<td>Ch 1</td>
<td>Control Register</td>
</tr>
<tr>
<td>12h</td>
<td>CTC</td>
<td>Ch 2</td>
<td>Control Register</td>
</tr>
<tr>
<td>13h</td>
<td>CTC</td>
<td>Ch 3</td>
<td>Control Register</td>
</tr>
<tr>
<td>18h</td>
<td>SID</td>
<td>Ch A</td>
<td>Data Register</td>
</tr>
<tr>
<td>19h</td>
<td>SID</td>
<td>Ch A</td>
<td>Data Register</td>
</tr>
<tr>
<td>1Ah</td>
<td>SID</td>
<td>Ch B</td>
<td>Data Register</td>
</tr>
<tr>
<td>1Bh</td>
<td>SID</td>
<td>Ch B</td>
<td>Data Register</td>
</tr>
<tr>
<td>1Ch</td>
<td>PID</td>
<td>Port A</td>
<td>Data Register (Not with Z841413)</td>
</tr>
<tr>
<td>1Dh</td>
<td>PID</td>
<td>Port A</td>
<td>Command Register (Not with Z841413)</td>
</tr>
<tr>
<td>1Eh</td>
<td>PID</td>
<td>Port B</td>
<td>Data Register (Not with Z841413)</td>
</tr>
<tr>
<td>1Fh</td>
<td>PID</td>
<td>Port B</td>
<td>Command Register (Not with Z841413)</td>
</tr>
<tr>
<td>20h</td>
<td>Watch-Dog Timer</td>
<td>Watch-Dog Timer</td>
<td>Master Register (WD7M7R)</td>
</tr>
<tr>
<td>21h</td>
<td>Watch-Dog Timer</td>
<td>Watch-Dog Timer</td>
<td>Control Register (WDTCR)</td>
</tr>
<tr>
<td>22h</td>
<td>Watch-Dog Timer</td>
<td>Interrupt Priority Register</td>
<td></td>
</tr>
<tr>
<td>23h</td>
<td>Watch-Dog Timer</td>
<td>Interrupt Priority Register</td>
<td></td>
</tr>
<tr>
<td>24h</td>
<td>Watch-Dog Timer</td>
<td>Interrupt Priority Register</td>
<td></td>
</tr>
<tr>
<td>25h</td>
<td>Watch-Dog Timer</td>
<td>Interrupt Priority Register</td>
<td></td>
</tr>
<tr>
<td>26h</td>
<td>Watch-Dog Timer</td>
<td>Interrupt Priority Register</td>
<td></td>
</tr>
<tr>
<td>27h</td>
<td>Watch-Dog Timer</td>
<td>Interrupt Priority Register</td>
<td></td>
</tr>
<tr>
<td>28h</td>
<td>Watch-Dog Timer</td>
<td>Interrupt Priority Register</td>
<td></td>
</tr>
<tr>
<td>29h</td>
<td>Watch-Dog Timer</td>
<td>Interrupt Priority Register</td>
<td></td>
</tr>
<tr>
<td>2Ah</td>
<td>Watch-Dog Timer</td>
<td>Interrupt Priority Register</td>
<td></td>
</tr>
<tr>
<td>2Bh</td>
<td>Watch-Dog Timer</td>
<td>Interrupt Priority Register</td>
<td></td>
</tr>
<tr>
<td>2Ch</td>
<td>Watch-Dog Timer</td>
<td>Interrupt Priority Register</td>
<td></td>
</tr>
<tr>
<td>2Dh</td>
<td>Watch-Dog Timer</td>
<td>Interrupt Priority Register</td>
<td></td>
</tr>
<tr>
<td>2Eh</td>
<td>Watch-Dog Timer</td>
<td>Interrupt Priority Register</td>
<td></td>
</tr>
<tr>
<td>2Fh</td>
<td>Watch-Dog Timer</td>
<td>Interrupt Priority Register</td>
<td></td>
</tr>
</tbody>
</table>

PIO REGISTERS

For more detailed information, please refer to the PIO Technical Manual. These registers are not in the Z841413.

Interrupt Vector Word

The PIO logic unit is designed to work with the Z80 CPU in interrupt Mode 3. This interrupt word must be programmed if interrupts are used. Bit D0 must be a zero (Figure 11).

Mode Control Word

Selects the port operating mode. This word is required and is written at any time (Figure 12).

IDO 0 1 2 3 4 5 6 7
Figure 12. PIO Mode Control Word

I/O Register Control Word

When Mode 3 is selected, the Mode Control Word is followed by the I/O Register Control Word. This word configures the I/O register, which defines which ports lines are inputs or outputs. A "1" indicates input while a "0" indicates output. This word is required when in Mode 3 (Figure 13).

Figure 13. I/O Register Control Word

Interrupt Control Word

In Mode 3 operation, handshake signals are not used. Interrupts are generated as a logic function of the input signal levels. The Interrupt Control Word sets the logic conditions and the logic levels required for generating an interrupt. Two logic conditions or functions are available: AND (if all input bits change to the active level an interrupt is triggered); OR (if any one of the input bits change to the active logic level, an interrupt is triggered). The user can program which input bits are to be considered as part of this logic function. Bit D0 sets the logic function, bit D1 sets the logic level, and bit D4 specifies a mask control word to follow (Figure 14).

Figure 14. Interrupt Control Word

Interrupt Mask Word

This word sets the mask control register, thus allowing any unused bits to be masked off. Any bits that are to be masked, then bit D4 of the Interrupt Control Word is set. When bit D4 of the interrupt Control Word is set, then the next word programmed is the Mask Control Word. To mask an input bit, the corresponding Mask Control Word bit is a "1" (Figure 15).

Figure 15. Mask Control Word

Interrupt Disable Word

This word can be used to enable or disable a port's interrupts without changing the rest of the port's interrupt conditions (Figure 16).
CTC CONTROL REGISTERS

For more detailed information, refer to the CTC Technical Manual.

Channel Control Word
This word sets the operating modes and parameters as described below. Bit 00 is a *1* to indicate that this is a Control Word (Figure 17).

![Figure 17. CTC Channel Control Word](image)

**Bit D6:** Mode Bit. This bit selects either Timer Mode or Counter Mode.

**Bit D5:** Precisor Factor. This bit selects the precision factor for use in the timer mode. Either divide-by-0 or divide-by-256 is available.

**Bit D4:** Clock/Trigger Edge Selector. This bit selects the active edge of the C/TKRC input pulses.

**Bit D3:** Timer Trigger. This bit selects the trigger mode for timer operation. Either automatic or external trigger may be selected.

**Bit D2:** Time Constant. This bit indicates that the next word programmed is time constant data for the counter.

**Bit D1:** Software Reset. Writing 1 to this bit indicates a software reset operation, which stops counting activities until another time constant word is written. (Figure 18).

**Time Constant Word**
Before a channel starts counting, it must receive a time constant word. The time constant value is anywhere between 1 and 256, with 0 being accepted as a count of 256 (Figure 18).

![Figure 18. CTC Time Constant Word](image)

**Interrupt Vector Word**
If one or more of the CTC channels have Interrupt enabled, then the Interrupt Vector Word must be programmed. Only the least significant bits of this word are programmed, and bit 00 must be "0." Bits D2-D1 are automatically modified by the CTC channels which it responds with an interrupt vector (Figure 19).

![Figure 19. CTC Interrupt Vector Word](image)

**SIO REGISTERS**
For more detailed information, refer to the SIO Technical Manual.

Read Registers. The SIO channel B contains three read registers while channel A contains only two that are read to contain status information. To read the contents of a register (rather than PRD), the program must first write a pointer to WRD in exactly the same manner as a write operation. The next I/O read cycle will place the contents of the selected read registers onto the data bus (Figure 20a, b, c).

![Figure 20a. SIO Read Register 0](image)

![Figure 20b. SIO Read Register 1](image)

![Figure 20c. SIO Read Register 2](image)

Write Registers. The SIO Channel B contains eight write registers while channel A contains only seven that are programmed to configure the operating mode characteristics of each channel. With the exception of WRD, programming the write registers is a two-step operation. The first operation is a pointerwritten to WRD which points to the selected register. The second operation is the actual control word that is written into the register to configure the SIO channel (Figure 21).
WATCh DOG CONTROL REGISTERS

There are two registers to control WatchDog Timer operation: the WatchDog Timer Master Register (WDTMR, IO Address F8h) and the WatchDog Command Register (WDTCR, IO Address F9h). WatchDog Time Logic has a "double-key" structure to prevent the WDT disabling error, which may lead to the WDT operation to stop due to program runaway. Programming the WDT follows this procedure. Also, these registers program the power-down mode of operation. The "Second key" is needed when turning off the WatchDog Timer.

Enabling the WDT: The WDT is enabled by setting the WDT Enable bit (D7, WDTEN) to "1" and the WDT Periodic field (DS, WDTP) to the desired time period. These command bits are in the WatchDog Timer Master Register (WDTMR, IO Address F8h).

Disabling the WDT: The WDT is disabled by clearing WDT Enable bit (WDTEN) in the WDTMR to "0" followed by writing "01h" to the WDT Command Register (WDTCR, IO Address F9h).
Clearing the WDT. The WDT can be cleared by writing "BBH" into the WDTO.

Watch Dog Timer Master Register (WDTMR, I/O address FAFH). This register controls the activities of the Watch Dog Timer and selects power-down mode of operation (Figure 22).

![Figure 22. Watch Dog Timer Master Register](image)

Bit D17. Watch Dog Timer Enable (WDE). This bit controls the activities of the Watch Dog Timer. The WDT can be enabled by setting the bit to "1". To disable WDT, write "0" to this bit followed by writing "BBH" in the WDTO Command Register. Watch Dog Timer... (Figure 23)

![Figure 23. Watch Dog Timer Command Register](image)

Bit D8-D0. WDT Periodic Delay (WDT.P). This two-bit field determines the desired delay period. Upon Power-on reset, this field sets to "11".

Bit D4-D3. HALT mode (HALTM). This two-bit field specifies one of four power-down modes. To change this field, write "BBH" to the WDTO command register, followed by a write to this register. For detailed descriptions of this field, please refer to the section "Mode of operations." Upon Power-on Reset, this field is set to 11, which specifies "RUN mode."

00 - IDLE 1 Mode
01 - IDLE 2 Mode
10 - ST0 Mode
11 - RUN Mode

![Figure 24. Interrupt Priority Register](image)

Interrupt Priority Register (ITPR, I/O address F4H)

This register (write only) is provided to determine the interrupt priority for the GTC, SIG and the PIO (Figure 24).

![Figure 25. System Control Register Pointer](image)

System Control Register Pointer (SCRP, I/O address F9H)

This register stores the pointer to the System Control Register (SCR, WCR, CSBR and MCR). This register is Read/Write and it holds the pointer value until modified. Upon Power-on Reset, all bits are cleared to zero. The pointer value, other than 00H to 0FH, is reserved and not written. Upon Power-on Reset, this register is set to "00H" (Figure 25).

![Figure 26. System Control Data Port](image)

System Control Data Port (SCDP, I/O address FEH)

This register is to access WCR, WMBR, CSBR and MCR (Figure 26).

Wait State Control Register (WCR, Control Register 00H). This register can be accessed through SCDP with the pointer value 00H in SCRP (Figure 27). To maintain compatibility with the Z84013015, the Z8401315C inserts the maximum number of wait states (set A bits of this register to one) for fifteen M1 cycles after Power-on Reset. It automatically clears the contents of this register (move to no wait state insertion) on the falling edge of the M1H signal unless software has programmed a value. If automatic wait state insertion is needed, the wait state is programmed within this time period. A read to WCR during this period will return 00H, unless programmed.
Figure 27. Wait State Control Register

This register has the following fields:

- **Interrupt Acknowledge (IACK)**: This 2-bit field specifies the number of wait states to be inserted during an interrupt.
- **RETI (Return From Interrupt)**: This 2-bit field specifies the number of wait states during RETI (return from interrupt).

For fifteen M1 cycles from Power-on Reset, bits 7-6 are set to "11", then cleared to "00" on the trailing edge of the 16th M1 signal, unless programmed.

- **Bit 5. Interval Vector Wait**: While this bit is set to one, the wait state generator inserts one wait state after the IACK signal goes active during the Interrupt acknowledge cycle. This is to give the vector read cycle time. While this bit is cleared to zero, no wait state is inserted (standard timing). For fifteen M1 cycles from Power-on Reset, this bit is cleared to "0" on the trailing edge of the 16th M1 signal, unless programmed.

- **Bit 4. Opcode Fetch Extension**: If this bit is set to "1", one additional wait state is inserted during the opcode fetch cycle. This is in addition to the number of wait states programmed in the Memory Wait field. For fifteen M1 cycles from Power-on Reset, this bit is cleared to "0" on the trailing edge of the 16th M1 signal, unless programmed.

**Figure 28. Memory Wait Boundary Register**

- **Bit D7-D4. Memory Wait High Boundary**: This field specifies the upper address boundary for Memory Wait.
- **Bit D3-D0. Memory Wait Low Boundary**: This field specifies the lower address boundary for Memory Wait.

Memory Wait states are inserted for the address range:

- **(D7-D4 of MWRB) + A15-A12 ≥ (D3-D0 of MWRB)**

This register is set to "000" on Power-on Reset, which specifies the address range for the Memory Wait as "0000h to FFFFh" (all Memory location) and CS1 (unended). The Chip Select signals are active for the address range:

- **CS0: (D3-D0 of CSRB) + A15-A12 ≥ 0000h to FFFFh**
- **CS1: (D7-D4 of CSRB) + A15-A12 ≥ 0000h to FFFFh**

**Figure 29. Chip Select Boundary Register**

- **Bit D7-D4. CS1 Boundary Address**: This field specifies the boundary address range for CS1. The bit values are ignored on Power-on Reset if the Chip Select signal is active. When the memory addresses are within this range, the Memory Wait State generator inserts Memory Wait States specified in the Memory Wait field of WGR (Figure 28).
Table 3. Device status in Halt state

<table>
<thead>
<tr>
<th>Mode</th>
<th>CPG</th>
<th>CPU</th>
<th>CTC</th>
<th>PIO</th>
<th>SIO</th>
<th>WDT</th>
<th>CLKOUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>IDLE1</td>
<td>O</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>O</td>
</tr>
<tr>
<td>IDLE2</td>
<td>O</td>
<td>O</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>O</td>
</tr>
<tr>
<td>STOP</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

Table 2. Power-down Modes

<table>
<thead>
<tr>
<th>Operation Mode</th>
<th>WDTMR Bit D4</th>
<th>Bit D3</th>
<th>Description at HALT State</th>
</tr>
</thead>
<tbody>
<tr>
<td>RUN Mode</td>
<td>1</td>
<td>0</td>
<td>The IRC continues the operation and continuously supplies a clock to the outside.</td>
</tr>
<tr>
<td>IDLE1 Mode</td>
<td>0</td>
<td>0</td>
<td>The internal oscillator's operation is continued. Clock output (CLKOUT) as well as internal clock to the CPU, PIO, SIO, CTC and the Watch Dog Timer is stopped at T4 state in the halt instruction operation code fetch cycle.</td>
</tr>
<tr>
<td>IDLE2 Mode</td>
<td>0</td>
<td>1</td>
<td>The internal oscillator and the CTC operation continues and supplies clock to the outside on the CLKOUT pin continuously. But the internal clock to the CPU, PIO, SIO and the Watch Dog Timer is stopped at O level of T4 state in the halt instruction operation code fetch cycle.</td>
</tr>
<tr>
<td>STOP Mode</td>
<td>1</td>
<td>0</td>
<td>All operations of the internal oscillator, clock (CLK) output, internal clock to the CPU, PIO, CTC, SIO and the Watch Dog Timer are stopped at O level of T4 state in the halt instruction operation code fetch cycle.</td>
</tr>
</tbody>
</table>

TIMING

Basic Timing

The basic timing is explained here with emphasis placed on the clock function relative to the clock generator. The following timing is identical for both the 284200 and 284200C.

- Operation code fetch cycle
- Memory Read/Write operation
- Input/Output operation
- Bus request acknowledge operation
- Maskable interrupt request operation
- Non-Maskable interrupt request operation
- Reset Operation

Figure 31. Timing of RUN Mode

(At HALT Instruction Command Execution)
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**NOTE:** The above information is extracted from the document and represents the physical and technical features of the device.
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