GPC® 150
General Purpose Controller Z84C15

TECHNICAL MANUAL
GPC® 150
General Purpose Controller Z84C15

TECHNICAL MANUAL

Single Euro size 100x160mm with interface to Abaco® industrial BUS; 84C15 CPU with 32 MHz crystal; up to 512K EPROM or FLASH EPROM and up to 512K RAM; through FG DOS the memory that exceeds 64K is managed as RAM/ROM disk. It is possible deleting and re-programming the on board FLASH, automatically, with the user program; serial EEPROM up to 8K; serial FLASH EPROM available in different sizes, up to 4M; 8 way Dip Switch and configuration jumper readable by software; activity LED, placed on the front side, driven through software; 2 RS 232 serial lines, one configurable in RS 422, RS 485 or Current Loop managed by the powerful SIO supporting HDLC, SDLC etc. protocols and software selectable baud rate, up to 115 Kbaud; 40 I/O TTL lines, set via software: 24 managed by PPI 82C55 and 16 managed by PIO; four 8 bits timer counters: 2 used as baud rate generator and 2 on I/O connector; 8 A/D converter lines with Sample & Hold, 5.5 µs, range 0÷2.5 or 0÷5V and possibility to work on differential inputs (±2.5 or ±5V), 12 bits+sign, managed by LM 12H458. It develops more than 140.000 conversions per second, it is provided with an internal sequencer, Self Calibration function, Conversion Rates programmation and it is able to check an analog input generating an INT when defined limits are excelled; power failure circuit capable to generate interrupt; Real Time Clock able to up date day, month, year, week day, seconds, minutes and hours. It can be programmed to issue an INT at intervals defined by software; Watch Dog resettable by software and display through LED; back up circuit for RAM and RTC provided of lithium battery and connector for external battery. The battery charge status can be acquired by software; single power supply +5Vdc, 260 mA; wide range of base software and development tools that allow card use with only a standard PC, connected through serial line. Among these: FGDOS 150; PASCAL 80; CBZ 80; NSB8; RSD 150; HI TECH C 80; GET 80; DDS MICROC 85; EMBEDDED PASCAL; NO ICE Z80; etc.
IMPORTANT

Although all the information contained herein have been carefully verified, grifo® assumes no responsibility for errors that might appear in this document, or for damage to things or persons resulting from technical errors, omission and improper use of this manual and of the related software and hardware. grifo® reserves the right to change the contents and form of this document, as well as the features and specification of its products at any time, without prior notice, to obtain always the best product.

For specific informations on the components mounted on the card, please refer to the Data Book of the builder or second sources.

SYMBOLS DESCRIPTION

In the manual could appear the following symbols:

- !: Attention: Generic danger
- ¥: Attention: High voltage

Trade Marks

GPC®, grifo®: are trade marks of grifo®.

Other Product and Company names listed, are trade marks of their respective companies.
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INTRODUCTION

The use of these devices has turned - IN EXCLUSIVE WAY - to specialized personnel.

The purpose of this handbook is to give the necessary information to the cognizant and sure use of the products. They are the result of a continual and systematic elaboration of data and technical tests saved and validated from the manufacturer, related to the inside modes of certainty and quality of the information.

The reported data are destined- IN EXCLUSIVE WAY- to specialized users, that can interact with the devices in safety conditions for the persons, for the machine and for the environment, impersonating an elementary diagnostic of breakdowns and of malfunction conditions by performing simple functional verify operations , in the height respect of the actual safety and health norms.

The informations for the installation, the assemblage, the dismantlement, the handling, the adjustment, the reparation and the contingent accessories, devices etc. installation are destined - and then executable - always and in exclusive way from specialized warned and educated personnel, or directly from the TECHNICAL AUTHORIZED ASSISTANCE, in the height respect of the manufacturer recommendations and the actual safety and health norms.

The devices can't be used outside a box. The user must always insert the cards in a container that respect the actual safety normative. The protection of this container is not threshold to the only atmospheric agents, but specially to mechanic, electric, magnetic, etc. ones.

To be on good terms with the products, is necessary guarantee legibility and conservation of the manual, also for future references. In case of deterioration or more easily for technical updates, consult the AUTHORIZED TECHNICAL ASSISTANCE directly.

To prevent problems during card utilization, it is a good practice to read carefully all the informations of this manual. After this reading, the user can use the general index and the alphabetical index, respectly at the begining and at the end of the manual, to find information in a faster and more easy way.

CARD VERSION

The present handbook is reported to the GPC® 150 card release 220599 and later. The validity of the bring informations is subordinate to the number of the card release. The user must always verify the correct correspondence among the two denotations. On the card the release number is present in more points both board printed diagram (serigraph) and printed circuit (for example near battery BT1 and connector CN1 both on the component sideand on the solder side).
The **GPC® 150** card is a powerful control and managing card in the 100x160mm standard single Europa size. It relies on the powerful **Industrial ABACO® BUS** and exploits the numerous intelligent and non intelligent peripherals, available on this BUS.

The **GPC® 150** is based on the powerful and diffuse **CPU 84C15 Zilog**, therefore being code compatible with the famous **Z80**, and it has considerable hardware resources available on board. The 8 lines of 13 bits high performances A/D converter are particularly interesting. Its modularity and the remarkable hardware resources allow this card to be easily used even in complex applications. Moreover this card is the right component for all the applications that require a lot of memory, in fact up to **5 M Bytes** can be mounted on board. Programming and exploiting the resources of this module is extremely easy thanks to **FGDOS** romated operative system. This latter supports high level languages such as BASIC, PASCAL, C compilers and so on; it drives the memory resources as **ROM/RAM disk** allowing an immediate use of this devices at high level. In addition to that the **GPC® 150** allows a direct management of **LCD** or **Fluorescent Displays**, matrix keyboard, parallel printer and **PCMCIA** RAM cards. The **FGDOS** affords truly notable develop and debug facilities, and allows to program directly on board a **FLASH** with the user program. The **GPC® 150** is equipped with a series of standard **Abaco®** connectors allowing immediate use of the many **BLOCK I/O** interface, or enabling a simple and inexpensive connections to equipment made by the user, or by third parties.

- Single **Euro** size 100x160mm with interface to **Industrial ABACO® BUS**.
- **84C15 CPU** with 32 MHz crystal.
- Up to **512K EPROM** or **FLASH EPROM** and up to **512K SRAM**. Through **FGDOS** the memory that exceed 64K is managed as **RAM/ROM disk**. It is possible deleting and re-programming the on borad **FLASH**, automatically, with the user program.
- **Serial EEPROM** up to 8K.
- **Serial FLASH EPROM** available in different sizes, up to 4M.
- 8 way **Dip Switch** and configuration jumper readable by software.
- **Activity LED**, placed on the front side, driven through software.
- 2 **RS 232** serial lines, one configurable in **RS 422**, **RS 485** or **Current Loop** managed by the powerful **SIO** supporting **HDLC**, **SDLC** etc. protocols and software selectable baud rate, up to 115 **KBAud**
- **40 I/O TTL** lines, set via software: 24 managed by **PPI 82C55** and 16 managed by **PIO**.
- **Four** 8 bits **timer counters**: 2 used ad baud rate generator and 2 on I/O connector.
- **8 A/D Converter** lines with **Sample & Hold**, 5,5 µs, range 0±2,5 or 0±5V and possibility to work on differential inputs (±2,5 or ±5V), 12 bits+sign, managed by **LM 12H458**. It develops more than **140.000** coverions per second, it is provided with an internal sequencer, **Self Calibration** function, **Conversion Rates** programmation and it is able to check an analog input generating an **INT** when defined limits are excelled.
- **Power Failure** circuit capable to generate interrupt.
- **Real Time Clock** able to up date day, month, year, week day, seconds, minutes and hours. It can be programmed to issue an **INT** at intervals defined by software.
- **Watch Dog** resettable by software and display through **LED**.
- **Back up** circuit for SRAM and RTC provided of **lithium battery** and connector for external battery. The battery charge status can be acquired by software.
- Single power supply **+5Vdc**, **260 mA**.
- Wide range of base software and development tools that allow card use with only a standard PC, connected through serial line. Among these: FGDOS 150; PASCAL 80; CBZ 80; NSB8; RSD 150; HI TECH C 80; GET 80; DDS MICROC 85; EMBEDDED PASCAL; NO ICE Z80; etc.

**SIO**

Microprocessor peripheral device that manages two lines for serial communication. It can be used to connect to external systems capable to support RS 232, RS 422, RS 485 and Current loop electric protocols. Simply by programming four registers allocated in the microprocessor I/O addressing space, the User can set the baud rate, stop bits number, length of character, parity and handshake of each serial line.

**TIMER COUNTER**

It is a microprocessor peripheral device that manages four 8 bit timers counters. Each channel can be set with a different prescaler and with a different operating mode (timer with external trigger, counter of rising edge or falling edge, etc.), including eventual interrupt generation. CTC is connected to the external electronics by two digital signals and it is completely driven by software programming four registers allocated in microprocessor I/O addressing space, by a specific control logic. Two channels out of four are used by the baud rate generator for the serial lines.

**PIO TTL I/O LINES**

It is a microprocessor peripheral device that manages 16 TTL I/O lines divided in two 8 bit parallel ports. The lines direction is software settable at bit level and interrupts can be generated. In this way an external status can obtain CPU control in any condition, with a fast response time. The PIO is completely driven by software programming four registers allocated in microprocessor I/O addressing space, by a specific control logic.

**REAL TIME CLOCK**

**GPC® 150** has installed on-board a Real Time Clock capable of a completely autonomous management of hours, minutes, seconds, day of month, month, year and day of week. The device is completely software programmable by 16 registers mapped in the CPU I/O space and is supplied by a back-up circuitry which warrants the validity of its data in any operating condition. In addition RTC section is capable to generate periodic interrupts, for example to wake the CPU away from halt, idle or stop conditions.

**MEMORY MANAGEMENT UNIT**

A specific MMU section has been designed to manage in a practical and efficient way the memory configurations that the **GPC® 150** board can assume. The use is provided with a 64K work area, which can be easily allocated anywhere in the 5128K maximum memory space.
CPU

The **GPC® 150** uses the powerful microprocessors 84C15 produced by ZILOG. This 8 bit microprocessor is code compatible with standard Z80 CPU and it has an extended instruction set, fast execution time, fast data handling and an efficient vectorized interrupt management.

Some of the most important 84C15 features are its internal peripheral devices, as below described:

- 16 I/O lines programmable at bit level, capable to generate interrupts (PIO);
- four 8 bit timers counters, with programmable prescaler (CTC);
- 2 synchronous or asynchronous serial lines, provided of hardware handshake signals (SIO);
- watch dog timer;
- wait state generator;
- programmable clock frequency;
- interrupt controller;
- idle mode or power down mode.

For further information, please refer to specific documentation of the manufacturing company, or to appendix B of this manual.

SERIAL COMMUNICATION

The serial communication lines are completely software configurable for protocol and speed (from 600 to 115200 Baud); simply by programming the microprocessor SIO and the on board baud rate generator, the User can set the baud rate, stop bits number, length of character, parity and handshake of each serial line. For further information about these programmable sections, please refer to chapter "BAUD RATE GENERATOR" and to appendix B of this manual.

One of the two serial lines is always buffered with RS 232 electric protocol, while the second one is hardware configurable in fact connecting some jumpers, the User can select the electric standard interface between RS 232, RS 422, RS 485 and Current loop; for RS 422-485 the transmitter activation and the line direction can be set by software. The chapter "SERIAL COMMUNICATION SELECTION" contains a detailed description of available hardware configurations.

Normally the card is provided with two RS 232 interfaces and a different configuration must be specified when ordering.

ABACO® BUS

One of the most important features of **GPC® 150** is its possibility to be interfaced to industrial **ABACO® BUS**. Thanks to its standard **ABACO® BUS** connector, the card can be connected to some of the numerous **grifo®** boards, both intelligent and not. For example the User can directly use cards for analog signals acquisition (A/D), cards for analog signals generation (D/A), cards for digital I/O signals management, cards with timers and counters, cards for temperature controls, etc. Through mother boards like **ABB 03** and **ABB 05** it is also possible to manage serie 3 and 4 boards, which are provided with **ABACO® I/O BUS**. So, **GPC® 150** becomes the right component for each industrial automation systems, in fact **ABACO® BUS** makes the card easily expandable with the best price/performance ratio.
FIGURE 1: BLOCK DIAGRAM
CLOCK DEVICES

On GPC® 150 there are three separate circuits with crystal to generate the clock signal for the microprocessor (32 MHz), A/D Converter section (8 MHz) and the timing signal for baud rate generator section (4.9152M Hz). The choice of using three circuits and as many separated crystals, has the advantage to change the microprocessor working speed (when best performances are required) without additional changes in communication software or firmware. The best time performances are always obtained both for execution time and serial communication, fulfilling the User necessity.

CONTROL LOGIC

The addresses of all peripheral device's registers and of memory devices on GPC® 150 are assigned through a specific control logic that allocates all these devices in the microprocessor addressing space.

For further information please refer to chapter "ADDRESSES AND MAPS" of this manual.

MEMORY DEVICES

On the card can be mounted up to 5128K of memory divided with a maximum of 512K Byte EPROM or FLASH EPROM, 512K Byte SRAM, two 2048K Byte serial FLASH EPROM modules and 8K Byte serial EEPROM. The memory configuration must be chosen considering the application to realize or the specific requirements of the user. Normally the card is provided with 128K RAM and 512 bytes of serial EEPROM, all different configurations must be specified from the user, at the moment of the order. By means of the on-board back-up circuit and the external battery, memory can keep datas also in absence of power supply. The addressing of memory devices is controlled by a specific on-board control logic, that provides to allocate the devices in the microprocessor address space. For further informations about memory configuration, sockets description and jumpers connection, please refer to chapter "HARDWARE", "PERIPHERIAL DEVICES SOFTWARE DESCRIPTION" and to the paragraph "MEMORY SELECTION".

WATCH DOG SECTIONS

GPC® 150 is provided with two separated Watch Dog circuits that can reset the card at programmable time intervals, if not retriggered. Watch dog circuits are used when the User want to exit from endless loops or to reset anomalous conditions not estimated by application program. There is a monostable section, inside the microprocessor, with programmable intervention time and a monostable/astable section, outside the microprocessor, with 1420 ms fixed intervention time. By software the User can perform a complete management of the devices, using specific registers allocated in microprocessor I/O addressing space.
A/D CONVERTER

The optional A/D Converter section on the GPC® 150 board is based on the powerful LM12H458 peripheral can acquire 8 channels with a maximum resolution of 12 bits plus sign bit in the range 0÷2.490V (optional 0÷5.000V to specify in the order) or current signals in the range 0÷20 mA or 4÷20 mA in "single ended" mode or 4 channels connected to differential signals in the range ±2.290 V (optional ±5.00 V) in "fully differential mode". This section is provided with Sample & Hold circuit, a fully-differential self-calibrating Analog-to-Digital converter capable of performing 5.5 μs conversion time and over 140,000 conversions per second. Some other features like: internal sequencer, DMA data transfer, two different self-calibration modes, programmable conversion rates, resolution settings, FIFO to store conversion data and autonomous limits control (this means monitoring an analog input and generating and interrupt when it is above or below either of the two limits), easy remarkably its management without requiring CPU intervents.

By software, all the section functions are programmable through 27 registers allocated in the I/O addressing space.

The code to require A/D converter optional section in the order is .AD.

MEMORY MANAGEMENT UNIT

A specific MMU section has been designed to manage in a practical and efficient way the memory configurations that the GPC® 150 board can assume. The use is provided with a 64K work area, which can be easily allocated anywhere in the 5128K maximum memory space.

PPI 82C55 TTL I/O LINES

It manages 24 TTL I/O lines divided in three 8 bit parallel ports. The lines direction is software settable at byte level. These I/O lines allow the possibility to connect several devices (for example: User interfaces) even when the handshake is completely software driven. The PPI 82C55 is completely driven by software programming four registers allocated in microprocessor I/O addressing space, by a specific control logic.

For further informations about the above described devices, please refer to the manufacturer documentations or to appendix B of this manual.
TECHNICAL FEATURES

GENERAL FEATURES

On board resources: 24 TTL programmable Input/Output TTL (PPI 82C55)
16 Input/Output (PIO)
4 eight bits TTL Timer Counter (CTC)
1 RS 232 bidirectional line
1 RS 232, RS 422, RS 485 or Current Loop bidirectional line
1 CPU internal Watch Dog
1 external Watch Dog
1 Real Time Clock (RTC)
1 eight dips Dip Switch
Industrial ABACO® BUS

Addressable memory:
IC 10: EPROM from 128K x 8 to 512K x 8
FLASH EPROM from 128K x 8 to 512K x 8
IC 8: SRAM 128K x 8 or 512Kx8
IC 34: serial EEPROM from 256 byte to 8192 byte
IC13: serial FLASH EPROM from 64Kx8 to 2048Kx8
IC14: serial FLASH EPROM from 64Kx8 to 2048Kx8

CPU:
ZILOG 84C15

CPU frequence: 32 MHz

A/D frequence: 8 MHz

Baud Rate generator frequence: 1,8432 MHz

A/D Converter resolution: 12 bit + sign

A/D conversion time: 5,5 µsec

Watch Dog intervent time:
from 940 msec to 2060 msec (typical 1420 msec)

PHYSICAL FEATURES

Size: (W x H x D):
EUROPE format : 100 x 160 x 15 mm

Weight:
185 g (basic configuration)

Connectors:
K1: 64 pins DIN 41612 M 90 degreeses A+C type C
CN1: 2 pins low profile vertical M
CN2: 5 pins low profile vertical M
CN3: 20 pins low profile vertical M
CN4: 20 pins low profile vertical M
CN5: 20 pins low profile 90 degrees M
CN6: 20 pins low profile 90 degrees M
CN7: 16 pins low profile 90 degrees M

Temperature range: from 0 to 70 Centigrad degrees
Relative humidity: 20% up to 90% (without condense)

**ELECTRIC FEATURES**

Power supply: +5 Vcc
Consumption on 5 Vdc: 252 mA in basic configuration
360 mA in full configuration (all options mounted)
On board back up battery: 3,0 Vdc; 1/2 AA
External back up battery: 3,6÷5 Vdc
Back up current: 3,4 μA (on board battery)
5,1 μA (3,6 V external battery)
Analog inputs: 0÷2,490 V; ±2,490 V; 0÷5,000 V; ±5,000 V
0÷20 mA; 4÷20 mA (through conversion module)
Analog inputs impedance: < 4KΩ
RS422, 485 termination network: line termination= 120Ω
Pull-up on positive= 3,3KΩ
Pull-down on negative= 3,3KΩ
Power Failure threshold: 52 mV prima before the reset occurs
INSTALLATION

In this chapter there are the information for a right installation and correct use of the card. The user can find the location and functions of each connectors, jumpers and some explanatory diagrams.

CONNECTIONS

The GPC®150 board has 8 connectors that can be linkeded to other devices or directly to the field, according to system requirements. In this paragraph there are connectors pin out, a short signals description (including the signals direction), connectors location (see figure 24) and some electrical diagrams that show the on board circuit of each connector.

**CN1 - EXTERNAL BACK UP BATTERY CONNECTOR**

CN1 is a 2 pins, vertical, male connector with 2,54mm pitch. Through CN1 the user can connect an external battery for SRAM and RTC back up when the power supply is switched off (for further information please refer to chapter "BACK UP").

![Figure 2: CN1 - External back up battery connector](image)

Signals description:

<table>
<thead>
<tr>
<th>Signal</th>
<th>Pin</th>
</tr>
</thead>
<tbody>
<tr>
<td>+Vbat</td>
<td>1</td>
</tr>
<tr>
<td>GND</td>
<td>2</td>
</tr>
</tbody>
</table>

- External back up battery positive pin
- External back up battery negative pin
CN4 - CONNECTOR FOR PPI 82C55 PORT B

CN4 is a 20 pins, male, vertical, low profile connector with 2.54 mm pitch. On CN4 connector are available PPI 82C55 port B signals that equal to 8 I/O digital lines. Any parameter of this device (like signals direction, data management mode, etc.) is completely software definible by programming the device itself. All signals are at TTL level and follow the standard pinout I/O ABACO® pin-out.

<table>
<thead>
<tr>
<th>PPI PB.1</th>
<th>1</th>
<th>2</th>
</tr>
</thead>
<tbody>
<tr>
<td>PPI PB.3</td>
<td>3</td>
<td>4</td>
</tr>
<tr>
<td>PPI PB.5</td>
<td>5</td>
<td>6</td>
</tr>
<tr>
<td>PPI PB.7</td>
<td>7</td>
<td>8</td>
</tr>
<tr>
<td>N.C.</td>
<td>9</td>
<td>10</td>
</tr>
<tr>
<td>N.C.</td>
<td>11</td>
<td>12</td>
</tr>
<tr>
<td>N.C.</td>
<td>13</td>
<td>14</td>
</tr>
<tr>
<td>N.C.</td>
<td>15</td>
<td>16</td>
</tr>
<tr>
<td>GND</td>
<td>17</td>
<td>18</td>
</tr>
<tr>
<td>N.C.</td>
<td>19</td>
<td>20</td>
</tr>
</tbody>
</table>

**Figure 3: CN4 - Connector for PPI 82C55 Port B**

Signals description:

- **PPI PB.n** = I/O - PPI 82C55 port B digital line n
- **Vdc** = O - Line connected to +5 Vdc power supply
- **GND** = - Ground signal
- **N.C.** = - Not connected
CN3 - CONNECTOR FOR PPI 82C55 PORT A AND C

CN3 is a 20 pins, male, vertical, low profile connector with 2.54 mm pitch. On CN3 connector are available PPI 82C55 port A and C signals that equal to 16I/O digital lines. Any parameter of this device (like signals direction, data management mode, etc.) is completely software definible by programming the device itself. All signals are at TTL level and follow the standard pinout I/O ABACO® pin-out.

Signals description:

PPI PA.n = I/O - PPI 82C55 port B digital line n
PPI PC.n = I/O - PPI 82C55 port B digital line n
Vdc = O - Line connected to +5 Vdc power supply
GND = - Ground signal
N.C. = - Not connected
**Figure 5: PPI I/O Lines Connection Diagram**

- **PORT A**: 8 Lines to PIN 1-8
- **PORT C**: 8 Lines to PIN 9-16
- **PPI 82C55**
- **CN3**: +5 Vdc
- **PORT B**: 8 Lines to PIN 1-8
- **CN4**: +5 Vdc
CN5 - A/D CONVERTER INPUTS CONNECTOR

CN5 is a 20 pins, male, 90°, low profile connector with 2.54 mm pitch. Through CN5 an external device can connect up to 8 analog inputs. These are low impedance lines directly connected to the on board A/D Converter and are provided with a capacitive filter. The inputs may vary in the range 0\(\pm\)2.490 V or 0\(\pm\)5.000 V single ended or in the range \(\pm\)2.490 V or \(\pm\)5.000 V fully differential. By installing an opportune conversion module it is possible to acquire 8 single ended channels as currents inputs in the ranges 0\(\div\)20 mA or 4\(\div\)20 mA. Conversion management is completely software driven through programming LM 12H458; signals location on this connector has been designed to reduce problems due to interference.

**Figure 6: CN5 - A/D CONVERTER INPUTS CONNECTOR**

Signals description:

- **CHn** = I - Analog input signal connected to A/D Converter n-th channel
- **AGND** = - Analog ground signal
- **+5 Vdc** = O - Power supply signal +5 Vcc
- **GND** = - Digital ground signal
- **N.C.** = - Not Connected
FIGURE 7: A/D CONVERTER INPUT DIAGRAM
CN7 - RS 232 SERIAL LINES AND TIMER COUNTER CONNECTOR

CN7 is a 16 pins, male, 90°, low profile connector with 2.54 mm pitch. Through CN7 it is possible to connect the RS 232 serial lines and the timer counters T0 and T1 to the external world. SIO and CTC are CPU internal devices. To manage the serial lines the User needs to connect specific jumpers in the proper positions and program specific CPU internal registers. The signals on this connector are at TTL level and RS 232 signals follow the CCITT specifications; signals location on this connector has been designed to reduce problems due to interference.

Signals description:

- **RXA, B RS232** = I - RS 232 serial line A, B Receive Data signal
- **TXA, B RS232** = O - RS 232 serial line A, B Transmit Data signal
- **CTS A, B RS232** = I - RS 232 serial line A, B Clear To Send signal
- **RTS A, B RS232** = O - RS 232 serial line A, B Request To Send signal
- **CLK Tn** = I - TTL level CTC n-th counter Clock Trigger
- **ZC Tn** = O - TTL level CTC n-th counter Clock Trigger Zero Count
- **GND** = - Ground signal
- **N.C.** = - Not Connected

![Figure 8: CN7 - RS 232 serial lines and Timer Counter connector](image-url)
FIGURE 9: TIMER COUNTER CONNECTION DIAGRAM

FIGURE 10: SERIAL COMMUNICATION CONNECTION DIAGRAM
CN6 - PIO I/O CONNECTOR

CN6 is a 20 pins, male, 90°, low profile connector with 2.54 mm pitch. On CN6 are available the two 8 bits parallel ports of CPU internal PIO that can be connected to the external world. Handshake lines are available on four pods on the board, to locate them please refer to figure 24. All these signals follow TTL standard.

![Figure 11: CN6 - PIO I/O Connector](image)

- **PIO PA.n** = I/O - CPU internal PIO port A n-th digital signal
- **PIO PB.n** = I/O - CPU internal PIO port A n-th digital signal
- **Vcc** = O - Power supply signal +5 Vcc
- **GND** = - Ground signal
- **N.C.** = - Not Connected
FIGURE 12: PIO CONNECTION DIAGRAM

On board pods PZ1, PZ2, PZ3 and PZ4 allow the User to connect to the RDY and /STB signals both for PIO Port A and PIO Port B.

Through these signals it is possible to implement high speed parallel communications.

To locate the pods on the board please refer to figure 24.
CN2 - CONNECTOR FOR RS 422, RS 485 AND CURRENT LOOP

CN2 is a 5 pins, vertical, male connector with 2,54mm pitch. This connector carries all the signals of RS 422, RS 485 and Current Loop serial line B. Signals location on this connector has been designed to reduce problems due to interference; all the signals follow the CCITT normatives for each of the communication standards used. Please remark that the Current Loop serial line is passive.

**Figure 13: CN2 - RS 422, RS 485 and Current Loop serial line B connector**

Signals description:

- **RXB- RS422** = I - RS 422 serial line B Receive Data Negative signal
- **RXB+RS422** = I - RS 422 serial line B Receive Data Positive signal
- **TXB- RS422** = O - RS 422 serial line B Transmit Data Negative signal
- **TXB+ RS422** = O - RS 422 serial line B Transmit Data Positive signal
- **RXTXB- RS485** = I/O - RS 485 serial line B Receive Data Negative signal
- **RXTXB+ RS485** = I/O - RS 485 serial line B Transmit Data Positive signal
- **RXB- C.L.** = I - Current Loop serial line B Receive Data Negative signal
- **RXB+ C.L.** = I - Current Loop serial line B Receive Data Positive signal
- **TXB- C.L.** = O - Current Loop serial line B Transmit Data Negative signal
- **TXB+ C.L.** = O - Current Loop serial line B Transmit Data Positive signal
- **+5 Vdc** = I - Power supply signal+5 Vcc
- **GND** = Ground signal
FIGURE 14: RS 232 POINT-TO-POINT CONNECTION EXAMPLE

FIGURE 15: RS 422 POINT-TO-POINT CONNECTION EXAMPLE

FIGURE 16: RS 485 POINT-TO-POINT CONNECTION EXAMPLE
Please remark that in a RS 485 network two forcing resistors must be connected across the net and two termination resistors (120 Ω) must be placed at its extremities, respectively near the Master unit and the Slave unit at the greatest distance from the Master.

Forcing and terminating circuitry is installed on GPC® 150 board. It can be enabled or disabled through specific jumpers, as explained later.

For further informations please refer to TEXAS INSTRUMENTS Data-Book, "RS 422 and RS 485 Interface Circuits", the introduction about RS 422-485.
**Figure 19:** 4 wires Current Loop point-to-point connection example

**Figure 20:** 2 wires Current Loop point-to-point connection example
Possible Current Loop connections are two: 2 wires and 4 wires. These connections are shown in figures 19 and 20 where it is possible to see the voltage for VCL and the resistances for current limitation (R). The supply voltage varies in compliance with the number of connected devices and voltage drop on the connection cable.

The choice of the values for these components must be done considering that:
- circulation of a 20 mA current must be guaranteed;
- potential drop on each transmitter is about 2.35 V with a 20 mA current;
- potential drop on each receiver is about 2.52 V with a 20 mA current;
- in case of shortcircuit each transmitter must dissipate at most 125 mW;
- in case of shortcircuit each receiver must dissipate at most 90 mW.

For further info please refer to HEWLETT-PACKARD Data Book, (HCPL 4100 and 4200 devices).
K1 - CONNECTOR FOR ABACO® BUS

K1 is a 64 pins, male, 90°, DIN 41612 connector with 2.54 pitch. On K1 are available all the industrial ABACO® BUS signals and it can be used for connections to many other peripheral cards. In the table below there are the standard pin outs both for 8 bits and 16 bits CPU and the signal connected on GPC® 150. All signals follow TTL standard.

<table>
<thead>
<tr>
<th>PIN</th>
<th>A 16 bit BUS</th>
<th>A 8 bit BUS</th>
<th>A GPC 150</th>
<th>C GPC 150</th>
<th>C 8 bit BUS</th>
<th>C 16 bit BUS</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
</tr>
<tr>
<td>2</td>
<td>+5 Vdc</td>
<td>+5 Vdc</td>
<td>+5 Vdc</td>
<td>+5 Vdc</td>
<td>+5 Vdc</td>
<td>+5 Vdc</td>
</tr>
<tr>
<td>3</td>
<td>D0</td>
<td>D0</td>
<td>D0</td>
<td>N.C.</td>
<td>N.C.</td>
<td>D8</td>
</tr>
<tr>
<td>4</td>
<td>D1</td>
<td>D1</td>
<td>D1</td>
<td>N.C.</td>
<td>N.C.</td>
<td>D9</td>
</tr>
<tr>
<td>5</td>
<td>D2</td>
<td>D2</td>
<td>D2</td>
<td>N.C.</td>
<td>N.C.</td>
<td>D10</td>
</tr>
<tr>
<td>6</td>
<td>D3</td>
<td>D3</td>
<td>D3</td>
<td>/INT</td>
<td>/INT</td>
<td>/INT</td>
</tr>
<tr>
<td>7</td>
<td>D4</td>
<td>D4</td>
<td>D4</td>
<td>/NMI</td>
<td>/NMI</td>
<td>/NMI</td>
</tr>
<tr>
<td>8</td>
<td>D5</td>
<td>D5</td>
<td>D5</td>
<td>N.C.</td>
<td>/HALT</td>
<td>D11</td>
</tr>
<tr>
<td>9</td>
<td>D6</td>
<td>D6</td>
<td>D6</td>
<td>N.C.</td>
<td>/MREQ</td>
<td>/MREQ</td>
</tr>
<tr>
<td>10</td>
<td>D7</td>
<td>D7</td>
<td>D7</td>
<td>/IORQ</td>
<td>/IORQ</td>
<td>/IORQ</td>
</tr>
<tr>
<td>11</td>
<td>A0</td>
<td>A0</td>
<td>A0</td>
<td>/RD</td>
<td>/RD</td>
<td>/RDLDS</td>
</tr>
<tr>
<td>12</td>
<td>A1</td>
<td>A1</td>
<td>A1</td>
<td>/WR</td>
<td>/WR</td>
<td>/WRLDS</td>
</tr>
<tr>
<td>13</td>
<td>A2</td>
<td>A2</td>
<td>A2</td>
<td>N.C.</td>
<td>/BUSAK</td>
<td>D12</td>
</tr>
<tr>
<td>14</td>
<td>A3</td>
<td>A3</td>
<td>A3</td>
<td>N.C.</td>
<td>/WAIT</td>
<td>/WAIT</td>
</tr>
<tr>
<td>15</td>
<td>A4</td>
<td>A4</td>
<td>A4</td>
<td>N.C.</td>
<td>/BUSRQ</td>
<td>D13</td>
</tr>
<tr>
<td>16</td>
<td>A5</td>
<td>A5</td>
<td>A5</td>
<td>/RESET</td>
<td>/RESET</td>
<td>/RESET</td>
</tr>
<tr>
<td>17</td>
<td>A6</td>
<td>A6</td>
<td>A6</td>
<td>N.C.</td>
<td>/M1</td>
<td>/IACK</td>
</tr>
<tr>
<td>18</td>
<td>A7</td>
<td>A7</td>
<td>A7</td>
<td>N.C.</td>
<td>/RFSH</td>
<td>D14</td>
</tr>
<tr>
<td>19</td>
<td>A8</td>
<td>A8</td>
<td>N.C.</td>
<td>N.C.</td>
<td>/MEMDIS</td>
<td>/MEMDIS</td>
</tr>
<tr>
<td>20</td>
<td>A9</td>
<td>A9</td>
<td>N.C.</td>
<td>N.C.</td>
<td>VDUSEL</td>
<td>A22</td>
</tr>
<tr>
<td>21</td>
<td>A10</td>
<td>A10</td>
<td>N.C.</td>
<td>N.C.</td>
<td>/IEI</td>
<td>D15</td>
</tr>
<tr>
<td>22</td>
<td>A11</td>
<td>A11</td>
<td>N.C.</td>
<td>N.C.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>23</td>
<td>A12</td>
<td>A12</td>
<td>N.C.</td>
<td>N.C.</td>
<td>CLK</td>
<td>CLK</td>
</tr>
<tr>
<td>24</td>
<td>A13</td>
<td>A13</td>
<td>N.C.</td>
<td>N.C.</td>
<td>/RDUDS</td>
<td></td>
</tr>
<tr>
<td>25</td>
<td>A14</td>
<td>A14</td>
<td>N.C.</td>
<td>N.C.</td>
<td>/WRUDS</td>
<td></td>
</tr>
<tr>
<td>26</td>
<td>A15</td>
<td>A15</td>
<td>N.C.</td>
<td>N.C.</td>
<td>A21</td>
<td></td>
</tr>
<tr>
<td>27</td>
<td>A16</td>
<td>A16</td>
<td>N.C.</td>
<td>N.C.</td>
<td>A20</td>
<td></td>
</tr>
<tr>
<td>28</td>
<td>A17</td>
<td>A17</td>
<td>N.C.</td>
<td>N.C.</td>
<td>A19</td>
<td></td>
</tr>
<tr>
<td>29</td>
<td>A18</td>
<td>A18</td>
<td>N.C.</td>
<td>N.C.</td>
<td>/R.T.</td>
<td>/R.T.</td>
</tr>
<tr>
<td>30</td>
<td>+12 Vdc</td>
<td>+12 Vdc</td>
<td>N.C.</td>
<td>N.C.</td>
<td>-12 Vdc</td>
<td>-12 Vdc</td>
</tr>
<tr>
<td>31</td>
<td>+5 Vdc</td>
<td>+5 Vdc</td>
<td>+5 Vdc</td>
<td>+5 Vdc</td>
<td>+5 Vdc</td>
<td>+5 Vdc</td>
</tr>
<tr>
<td>32</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
</tr>
</tbody>
</table>

Figure 22: K1 - ABACO® BUS connector
Signals description:

8 bits CPU

\[
\begin{array}{lcl}
\text{A0-A15} & = & \text{O} \quad \text{- Address BUS} \\
\text{D0-D7} & = & \text{I/O} \quad \text{- Data BUS} \\
\text{INT} & = & \text{I} \quad \text{- Interrupt request} \\
\text{NMI} & = & \text{I} \quad \text{- Non Maskable Interrupt} \\
\text{HALT} & = & \text{O} \quad \text{- Halt state} \\
\text{MREQ} & = & \text{O} \quad \text{- Memory Request} \\
\text{IORQ} & = & \text{O} \quad \text{- Input Output Request} \\
\text{RD} & = & \text{O} \quad \text{- Read cycle status} \\
\text{WR} & = & \text{O} \quad \text{- Write cycle status} \\
\text{BUSAK} & = & \text{O} \quad \text{- BUS Acknowledge} \\
\text{WAIT} & = & \text{I} \quad \text{- Wait} \\
\text{BUSRQ} & = & \text{I} \quad \text{- BUS Request} \\
\text{RESET} & = & \text{O} \quad \text{- Reset} \\
\text{M1} & = & \text{O} \quad \text{- Machine cycle one} \\
\text{RFSH} & = & \text{O} \quad \text{- Refresh for dynamic RAM} \\
\text{MEMDIS} & = & \text{I} \quad \text{- Memory Display} \\
\text{VDUSEL} & = & \text{O} \quad \text{- VDU Selection} \\
\text{IEI} & = & \text{I} \quad \text{- Interrupt Enable Input} \\
\text{CLK} & = & \text{O} \quad \text{- System clock} \\
\text{R.B.} & = & \text{I} \quad \text{- Reset button} \\
\text{+5 Vdc} & = & \text{I} \quad \text{- Power supply at +5 Vdc} \\
\text{+12 Vdc} & = & \text{I} \quad \text{- Power supply at +12 Vdc} \\
\text{-12 Vdc} & = & \text{I} \quad \text{- Power supply at -12 Vdc} \\
\text{GND} & = & \text{- Ground signal} \\
\end{array}
\]

16 bits CPU

\[
\begin{array}{lcl}
\text{A16-A22} & = & \text{O} \quad \text{- Address BUS} \\
\text{D8-D15} & = & \text{I/O} \quad \text{- Data BUS} \\
\text{RD UDS} & = & \text{O} \quad \text{- Read Upper Data Strobe} \\
\text{WR UDS} & = & \text{O} \quad \text{- Write Upper Data Strobe} \\
\text{IACK} & = & \text{O} \quad \text{- Interrupt Acknowledge} \\
\text{RD LDS} & = & \text{O} \quad \text{- Read Lower Data Strobe} \\
\text{WR LDS} & = & \text{O} \quad \text{- Write Lower Data Strobe} \\
\end{array}
\]

N.B.
Directionality indications as above stated are referred to a master (CPU o GPC®) board and have been kept untouched to avoid ambiguity in case of multi-boards systems.
TRIMMERS AND CALIBRATION

On **GPC® 150** is available a trimmer, named **RV1**, that calibrates the Vref voltage of the A/D Converter section. The **GPC® 150** is subjected to a careful test that verifies and calibrates all the card sections. To easily locate the trimmer, please refer to figure 24. The calibration is executed in laboratory, with a controlled +20 °C room temperature, following these steps:

- The A/D voltage reference (Vref) is calibrated through RV1 trimmer, by using a 5 digits precision multimeter, to a value of +2.4900 Vdc or +5.0000 Vdc, on test point TP1.

- The correspondence between the analog input signal and the combination read from A/D is verified. This check is performed with a reference signal connected to A/D inputs and testing that the A/D combination and the theoric combination differ at maximum of the A/D section errors sum.

- The trimmer is blocked with paint.

The analog interfaces use high precision components that are selected during mounting phase to avoid complicate and long calibration procedures. After the calibration, the on board trimmer is blocked with paint to maintain calibration also in presence of mechanic stresses (vibrations, movements, delivery, etc.).

The user must not modify the card calibration, but if thermic drifts, time drifts and so on, make necessary a new calibration, the user must strictly follow the previous described procedure. The circuitry that generates the reference voltage defines also the full range for all the 8 analog input channels; by software it is possible to define the signals acquisition modality between "single ended" (8 inputs grounded to AGND in the range 0÷2.490 V or 0÷5.000 V) and "fully differential" (4 differential inputs in the range ±2.490 V or ±5.000 V), as described in the appendix B of this manual. 

The full range value must be specified in the order, in fact this implies a difference in mounting procedure and calibration process. Without any explicit indication the board is delivered with standard full range value of 2.490 V.

The User most NOT intervent on the circuit that generates the reference voltage, however if this should be necessary (example: for time derives) then he/she must follow the above mentioned procedure. 

To easily locate RV1 and TP1 please refer to figure 24.

TEST POINT

The board is provided with a test point called TP1, that allows to read, through a galvanically isolated multimeter, the reference voltage which is calibrated in laboratory and whose value is Vref=2.4900 V (optional 5.000 V). TP1 is made of two contacts:

- **pin +** -> Vref
- **pin -** -> GND

To easily locate the test point contacts please refer to figure 24, while for further informations about Vref signal please refer to the paragraph “TRIMMER AND CALIBRATION”.

---

**Page 28**
I/O CONNECTION

To prevent possible connecting problems between **GPC® 150** and the external systems, the user has to read carefully the information of the previous paragraphs and he must follow these instructions:

- For RS 232, RS 422, Current Loop or RS 485 communication signals the User must follow the standard rules of these protocols.

- For all TTL signals the user must follow the rules of this electric standard. The connected digital signal must be always referred to card digital ground (GND). For TTL signals, the 0 Vdc level corresponds to logic state "0", while 5Vdc level corresponds to logic state "1".

- The analog inputs (A/D section) must be connected to low impedance signals in the following ranges: 0±2.490 V or 0±5.000 V or ±2.490 V or ±5.000 V according to selected voltage reference (Vref) or 0÷20 mA or 4÷20 mA if the conversion module is installed. Remember that the eight analog inputs available on CN5 are provided of filter capacitors that ensure an higher stability of the acquired signals, but reduce at the same time the bandwidth frequency. For further informations please refer to the paragraph “TYPE OF ANALOG INPUT SELECTION”.

TYPE OF ANALOG INPUT SELECTION

**GPC® 150** board can accept analog voltage and/or current inputs, as described in the previous paragraphs and chapters. The input type selection must be made during the order phase and is performed mounting a specific voltage-current conversion module (option code .8420) made by precision resistors. In detail:

- R30 -> channel 0
- R31 -> channel 1
- R32 -> channel 2
- R33 -> channel 3
- R34 -> channel 4
- R35 -> channel 5
- R36 -> channel 6
- R37 -> channel 7

Should the voltage-current conversion module not to be mounted (default case) the corresponding channel accepts a voltage input signal in the range 0÷2.490 V; otherwise a current input signal is accepted.

The value of the above mentioned resistors is obtained by the following spread:

\[ R = \frac{2.490 \text{ V}}{I_{\text{max}}} \]

Usually the voltage-current conversion modules are made using 124 Ω precision resistors, corresponding to 4÷20 mA or 0÷20 mA.

Any eventual configuration out of this standard should be asked directly to **grifo®**.

To easily locate the voltage-current conversion module please refer to figure 24.
VISUAL FEEDBACK

GPC® 150 board is provided with six LEDs to signal status conditions, as described in the following table:

<table>
<thead>
<tr>
<th>LEDs</th>
<th>COLOUR</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>LD1</td>
<td>Red</td>
<td>It indicates the activation of the external Watch Dog circuitry.</td>
</tr>
<tr>
<td>LD2</td>
<td>Red</td>
<td>It indicates the activation of the /INT signal.</td>
</tr>
<tr>
<td>LD3</td>
<td>Yellow</td>
<td>RUN/DEBUG jumper in RUN position.</td>
</tr>
<tr>
<td>LD4</td>
<td>Green</td>
<td>RUN/DEBUG jumper in DEBUG position.</td>
</tr>
<tr>
<td>LD5</td>
<td>Red</td>
<td>It indicates the CPU HALT status.</td>
</tr>
<tr>
<td>LD6</td>
<td>Green</td>
<td>Software manageable LED.</td>
</tr>
</tbody>
</table>

**FIGURE 23: VISUAL FEEDBACK TABLE**

The main purpose of these LEDs is to give a visual indication of the board status, making easier the operations of system working verify. To easily locate these LEDs on the board, please refer to figure 24.

DIGITAL I/O INTERFACES

Through CN3, CN4 and CN6 (I/O Abaco® standard connector) the GPC® 150 card can be connected to all of the numerous grifo® boards featuring the same standard pin out. Installation of these interface is very easy; in fact only a 20 pins flat cable (code FLT.20+20) is required, while the software management of these interfaces is as easy; in fact most of the software packages available for GPC® 150 card are provided with the necessary procedures. Remarkable modules are:

- **QTP 16P, QTP 24P, KDL x24, KDF 224, DEB 01**, etc. that solve all the local operator interfacing problems. These modules are provided with all the resources needed to obtain a high-level human-machine interface (they feature alphanumeric displays, matrix keyboard and visualization LEDs) at a short distance from GPC® 150 card. The available software drivers allow to manage the operator interface resources directly through the high-level instructions for console management.

- **IAC 01, DEB 01**: it is an interface for CENTRONICS parallel printer that can be connected with a standard printer cable. The printer is managed by software through the high level instructions of the selected programming language (LPRINT for BASIC, PRINTF for C, etc.).

- **MCI 64**: it a large mass memory support that can directly manage the PCMCIA memory cards (RAM, FLASH, ROM, etc.) in their available sizes. About software the developed drivers provide a complete file system interfacing allowing to access the informations stored in the memory card directly through the high-level file management instructions.

- **RBO xx, TBO xx, XBI xx, OBI xx**: these are buffer interfaces for I/O TTL signals. With these modules the TTL input signals are converted in NPN or PNP optoisolated inputs and the TTL output signals are converted in relays or transistor optoisolated outputs. Some of the above mentioned interfaces can be connected directly to CN4.

For more informations refer to "EXTERNAL CARDS" chapter and the software tools documentation.
JUMPERS

On GPC® 150 there are 12 jumpers for card configuration. Connecting these jumpers, the user can define for example the memory type and size, the peripheral devices functionality and so on. Below there is the jumpers list, location and function:

<table>
<thead>
<tr>
<th>JUMPERS</th>
<th>N. PINS</th>
<th>USE</th>
</tr>
</thead>
<tbody>
<tr>
<td>J1</td>
<td>2</td>
<td>Connects CPU /INT signal to RTC.</td>
</tr>
<tr>
<td>J2</td>
<td>3</td>
<td>Selects size for SRAM of IC8.</td>
</tr>
<tr>
<td>J3</td>
<td>2</td>
<td>Connects on board Lithium battery to the back up circuitry.</td>
</tr>
<tr>
<td>J4</td>
<td>4</td>
<td>Connects the Watch Dogs to /RESET signal or to CPU /INT signal.</td>
</tr>
<tr>
<td>J5</td>
<td>5</td>
<td>Selects the type of device for IC10.</td>
</tr>
<tr>
<td>J6</td>
<td>2</td>
<td>Connects the CPU /NMI signal to the power failure alarm signal.</td>
</tr>
<tr>
<td>J7</td>
<td>3</td>
<td>Selects RUN/DEBUG mode.</td>
</tr>
<tr>
<td>J8</td>
<td>2</td>
<td>Connects the CPU /INT signal to A/D converter.</td>
</tr>
<tr>
<td>J9</td>
<td>3</td>
<td>Selects directionality and working modality for serial line B in RS 422, RS 485.</td>
</tr>
<tr>
<td>J10</td>
<td>3</td>
<td>Selects communication protocol for serial line B (RS 232, RS 422, RS 485, Current Loop).</td>
</tr>
<tr>
<td>J11, J12</td>
<td>2</td>
<td>Connect the RS 422, RS 485 termination network.</td>
</tr>
</tbody>
</table>

FIGURE 25: JUMPERS SUMMARIZING TABLE

The following tables describe all the right connections of GPC® 150 jumpers with their relative functions. To recognize these valid connections, please refer to the board printed diagram (serigraph) or to figure 33 of this manual, where the pins numeration is listed; for recognizing jumpers location, please refer to figure 26.

The "*" used in the following tables, denotes the default connection, or on the other hand the connection set up at the end of testing phase, that is the configuration the User receives.
FIGURE 26: JUMPERS LOCATION
## 2 PINS JUMPERS

<table>
<thead>
<tr>
<th>JUMPERS</th>
<th>CONNECTION</th>
<th>USE</th>
<th>DEF.</th>
</tr>
</thead>
<tbody>
<tr>
<td>J1</td>
<td>not connected</td>
<td>It does not connect CPU /INT signal to RTC section.</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>connected</td>
<td>It connects CPU /INT signal to RTC section.</td>
<td></td>
</tr>
<tr>
<td>J3</td>
<td>not connected</td>
<td>It does not connect BT1 battery to back up circuitry.</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>connected</td>
<td>It connects BT1 battery to back up circuitry.</td>
<td></td>
</tr>
<tr>
<td>J6</td>
<td>not connected</td>
<td>It does not connect CPU /NMI signal to power failure section.</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>connected</td>
<td>It connects CPU /NMI signal to power failure section.</td>
<td></td>
</tr>
<tr>
<td>J8</td>
<td>not connected</td>
<td>It does not connect CPU /INT signal to A/D converter section.</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>connected</td>
<td>It connects CPU /INT signal to A/D converter section.</td>
<td></td>
</tr>
<tr>
<td>J11</td>
<td>not connected</td>
<td>It does not connect termination and forcing circuitry to serial line B in RS 485 or RS 422.</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>connected</td>
<td>It connects termination and forcing circuitry to serial line B in RS 485 or RS 422.</td>
<td></td>
</tr>
<tr>
<td>J12</td>
<td>not connected</td>
<td>It does not connect termination and forcing circuitry to serial line B in RS 485 or RS 422.</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>connected</td>
<td>It connects termination and forcing circuitry to serial line B in RS 485 or RS 422.</td>
<td></td>
</tr>
</tbody>
</table>

**Figure 27: 2 pins jumpers table**

The "*" used in the following tables, denotes the default connection, or on the other hand the connection set up at the end of testing phase, that is the configuration the User receives.
### 3 PINS JUMPERS

<table>
<thead>
<tr>
<th>JUMPERS</th>
<th>CONNECTION</th>
<th>USE</th>
<th>DEF.</th>
</tr>
</thead>
<tbody>
<tr>
<td>J2</td>
<td>position 1-2</td>
<td>It sets IC 8 for 128KBytes of SRAM.</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>position 2-3</td>
<td>It sets IC 8 for 512KBytes of SRAM.</td>
<td></td>
</tr>
<tr>
<td>J7</td>
<td>position 1-2</td>
<td>It selects RUN modality, indicated by the lighting LED LD4.</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>position 2-3</td>
<td>It selects DEBUG modality, indicated by the lighting LED LD3.</td>
<td></td>
</tr>
<tr>
<td>J9</td>
<td>position 1-2</td>
<td>It sets RS 485 communication protocol for serial line B.</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>position 2-3</td>
<td>It sets RS 422 communication protocol for serial line B.</td>
<td></td>
</tr>
<tr>
<td>J10</td>
<td>position 1-2</td>
<td>It connects CPU internal SIO /RXDB signal to the reception pin of RS 232 driver.</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>position 2-3</td>
<td>It connects CPU internal SIO /RXDB signal to the reception pin of RS 422, RS 485 or Current Loop driver.</td>
<td></td>
</tr>
</tbody>
</table>

**Figure 28: 3 pins jumpers table**

### 4 PINS JUMPER

<table>
<thead>
<tr>
<th>JUMPER</th>
<th>CONNECTION</th>
<th>USE</th>
<th>DEF.</th>
</tr>
</thead>
<tbody>
<tr>
<td>J4</td>
<td>position 1-2</td>
<td>It connects the CPU internal Watch Dog to the CPU /INT signal.</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>position 2-3</td>
<td>It connects the CPU internal Watch Dog to the reset signal.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>position 3-4</td>
<td>It connects the external Watch Dog to the reset signal.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>not connected</td>
<td>It does not connect any of the Watch Dogs to the reset signal nor to the /INT signal.</td>
<td></td>
</tr>
</tbody>
</table>

**Figure 29: 4 pins jumper table**

### 5 PINS JUMPER

<table>
<thead>
<tr>
<th>JUMPER</th>
<th>CONNECTION</th>
<th>USE</th>
<th>DEF.</th>
</tr>
</thead>
<tbody>
<tr>
<td>J5</td>
<td>position 1-2 and 3-4</td>
<td>It sets IC10 for EPROM.</td>
<td>*</td>
</tr>
<tr>
<td></td>
<td>position 2-3 and 4-5</td>
<td>It sets IC10 for FLASH EPROM.</td>
<td></td>
</tr>
</tbody>
</table>

**Figura 30: 5 pins jumper table**
RESET AND WATCH DOG

On **GPC® 150** there are two separated Watch Dog circuits that are really efficient and easy to use. The most important features of the external Watch Dog circuitry are:

- astable mode;
- intervention time fixed at 1420 ms (modifiable by hardware);
- enable function by hardware;
- retrigger by software;

In astable mode when intervention time is elapsed the circuit becomes active, it stays active till the end of reset time (180 msec) and after it is again deactivated. The external Watch Dog intervent is signaled by the lighting of LED LD1.

The most important features of the CPU internal Watch Dog circuitry are:

- monostable mode;
- intervention time programmable by software;
- enable function by software and hardware;
- retrigger by software;

In monostable mode when intervention time is elapsed the circuit becomes active and it stays active as far as a reset or power on happens.

In response to a /RESET signal activation and successive deactivation the board restarts the execution of the program stored at address 0000H on IC10 (EPROM or FLASH EPROM).

Please remark that /RESET signal generated by **GPC® 150** the board is connected also to pin 16C of K1 connector. Other reset sources, in addition to the Watch Dog circuits, are: CPU internal peripherals, RTC, reset contact (R.T., pin 29C of connector K1), A/D converter and power good circuitry.

About retrigger operation of internal and external watch dog circuits, please refer to paragraph "WATCH DOG" in chapter "PERIPHERAL DEVICES SOFTWARE DESCRIPTION" and to appendix B of this manual.

BACK UP

**GPC® 150** has an on-board lithium battery BT1 for the back up of SRAM and RTC content when power supply is switched off. Jumper J3 connects physically the battery so it can be disconnected to save its duration whenever back-up is not needed. Through CN1 connector it is possible to connect an external battery: configuration of jumper J3 does not affect the working of this battery and it can replace BT1 completely.

Please refer to the paragraph "ELECTRIC FEATURES" to choose the type of the external back-up battery, to easily locate see see figure 24.
POWER FAILURE

In addition to the CPU controlled power management circuitry, GPC® 150 card also features an efficient power failure circuitry. Through jumper J6 this latter can be connected to the microprocessor /NMI interrupt signal.

The task of this circuitry is to keep under control power supply voltage and activate on output to request a CPU action when this voltage reaches a value lower than a threshold (52 mV above the reset intervent) and jumper J6 is connected.

Please remark that the time interval between power failure activation and reset activation changes according to the type of supply being used; it is however about 100 µsec, long enough only to execute a fast response routine (for example to save a flag in the backed SRAM).

Typical use of power failure is to inform the board about the imminent power supply black out, so the CPU can save appropriate informations.

INTERRUPTS

A remarkable feature of GPC® 150 card is the powerful interrupt management. Here follows a short description of which devices can generate interrupts and their modalities; for further informations about interrupts management please refer to the microprocessor data sheet or to the appendix B of this manual.

- ABACO® BUS  -> Generates a CPU /NMI through K1 connector /NMI signal. Generates normal /INT, without regard for the daisy chain priority, through K1 connector /INT signal.

- Power failure  -> Generates a CPU /NMI, according to the connection of jumper J6.

- Real Time Clock  -> Generates normal /INT, without regard for the daisy chain priority, according to the connection of jumper J1.

- A/D Converter  -> Generates normal /INT, without regard for the daisy chain priority, according to the connection of jumper J8.

- Internal Watch dog  -> Generates normal /INT, without regard for the daisy chain priority, according to the connection of jumper J4.

- CPU peripherals  -> CPU internal sections CTC, SIO, PIO generate normal or vectored /INT, respecting the daisy chain priority.

The daisy chain on the GPC® 150 board is made only of SIO, PIO and CTC and can be software programmed through one of the microprocessor internal registers. This way the User can always respond promptly and efficiently to any external event, also deciding the priority to assign to the several event sources.

For further informations please refer to appendix B of this manual.
SERIAL COMMUNICATION SELECTION

Serial line A can be buffered only as RS 232 while serial line B can be buffered in RS 232, RS 422 or RS 485. By hardware can be selected which one of these electric standards is used, through jumpers connection (as described in the previous tables) and drivers installation. By software the serial line can be programmed to operate with all the standard physical protocols, in fact the bits per character, parity, stop bits and baud rates can be decided by setting opportunes CPU internal registers. In the following paragraphs there are all the informations on serial communication configurations. Some devices needed for RS 422, RS 485 and Current Loop configurations are not mounted on the board in standard configuration; this is why each fist non-standard (non-RS 232) serial configuration for line B must be always performed by grifo® technicians. This far the User can change in autonomy the configuration following the informations below:

- SERIAL LINE B IN RS 232 (default configuration)
  IC21 = driver MAX 202
  J9 = don’t care
  J10 = position 1-2
  J11, J12 = don’t care

- SERIAL LINE B IN CURRENT LOOP (option .CLOOP)
  IC21 = don’t care
  J9 = don’t care
  J10 = position 2-3
  J11, J12 = not connected
  IC28 = HCPL 4100

Please remark that Current Loop serial interface is passive, so it must be connected an active Current Loop serial line, that is a line provided with its own power supply. Current Loop interface can be employed to make both point-to-point and multi-point connections through a 2-wires or a 4-wires connection.

- SERIAL LINE B IN RS 422 (option .RS 422)
  IC21 = don’t care
  J9 = position 2-3
  J10 = position 2-3
  J11, J12 = (*1)

Status of signal /RTSB, which is software managed, allows to enable or disable the transmitter as follows:

/RTSB = low level = logic state 0 -> transmitter enabled
/RTSB = high level = logic state 1 -> transmitter disabled

In point-to-point connections, signal /RTSB can be always kept low (transmitter always enabled), while in multi-point connections transmitter must be enabled only when a transmission is requested.
FIGURE 31: SERIAL COMMUNICATION DRIVERS LOCATION
- SERIAL LINE B IN RS 485 (option .RS 485)

<table>
<thead>
<tr>
<th>Pin</th>
<th>Configuration</th>
</tr>
</thead>
<tbody>
<tr>
<td>J9</td>
<td>position 1-2</td>
</tr>
<tr>
<td>J10</td>
<td>position 2-3</td>
</tr>
<tr>
<td>J11, J12</td>
<td>(*1)</td>
</tr>
</tbody>
</table>

| IC21 | = don’t care   |
| IC25 | = SN 75176 or MAX 483 |
| IC26 | = no device    |
| IC27 | = no device    |
| IC28 | = no device    |

In this modality the signals to use are pins 4 and 5 of connector CN2, that become transmission or reception lines according to the status of signal /RTSB, managed by software, as follows:

/RTSB = low level = logic state 0 -> transmitter enabled
/RTSB = high level = logic state 1 -> transmitter disabled

This kind of serial communication can be used for multi-point connections, in addition it is possible to listen to own transmission, so the User is allowed to verify the success of transmission. In fact, any conflict on the line can be recognized by testing the received character after each transmission.

(*1) If using the RS 422 or RS 485 serial line, it is possible to connect the terminating and forcing circuit on the line by using J11 and J12. This circuit must be always connected in case of point-to-point connections, while in case of multi-point connections it must be connected only in the farthest boards, that is on the edges of the communication line.

When a reset or a power on occur, signal /RTSB is kept to a logic level high, so in one of these two cases driver RS 485 is receiving or RS 422 driver is disabled, avoiding eventual conflicts in communication.

For further informations about serial communication please refer to the examples of figures 14÷20 and to appendix B of this manual.

CONFIGURATION INPUTS

GPC® 150 is provided with an on board 8 pins Dip Switch (DSW1) and jumper (J7), the jumper selects the RUN/DEBUG modality, typically used for system configuration and software readable.

Most common applications for these devices are working conditions settings or firmware parameters input, etc.

Configuration inputs read modalities can be found in the chapter "PERIPHERAL DEVICES SOFTWARE DESCRIPTION", while to easily locate them on the board please refer to figures 24 and 26.
MEMORY SELECTION

On GPC® 150 can be mounted up to 5128K bytes of memory divided in several configurations, as described in the following table:

<table>
<thead>
<tr>
<th>IC</th>
<th>DEVICE</th>
<th>SIZE</th>
<th>JUMPERS POSITION</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>EPROM</td>
<td>128K Byte</td>
<td>J5 in position 1-2, 3-4</td>
</tr>
<tr>
<td></td>
<td>EPROM</td>
<td>256K Byte</td>
<td>J5 in position 1-2, 3-4</td>
</tr>
<tr>
<td></td>
<td>EPROM</td>
<td>512K Byte</td>
<td>J5 in position 1-2, 3-4</td>
</tr>
<tr>
<td></td>
<td>FLASH EPROM</td>
<td>128K Byte</td>
<td>J5 in position 2-3, 4-5</td>
</tr>
<tr>
<td></td>
<td>FLASH EPROM</td>
<td>512K Byte</td>
<td>J5 in position 2-3, 4-5</td>
</tr>
<tr>
<td>8</td>
<td>SRAM</td>
<td>128K Byte</td>
<td>J2 in position 1-2</td>
</tr>
<tr>
<td></td>
<td>SRAM</td>
<td>512K Byte</td>
<td>J2 in position 2-3</td>
</tr>
<tr>
<td>13</td>
<td>FLASH EPROM</td>
<td>64K÷2M Byte</td>
<td>-</td>
</tr>
<tr>
<td>14</td>
<td>FLASH EPROM</td>
<td>64K÷2M Byte</td>
<td>-</td>
</tr>
<tr>
<td>19</td>
<td>EEPROM</td>
<td>256÷8K Byte</td>
<td>-</td>
</tr>
</tbody>
</table>

**Figure 32: Memory selection table**

All the above described devices must feature a JEDEC compliant pin out except for the serial EEPROM installed on IC19 that must be requested to grifo® in the ordering phase. To determine the name of the memory devices that can be mounted, please refer to the manufacturer documentation.

GPC® 150 is delivered in its default configuration, this means 128K SRAM on IC8 and 512 bytes serial EEPROM on IC19; any different memory configuration can be mounted by the User in autonomy or requested to grifo® in the order. Below are reported the order codes for the several optional memory configurations:

- .512K -> 512K SRAM
- .FS  -> 2M serial FLASH EPROM
- .EE08 -> 1K serial EEPROM
- .EE16 -> 2K serial EEPROM
- .EE64 -> 8K serial EEPROM

For further information about memory options and their cost please contact grifo®, while to easily locate the memory devices on the board please refer to figure 26.
SOFTWARE DESCRIPTION

A wide selection of software development tools can be obtained, allowing use of the module as a system for its own development, both in assembler and in other high level languages; in this way the User can easily develop all the requested application programs in a very short time. Generally all software packages available for the mounted microprocessor, or for the Z80 family, can be used:

GET 80
It is a complete program with Editor, Communication driver, and Mass Memory management for all Z80 family cards. This program, developed by grifo®, allows to operate in the best conditions when GDOS, FGDOS or xGDOS MCI software tools are used; GET 80 is supplied when one of these tools is ordered and it is personalized with name and general data of the customer. A useful list of pull down menus and the possibility of using mouse, make program use very comfortable. GET 80 program can be executed both on MS-DOS system and on MACINTOSH computers too, through SOFT-PC program. It is supplied on MS-DOS 3”1/2 floppy disk with the documentation on GDOS 80 manual.

GDOS 150
It is a complete development Tool for GPC® 150 card. It is supplied together with GET 80 program to allow an easy and immediate use of this powerful development system. GDOS is divided in two different structures: the first one works on PC maintaining serial communication with the second one. The second structure is on EPROM, it works on board of the card and it is an efficient operating system that executes many low level functions and, at the same time, it allows high level language use. The combination of the said structures results in a complete machine, in fact the card uses PC resources (like floppy disk, hard disk, printer, keyboard, monitor, etc.) as its own peripheral devices. This resulting “virtual machine” performs operation in a transparent way for the User, so this latter can operate with the same modality of standard PC languages. It is really interesting the compatibility of GDOS with all CP/M program and languages; so, if the User has experience, knowledge or developed applications with CP/M, he can use immediately GDOS, without any changes. Moreover, GDOS can manage all memory devices exceeding 64K Bytes as RAM disk and ROM disk. The on board RAM devices can directly be used performing data read and write operations with the confortable file formats. This software tools is supplied on EPROM with MS-DOS GET 80 floppy disk, some examples, utilities and the operating system documentation.

FGDOS 150
It is really similar to GDOS, but it can program and erase the on board FLASH EPROM with the application program developed from the User. In this way the external EPROM programmer is not necessary to store definitely the program and it is possible to modify or to add code directly on the installed machine, through a portable PC. This software tools is supplied on FLASH EPROM with MS-DOS GET 80 floppy disk, some examples, utilities and the operating system documentation.

NOICE
It is a PC hosted debugger consists of a target specific DOS program, NOICExxx.EXE, and a target resident monitor program. The two programs communicate via RS 232. NOICE includes: source level debug; a disassembler; a file viewer; memory display and editing; a virtually unlimited number of breakpoints; hardware free single step; definition of symbols; the ability to record and play back files of commands; on line help.
xGDOS MCI 150
It is a version of GDOS or FGDOS software tools, capable of PCMCIA Memory Card management. Using MCI 64 card, the GDOS operating system manages memory cards as RAM disk or ROM disk. All applications with data acquisition and data logging can be realized with high level languages that manage data on files, with a fast development time and without any software complication. This software tool is supplied on EPROM or FLASH EPROM with MS-DOS GET 80 floppy disk, some examples, utilities and the operating system documentation.

CBZ-80
Is is a Basic Compiler that generates a really compact and fast code. It must work together with any GDOS version and it can exceed the 64K memory limits of Z80 family microprocessors through CHAIN modality. More than one application program can be saved in RAM and/or ROM disks and subsequently executed. In conjunction to the powerful GET 80 Editor the CBZ 80 program becomes a comfortable and really efficient development system for any kind of application program. This program is supplied as ROM DISK file in GDOS EPROM or FLASH EPROM and on MS-DOS floppy disk with some examples and manual.

PASCAL 80
It is an efficient and complete PASCAL Compiler for Z80 family cards, with features similar to Release 3.0 of Borland Turbo PASCAL. It must work together with any GDOS version and it can exceed the 64K memory limits of Z80 family microprocessors through OVERLAY modality. More than one application program can be saved in RAM and/or ROM disks and subsequently executed. The terminal emulation of GET 80 program support the typical full screen PASCAL Editor, including the attributes management. This program is supplied as ROM DISK file in GDOS EPROM or FLASH EPROM and on MS-DOS floppy disk with some example and manual.

RSD 150
This software tools is a Remote Symbolic Debugger with two operating mode. The first one is a monitor debugger modality with software emulation on P.C.; the second is a remote monitor debugger modality that execute code directly on the card. Through serial communication the User can: download an HEX file and associated symbol table, debug code in symbolic mode, execute code in step by step mode or in real time mode, set breakpoint, dump and modify memory and registers, etc. RSD software tool supports both Z80 and Z180 instruction sets. Really interesting is the program execution management, in fact many hardware and software breakpoint are supported. RSD can be used together with assembler tools, like ZASM 80, and C Compiler CC 80. It is supplied on EPROM and on MS-DOS floppy disk with technical manual.

ZASM 80
It is a macro cross assemler that operates on any PC with MS-DOS operating system. It supports both Z80 and Z180 instruction sets. The generated code can be debugged on PC, through software simulation, or directly on target card, through remote modality, using RSD software tools. ZASM 80 is compatible with C Compiler CC 80 of which it assemble the compilation result. It is supplied on MS-DOS floppy disk with technical manual.
CC 80
It is a complete C Compiler with ANSI/ISO standard, provided of floating point procedure, that can generate code for Z80 and Z180 family microprocessors. It works together with cross assembler ZASM 80 and Symbolic Debugger RSD.
It is supplied on MS-DOS floppy disk with technical manual.

HI TECH C 80
Professional C Cross Compiler of Hi-Tech Software Inc. This Compiler is terribly fast and it generates a small quantity of code. This result is due to advanced techniques in optimizing the generated code based on Artificial Intelligence techniques which allow to get a very compact and very fast code. The package includes: IDE, Compiler, Code optimizer, Assembler, Linker, Remote Debugger and so on. This tool is Full ANSI/ISO Standard and Full Library Source Code. Once the porting of the Remote-Debugger module is done, this tool allows the user the software debugging directly on the hardware that he is experimenting. This type of specialization of the Remote-Debugger its available from now ant it is supplied with all grifo® CPU cards’. This software package is on 3” 1/2 diskettes under MS-DOS format along with user manual. This version supports these following CPUs: Z80, Z180, 84C011, 84C11, 84C013, 80C13, 84C015, 84C15, 64180, NCS800, Z181, Z182.

DDS MICRO C 85
Low cost cross compiler for C source program. It is a powerful software tool that includes editor, C compiler (integer), assembler, optimizer, linker, library, and remote debugger, in one easy to use integrated development environment. There are also included the library sources and many utilities programs.
FIGURE 33: COMPONENTS MAP
ADDRESSES AND MAPS

In this chapter are reported all information about card use, related to hardware and software. For example, the registers addresses and the memory allocation are described below.

ON BOARD RESOURCES ALLOCATION

The card devices addresses are managed by a specific control logic, realized with programmable logic devices. This control logic allocates SRAM, EPROM and peripheral devices in a comfortable way for the User.

The control logic is able to manage separately Input/Output peripherals and on board memory. CPU 84C15 is capable to address directly 64K Byte of memory and 256 I/O addresses, the control logic provides on board memory and peripheral devices allocation inside the 5128K Byte address space. The maps management is completely driven by software through the MMU circuit programmation: the used memory can be selected and divided in 32K Byte size segments. About I/O maps the control logic avoids every conflicts problems between CPU internal and external peripherals.

Summarizing the control logic allocates:

- **ABACO® BUS**
  - Up to 512K Byte of EPROM or FLASH EPROM installed on IC10
  - Up to 512K Byte of SRAM installed on IC8
  - Up to 2048K Byte of serial FLASH EPROM installed on IC13
  - Up to 2048K Byte of serial FLASH EPROM installed on IC14
  - Up to 8K Byte of serial EEPROM, installed on IC19
  - SIO
  - CTC
  - PIO
  - RTC
  - A/D Converter
  - Memory Management Unit circuitry
  - Configuration Dip Switch DSW1
  - Activity LED
  - Watch Dog circuits

The addresses of all these devices are described in the following paragraphs and can't be set with different values. If some different specific maps are required, please contact directly grifo®.
I/O ADDRESSES

The on board control logic manages the allocation of all the peripheral devices registers in the microprocessor I/O space, that is 256 bytes long. Next table shows names, addresses, meanings and directions of peripheral device registers (including the internal microprocessor ones).

<table>
<thead>
<tr>
<th>DEVICE</th>
<th>REG.</th>
<th>ADDRESS</th>
<th>R/W</th>
<th>MEANING</th>
</tr>
</thead>
<tbody>
<tr>
<td>RTC 62421</td>
<td>S1</td>
<td>00H</td>
<td>R/W</td>
<td>Units of seconds data register</td>
</tr>
<tr>
<td></td>
<td>S10</td>
<td>01H</td>
<td>R/W</td>
<td>Decines of seconds data register</td>
</tr>
<tr>
<td></td>
<td>M11</td>
<td>02H</td>
<td>R/W</td>
<td>Units of minutes data register</td>
</tr>
<tr>
<td></td>
<td>M10</td>
<td>03H</td>
<td>R/W</td>
<td>Decines of minutes data register</td>
</tr>
<tr>
<td></td>
<td>H1</td>
<td>04H</td>
<td>R/W</td>
<td>Units of hours data register</td>
</tr>
<tr>
<td></td>
<td>H10</td>
<td>05H</td>
<td>R/W</td>
<td>Decines of hours data register; AM/PM</td>
</tr>
<tr>
<td></td>
<td>D1</td>
<td>06H</td>
<td>R/W</td>
<td>Units of day data register</td>
</tr>
<tr>
<td></td>
<td>D10</td>
<td>07H</td>
<td>R/W</td>
<td>Decines of day data register</td>
</tr>
<tr>
<td></td>
<td>MO1</td>
<td>08H</td>
<td>R/W</td>
<td>Units of month data register</td>
</tr>
<tr>
<td></td>
<td>MO10</td>
<td>09H</td>
<td>R/W</td>
<td>Decines of month data register</td>
</tr>
<tr>
<td></td>
<td>Y1</td>
<td>0AH</td>
<td>R/W</td>
<td>Units of year data register</td>
</tr>
<tr>
<td></td>
<td>Y10</td>
<td>0BH</td>
<td>R/W</td>
<td>Decines of year data register</td>
</tr>
<tr>
<td></td>
<td>W</td>
<td>0CH</td>
<td>R/W</td>
<td>Day of week data register</td>
</tr>
<tr>
<td></td>
<td>REGD</td>
<td>0DH</td>
<td>R/W</td>
<td>D control and status register</td>
</tr>
<tr>
<td></td>
<td>REGE</td>
<td>0EH</td>
<td>R/W</td>
<td>E control and status register</td>
</tr>
<tr>
<td></td>
<td>REGF</td>
<td>0FH</td>
<td>R/W</td>
<td>F control and status register</td>
</tr>
<tr>
<td>CTC</td>
<td>CTC0</td>
<td>10H</td>
<td>R/W</td>
<td>Channel 0 data status register</td>
</tr>
<tr>
<td></td>
<td>CTC1</td>
<td>11H</td>
<td>R/W</td>
<td>Channel 1 data status register</td>
</tr>
<tr>
<td></td>
<td>CTC2</td>
<td>12H</td>
<td>R/W</td>
<td>Channel 2 data status register</td>
</tr>
<tr>
<td></td>
<td>CTC3</td>
<td>13H</td>
<td>R/W</td>
<td>Channel 3 data status register</td>
</tr>
<tr>
<td>PPI 82C55</td>
<td>PA</td>
<td>14H</td>
<td>R/W</td>
<td>Port A data register</td>
</tr>
<tr>
<td></td>
<td>PB</td>
<td>15H</td>
<td>R/W</td>
<td>Port B data register</td>
</tr>
<tr>
<td></td>
<td>PC</td>
<td>16H</td>
<td>R/W</td>
<td>Port C data register</td>
</tr>
<tr>
<td></td>
<td>RC</td>
<td>17H</td>
<td>R/W</td>
<td>Control and command register</td>
</tr>
<tr>
<td>SIO</td>
<td>RDA</td>
<td>18H</td>
<td>R/W</td>
<td>Serial line A data register</td>
</tr>
<tr>
<td></td>
<td>RSA</td>
<td>19H</td>
<td>R/W</td>
<td>Serial line A status register</td>
</tr>
<tr>
<td></td>
<td>RDB</td>
<td>1AH</td>
<td>R/W</td>
<td>Serial line B data register</td>
</tr>
<tr>
<td></td>
<td>RSB</td>
<td>1BH</td>
<td>R/W</td>
<td>Serial line B status register</td>
</tr>
<tr>
<td>PIO</td>
<td>PAD</td>
<td>1CH</td>
<td>R/W</td>
<td>Port A data register</td>
</tr>
<tr>
<td></td>
<td>PAS</td>
<td>1DH</td>
<td>W</td>
<td>Port A control register</td>
</tr>
<tr>
<td></td>
<td>PBD</td>
<td>1EH</td>
<td>R/W</td>
<td>Port B data register</td>
</tr>
<tr>
<td></td>
<td>PBS</td>
<td>1FH</td>
<td>W</td>
<td>Port B control register</td>
</tr>
</tbody>
</table>

**Figure 34: I/O addresses table - Part 1**
<table>
<thead>
<tr>
<th>DISP.</th>
<th>REG.</th>
<th>INDIRIZZO</th>
<th>R/W</th>
<th>SIGNIFICATO</th>
</tr>
</thead>
<tbody>
<tr>
<td>A/D LM12458</td>
<td>IRL0:7</td>
<td>20H±2EH (even)</td>
<td>R/W</td>
<td>Sequencer instruction register low 0±7</td>
</tr>
<tr>
<td></td>
<td>IRH0:7</td>
<td>21H±2FH (odd)</td>
<td>R/W</td>
<td>Sequencer instruction register high 0±7</td>
</tr>
<tr>
<td></td>
<td>CNTL</td>
<td>30H</td>
<td>R/W</td>
<td>Configuration register low</td>
</tr>
<tr>
<td></td>
<td>CNTH</td>
<td>31H</td>
<td>R/W</td>
<td>Configuration register high</td>
</tr>
<tr>
<td></td>
<td>INTENL</td>
<td>32H</td>
<td>R/W</td>
<td>Interrupt abilitation register low</td>
</tr>
<tr>
<td></td>
<td>INTENH</td>
<td>33H</td>
<td>R/W</td>
<td>Interrupt abilitation register high</td>
</tr>
<tr>
<td></td>
<td>INTSTL</td>
<td>34H</td>
<td>R</td>
<td>Interrupt status register low</td>
</tr>
<tr>
<td></td>
<td>INTSTH</td>
<td>35H</td>
<td>R</td>
<td>Interrupt status register high</td>
</tr>
<tr>
<td></td>
<td>TMRL</td>
<td>36H</td>
<td>R/W</td>
<td>Timer register low</td>
</tr>
<tr>
<td></td>
<td>TMRH</td>
<td>37H</td>
<td>R/W</td>
<td>Timer register high</td>
</tr>
<tr>
<td></td>
<td>FIFOL</td>
<td>38H</td>
<td>R</td>
<td>Conversions to FIFO register low</td>
</tr>
<tr>
<td></td>
<td>FIFOH</td>
<td>39H</td>
<td>R</td>
<td>Conversions to FIFO register high</td>
</tr>
<tr>
<td></td>
<td>LIMSTL</td>
<td>3AH</td>
<td>R</td>
<td>Limits status register low</td>
</tr>
<tr>
<td></td>
<td>LIMSTH</td>
<td>3BH</td>
<td>R</td>
<td>Limits status register high</td>
</tr>
<tr>
<td>ABACO® BUS</td>
<td>BUS</td>
<td>40H±E7H</td>
<td>R/W</td>
<td>ABACO® BUS addresses</td>
</tr>
<tr>
<td>REG. INTERNI</td>
<td>SCRP</td>
<td>EEH</td>
<td>R/W</td>
<td>Microprocessor inside registers address register</td>
</tr>
<tr>
<td></td>
<td>SCDP</td>
<td>EFH</td>
<td>R/W</td>
<td>Microprocessor inside registers data register</td>
</tr>
<tr>
<td>W.D. INTERNO</td>
<td>WDTMR</td>
<td>F0H</td>
<td>R/W</td>
<td>Internal Watch Dog programming register</td>
</tr>
<tr>
<td></td>
<td>WDTMR</td>
<td>F1H</td>
<td>W</td>
<td>Internal Watch Dog access register</td>
</tr>
<tr>
<td></td>
<td>INTPR</td>
<td>F4H</td>
<td>W</td>
<td>Interrupt priority register</td>
</tr>
<tr>
<td></td>
<td>BAT</td>
<td>F8H</td>
<td>R</td>
<td>Battery status register</td>
</tr>
<tr>
<td>M. M. U.</td>
<td>MEM</td>
<td>F8H</td>
<td>W</td>
<td>MMU setting register</td>
</tr>
<tr>
<td></td>
<td>DSW1</td>
<td>FCH</td>
<td>R</td>
<td>Dip Switch register</td>
</tr>
<tr>
<td>WD. EXT.</td>
<td>RWD</td>
<td>FCH</td>
<td>R</td>
<td>External Watch Dog retrigger register</td>
</tr>
<tr>
<td>LD6</td>
<td>LEDW</td>
<td>FCH</td>
<td>W</td>
<td>Activity LED set status register</td>
</tr>
<tr>
<td></td>
<td>LEDR</td>
<td>F8H</td>
<td>R</td>
<td>Activity LED get status registertà</td>
</tr>
<tr>
<td>SFLASH</td>
<td>SF1</td>
<td>F8H</td>
<td>R/W</td>
<td>Serial FLASH management register</td>
</tr>
<tr>
<td></td>
<td>SF2</td>
<td>FCH</td>
<td>W</td>
<td>Serial FLASH data write register</td>
</tr>
</tbody>
</table>

**Figure 35: I/O Addresses Table - Part 2**

For a detailed description of the registers function, please refer to next chapter "PERIPHERAL DEVICES SOFTWARE DESCRIPTION".
ABACO® BUS ADDRESSES

The GPC® 150 control logic defines ABACO® BUS addresses and only these addresses must be used to manages correctly the BUS. As described in figures 34 and 35, only the addresses from 40H to E7H are available for ABACO® BUS. Any I/O operations at each one of these addresses enables the /IORQ signal and the other control signals of K1 connector and the I/O operations is performed on the connected peripheral cards.

MEMORIES MAPPING

The total 5128K Byte of memory supported by the card are divided this way:

- Up to 512K Byte of EPROM or 512K Byte of FLASH EPROM allocated in the memory space
- Up to 512K Byte of SRAM allocated in the memory space
- Up to 4MByte of serial FLASH EPROM on two 2MByte max devices each allocated in the I/O space
- Up to 8K Byte of serial EEPROM allocated in the I/O space

GPC® 150 can directly manage at most 64K bytes of memory that is the microprocessor logic addressable space. On the board this logic space can be divided in two 32K Byte pages: both SRAM and EPROM can be installed on the low page, while only SRAM can be installed on the high page. MMU circuitry, driven through a simple software management, takes care to divide the addressable space in 32K Byte pages and to make them available directly into the CPU addressing space. It is possible to address indirectly a memory area much greater than the area nomally accessible by the CPU just programming the MEM register. Here follow two figures that show the possible memory devices configurations, for further informations please refer to the paragraph "MEMORY MANAGEMENT UNIT", while to easily locate the memory deviced refer to figure 24.

Some software packages, like GDOS and FGDOS, are capable to manage in autonomy the MMU circuitry to make address in the CPU addressable memory area all the available memory without bothering the User.

When a power on or a reset occour, R/E signal is set to 0, so the board starts executing the code located at the logical address 0000H of page 0 on EPROM or FLASH EPROM installed IC10.
Figure 36: Memory mapping with R/E=0
Figure 37: Memory mapping with R/E=1
PERIPHERAL DEVICES SOFTWARE DESCRIPTION

In the previous paragraphs are described the external registers addresses, while in this one there is a specific description of registers meaning and function (please refer to I/O addresses table, for the registers names and addresses values). For a more detailed description of the devices, please refer to manufacturing company documentation; for microprocessor internal peripheral devices, not described in this paragraph, refer to appendix B. In the following paragraphs the D7:D0 and .0:.7 indications denote the eight bits of the combination used in I/O operations.

MEMORY MANAGEMENT UNIT

An efficient MMU circuitry takes care to allocate in the CPU addressing space all the memory devices that can be installed on **GPC® 150**. This section can be programmed through the MEM register, which is allocated in the I/O addressing space. The bits of MEM register have the following meaning:

<table>
<thead>
<tr>
<th>MEM:</th>
<th>Meaning of bits</th>
</tr>
</thead>
<tbody>
<tr>
<td>MEM.7</td>
<td>R/E: SRAM (D7=1) or EPROM/FLASH EPROM (D7=0) selector, for the low page (0000H:7FFFH) of the CPU addressing space</td>
</tr>
<tr>
<td>MEM.6</td>
<td>A18 x IC10 and /A18 x IC8</td>
</tr>
<tr>
<td>MEM.5</td>
<td>A17 x IC10 and /A17 x IC8</td>
</tr>
<tr>
<td>MEM.4</td>
<td>A16 x IC10 and /A16 x IC8</td>
</tr>
<tr>
<td>MEM.3</td>
<td>A15 x IC10 and /A15 x IC8</td>
</tr>
<tr>
<td>MEM.2,1,0</td>
<td>Please refer to the paragraph &quot;SERIAL FLASH EPROM&quot;</td>
</tr>
</tbody>
</table>

Only bits D3:D7 define which page of SRAM installed IC8 or EPROM or FLASH EPROM installed on IC10 must be addressed.

When a reset or a Power On occur all the bits of MEM register are reset (all bits 0); this means to program the MMU section where the low 32K Bytes page consists of page 0 EPROM or FLASH EPROM installed on IC10 and the high 32K Bytes page consists of page 0 SRAM installed on IC8. Please refer to the following table, also remembering figures 36 and 37, for an overview of all the possible MMU section configurations.

"X" means non significant bit, that is that bit can be "1" or "0" without influencing the setting there described.
<table>
<thead>
<tr>
<th>PAGE 32K LOW</th>
<th>PAGE 32K HIGH</th>
<th>MEM REGISTER</th>
</tr>
</thead>
<tbody>
<tr>
<td>0: IC10</td>
<td>0: IC8</td>
<td>00000XXXXB = 00H</td>
</tr>
<tr>
<td>1: IC10</td>
<td>0: IC8</td>
<td>00001XXXXB = 08H</td>
</tr>
<tr>
<td>2: IC10</td>
<td>0: IC8</td>
<td>00010XXXXB = 10H</td>
</tr>
<tr>
<td>3: IC10</td>
<td>0: IC8</td>
<td>00011XXXXB = 18H</td>
</tr>
<tr>
<td>4: IC10</td>
<td>0: IC8</td>
<td>00100XXXXB = 20H</td>
</tr>
<tr>
<td>5: IC10</td>
<td>0: IC8</td>
<td>00101XXXXB = 28H</td>
</tr>
<tr>
<td>6: IC10</td>
<td>0: IC8</td>
<td>00110XXXXB = 30H</td>
</tr>
<tr>
<td>7: IC10</td>
<td>0: IC8</td>
<td>00111XXXXB = 38H</td>
</tr>
<tr>
<td>8: IC10</td>
<td>0: IC8</td>
<td>01000XXXXB = 40H</td>
</tr>
<tr>
<td>9: IC10</td>
<td>0: IC8</td>
<td>01001XXXXB = 48H</td>
</tr>
<tr>
<td>10: IC10</td>
<td>0: IC8</td>
<td>01010XXXXB = 50H</td>
</tr>
<tr>
<td>11: IC10</td>
<td>0: IC8</td>
<td>01011XXXXB = 58H</td>
</tr>
<tr>
<td>12: IC10</td>
<td>0: IC8</td>
<td>01100XXXXB = 60H</td>
</tr>
<tr>
<td>13: IC10</td>
<td>0: IC8</td>
<td>01101XXXXB = 68H</td>
</tr>
<tr>
<td>14: IC10</td>
<td>0: IC8</td>
<td>01110XXXXB = 70H</td>
</tr>
<tr>
<td>15: IC10</td>
<td>0: IC8</td>
<td>01111XXXXB = 78H</td>
</tr>
<tr>
<td>0: IC8</td>
<td>0: IC8</td>
<td>10000XXXXB = 80H</td>
</tr>
<tr>
<td>1: IC8</td>
<td>0: IC8</td>
<td>10001XXXXB = 88H</td>
</tr>
<tr>
<td>2: IC8</td>
<td>0: IC8</td>
<td>10010XXXXB = 90H</td>
</tr>
<tr>
<td>3: IC8</td>
<td>0: IC8</td>
<td>10011XXXXB = 98H</td>
</tr>
<tr>
<td>4: IC8</td>
<td>0: IC8</td>
<td>10100XXXXB = A0H</td>
</tr>
<tr>
<td>5: IC8</td>
<td>0: IC8</td>
<td>10101XXXXB = A8H</td>
</tr>
<tr>
<td>6: IC8</td>
<td>0: IC8</td>
<td>10110XXXXB = B0H</td>
</tr>
<tr>
<td>7: IC8</td>
<td>0: IC8</td>
<td>10111XXXXB = B8H</td>
</tr>
<tr>
<td>8: IC8</td>
<td>0: IC8</td>
<td>11000XXXXB = C0H</td>
</tr>
<tr>
<td>9: IC8</td>
<td>0: IC8</td>
<td>11001XXXXB = C8H</td>
</tr>
<tr>
<td>10: IC8</td>
<td>0: IC8</td>
<td>11010XXXXB = D0H</td>
</tr>
<tr>
<td>11: IC8</td>
<td>0: IC8</td>
<td>11011XXXXB = D8H</td>
</tr>
<tr>
<td>12: IC8</td>
<td>0: IC8</td>
<td>11100XXXXB = E0H</td>
</tr>
<tr>
<td>13: IC8</td>
<td>0: IC8</td>
<td>11101XXXXB = E8H</td>
</tr>
<tr>
<td>14: IC8</td>
<td>0: IC8</td>
<td>11110XXXXB = F0H</td>
</tr>
<tr>
<td>15: IC8</td>
<td>0: IC8</td>
<td>11111XXXXB = F8H</td>
</tr>
</tbody>
</table>

**Figure 38: Possible MMU section configurations table**

**A/D Converter**

Please refer to appendix B where the software description of A/D Converter LM 12H458 is reported. Should these informations be still insufficient it is suggested to consult the manufacturer technical documentation.
EXTERNAL WATCH DOG

Retrigger operation of GPC® 150 external Watch Dog circuit is performed with a simple input operation at the address of register RWD. To avoid external Watch Dog activation it is indispensable to perform retrigger operations at regular time periods and the duration of these periods must be smaller than intervention time. If retrigger doesn't happen as before described and jumper J4 is connected in position 3-4, when intervention time is elapsed, the card is reset. By default the intervention time is about 1.4 s and jumper J4 does NOT connect external Watch Dog to reset circuitry.

SERIAL EEPROM

For informatons about the management of serial EEPROM module installed on IC19, please refer to the documentation of the software package used to program the board. This technical manual reports no further informations about the serial EEPROM management because this activity employs a very deep knowledge of the device itself. For this, its complete management is affordable through the high level instructions of the software package being used.

Please remark that the first 32 bytes (0÷31) are reserved so the User should avoid to modify their value. Control logic allows serial EEPROM software management through /SYNCA, /DTRA and /DTRB SIO signals, these are the connections:

/SYNCA  ->  DATA input signal  (SDA)
/DTRB    ->  DATA output signal  (SDA)
/DTRA    ->  CLOCK signal        (SCL)

Known the serial EEPROM management circuitry hardware implementation, please remark that signals A0,A1,A2 of this device's slave address are all set to logic 0. Bit logic status 0 corresponds to low logic status (=0V) of the corresponding signal, while bit logic status 1 corresponds to low logic status (=0V).

For further informations about SIO signals management modalities please refer to proper technical documentation of appendix B of this manual.

BATTERY STATUS

Status of on board battery BT1 installed on GPC® 150 can be acquired by software, performing a simple input operation from the address of BAT register and extracting bit 3, that has the following meaning:

BAT.3 = 0  ->  battery discharged  (<2,265 V)
BAT.3 = 1  ->  battery charged     (> 2,265 V)

For further informations about on board battery and back up circuitry please refer to proper previous paragraphs.
CONFIGURATION INPUTS

GPC® 150 is provided with 9 software acquirable User settable configuration inputs divided as follows.
Dip Switch DSW1 can be acquired by software, performing a simple input operation from the address of DSW1 register. This is the correspondance between Dip Switch signals and DSW1 bits:

<table>
<thead>
<tr>
<th>DSW1.7</th>
<th>-&gt;</th>
<th>Dip Switch 8</th>
</tr>
</thead>
<tbody>
<tr>
<td>DSW1.6</td>
<td>-&gt;</td>
<td>Dip Switch 7</td>
</tr>
<tr>
<td>DSW1.5</td>
<td>-&gt;</td>
<td>Dip Switch 6</td>
</tr>
<tr>
<td>DSW1.4</td>
<td>-&gt;</td>
<td>Dip Switch 5</td>
</tr>
<tr>
<td>DSW1.3</td>
<td>-&gt;</td>
<td>Dip Switch 4</td>
</tr>
<tr>
<td>DSW1.2</td>
<td>-&gt;</td>
<td>Dip Switch 3</td>
</tr>
<tr>
<td>DSW1.1</td>
<td>-&gt;</td>
<td>Dip Switch 2</td>
</tr>
<tr>
<td>DSW1.0</td>
<td>-&gt;</td>
<td>Dip Switch 1</td>
</tr>
</tbody>
</table>

The signals are in complemented logic, this means that a dip ON gives a logic status 0 on the corresponding bit, while a dip OFF gives a logic status 1.
Please remark that Dip Switch status acquisition implies also external Watch Dog retrigger, because RWD register and DSW1 register are allocated at the same I/O address.

Configuration jumper J7 is connected to /SYNCB SIO signal.
Jumper J7 connected in position 1-2 gives logic status 0, while connection in position 2-3 gives logic status 1. For further informations about the acquisition of /SYNCB signal status, please refer to the proper technical documentation of appendix B of this manual.
Jumper J7 (RUN/DEBUG) works as selector of RUN modality (position 1-2) or DEBUG modality (position 2-3). This feature is used by some of grifo® software packages.

ACTIVITY LED

On board control logic allows the management of an activity LED, called LD6, through LEDR and LEDW registers:

<table>
<thead>
<tr>
<th>LEDW.0</th>
<th>-&gt;</th>
<th>set LD6 status</th>
</tr>
</thead>
<tbody>
<tr>
<td>LEDR.1</td>
<td>-&gt;</td>
<td>get LD6 status</td>
</tr>
</tbody>
</table>

The LED can be lit performing on output operation to the allocation address of register LEDW with the corresponding bit (bit 0) set to logical 1. Of course, the LED can be turned off through the same output operation with the corresponding bit reset to logical 0.
The status of the activity LED can be acquired by software performing an input operation at the address of register LEDR and extracting bit 1.
Please remark that register LEDW has the same allocation address of register SF2, so every write operation to the bits of this register must consider the effects on the other device.
Register LEDW is reset (all bits 0) when a reset or a power on occur, so after one of such events LED is turned off.
SERIAL FLASH EPROM

For informations about the management of serial FLASH EPROM modules installed on IC13 and IC14, please refer to the documentation of the software package used to program the board. This technical manual reports no further informations about the serial FLASH EPROMs management because this activity employs a very deep knowledge of the device itself. For this, its complete management is affordable through the high level instructions of the software package being used. Control logic allows serial FLASH EPROM modules software management through some bits of SF1 and SF2 registers, these are the correspondances:

**SF1 REGISTER in OUTPUT**

- SF1.0 -> CLOCK signal for IC13 and IC14 (SCK)
- SF1.1 -> chip select (abilitation) for IC14 (/CS)
- SF1.2 -> chip select (abilitation) for IC13 (/CS)

**SF1 REGISTER in INPUT**

- SF1.0 -> input data signal from IC13 and IC14 (SO)

**SF2 REGISTER in OUTPUT**

- SF2.7 -> output data signal to IC13 and IC14 (SI)

Known the serial FLASH EPROMs management circuitry hardware implementation, please remark that signals /WP and RDY of these devices are all set to logic 1. Bit logic status 0 corresponds to low logic status (=0V) of the corresponding signal, while bit logic status 1 corresponds to low logic status (=0V).

Please remark that SF1 and SF2 registers allocated at the same I/O address of respectively of MMU and LEDW registers, so every write operation to the bits of these registers must consider the effects on the other devices.

Registers SF1 and SF2 are reset (all bits 0) when a reset or a power on occour, so after one of such events serial FLASH EPROMs are disabled.

**BAUD RATE GENERATOR**

The SIO frequencies generation section is capable to generate two separated baud rates that can vary in the range 600 Baud \( \div \) 115200 Baud, picking the seven most common used values. **GPC® 150** card allows to set the communication speeds performing a simple output instruction to the CTC2 and CTC3 I/O addresses. In fact timer counters 2 and 3 of microprocessor CTC section are used to generate the baud rate respectively for serial line A and B.

To make the CTC channels operate as baud rate generators it is essential to program them as follows:

- Give a channel reset command = output to CTCn control register the value 03H.
- Give a channel control word that: disables interrupt, selects timer mode, selects a descending front, and loads a time constant = output to CTCn control register the value 45H.
- Load the time constant corresponding to the baud rate required = output to CTCn control register the value indicated by the following table.
Figure 39: Baud rate time constants table

All CTC channels are disabled after a reset or a Power On, and so the baud rate generators. For further informations please refer to the proper paragraph of Appendix B in this manual.

REAL TIME CLOCK

This peripheral is allocated in 16 consecutives I/O addresses, 3 of which correspond to status registres while the remaining 13 are for datas. Data registers are used both for read operations (of the current time and date) and write operations (to initialize the time and date) just like the status registers which are used in write operations (to program the operative mode) and in read operations (to acquire the RTC status). Here follows a list of the RTC data registers’ meanings:

<table>
<thead>
<tr>
<th>SEC1</th>
<th>- Units of seconds</th>
<th>- 4 least significant bits of SEC1.3:SEC1.0</th>
</tr>
</thead>
<tbody>
<tr>
<td>SEC10</td>
<td>- Decines of secondi</td>
<td>- 3 least significant bits of SEC10.2:SEC10.0</td>
</tr>
<tr>
<td>MIN1</td>
<td>- Units of minutes</td>
<td>- 4 least significant bits of MIN1.3:MIN1.0</td>
</tr>
<tr>
<td>MIN10</td>
<td>- Decines of minutes</td>
<td>- 3 least significant bits of MIN10.2:MIN10.0</td>
</tr>
<tr>
<td>HOU1</td>
<td>- Units of hours</td>
<td>- 4 least significant bits of HOU1.3:HOU1.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>The third bit of HOU10.2 indicates AM/PM</td>
</tr>
<tr>
<td>DAY1</td>
<td>- Units of day number</td>
<td>- 4 least significant bits of DAY1.3:DAY1.0</td>
</tr>
<tr>
<td>DAY10</td>
<td>- Decines of day number</td>
<td>- 2 least significant bits of DAY10.1:DAY10.0</td>
</tr>
<tr>
<td>MON1</td>
<td>- Units of month</td>
<td>- 4 least significant bits of MON1.3:MON1.0</td>
</tr>
<tr>
<td>MON10</td>
<td>- Decines of month</td>
<td>- 1 least significant bit of MON10.0</td>
</tr>
<tr>
<td>YEA1</td>
<td>- Units of year</td>
<td>- 4 least significant bits of YEA1.3:YEA1.0</td>
</tr>
<tr>
<td>YEA10</td>
<td>- Decines of year</td>
<td>- 4 least significant bits of YEA10.3:YEA10.0</td>
</tr>
<tr>
<td>WEE</td>
<td>- Day of the week</td>
<td>- 3 least significant bits of WEE.2:WEE.0</td>
</tr>
</tbody>
</table>

For this last register the three least significant bits mean:

<table>
<thead>
<tr>
<th>WEE.2</th>
<th>WEE.1</th>
<th>WEE.0</th>
<th>Day of the week</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Sunday</td>
</tr>
</tbody>
</table>
The meaning of the three control registers is:

**REG D = NU NU NU NU 30S IF B H**

where:
- **NU** = Not used.
- **30S** = If high (1) it allows a 30 seconds correction of the time. Once set the RTC seconds are reset and the minutes increased, if the previous seconds was equal or greater than 30.
- **IF** = It manages the RTC interrupt status. When read it shows the current interrupt status (1 active and vice versa), when reset to 0 it disables the RTC interrupt signal if the interrupt mode is selected.
- **B** = Indicates whether R/W operations can be performed on the registers:
  - 1 -> operations are not permitted and vice versa.
- **H** = If high (1) it stores the written time and date.

**REG E = NU NU NU NU T1 T0 I M**

where:
- **NU** = Not used.
- **T1** T0 = Determines the duration of the internal counters interrupt cycle.
  - 0 0 -> 1/64 second
  - 0 1 -> 1 second
  - 1 0 -> 1 minute
  - 1 1 -> 1 hour
- **I** = It defines the interrupt operating mode:
  - 1 -> it selects interrupt mode: when the selected duration elapses the interrupt is enabled and then disabled only with a reset of bit IF of control register D;
  - 0 -> it selects the standard mode: when the selected duration elapses the interrupt is enabled and then disabled only after 7.8 msec.
- **M** = It masks the interrupt status:
  - 1 -> interrupt masked: the RTC interrupt signal is always disabled;
  - 0 -> interrupt not masked: the RTC interrupt signal reflects interrupt status.

**REG F = NU NU NU NU T 24/12 S R**

where:
- **NU** = Not used.
- **T** = It determines from which internal counter to take the counting signal:
  - 1 -> main counter (fast counter for test);
  - 0 -> 15th counter.
- **24/12** = It determines the hours counting mode:
  - 1 -> 0-23;
  - 0 -> 1-12 with AM/PM.
S = If high (1) it stops the clock time counting until the next enabling (0).
R = If high (1) it resets all the internal counters.

After a reset or a power on occur, the RTC is not reinitialized, in order to warrant the conservation of its content, after such events, through the back up circuitry.

**PPI 82C55**

This external peripheral device is managed through 4 registers: one status register (CNT) and three data registers (PDA, PDB, PDC). The data registers are available both for input operation (to obtain signal status) and for output operation (to set signal status) with the correspondence described in figure 34. The PPI 82C55 can work in three different modes:

MODE 0 = it provides two 8 bits bidirectional ports (A, B) and two 4 bits bidirectional ports (C LOW, C HIGH); output signals are latched and input signals are not latched; no handshake signals are provided.

MODE 1 = it provides two 12 bits ports (A+C LOW and B+C HIGH) where ports A and B are used as 8 I/O lines and port C are used as 4 handshake lines. Both inputs and outputs are latched.

MODE 2 = it provides a 13 bits port (A+C ÷ 7) where port A is used as 8 I/O lines and the 5 bits of port C are used as handshake, and a 11 bits port (B+C0 ÷ 2) where port B is used as 8 I/O lines and the 3 bits of port C are used as handshakes. Both inputs and outputs are latched.

The device is programmed writing an 8 bits word in the status register CNT, with the following bits meaning:

\[
CNT = SF \ M1 \ M2 \ A \ CH \ M3 \ B \ CL
\]

where:
SF = mode Set Flag: if activated (1) the device is enabled for standard I/O operation
M1 M2 = mode selection:
0 0 = mode 0
0 1 = mode 1
1 X = mode 2
A = port A direction: 1=input; 0=output
CH = port C HIGH direction: 1=input; 0=output
M3 = mode selection: 1=mode 1; 0=mode 0
B = port B direction: 1=input; 0=output
CL = port C LOW direction: 1=input; 0=output

After Reset or power on PPI 82C55 is programmed in mode 0 with all three ports in input; in this way any connection of PPI 82C55 signals can be used without conflict problems.

**CPU INTERNAL DEVICES**

For further informations about CPU internal devices please refer to technical documentation on appendix B of this manual.
EXTERNAL CARDS

GPC® 150 can be connected to a wide range of block modules and operator interface system produced by grifo®, or to many system of other companies. The on board resources can be expanded with a simple connection to the numerous peripheral grifo® boards, both intelligent and not, thanks to its standard ABACO® BUS connector. Even cards with ABACO® I/O BUS can be connected, by using the proper mother boards.

Hereunder some of these cards are briefly described; ask the detailed information directly to grifo®, if required.

**KDL X24 - KDF 224**
Keyboard Display LCD 2,4 rows 24 keys
Interface with Fluorescent or LCD display. LEDs backlit, 20x2 or 20x4 characters; up to 24 keys matrix keyboard connector. It is directly driven by a 20 pins ABACO® I/O standard connector; High level languages supported; standard pinout for telephone keyboard.

**QTP 24 - QTP 24P**
Quick Terminal Panel 24 keys with Parallel interface
Intelligent user panel equipped with Fluorescent or LCD display, LEDs backlit, 20x2 or 20x4 characters; RS 232, RS 422, RS 485 or current loop serial line; serial E2 for set up and message. Possibility of re-naming keys, LEDs and panel name by inserting label with new name into the proper slot; 24 Keys and 16 LEDs with blinking attribute and buzzer manageable by software; built in power supply; RTC option, reader of magnetic badge and relay. The QTP 24P is low cost no intelligent (passive) version. It is directly driven from 16 TTL I/O lines; high level languages supported.

**QTP G28**
Quick Terminal Panel - LCD Graphic, 28 keys
LCD display 240x128 pixels, CFC backlit; Optocoupled RS 232 line and additional RS 232/422/485/ C. L. line; CAN line controller; E2 for set up; RTC and RAM lithium backed; primary graphic object; possibility of re-naming keys, LEDs and panel name; 28 keys and 16 LEDs with blinking attribute and buzzer manageable by software; Buzzer; built-in power supply; reader of magnetic badge and relay option.

**ABB 03**
ABACO® Block BUS 3 slots
3 slots ABACO® mother board; 4 TE pitch connectors; ABACO® I/O BUS connector; screw terminal for power supply; connection for DIN C type and Ω rails.

**ABB 05**
ABACO® Block BUS 5 slots
5 slots ABACO® mother board with power supply. Double power supply built in; 5Vdc 2,5A section for powering the on board logic; second section at 24Vdc 400mA galvanically coupled, for the optocoupled input lines. Auxiliary connector for ABACO® I/O BUS. Connection for DIN Ω rails.

**MCI 64**
Memory Cards Interfaces 64 MBytes
Interfacing card for managing 68 pins PCMCIA memory cards, it is directly driven from any ABACO® I/O standard connector; High level languages GDOS supported.
FIGURE 40: POSSIBLE CONECTIONS DIAGRAM

- **ANY I/O TYPE**
  - CI/O R16
  - RKD LT
  - LAD 15
  - IPC 52

- **ANY MOTHER BOARD TYPE WITH ABACO® BUS**

- **EXTERNAL LITHIUM BATTERY 3.6 V for Back up**

- **CURRENT to VOLTAGE CONVERTER with 8 A-V modules**

- **12 Bits+Sign Analog voltage inputs:**
  - 0–2.490 V, 0–5.000 V
  - 0–20 mA, 4–20 mA

- **FBC 116 NCS 01**

- **RS 232, RS 422, RS 485, current loop serial lines**

- **ANY CPU TYPE**
  - GPC® 552
  - GPC® 15R
  - etc.

- **DIGITAL I/O INTERFACES:**
  - QTP xxP
  - PRINTER
  - MEMORY CARD

- **40 DIGITAL TTL I/O LINES**
  - Direct to XBI 01, OBI 01, RBO 08, etc...
  - OPTO RELAY
  - TRANSISTOR COUPLED

- **POWER SUPPLY**
  - +5Vdc ONLY

- **PC or Macintosh**

- **PLC**

- **ANY MOTHER BOARD TYPE WITH ABACO® BUS**

- **MEMORY CARD QTP xxP**

- **DIGITAL I/O INTERFACES:**
  - CURRENT to VOLTAGE CONVERTER with 8 A-V modules

- **EXTRA LITHIUM BATTERY 3.6 V for Back up**

- **2 COUNTERS or 2 TIMERS**

- **12 Bits+Sign Analog voltage inputs:**
  - 0–2.490 V, 0–5.000 V
  - 0–20 mA, 4–20 mA
IAC 01
Interface Adapter Centronics
Interface between ABACO® standard I/O 20 pins connector and D 25 pins connector with Centronics standard pin out.

IBC 01
Interface Block Communication
Conversion card for serial communication, 2 RS 232 lines; 1 RS 422–485 line; 1 optical fibre line; selectable DTE/DCE interface; quick connection for DIN 46277-1 and 3 rails.

OBI N8 - OBI P8
Opto BLOCK Input NPN-PNP
Interface between 8 NPN, PNP optocoupled and displayed input lines, with screw terminal and ABACO® standard I/O 20 pins connector; power supply section; connection for DIN Ω rails.

TBO 01 - TBO 08
Transistor BLOCK Output
Interface for ABACO® standard I/O 20 pins connector; 16 or 8 transistor output lines 45 Vdc 3 A open collector; screw terminal; optocoupled and displayed lines; connection for DIN 247277-1 and 3 rails.

RBO 08 - RBO 16
Relé BLOCK Output
Interface for ABACO® standard I/O 20 pins connector; 8 or 16 displayed Relays 3A with MOV; screw terminal; connection for DIN Ctype and Ω rails.

FBC 20 - FBC 120
Flat Block Contact 20 vie
Interfaccia tra 2 o 1 connettori a perforazione di isolante (scatolino da 20 vie maschi) e la filatura da campo (morsettiere a rapida estrazione). Attacco rapido per guide tipo DIN 46277-1 e 3.

DEB 01
Didactic Experimental Board
Supporting card for 16 TTL I/O lines use. It includes: 16 keys, 16 LEDs, 4 digits, 16 keys matrix keyboard, Centronics printer interface, LCD display and fluorescent display interface, GPC® 68 I/O connector, field connection with screw terminal.

IAL 42
Interface Adapter LCD
Interface between 16 I/O TTL available on I/O ABACO® standard connector and 14 pins lowprofile male connector featuring standard pin-out for fluorescent LCD displays management.

XBI 01
miXed BLOCK Input Output
Interface for ABACO® standard I/O 20 pins connector; 8 transistor output lines 45 Vdc 3A; 8 input lines; screw terminal; optocoupled and displayed I/O lines; connection for DIN 247277-1 and 3 rails.
XBI R4 - XBI T4
miXed BLOCK Input-Output
Interface for ABACO® standard I/O 20 pins connector; 4 Relays 3A with MOV or 4 optocoupled Transistors 3A open collectors; 4 input lines optocoupled; screw terminal; connection for DIN C type and Ω rails.

CI/O R16
16 Coupled Input Output with relays
16 optocoupled inputs with low frequency filter; standard rate +24 Vdc input voltage; 16 microrelays 1 A output lines; 24 Vac noise suppressor, type MOV; I/O displayed through LEDs.

IPC 52
Intelligent Peripheral Controller, 24 analogic input
This intelligent peripheral card acquires 24 independent analogic input lines: 8 PT 100 or PT 1000 sensors, 8 J, K, S, T thermocouples, 8 analog input ±2Vdc or 4÷20mA; 16 bits + sign A/D section; 0.1 °C resolution; 32K RAM for local data logging; buzzer; 16 TTL I/O lines; 5 or 8 conversion per second; facility of networking up to 127 IPC 52 cards using serial line. BUS interfacing or through RS 232, RS 422, RS 485 or current loop line. Only 5Vdc power supply.

DAC 16
Digital to Analog Converter 16 bits
2 Digital to Analog converter, 16 bits galvanically insulated; programmed data displayed; ± 10 Vdc output; gain and offset setting; 8 bit Bus; standard addressing.

RKD LT
Remote Keyboard Display controller
Video terminal able to manage many different graphic LCD or alphanumeric fluorescent LCD or displays; matrix keyboard input; BUS or serial interfacing; 1 RS 232 line; additional RS 232, RS 422-485 or Current Loop line; serial EEPROM for set-up; primary graphic object; LEDs driving; Buzzer.

UCC A2
UART Communication Cards, 2 lines
2 Independent RS 232, RS 422, RS 485 or Current Loop lines. Each line: 3 characters buffer; Asynchronous communication from 50 to 115K baud. Parity, bit stop and data length is software programmable.

PCI 01
Peripheral Coupled 32 Inputs
32 optocoupled input lines displayed through LEDs with Pi-Greek filter; standard rate 24 Vdc input voltage; 8/16 bits Bus extended addressing.

JMS 34
Jumbo Multifunction Support for Axis control
Generic peripheral axis control card. 3 optocoupled acquisition channels, with 16 bits bidirectional counter, for incremental encoder. 4 12bits ±10Vdc D/A channels. 8 Opto-in; 8 NPN Opto-output 40Vdc 500 mA. All I/O lines displayed with LEDs.
BIBLIOGRAPHY

Here follows a list of manuals that can be a source of further information about the devices installed on GPC® 150.

TEXAS INSTRUMENTS Manual: The TTL Data Book - SN54/74 Families
TEXAS INSTRUMENTS Manual: RS-422 and RS-485 Interface Circuits
HEWLETT PACKARD Manual: Optoelectronics Designer’s Catalog
NEC Manual: Microprocessors and Peripherals - Volume 3
NEC Manual: Memory Products
AMD Manual: Flash Memory Products
MAXIM Manual: New Releases Data Book - Volume IV
XICOR Manual: Data Book
NATIONAL SEMICONDUCTOR Manual: LM12458 12-Bit + Sign Data Acquisition System
SEIKO EPSON Data Sheet: RTC-62421 Real Time Clock module
ATMEL Manual: Serial Data FLASH

Please connect to the manufactures Web sites to get the latest version of all manuals and data sheets.
APPENDIX A: ELECTRIC DIAGRAMS

This chapter shows the electric diagram of the most frequently used interfaces for GPC® 150. Every one of these interfaces can be made by the User in autonomy, while only few of them are grifo® standard boards and can be ordered.

**Figure A1: IAC 01 Electric Diagram**
Figure A2: KD X x24 Electric Diagram

<table>
<thead>
<tr>
<th>Title: KDL/F-2/424</th>
<th>grifo®</th>
<th>Date: 22-07-1998</th>
<th>Rel. 1.2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Page: 1 of 1</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

External Keyboard 4x6

LCD20x2 LCD20x4 Futaba VFD
R1= 10 Ω N.M. N.M.
R2= 10 Ω N.M. N.M.
R3= 10 Ω N.M. N.M.
R4= 10 Ω N.M. N.M.
R5= 10 Ω N.M. N.M.
R6= 10 Ω N.M. N.M.
R7= 10 Ω N.M. N.M.
R8= 10 Ω N.M. N.M.
R9= 10 Ω N.M. N.M.
R10= 22 KΩ 9+1 SIP
R11= 22 KΩ 9+1 SIP
R12= 10 KΩ trimmer
C1= 100 nF
C2= 22 nF 63V Tantalium
C3= 100 nF
C4= 22 nF 63V Tantalium
CN1= 2 pins mini male connector
CN2= 10 pins male strip
CN3= 20 pins male low profile connector
CN4= LCD L214 (20x4)
CN5= Futaba VFD20x2
CN6= LCD L2012 (20x2)
IC1= 7407
J1= 2 pins female jumper
FIGURE A3: QTP 16P ELECTRIC DIAGRAM

Title: QTP 16P
Date: 22-07-1998
Rel. 1.2
Page: 1 of 1

GPC® 150 Rel. 5.00
Figure A4: QTP 24P Electric Diagram - Part 1
FIGURE A5: QTP 24P ELECTRIC DIAGRAM - PART 2
APPENDIX B: ON BOARD COMPONENTS DESCRIPTION

CPU Z84C15

FEATURES

- Z84C00 Z80 CPU with Z84C30 CTC, Z84C4X SIO, CGC, Watch Dog Timer (WDT). In addition, Z84C15 and Z84015 have Z84C20 PIO.
- High speed operation 6, 10 MHz
- 16 MHz operation for Z84C15 only.
- Low power consumption in four operation modes:
  - 41 mA Typ. (Run mode)
  - 6 mA Typ. (Idle1 mode)
  - 50 μA Typ. (Idle2 mode)
  - 0.6 μA Typ. (Stop mode)
- Wide operational voltage range (5V ± 10%)
- TTL/CMOS compatible.
- Z84013 features:
  - Z84C00 Z80 CPU
  - On-chip two channel SIO (Z80 SIO)
  - On-chip four channel Counter Timer Controller (Z80 CTC)
  - Built-in Clock Generator Controller (CGC).
- Z84C15 features:
  - Built-in Watch Dog Timer (WDT).
  - Noise filter to CLX/TRG inputs of the CTC.
  - 84-pin PLCC package.

Z84C15 enhancements to Z84013/Z84015:

- Power-on reset.
- Addition of two chip select pins.
- 32-bit CRC for Channel A of SIO.
- Wait state generator.
- Simplified EV mode selection.
- Schmitt-trigger inputs to transmit and receive clocks of the SIO.
- Crystal divide-by-one mode.
- 100-pin QFP (Z84C15 only)

GENERAL DESCRIPTION

The Intelligent Peripheral Controller (IPC) is a series of highly superintegrated devices with four versions. The Z84C13 and the Z84C15 are upward compatible versions of the Z84013 and the Z84015. The Z84015 is a CMOS 8-bit microprocessor integrated with the CTC, SIO, CGC, WDT and the PIO into a single 100-pin Quad Flat Pack (QFP) package. The Z84013 is the Z84015 without PIO, and is housed in a 84-pin PLCC package. The Z84C13 is the Z84013 with enhancements and the Z84C15 is the Z84015 with enhancements. These high-end superintegrated intelligent peripheral controllers are targeted for a broad range of applications ranging from error correcting modems to enhancement/cost reductions of existing hardware using Z80-based discrete peripherals. Figures 1 and 2 show the difference between the Z84013/015 and the Z84013/015.

Hereinafter, use the word IPC on the description covering all versions (Z84C13/Z84C15 and Z84013/Z84015). Use Z84C13/C15 on the description that applies only to the Z84C13 and Z84C15, and use Z84013/015 on the description that applies only to the Z84013 and Z84015.
CPU SIGNALS

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Input/Output, 3-State</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>AD0-A15</td>
<td>16-1(x13), 6-1, 100-91(x15)</td>
<td>I/O</td>
<td>16-bit address bus. Specifies I/O and memory addresses to be accessed. During the refresh period, addresses for refreshing are output. The bus is an input when the external master is accessing the on-chip peripherals.</td>
</tr>
<tr>
<td>DO D7</td>
<td>63-76(x13), 88-92(x15)</td>
<td>I/O</td>
<td>8-bit tri-directional data bus. When the on-chip CPU is accessing on-chip peripherals, these lines are set to output and hold the data to/from on-chip peripherals.</td>
</tr>
<tr>
<td>JR D3</td>
<td>30(x13), 14(x15)</td>
<td>I/O</td>
<td>Read signal. CPU read signal for accessing data from memory or I/O devices. When an external master is accessing the on-chip peripherals, it is an input signal.</td>
</tr>
<tr>
<td>WR D1</td>
<td>20(x13), 13(x15)</td>
<td>I/O</td>
<td>Write Signal. This signal is output when data, to be stored in a specified memory or peripheral LSI, is on the MPU data bus. When an external master is accessing the on-chip peripherals, it is an input signal.</td>
</tr>
<tr>
<td>MREQ D2</td>
<td>23(x13), 17(x15)</td>
<td>I/O, 3-State</td>
<td>Memory request signal. When an effective address for memory access is on the address bus, “0” is output. When an external master is accessing the on-chip peripherals, it is an input signal.</td>
</tr>
<tr>
<td>IORQ D4</td>
<td>21(x13), 15(x15)</td>
<td>I/O</td>
<td>I/O request signal. When addresses for I/O are on the lower 8 bits (A7-A0) of the address bus in the I/O operation, “0” is output. In addition, the IORQ signal is output with the M1 signal at the time of interrupt acknowledgement cycle to inform peripheral LSI of the start of the interrupt response vector when put on the data bus. When an external master is accessing the on-chip peripherals, it is an input signal.</td>
</tr>
<tr>
<td>M1 D7</td>
<td>17(x13), 8(x15)</td>
<td>I/O</td>
<td>Machine cycle “1”. MREQ and “0” are output together in the operation code fetch cycle. M1 is output for every opcode fetch when a two-byte opcode is executed. In the maskable interrupt acknowledge cycle, this signal is output together with IORQ. It is 3-stated in EV mode.</td>
</tr>
</tbody>
</table>

PIN DEFINITIONS

The pin assignment for each device is shown in Figures 3 and 4. Following is the description on each pin. For the description and the pin number, it stated as "x13" or "x15", that applies to both Z84C131/Z84C151 or Z84C15/Z84D15. Otherwise, Q13 for Z84C13, Q15 for Z84D15, Q13 for Z84D13 and Q15 for Z84D15.

Figure 4. Z84015/Z84C15 Pin-out Assignments
### CPU SIGNALS (Continued)

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Input/Output, State</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>RFSH</td>
<td>26(x13), 7(x15)</td>
<td>Out, 3-State</td>
<td>The reflush signal. When the dynamic memory refresh address is on the lower order byte of the address bus, RFSH is active along with NREQ signal. This pin is 3-state in BY mode.</td>
</tr>
<tr>
<td>INT</td>
<td>25(x13), 18(x15)</td>
<td>Open drain</td>
<td>Maskable interrupt request signal. Interrupt is generated by peripheral LSI. The signal is accepted if the interrupt enable flag (IF) is set to &quot;1&quot;. The INT signal of on-chip peripheral is internally wired OR without pull-up resistors and requires external pull-up. Also, interrupts from on-chip peripherals go out from this pin.</td>
</tr>
<tr>
<td>INMI</td>
<td>56(x13), 60(x15)</td>
<td>In</td>
<td>Non-maskable interrupt request signal. This interrupt request has a higher priority than the maskable interrupt request and does not rely upon the state of the interrupt enable flag (IF).</td>
</tr>
<tr>
<td>HALT</td>
<td>31(x13), 81(x15)</td>
<td>Out, 3-State</td>
<td>Hold signal. Indicates that the CPU has executed a HALT instruction. This signal is 3-state in EM mode.</td>
</tr>
<tr>
<td>BUSREQ</td>
<td>18(x13), 120(x15)</td>
<td>In</td>
<td>BUS request signal. BUSREQ requests placement of the address bus, data bus, NREQ, JOP, JRD and WR signals into the high impedance state. BUSREQ is normally wired OR and a pull-up resistor is externally connected.</td>
</tr>
<tr>
<td>BUSACK</td>
<td>20(x13), 12(x15)</td>
<td>Out (D130/C16), Out/3-State (C19/C16)</td>
<td>Bus Acknowledge signal. In response to BUSREQ signal. BUSACK signals the address bus, data bus, NREQ, JOP, JRD and WR signals have been placed in the high impedance state.</td>
</tr>
</tbody>
</table>

Note: For the Z84C130, the BUSACK signal will be 3-state during BY mode. For the Z84C130C15 the BUSACK will be 3-state during BY mode.

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Input/Output, State</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>ATRF</td>
<td>55(x13), 70(x15)</td>
<td>Out</td>
<td>1-bit auxiliary address bus Output is the same as bus A7 (AT) of the address bus. However, during a refresh cycle, this pin outputs the address which is the most significant bit of the 8-bit refresh address signal linked to the lower order 7 bits of the address bus.</td>
</tr>
</tbody>
</table>

### CTC SIGNALS

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Input/Output, State</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLKT/RE6 - CLKT/RE23</td>
<td>75-77(x13), 81-83(x15)</td>
<td>In</td>
<td>External clock trigger input. These four CLK/RE pins correspond to four Counter/Timer Channels. In the counter modes, each active edge will cause the down-counter to decrement by one. In timer mode, an active edge will start the timer. It is programmable whether the active edge is rising or falling.</td>
</tr>
<tr>
<td>ZC/TOO - ZC/TO3</td>
<td>69-71(x13), 74-77(x15)</td>
<td>Out</td>
<td>Zero counter output signal. In either timer or counter mode, pulses are output when the down-counter has reached zero.</td>
</tr>
</tbody>
</table>

### SIO SIGNALS

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Input/Output, State</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>M/RDYA, M/RD YB</td>
<td>32, 34(x13), 32, 52(x15)</td>
<td>Out</td>
<td>Wait/Ready signal A and Wait/Ready signal B. Used as WAIT or READY depending upon SIO programming. When programmed as WAIT they go active at &quot;1&quot;, alerting the CPU that addressed memory or I/O devices are not ready by requesting the CPU to wait. When programmed as READY, they are active at &quot;0&quot; which determines when a peripheral device associated with a DMA pin is ready to receive data.</td>
</tr>
<tr>
<td>SYNCA, SYNCH</td>
<td>20, 23(x13), 31, 34(x15)</td>
<td>I/O</td>
<td>Synchronous signals in asynchronous receive mode, they act as ACS and JSC. In external sync mode, these signals act as inputs. In internal sync mode, they act as outputs.</td>
</tr>
<tr>
<td>RXA, RXD</td>
<td>34, 52(x13), 32, 52(x15)</td>
<td>In</td>
<td>Serial receive data signal</td>
</tr>
</tbody>
</table>
### SIO SIGNALS (Continued)

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Input/Output, 3-State</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>/RXCA, /RXCB</td>
<td>35.51(x13), 33.49(x15)</td>
<td>In</td>
<td>Receive clock signal. In the asynchronous mode, the receive clocks can be 1, 16, 32, or 64 times the data transfer rate.</td>
</tr>
<tr>
<td>/TXCA, /TXCB</td>
<td>35.50(x13), 34.48(x15)</td>
<td>In</td>
<td>Transmitter clock signal. In the asynchronous mode, the transmitter clock can be 1, 16, 32, or 64 times the data transfer rate.</td>
</tr>
<tr>
<td>TDA, TDB</td>
<td>37.49(x13), 37.47(x15)</td>
<td>Out</td>
<td>Serial transmit data signal.</td>
</tr>
<tr>
<td>OLEDRA, ODLRB</td>
<td>38.48(x13), 38.46(x15)</td>
<td>Out</td>
<td>Data terminal ready signal. When ready, these signals go active to enable the terminal transmitter. When not ready, they go inactive to disable the transfer from the terminal.</td>
</tr>
<tr>
<td>JITSA, JITSB</td>
<td>39.47(x13), 37.45(x15)</td>
<td>Out</td>
<td>Request to send signal. &quot;0&quot; when transmitting serial data. They are active when enabling the receivers to transmit data.</td>
</tr>
<tr>
<td>JITSA, JITSB</td>
<td>40.46(x13), 38.44(x15)</td>
<td>In</td>
<td>Clear to send signal. When &quot;0&quot;, after transmitting these signals the modem is ready to receive serial data. When ready, these signals go active to enable terminal transmitter. When not ready, these signals go inactive to disable transfer from the terminal.</td>
</tr>
<tr>
<td>LDCDA, LCDDB</td>
<td>41.46(x13), 38.43(x15)</td>
<td>In</td>
<td>Data carrier detect signal. When &quot;0&quot;, serial data can be received. These signals are active to enable receivers to transmit.</td>
</tr>
</tbody>
</table>

### SYSTEM CONTROL SIGNALS

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Input/Output, 3-State</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>EI</td>
<td>60(x13), 71(x15)</td>
<td>In</td>
<td>Interrupt enable input signal. EI is used with the IEC to form a priority daisy chain when there is more than one interrupt driven peripheral.</td>
</tr>
<tr>
<td>IEO</td>
<td>69(x13), 70(x15)</td>
<td>Out</td>
<td>The interrupt enable output signal in the daisy chain interrupt control. IEO controls the interrupt of external peripherals. IEO is active when IBI is &quot;1&quot; and the CPU is not servicing an interrupt from the on-chip peripherals.</td>
</tr>
<tr>
<td>XCS0 (C13/15 only)</td>
<td>42(x13), 40(x15)</td>
<td>Out</td>
<td>Chip Select 0. Used to access external memory or I/O devices. This pin has been assigned to &quot;CS&quot; pin on Z8401/03/05. The signal is decoded only from A15-A12 without control signals. Refer to &quot;Functional Description&quot; on-chip select signals for further explanation.</td>
</tr>
</tbody>
</table>

### SYSTEM CONTROL SIGNALS (Continued)

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Input/Output, 3-State</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>ASEL</td>
<td>40(x13), 40(x15)</td>
<td>Out</td>
<td>Chip Select 1. Used to access external memory or I/O devices. This pin has been assigned to A06 on Z8401/03/05. The signal is decoded only from A15-A12 without control signals. Refer to &quot;Functional Description&quot; on-chip select signals for further explanation.</td>
</tr>
<tr>
<td>WOTOUT</td>
<td>61(x13), 73(x15)</td>
<td>Out</td>
<td>Watch Dog Timer Output signal. Output pulse width depends on the externally connected pin.</td>
</tr>
<tr>
<td>RESET</td>
<td>29(x13), 9(x15)</td>
<td>Input</td>
<td>Input[12/15], I/O (Open Drain) [13/15]. Reset signal. RESET signal is used for initializing MPU and other devices in the system. Also used to return from the standby state in the STOP or IDLE modes.</td>
</tr>
</tbody>
</table>

Note: For the Z80A/12, Z80A/15, the RESET must be kept in active state for a period of at least three system clock cycles.
SYSTEM CONTROL SIGNALS (Continued)

**Note:** For the Z8413/15, to access on-chip resources from the CPU (e.g., I/O CPU, the CPU is electrically disconnected. A15-A0, I/M/R, Z/O, IN and I/O are charged to input. 07-Os charged to direction. All I/O not and IN/O are put into high impedance mode when the EV pin is set to "1", and BUSACK is 1 state. For details, please refer to "Functional Description" on EV mode.

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Input/Output, 3-State</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>ICT</td>
<td>42(013), 40(015), Not with 13/15</td>
<td>Out</td>
<td>Test pins. Used in the open state.</td>
</tr>
<tr>
<td>NC</td>
<td>24, 27, 67, 69(013), flat w/ x15</td>
<td>Not connected.</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>43, 84(013), 41, 90(015)</td>
<td>Power Supply</td>
<td>+5 Volts</td>
</tr>
<tr>
<td>VSS</td>
<td>22, 60(013), 18, 64(015)</td>
<td>Power Supply</td>
<td>0 Volts</td>
</tr>
</tbody>
</table>

**PIO SIGNALS** (for the Z84x15 only)

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Input/Output, 5-State</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>/ASTB</td>
<td>1(015)</td>
<td>In</td>
<td>Port A strobe pulse from a peripheral device. The signal is used each handshake between Port A and external circuits. The meaning of this signal depends on the mode of operation selected for Port A (see &quot;PIO Basic Timing&quot;).</td>
</tr>
<tr>
<td>/STB</td>
<td>81(015)</td>
<td>In</td>
<td>Port B strobe pulse from a peripheral device. The signal is used each handshake between Port B and external circuits. The meaning of this signal is the same as /ASTB except when Port A is in mode 2 (see &quot;PIO Basic Timing&quot;).</td>
</tr>
<tr>
<td>ARDY</td>
<td>20(015)</td>
<td>Out</td>
<td>Register A ready signal. Used as the handshake between Port A and external circuits. The meaning of this signal depends on the mode of operation selected for Port A (see &quot;PIO Basic Timing&quot;).</td>
</tr>
<tr>
<td>BRDY</td>
<td>62(015)</td>
<td>Out</td>
<td>Register B ready signal. Used as the handshake between Port B and external circuits. The meaning of this signal is the same as ARDY except when Port B is in mode 2 (see &quot;PIO Basic Timing&quot;).</td>
</tr>
<tr>
<td>PA7-PA0</td>
<td>22-25(015)</td>
<td>IO, 3-State</td>
<td>Port A data signals. Used for data transfer between Port A and external circuits.</td>
</tr>
<tr>
<td>PB7-PB0</td>
<td>52-55(015)</td>
<td>IO, 3-State</td>
<td>Port B data signals. Used for transfer between Port B and external circuits.</td>
</tr>
</tbody>
</table>

The following pins have different functions between 013/015 and 13/15

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin # X13</th>
<th>Pin # X15</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>RESET</td>
<td>29</td>
<td>9</td>
<td>Functionality is different.</td>
</tr>
<tr>
<td>AWAIT</td>
<td>15</td>
<td>15</td>
<td>Functionality is different.</td>
</tr>
<tr>
<td>SV</td>
<td>55</td>
<td>57</td>
<td>Functionality is different.</td>
</tr>
<tr>
<td>MDOUT</td>
<td>61</td>
<td>75</td>
<td>Push-pull output on Z8413/15. Open drain on Z84 C13/15</td>
</tr>
<tr>
<td>ICT</td>
<td>45, 46</td>
<td>45, 46</td>
<td>(Test pin) on Z8413/15.</td>
</tr>
<tr>
<td>TxCA, TxCB, RxQA and RxQB</td>
<td>30, 36, 50, 51</td>
<td>33, 34, 48, 49</td>
<td>On Z8413/15, these signals have Schmitt-triggered inputs</td>
</tr>
<tr>
<td>/ASTB</td>
<td>29</td>
<td>12</td>
<td>In EV mode, 3-state on Z8413/15.</td>
</tr>
</tbody>
</table>

FUNCTIONAL DESCRIPTION

Figure 5(a) shows the functional block diagram of the Z8413/15 (and Figure 5(b) shows the functional block diagram of the Z8413C15). As described earlier, the only difference between the Z8413 and the Z8415 is the PIO not being available on the Z8413.

Functionally, the only difference is that the Z8413, Z84C13, and Z84015 CPU are configured as the data transfer interface to the port that indicates when data transfer has occurred. Each of these ports can be programmed to interrupt the CPU upon the occurrence of specified status conditions, and generate unique interrupt vectors when the CPU responds to the ports. For more information on the operation of this portion of the logic, please refer to the Z8413/015 Product Specification and Technical Manual.

All of the Z8413/015 CPU and its peripheral functions are forward compatible with the Z84C15 and Z84015 CPU functions. These two parts have several modes of operation: input, output, bi-directional, or bit control mode. Each port has two handshake signals (RDY and ATN) which are used to control data transfers. The RDY signal indicates that the port is ready to data transfer and the ATN signal is sent to the port that indicates when data transfer has occurred. Each of these ports can be programmed to interrupt the CPU upon the occurrence of specified status conditions, and generate unique interrupt vectors when the CPU responds to the ports. For more information on the operation of this portion of the logic, please refer to the Z8413/015 Product Specification and Technical Manual.

Z84C30 Counter/Timer Logic Unit

This logic unit provides the user with four individual 8-bit Counter/Timer Channels that are compatible with the Z84C015. The Counter/Timer Channels can be programmed by the CPU for a range of counting and timing applications. The CPU can configure the logic to interface to a wide range of external devices and a CPU through the use of two 8-bit parallel ports (Figure 6). The CPU interfaces to these parallel ports (input/output) through the use of two 8-bit parallel ports. Each channel can generate a unique interrupt vector in response to the interrupt acknowledge cycle.
Figure 6. PIO Block Diagram

Figure 7. CTC Block Diagram

Z84C4x Serial I/O Logic Unit
This logic unit provides the user with high-speed multi-
protocol serial I/O channels that are completely compat-
ible with the Z84C4x SIO. Their basic functions are serial-to-
parallel and parallel-to-serial converters can be pro-
grammed by a CPU for a broad range of serial communi-
cations applications. Each channel, designated Channel A and Channel B, is capable of supporting all common
synchronous and asynchronous protocols (Manchester, Bi-trigger, and SDLC/HDL, byte or bit oriented - Figure 8).
Z84C13C15 Only: As an enhancement to the Z84C13C15, the Z84C13C15 can handle a 32-bit CRC on Channel A
and 8-bit CRC on Channel B. A clock input is also provided on the TJC and JRC pins of both channels.
Watch Dog Timer (WDT) Logic Unit
This logic unit has been superimposed into the IPC. It detects an operation error, caused by the program runaway, and returns to normal operation. Figure 9, shows the block diagram of the WDT. Upon Power-On Reset, the unit is enabled. If WDT is not required, but WDTOUT is connected to RESET or any other circuit, it has to be disabled. During the power-down mode of operation (either IDLE or STOP), the Watch Dog Timer is halted.

WDT Output (WDTOUT pin). When the WDT is used, the "0" level signal is output from the WDTOUT pin after a duration of time specified in the WDTIP or in the WDMR. The output pulse width is one of the following, depending on the WDTOUT pin connection.

- The WDTOUT is connected to the RESET pin. The "0" level is pulled for 512C (System clock cycles).
- The WDTOUT is connected to a pin other than the RESET pin. The "0" level is held until the Watch Dog timer is cleared by software, or by the RESET pin.

CGC Logic Unit. The IPC has CGC (Clock Generator Controller) unit. This unit is identical to the one with the Z84C01 and the Z84CGO, and supports power-down modes of operation. The output from this unit is on the pin called CGOUT, and is connected to the system clock internally. The CLKN pin is the system clock input. The user can connect CGOUT to CLKN to utilize the CGC unit for supply external clock from CLKN pin.

The CGC unit allows crystal input (XTAL1, XTAL2) or External Clock input on the XTAL1 pin. It has clock divide-by-two-by-two circuits and generates a half-speed clock to the input.

Z84019C01S Only. If the system clock is provided on the CLKN pin, none of the power-down mode (except RUN mode) is supported.

Z84C13C15 Only. If the system clock is provided on the CLKN pin, only the IDLE2 mode is applicable. In this mode, if the HALT instruction is executed, the internal clock to the CTC is kept on "Continuous", but the clock to the other components (CPU, IO, SIO, and Watch Dog Timer) are stopped. The divide-by-two circuit of the CGC unit can be stopped by programming bit D4 of the WDTMR (see "Programming" section). Upon Power-On Reset, it comes up in divide-by-two mode.

System Clock Generation
The IPC has a built-in oscillator circuit and the required clock can be easily generated by connecting a crystal to the external terminals (XTAL1, XTAL2). Clock output is the same frequency as half the speed of the crystal frequency. Examples of oscillator connections are shown in Figure 10.
The Wait State Control Register can be programmed to generate multiple Wait states during different CPU cycles as follows:

- Memory Wait and Opcode wall. The Wait State Generator can interrupt 0 to 3 wait states in memory accesses. Additionally, one added wait state can be inserted during an IM (Opcode fetch) cycle, because IM cycle's timing requirement is tighter than memory Read/Write cycles. It generates the selected Wait state in the Memory Access to a specified address range, which is programmed in the Wait State Control Block.

- I/O Wait. The Wait State Generator can insert 0, 1, 2, 4 or 8 wait states in I/O accesses. Regardless of the programming in the field, if no I/O wait states are inserted for accesses to certain peripherals.

- Interrupt Vector Wait. During Interrupt acknowledge cycle, the Wait State Generator can interrupt one wait state after J6Q goes active, to extend the time between J6Q fall to vector fetch by CPU. It allows a slow vector response device.

- Interrupt Daisy Chain Wait and RETI sequence extension. During Interrupt acknowledge cycle, the Wait State Generator can insert 0, 2, 4 or 8 wait states at the end of an external interrupt (except INT0). Otherwise, the RETI pin remains in the active state for a period of at least 3 system clock cycles if there are power-on reset circuits outside of this device, driven with OPEN-COL style pull-up resistors because "RSTI" signal is driven low by the board mentioned above during the Power-on sequence. If the external Power-on reset circuit has pull-up type drivers and they drive the "RESET" pin to "1" during that period, it may cause damage. In particular, when using 284C13C15 in the 28401315 socket, the modification may be required on the external reset circuit.

- Chip Select Signals (Z84C13C15 Only)

  - The 284C13C15 has an enhanced feature of adding two chip select (CS0, CS1) pins. Each chip select signal (CS0, CS1) is driven by 3-state output. The boundary value for each chip select signal is 4-bit wide, and compare with 15:16 of the address. Each Chip Select signal goes active when:

    - CS0 (CSO0 = CS15, CS01 = CS16) is driven high by 3-state output.
    - CS1 (CSO2 = CS17, CS13 = CS18) is driven high by 3-state output.

  - In 28413C15, CS0 and CS1 can be disabled in power-up sequence by the boundary value of "F" cutting CS0 and CS1 go active for all memory accesses.

- Clock Divide-by-one option
- Reset Output Disable
- 32-bit CRC Generator/Cycling

- Clock Divide-by One Option. This feature is programmed through Bit 0 of MCR. Upon Power-On reset, the Clock from on-chip CGC is passed through a divide-by-two circuit. By setting this bit to 1, the divide-by-two circuit is bypassed so the clock on the CLKOUT pin is equal to XTAL input. If the clock is applied to the CLKIN pin from external clock source, the status of this bit is ignored. Upon Power-On reset, it is cleared to 0. For details, please refer to the Programming section.

- Reset Output Disable. This feature is programmed through Bit 0 of MCR. This bit is cleared to 0 when the GIC/IO is placed in power-down mode. Upon Power-On reset, the GIC/IO is placed in power-down mode. Upon Power-On reset, the GIC/IO is placed in power-down mode.
**Table 1. I/O Control Register Address**

<table>
<thead>
<tr>
<th>Address</th>
<th>Device</th>
<th>Channel</th>
<th>Register</th>
</tr>
</thead>
<tbody>
<tr>
<td>1Ch</td>
<td>CTC</td>
<td>Ch 0</td>
<td>Control Register</td>
</tr>
<tr>
<td>11h</td>
<td>CTC</td>
<td>Ch 1</td>
<td>Control Register</td>
</tr>
<tr>
<td>12h</td>
<td>CTC</td>
<td>Ch 2</td>
<td>Control Register</td>
</tr>
<tr>
<td>13h</td>
<td>CTC</td>
<td>Ch 3</td>
<td>Control Register</td>
</tr>
<tr>
<td>14h</td>
<td>SIO</td>
<td>Ch A</td>
<td>Data Register</td>
</tr>
<tr>
<td>15h</td>
<td>SIO</td>
<td>Ch A</td>
<td>Data Register</td>
</tr>
<tr>
<td>16h</td>
<td>SIO</td>
<td>Ch B</td>
<td>Data Register</td>
</tr>
<tr>
<td>1Ch</td>
<td>PIO</td>
<td>Port A</td>
<td>Data Register (Not with Z84x13)</td>
</tr>
<tr>
<td>11h</td>
<td>PIO</td>
<td>Port A</td>
<td>Command Register (Not with Z84x13)</td>
</tr>
<tr>
<td>12h</td>
<td>PIO</td>
<td>Port B</td>
<td>Data Register (Not with Z84x13)</td>
</tr>
<tr>
<td>13h</td>
<td>PIO</td>
<td>Port B</td>
<td>Command Register (Not with Z84x13)</td>
</tr>
<tr>
<td>10h</td>
<td>Watch-Dog Timer</td>
<td>Port A</td>
<td>Master Register (WDT/MR)</td>
</tr>
<tr>
<td>11h</td>
<td>Watch-Dog Timer</td>
<td>Port A</td>
<td>Control Register (WDTCR)</td>
</tr>
<tr>
<td>12h</td>
<td>Watch-Dog Timer</td>
<td>Port B</td>
<td>Command Register (WDTCR) (Not with Z84x13)</td>
</tr>
<tr>
<td>13h</td>
<td>Interrupt Priority Register</td>
<td>Port B</td>
<td>Master Register (WD7/MR)</td>
</tr>
</tbody>
</table>

**PIO Registers**

For more detailed information, please refer to the PIO Technical Manual. These registers are not in the Z84x13.

**Interrupt Vector Word**

The PIO logic unit is designed to work with the Z80 CPU in interrupt mode. The interrupt word must be programmed if interrupts are used. Bit D0 must be a zero (Figure 11).

**Mode Control Word**

Selects the port operating mode. This word is required and is written at any time (Figure 12).

**Figure 12. PIO Mode Control Word**

**I/O Register Control Word**

When Mode 3 is selected, the Mode Control Word is followed by the I/O Register Control Word. This word configures the I/O register, which defines which port lines are inputs or outputs. A '1' indicates input while a '0' indicates output. This word is required when in Mode 3 (Figure 13).

**Figure 13. I/O Register Control Word**

**Interrupt Control Word**

In Mode 3 operation, handshake signals are not used. Interrupts are generated as a logic function of the input signal levels. The Interrupt Control Word sets the logic conditions and the logic levels required for generating an interrupt. Two logic conditions or functions are available: AND (if all input bits change to the active level, an interrupt is triggered), OR (if any one of the input bits change to the active logic level, an interrupt is triggered). The user can program which input bits are to be considered as part of this logic function. Bit D0 sets the logic function, bit D1 sets the logic level, and bit D2 specifies a mask control word to follow (Figure 14).

**Figure 14. Interrupt Control Word**

**Interrupt Disable Word**

This word can be used to enable or disable a port's interrupts without changing the rest of the port's interrupt conditions (Figure 15).
Figure 21. SIO Write Registers

WATCH DOG CONTROL REGISTERS

There are two registers to control Watch Dog Timer operations. These are: Watch Dog Timer Master Register (WDTMR; IO Address F9H) and the WDT Command Register (WDTCR; IO Address F8H). Watch Dog Time Logic has a "double-key" structure to prevent the WDT disabling error, which may lead to the WDT operation to stop due to program runaway. Programming the WDT follows this procedure. Also, these registers program the power-down mode of operation. The "Second key" is needed when turning off the Watch Dog Timer.

Enabling the WDT. The WDT is enabled by setting the WDT Enable bit (B7:WDTEN) to "1" and the WDT Periodic field (DS:DD:WDTP) to the desired time period. These command bits are in the Watch Dog Timer Master Register (WDTMR; IO Address F9H).

Disabling the WDT. The WDT is disabled by clearing WDT Enable bit (WDTEN) in WDTMR to "0" followed by writing "01" to the WDT Command Register (WDTCR; IO Address F8H).
Clearing the WDT. The WDT can be cleared by writing "00" into the WDTCH.

Watch Dog Timer Master Register (WDTMR; I/O address F9H). This register controls the activities of the Watch Dog Timer and selects power-down mode of operation (Figure 22).

Figure 22. Watch Dog Timer Master Register

Bit D7. Watch Dog Timer Enable (WDE). This bit controls the activities of the Watch Dog Timer. The WDE can be enabled by setting the bit to "1" and disabled by writing "0" to this bit. The WDT is disabled if the WDE is set to "0".

Bit D6. Watch Timer Period (WTP). This bit controls the activity of the Watch Timer. The WTP can be set to "1" for a period of 2^11 cycles.

Bit D5. Watch Timer Period (WTP). This bit controls the activity of the Watch Timer. The WTP can be set to "1" for a period of 2^11 cycles.

Bit D4-D0. HALT mode (HALTM). This two-bit field specifies one of a four power-down modes. To change the field, write "DBH" to the WDT command register, followed by a write to the register. For details on how to change the field, please refer to the section "Mode of operations." Upon Power-on Reset, this field is set to "0", which specifies "RUN mode."

00 - IDLE 1 Mode
01 - IDLE 2 Mode
10 - STOP 1 Mode
11 - RUN Mode

Bit D2-D1. Reserved. These two bits are reserved and should always be programmed as "0H". A read to these bits returns "0H".

Watch Dog Timer Command Register (WDTCR; I/O address F8H). In conjunction with the WDTMR, this register works as a "Second key" for the Watch Dog Timer. This register is write-only (Figure 23).

Write 8H after clearing WDE to "0". Disable WDT. Write 4EH - Clear WDT. Write 86H followed by a write to HALTM - Change Power-down mode.

Figure 23. Watch Dog Timer Command Register

Interrupt Priority Register (ITP; I/O address F4H)

This register is write-only and provides the priority for the GTC, SIO, and the PIO (Figure 24).

Bit E7-E0. Reserved. These bits are reserved and should always be programmed as "0H". A read to these bits returns "0H".

Bit D7-D0. Reserved. These bits are reserved and should always be programmed as "0H". A read to these bits returns "0H".

System Control Data Port (SCDP; I/O address F0H)

This register is write-only and provides the priority for the GTC, SIO, and the PIO (Figure 25).

Bit E7-E0. Reserved. These bits are reserved and should always be programmed as "0H". A read to these bits returns "0H".

Figure 24. Interrupt Priority Register

System Control Register Pointer (SCRP; I/O address F1H)

This register stores the pointer to the System Control Register (SCDR; I/O address F0H). The register is read-only and returns the pointer value when read. Upon Power-on Reset, this register is set to "00H" (Figure 26).

Figure 25. System Control Register Pointer

System Control Data Port (SCDP; I/O address F0H)

This register is write-only and provides the priority for the GTC, SIO, and the PIO (Figure 26).

Bit E7-E0. Reserved. These bits are reserved and should always be programmed as "0H". A read to these bits returns "0H".

Figure 26. System Control Data Port

Register for System Configuration

The following registers are not available on 28431/3C/15:

There are four indirectly accessible registers to determine system configuration with the 28431/3C/15. These indirectly accessible registers are: Wait State Control Register (WSC), Memory Wait Boundary Register (MWBR; Control Register 0CH), Memory Wait Boundary Register (MWBR; Control Register 0CH), and Miss Memory Control Register (MMCR; Control Register 0CH). To access these registers, 284313C/15 writes "register number to be accessed" to the System Control Register Pointer (SCRP, I/O address F1H), and then accesses the target register through the System Control Data Port (SCDP; I/O address F0H). The pointer which writes into SCDP is kept until modified.

System Control Register Pointer (SCRP; I/O address F1H)

This register stores the pointer to access System Control Registers (SCDR; I/O address F0H). This register is read-only and returns the pointer value when read. Upon Power-on Reset, all bits are cleared to zero. The pointer value, rather than 00H to 0FH, is reserved and not written. Upon Power-on Reset, this register is set to "00H" (Figure 27).

System Control Data Port (SCDP; I/O address F0H)

This register is write-only and provides the priority for the GTC, SIO, and the PIO (Figure 28).

Bit E7-E0. Reserved. These bits are reserved and should always be programmed as "0H". A read to these bits returns "0H".

Wait State Control Register (WSC, Control Register 0CH)

This register can be accessed through SCDP with the pointer value 00H. It automatically clears the contents of this register (move to non-wait state insertion) on the falling edge of the 18th clock signal unless software has programmed a value. If automatic wait state insertion is enabled, the wait state is programmed within the time period. A read to WSCR during this period will return 00H, unless programmed.
**Figure 27. Wait State Control Register**

This register has the following fields:

- **Interrupt Acknowledge**: This field is set to "11" when an Interrupt acknowledge cycle is received by the CPU. If set to "01" or "10", an 8-bit stall is inserted.
- **Retry Cycle**: This field is set to "11" when the retry cycle is going active.
- **Op Code Wait**: This field is set to "00" when an op code is being received.
- **Wait States**: This field specifies the number of wait states to be inserted during a retry cycle.

For fifteen M1 cycles from Power-on Reset, bits 7-6 are set to "11", then cleared to "00" on the trailing edge of the 16th M1 signal, unless programmed.

**Figure 28. Memory Wait Boundary Register**

This register specifies the upper address boundary for Memory Wait.

**Figure 29. Chip Select Boundary Register**

This register specifies the lower address boundary for Memory Wait.

**Figure 30. Misc Control Register**

This register specifies miscellaneous options for the system.
Table 2. Power-down Modes

<table>
<thead>
<tr>
<th>Operation Mode</th>
<th>WDTMR Bit D4</th>
<th>Bit D3</th>
<th>Description at HALT State</th>
</tr>
</thead>
<tbody>
<tr>
<td>RUN Mode</td>
<td>1</td>
<td>1</td>
<td>The LPC continues the operation and continuously supplies a clock to the outside.</td>
</tr>
<tr>
<td>IDLE1 Mode</td>
<td>0</td>
<td>0</td>
<td>The internal oscillator operation is continued. Clock output (CLKOUT) as well as internal clock to the CPU, PIO, SIO, CTC and the Watch Dog Timer is stopped at &quot;0&quot; level of T4 state in the halt instruction operation code fetch cycle.</td>
</tr>
<tr>
<td>IDLE2 Mode</td>
<td>0</td>
<td>1</td>
<td>The internal oscillator and the CTC operation continues and supplies clock to the outside on the CLKOUT pin continuously. But the internal clock to the CPU, PIO, SIO and the Watch Dog Timer are stopped at &quot;0&quot; level of T4 state in the halt instruction operation code fetch cycle.</td>
</tr>
<tr>
<td>STOP Mode</td>
<td>1</td>
<td>0</td>
<td>All operations of the internal oscillator, clock (CLK) output, internal clock to the CPU, PIO, CTC, SIO and the Watch Dog Timer are stopped at &quot;0&quot; level of T4 state in the halt instruction operation code fetch cycle.</td>
</tr>
</tbody>
</table>

Table 3. Device status in Hold state

<table>
<thead>
<tr>
<th>Mode</th>
<th>CTC</th>
<th>CPU</th>
<th>PIO</th>
<th>SIO</th>
<th>WDT</th>
<th>CLKOUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>IDLE1</td>
<td>0</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>IDLE2</td>
<td>0</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>0</td>
</tr>
<tr>
<td>STOP</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>RUN</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

O: Operating; X: Stop

TIMING

Basic Timing

The basic timing is explained here with emphasis placed on the halt function relative to the clock generator. The following items are identical to those for the 284300. Refer to the data sheet for the 284300.

- Operation code fetch cycle
- Memory Read/Write operation
- Input/Output operation
- Bus request acknowledge operation
- Maskable interrupt request operation
- Non-Maskable interrupt request operation
- Reset Operation

Operation When HALT Instruction is Executed: When the CPU latches a halt instruction in the operation code fetch cycle, HALT goes active (Low) in sync with the falling edge of T4 state before the peripheral LSI and CPU stops the operation. After this, the system clock generator starts depending upon the operation mode (RUN Mode, IDLE Mode or STOP Mode). If the internal system clock is running, the CPU continues to execute NOP instruction even in the halt state.

RUN Mode (HALT = 11). Shown in Figure 31 is the basic timing when the halt instruction is executed in RUN Mode.

Figure 31. Timing of RUN Mode

(at HALT Instruction Command Execution)
LM12454/LM12458/LM12H458
12-Bit + Sign Data Acquisition System with Self-Calibration

General Description

The LM12454, LM12458, and LM12H458 are highly integrated Data Acquisition Systems. Operating on just 5V, they combine a fully-differential self-calibrating (correcting linearity and zero errors) 13-bit (12-bit + sign) analog-to-digital converter (ADC) and sample-and-hold (S/H) with extensive analog functions and digital functionality. Up to 32 consecutive conversions, using two’s complement format, can be stored in an internal 32-word (16-bit wide) FIFO data buffer. An internal 8-word RAM can store the conversion sequence for up to eight acquisitions through the LM12(H)458’s eight-input multiplexer. The LM12454 has a four-channel multiplexer, a differential multiplexer output, and a differential S/H input. The LM12454 and LM12(H)458 can also operate with 8-bit + sign resolution and in a supervisory “watchdog” mode that compares an input signal against two programmable limits.

Programmable acquisition times and conversion rates are possible through the use of internal clock-driven timers. The reference voltage input can be externally generated for absolute or ratiometric operation or can be derived using the internal 2.5V bandgap reference.

All registers, RAM, and FIFO are directly addressable through the high speed microprocessor interface to either an 8-bit or 16-bit databus. The LM12454 and LM12(H)458 include a direct memory access (DMA) interface for high-speed conversion data transfer.

An evaluation/interface board is available. Order number LM12458EVAL.

Additional applications information can be found in applications notes AN-906, AN-947 and AN-949.

Key Specifications

$\left( f_{\text{CLK}} = 5 \text{ MHz}; 8 \text{ MHz}, H \right)$

- Resolution 12-bit + sign or 8-bit + sign
- 13-bit conversion time $8.8 \mu s, 5.5 \mu s (H) \text{ (max)}$
- 9-bit conversion time $4.2 \mu s, 2.6 \mu s (H) \text{ (max)}$
- 13-bit Through-put rate $88k \text{ samples/s (min)}, 140k \text{ samples/s (H) (min)}$
- Comparison time $2.2 \mu s \text{ (max)}, 1.4 \mu s (H) \text{ (max)}$
- ILE $\pm 1 \text{ LSB (max)}$
- $V_{\text{IN}}$ range GND to $V_{A+}$
- Power dissipation $30 \text{ mW, 34 mW (H) (max)}$
- Stand-by mode $50 \mu W \text{ (typ)}$
- Single supply 3V to 5.5V

Features

- Three operating modes: 12-bit + sign, 8-bit + sign, and “watchdog”
- Single-ended or differential inputs
- Built-in Sample-and-Hold and 2.5V bandgap reference
- Instruction RAM and event sequencer
- 8-channel (LM12(H)458), 4-channel (LM12454) multiplexer
- 32-word conversion FIFO
- Programmable acquisition times and conversion rates
- Self-calibration and diagnostic mode
- 8- or 16-bit wide databus dmicroprocessor or DSP interface

Applications

- Data Logging
- Instrumentation
- Process Control
- Energy Management
- Inertial Guidance

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The analog input multiplexer can be configured for any combination of single-ended or fully differential operation. Each input is referenced to ground when a multiplexer channel operates in the single-ended mode. Fully differential analog input channels are formed by pairing any two channels together.

The LM12454's multiplexer outputs and S/H inputs (MUX-in) are designed to operate at its minimum acquisition time (1.13 µs, 12 bits) when the source impedance, $R_s$, is less than 600 Ω and $f_{CLK}$ is 8 MHz. When $R_s < 600$ Ω and $f_{CLK} = 4.17$ kHz, the internal S/H's acquisition time can be increased to a maximum of 4.88 µs (12 bits, $f_{CLK} = 8$ MHz). See Section 2.1 (Instruction RAM "00") Bits 12–15 for more information.

An internal 2.5V bandgap reference output is available at pin 44. This voltage can be used as the ADC reference for ratio-metric conversion or as a virtual ground for front-end analog conditioning circuits. The $V_{REF+}$ and $V_{REF−}$ pins should be bypassed to ground with a 100 µF capacitor.

Microprocessor overhead is reduced through the use of the internal conversion FIFO. Thirty-two consecutive conversions can be completed and stored in the FIFO without any microprocessor intervention. The microprocessor can, at any time, interrogate the FIFO and retrieve its contents. It can also wait for the LM12454 to issue an interrupt when the FIFO is full or after any number (≤32) of conversions have been stored.

Conversion sequencing, internal timer interval, multiplexer configuration, and many other operations are programmed and set in the Instruction RAM. A diagnostic mode is available that allows verification of the LM12454's operation. The diagnostic mode is disabled in the LM12454. This mode internally connects the voltages present at the $V_{IN+}$, $V_{IN−}$, $V_{REF+}$, and GND pins to the internal DAC's $V_{IN+}$ and $V_{IN−}$ S/H inputs. This mode is activated by setting the Diagnostic bit (Bit 11) in the Configuration register to a "1." More information concerning this mode of operation can be found in Section 2.2.

2.0 Internal User-Programmable Registers

INSTRUCTION RAM

The instruction RAM holds up to eight sequentially executable instructions. Each 48-bit long instruction is divided into three 16-bit sections. READ and WRITE operations can be issued to each 16-bit section using the instruction's address and the 2-bit "RAM pointer" in the Configuration register. The eight instructions are located at addresses 0000 through 0111 (A4–A1, BW = 0) when using a 16-bit wide data bus, or at addresses 00000 through 01111 (A4–40, BW = 1) when using an 8-bit wide data bus. They can be accessed and programmed in random order.
2.0 Internal User-Programmable Registers (Continued)

Any Instruction RAM READ or WRITE can affect the sequencer’s operation. The Sequencer should be stopped by setting the RESET bit to a “1” or by resetting the START bit in the Configuration Register and waiting for the instruction to finish execution before any Instruction RAM READ or WRITE is initiated.

A soft RESET should be issued by writing a “1” to the Configuration Register’s RESET bit after any READ or WRITE to the Instruction RAM.

The three sections in the Instruction RAM are selected by the Configuration Register’s 2-bit “RAM Pointer,” bits D8 and D9. The first 16-bit Instruction RAM section is selected with the RAM Pointer equal to “00.” This section provides multiplexer channel selection, as well as resolution, acquisition time, etc. The second 16-bit section holds “watchdog” limit #1, its sign, and an indicator that shows that an interrupt can be generated if the input signal is greater or less than the programmed limit. The third 16-bit section holds “watchdog” limit #2, its sign, and an indicator that shows that an interrupt can be generated if the input signal is greater or less than the programmed limit.

Instruction RAM “00”

Bit 0 is the LOOP bit. It indicates the last instruction to be executed in any instruction sequence when it is set to a “1.” The next instruction to be executed will be instruction 0.

Bit 1 is the PAUSE bit. This controls the Sequencer’s operation. When the PAUSE bit is set (“1”), the Sequencer will stop after reading the current instruction and before executing it, and the start bit in the Configuration register is automatically reset to a “0.” Setting the PAUSE also causes an interrupt to be issued. The Sequencer is restarted by placing a “1” in the Configuration register’s Bit 0 (Start bit).

After the Instruction RAM has been programmed and the RESET bit is set to “1,” the Sequencer retrieves Instruction 000, decodes it, and waits for a “1” to be placed in the Configuration’s START bit. The START bit value of “0” overrides the action of Instruction 000’s PAUSE bit when the Sequencer is started. Once started, the Sequencer executes Instruction 000 and retrieves, decodes, and executes each of the remaining instructions. No PAUSE Interrupt (INT 5) is generated the first time the Sequencer executes Instruction 000 having a PAUSE bit set to “1.” When the Sequencer encounters a LOOP bit or completes all eight instructions, Instruction 000 is reloaded and decoded. A set PAUSE bit in Instruction 000 now halts the Sequencer before the instruction is executed.

Bits 2–4 select which of the eight input channels (‘000’ to ‘111’) for IN0–IN7) will be configured as non-inverting inputs to the LM12454’s D/A converter. (See Page 27, Table 1.) They select which of the four input channels (‘000’ to ‘011’) for IN0–IN4 will be configured as non-inverting inputs to the LM12454’s ADC. (See Page 27, Table 2.)

Bits 5–7 select which of the seven input channels (‘001’ to ‘111’) for IN1–IN7) will be configured as inverting inputs to the LM12454’s D/A converter. (See Page 27, Table 1.) They select which of the three input channels (‘000’ to ‘011’) for IN1–IN4 will be configured as inverting inputs to the LM12454’s ADC. (See Page 27, Table 2.) Fully differential operation is created by selecting two multiplexer channels, one operating in the non-inverting mode and the other operating in the inverting mode. A code of ‘000’ selects ground as the inverting input for single-ended operation.

Bit 8 is the SYNC bit. Setting Bit 8 to “1” causes the Sequencer to suspend operation at the end of the internal S/H’s acquisition cycle and to wait until a rising edge appears at the SYNC pin. When a rising edge appears, the S/H acquires the input signal magnitude and the ADC performs a conversion on the signal next rising edge. When the SYNC pin is used as an input, the Configuration register’s “1/O Select” bit (Bit 7) must be set to a “0.” With SYNC configured as an input, it is possible to synchronize the start of a conversion to an external event. This is useful in applications such as digital signal processing (DSP) where the exact timing of conversions is important.

When the LM12454 are used in the “watchdog” mode with external synchronization, two rising edges on the SYNC input are required to initiate two comparisons. The first rising edge initiates the comparison of the selected analog input signal with Limit #1 (found in Instruction RAM “01”) and the second rising edge initiates the comparison of the same analog input signal with Limit #2 (found in Instruction RAM “10”). Bit 9 is the TIMER bit. When Bit 9 is set to “1,” the Sequencer will halt until the internal 16-bit Timer counts down to zero. During this time interval, no “watchdog” comparisons or analog-to-digital conversions will be performed.

Bit 10 selects the ADC conversion resolution. Setting Bit 10 to “1” selects 8-bit + sign and when reset to “0” selects 12-bit + sign.

Bit 11 is the “watchdog” comparison mode enable bit. When operating in the “watchdog” comparison mode, the selected analog input signal is compared with the programmable values stored in Limit #1 and Limit #2 (see Instruction RAM “01” and “10”). Setting Bit 11 to “1” causes two comparisons of the selected analog input signal with the two stored limits. When Bit 11 is reset to “0,” an 8-bit + sign or 12-bit + sign (depending on the state of Bit 10 of Instruction RAM “00”) conversion of the input signal can take place.

FIGURE 13. LM12454 Memory Map for 16-Bit Wide Databus (BW = “0,” Test Bit = “0” and A0 = Don’t Care)
### 2.0 Internal User-Programmable Registers (Continued)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Purpose</th>
<th>Type</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit 0</td>
<td>Instruction RAM “00”</td>
<td>R/W</td>
<td>Don’t Care</td>
<td>2.0 Internal User-Programmable Registers</td>
<td>Acquire Time</td>
<td>Watchdog</td>
<td>Timer</td>
<td>Sync</td>
<td>Interf</td>
<td>Sign</td>
</tr>
<tr>
<td>Bit 1</td>
<td>Instruction RAM “01”</td>
<td>R/W</td>
<td>Don’t Care</td>
<td>2.0 Internal User-Programmable Registers</td>
<td>Comparison Limit #1</td>
<td>X/X</td>
<td>Sign</td>
<td>Interf</td>
<td>Bit0</td>
<td></td>
</tr>
<tr>
<td>Bit 2</td>
<td>Instruction RAM “10”</td>
<td>R/W</td>
<td>Don’t Care</td>
<td>2.0 Internal User-Programmable Registers</td>
<td>Comparison Limit #2</td>
<td>X/X</td>
<td>Sign</td>
<td>Interf</td>
<td>Bit0</td>
<td></td>
</tr>
<tr>
<td>Bit 3</td>
<td>Instruction RAM “11”</td>
<td>R/W</td>
<td>Don’t Care</td>
<td>2.0 Internal User-Programmable Registers</td>
<td>Comparison Limit #3</td>
<td>X/X</td>
<td>Sign</td>
<td>Interf</td>
<td>Bit0</td>
<td></td>
</tr>
</tbody>
</table>

**Note 22:** LM12454 (Refer to Table 2).

**Note 23:** LM12454 only. Must be set to “0” for the LM12454.

---

**2.2 Configuration Register**

The Configuration register in LM12454 (A4–A1, BW = 0) or 1005 (A4–A0, BW = 1) is a 16-bit control register with read/write capability. It acts as the LM32454’s and LM32458’s control panel holding global information as well as start/stop, reset, self-calibration, and start-by commands.

Bit 0 is the START/STOP bit. Reading Bit 0 returns an indication of the Sequencer’s status. A “0” indicates that the Sequencer is stopped and waiting to execute the next instruction. A “1” shows that the Sequencer is running. Writing a “0” halts the Sequencer when the current instruction has finished execution. The next instruction to be executed is pointed to by the instruction pointer found in the status register. A “1” restarts the Sequencer with the instruction currently pointed to by the instruction pointer. (See Bits 8–10 in the Interrupt Status register.)

Bit 1 is the LM32454’s system RESET bit. Writing a “1” to Bit 1 stops the Sequencer (resetting the Configuration register’s START/STOP bit), resets the Instruction pointer to “000”, (in the Interrupt Status register), clears the Conversion FIFO, and resets all interrupt flags. The RESET bit will return to “0” after two clock cycles if it is forced high by writing a “1” into the Configuration register’s standby bit. If a reset signal is internally generated when power is first applied, it will point to the part. No operation should be started until the RESET bit is cleared.

Writing a “1” to Bit 2 initiates an auto-zero offset voltage calibration. Unlike the eight-sample auto-zero calibration performed during the full calibration procedure, Bit 2 initiates a “short” auto-zero by sampling the offset once and creating a correction coefficient (full calibration averages eight samples of the comparator offset voltage when that offset is not the correct, or offset, is not the result of the current sampling). The Sequencer is running when Bit 2 is set to “1”, an auto-zero starts immediately after the conclusion of the currently running instruction. Bit 2 is reset automatically to a “0” and an interrupt flag (Bit 3, the Interrupt Status register) is set at the end of the auto-zero (16 clock cycles). After completion of an auto-zero calibration, the Sequencer fetches the instruction RAM’s pointer and resumes execution. If the Sequencer is stopped, an auto-zero is performed immediately at the time requested.

Writing a “1” to Bit 3 initiates a complete calibration process that includes a “long” auto-zero and offset voltage calibration. This calibration averages eight samples of the comparator offset voltage when creating a correction coefficient, followed by an ADC linearity calibration. This complete calibration is started after the currently running instruction is completed. If the Sequencer is running when Bit 3 is set to “1”, Bit 3 is reset automatically to a “0” and an interrupt flag (Bit 4, the Interrupt Status register) will be generated at the end of the calibration procedure (464 clock cycles). After completion of a full auto-zero and linearity calibration, the Sequencer fetches the next instruction as pointed to by the Instruction RAM’s pointer and resumes execution. If the Sequencer is stopped, a full calibration is performed immediately at the time requested.

Bit 4 is the Standby bit. Writing a “1” to Bit 4 immediately places the LM32454/548 in Standby mode. Normal operation returns when Bit 4 is reset to a “0”. The Standby com
2.0 Internal User-Programmable Registers (Continued)

TABLE 1. LM12(H)458 Input Multiplexer Channel Configuration Showing Normal & Diagnostic Mode

<table>
<thead>
<tr>
<th>Channel</th>
<th>Selection</th>
<th>Normal Mode</th>
<th>Diagnostic Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>IN0</td>
<td>GND</td>
<td>V IN+</td>
</tr>
<tr>
<td>001</td>
<td>IN1</td>
<td>IN1</td>
<td>IN1</td>
</tr>
<tr>
<td>010</td>
<td>IN2</td>
<td>IN2</td>
<td>IN2</td>
</tr>
<tr>
<td>011</td>
<td>IN3</td>
<td>IN3</td>
<td>IN3</td>
</tr>
<tr>
<td>100</td>
<td>IN4</td>
<td>IN4</td>
<td>IN4</td>
</tr>
<tr>
<td>101</td>
<td>IN5</td>
<td>IN5</td>
<td>IN5</td>
</tr>
<tr>
<td>110</td>
<td>IN6</td>
<td>IN6</td>
<td>IN6</td>
</tr>
<tr>
<td>111</td>
<td>IN7</td>
<td>IN7</td>
<td>IN7</td>
</tr>
</tbody>
</table>

The Interrupt Status register's Bit 1 (in the Interrupt Status register's Bit 1) the Sequencer automatically inserts a auto-zero before every conversion or “watchdog” conversion, depending on the logic state of Bit 9 in the Instruction RAM's second and third sections, an interrupt will be generated either when the input signal's magnitude is greater than or less than the programmed value (in the Interrupt Enable register). See Section 2.3 for more information about each of the eight internal interrupts.

Interrupt 1 is generated whenever the analog input voltage on a selected multiplexer channel crosses a limit while the LM12(H)454/8 are operating in the “watchdog” comparison mode. Two sequential comparisons are made when the LM12(H)454/8 are executing a “watchdog” instruction. Depending on the logic state of Bit 9 in the Instruction RAM’s second and third sections, an interrupt will be generated either when the input signal’s magnitude is greater than or less than the programmed value (in the Instruction RAM). See Section 2.9 description.) The Limit Status register will indicate which interrupt was generated and which instruction was executing when the limit was crossed.

Interrupt 1 is generated when the Sequencer reaches the instruction counter value specified in the Interrupt Enable register’s Bits 8–10. This flag appears before the instruction’s execution begins but is automatically set to “0” by software when both V IN+ and V IN− are within the diagnostic mode typically results in a full-scale output.

2.3 INTERRUPTS

The LM12(H)454/458 have eight possible interrupts, all with the same priority. Any of these interrupts will cause a hardware interrupt to appear on the INT pin (31).

2.0 Internal User-Programmable Registers (Continued)

The completion of a full auto-zero and linearity self-calibration generates Interrupt 4.

Interrupt 4 is generated when the Sequencer encounters an instruction that has its Pause bit (Bit 1 in Instruction RAM ‘00’) set to “1”.

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2.3 INTERRUPTS

The completion of a full auto-zero and linearity self-calibration generates Interrupt 4.
2.0 Internal User-Programmable Registers (Continued)

Bits 8–15 show the Limit #2 status. Each bit will be set high ("1") when the corresponding instruction's input voltage exceeds the threshold stored in the instruction's Limit #2 register. When, for example, the input to instruction 6 meets the value stored in the Instruction #2 register, Bit 14 in the Limit Status register will be set to a "1".

2.7 TIMER

The LM12/H4548 have an onboard 16-bit timer that includes a 5-bit pre-scaler. It uses the clock signal applied to pin 23 as its input. It can generate time intervals of 0 through 2^15 clock cycles in steps of 2^27. This time interval can be used to delay the execution of instructions. It can also be used to slow the conversion rate when converting slowly changing signals. This can reduce the amount of redundant data stored in the FIFO and retrieved by the controller.

The user-defined timing value used by the Timer is stored in the 16-bit READ/WRITE Timer register at location 1011 (A4–A1, BW = 0) or 1011x (A4–A0, BW = 1) and is pre-loaded automatically. Bits 0–7 hold the preset value's low byte and Bits 8–15 hold the high byte. The Timer is activated by the Sequencer only if the current instruction's Bit 9 is set ("0"). If the equivalent decimal value of "N" (0 ≤ N ≤ 2^15) is written inside the 16-bit Timer register and the Timer is enabled by setting an instruction's bit 9 to a "1", the Sequencer will delay the same instruction's execution by halting at state 3 (S3), as shown in Figure 35, for 32 N + 2 clock cycles.

2.8 DMA

The DMA works in tandem with Interrupt 2. An active DMA Request on pin 32 (DMARQ) requires that the FIFO Interrupt enable be enabled. The voltage on the DMARQ pin goes high when the number of conversions in the FIFO equals the 5-bit value stored in the Interrupt Enable register (bits 11–15). The voltage on the INT pin goes low at the same time as the voltage on the DMARQ pin goes high. The voltage on the DMARQ pin goes low when the FIFO is emptied. The Interrupt Status register must be read to clear the FIFO interrupt flag in order to enable the next DMA request.

DMA operation is optimized through the use of the 16-bit data bus connection (a logic "0" applied to the BW pin). Using this bus width allows DMA controllers that have single-address Read/Write capability to easily interface the FIFO. Using DMA on an 8-bit data bus is more difficult. Two read operations (low byte, high byte) are needed to retrieve each conversion result from the FIFO. Therefore, the DMA controller must be able to repeatedly access two constant addresses when transferring data from the LM12/H4548 to the host system.

3.0 FIFO

The result of each conversion stored in an internal read-only FIFO (First-In, First-Out) register. It is located at 1100 (A4–A1, BW = 0 or 1100x (A4–A0, BW = 1). This register has 32 16-bit wide locations. Each location holds 13-bit data. Bits 0–3 hold the four LSB's in the 12 bits + sign mode or "1110" in the 8 bits + sign mode. Bits 4–11 hold the eight MSB's and Bit 12 holds the sign bit. Bits 13–15 can hold either the sign bit, extending the register's two's complement data format to a full sixteen bits or the instruction address that generated the conversion and the resulting data. These modes are selected according to the logic state of the Configuration register's Bit 5.

The FIFO status should be read in the Interrupt Status register (Bits 11–15) to determine the number of conversion results that are held in the FIFO before retrieving them. This will help prevent conversion data corruption that may take place if the number of reads are greater than the number of conversion results contained in the FIFO. Trying to read the FIFO when it is empty may corrupt new data being written into the FIFO. Writing more than 32 conversion data into the FIFO by the ADC results in loss of the first conversion data. Therefore, to prevent data loss, it is recommended that the LM12/H4548 interrupt capability be used to inform the system controller that the FIFO is full.

The lower portion (A0 = 0) of the data word (Bits 0–7) should be read first followed by a read of the upper portion (A0 = 1) when using the 8-bit bus width (BW = 1). Reading the upper portion first causes the data to shift down, which results in loss of the lower byte.

Bits 0–12 hold 12-bit + sign conversion data. Bits 0–3 will show the Limit #2 status. Each bit will be set high ("1") when the corresponding instruction's input voltage exceeds the threshold stored in the Instruction #2 register. When, for example, the input to instruction 6 meets the value stored in the Instruction #2 register, Bit 14 in the Limit Status register will be set to a "1".

State 3: Run the internal 16-bit Timer. The number of clock cycles for this state varies according to the value stored in the Timer register. The number of clock cycles is found by using the expression below:

\[ 32T + 2 \]

where \( T \) is the generated conversion and the resulting data. These modes are selected according to the logic state of the Configuration register's Bit 5.

State 4: Perform first comparison. This state is 5 clock cycles long.

State 6: Perform calibration. If bit 2 or bit 6 of the Configuration register is set to a "1", state 6 is 76 clock cycles long. If the Configuration register's bit 3 is set to a "1", state 6 is 4944 clock cycles long.

State 7: Run the acquisition delay and read Limit #1's value. This state takes 44 clock cycles when using the 12-bit + sign mode or 21 clock cycles when using the 8-bit + sign mode. The "watchdog" mode takes 5 clock cycles.

State 8: The Sequencer can go through eight states during instruction execution:

- State 0: The current instruction's first 16 bits are read from the Instruction RAM "00". This state is one clock cycle long.
- State 1: Checks the state of the Calibration and Start bits. This is the "active" state whenever the Sequencer is stopped using the reset, a Pause command, or the Start bit is reset low ("0"). When the Start bit is set to a "1", this state is one clock cycle long.
- State 2: Performs calibration. If the bit 2 or bit 6 of the Configuration register is set to a "1", state 2 is 76 clock cycles long. If the Configuration register's bit 3 is set to a "1", state 2 is 4944 clock cycles long.
- State 3: Run the internal 16-bit Timer. The number of clock cycles for this state varies according to the value stored in the Timer register. The number of clock cycles is found by using the expression below:

\[ 32T + 2 \]

where \( T \) is the generated conversion and the resulting data. These modes are selected according to the logic state of the Configuration register's Bit 5.

State 7: Run the acquisition delay and read Limit #1's value. This state takes 44 clock cycles when using the 12-bit + sign mode or 21 clock cycles when using the 8-bit + sign mode. The "watchdog" mode takes 5 clock cycles.
4.0 Sequencer (Continued)

5.0 Analog Considerations

5.1 REFERENCE VOLTAGE

The difference in the voltages applied to the VREF+ and VREF− defines the analog input voltage span (the difference between the voltages applied between two multiplexer inputs or the voltage applied to one of the multiplexer inputs and analog ground, over which ±4096 positive and 4096 negative codes exist. The voltage sources driving VREF+, or VREF− must have very low output impedance and noise.

The ADC can be used in either ratiometric or absolute reference applications. In ratiometric systems, the analog input voltage is proportional to the voltage used for the ADC’s reference voltage. When this voltage is the system power supply, the VREF+ pin is connected to V+ and VREF− is connected to GND. This technique relaxes the system reference stability requirements because analog input voltage and the ADC reference voltage move together. This maintains the same output code for given input conditions.

For absolute accuracy, where the analog input voltage varies between specific voltage limits, time and temperature stable voltage source can be connected to the reference inputs. Typically, the reference voltage’s magnitude will require an initial adjustment to null reference voltage induced full-scale error.

When using the LM12(H)454/8’s internal 2.5V bandgap reference, a parallel combination of a 100 μF capacitor and a 0.1 μF capacitor connected to the VREFOUT pin is recommended for low noise operation. When left unconnected, the reference remains stable without a bypass capacitor. However, ensure that stray capacitance at the VREFOUT pin remains below 50 pF.

5.2 INPUT RANGE

The LM12(H)454/8’s fully differential ADC and reference voltage inputs generate a two-complement output that is found by using the equation below.

\[
\text{output code} = \frac{V_{IN+} - V_{IN-}}{V_{REF+} - V_{REF-}} \cdot 2^{11} \quad (12-bit)
\]

\[
\text{output code} = \frac{V_{IN+} - V_{IN-}}{V_{REF+} - V_{REF-}} \cdot 2^{8} \quad (8-bit)
\]

Round up to the nearest integer value between +4095 to 4095 for 12-bit resolution and between +255 to 255 for 8-bit resolution. If the result of the above equation is not a whole number. As an example, VREF+ = 2.5V, VREF− = 1V, VIN+ = 1.5V, and VIN− = GND. The 12-bit + sign output code is positive full-scale, 0x111111111111. If VREF+ = 5V, VREF− = 1V, VIN+ = 3V, and VIN− = GND, the 12-bit + sign output code is 0x110000000000.

5.3 INPUT CURRENT

A charging current flows into or out of (depending on the input voltage polarity) the analog input pins, IN0–IN7 at the start of the analog input acquisition time (tACQ). This current’s peak value will depend on the actual input voltage applied.

5.4 INPUT SOURCE RESISTANCE

For low impedance voltage sources (<100Ω) for 5 MHz operation and <50Ω for 8 MHz operation, the input charging current will decay, before the end of the S/H’s acquisition time, to a value that will not introduce any conversion errors. For higher source impedances, the S/H’s acquisition time can be increased. As an example, operating with a 5 MHz clock frequency and maximum acquisition time, the LM12(H)454/8’s analog inputs can handle source impedance as high as 6.67 kΩ. When operating at 8 MHz and maximum acquisition time, the LM12(H)454/8’s analog inputs can handle source impedance as high as 4.17 kΩ.

5.5 INPUT BYPASS CAPACITANCE

External capacitors (0.01 µF–0.1 µF) can be connected between the analog input pins and analog ground to filter any noise caused by inductive pickup associated with long input leads. This will not degrade the conversion accuracy.

5.6 NOISE

The leads to each of the analog multiplexer input pins should be kept as short as possible. This will minimize input noise and clock frequency coupling that can cause conversion errors. Input filtering can be used to reduce the effects of the noise sources.

5.7 POWER SUPPLIES

Noise spikes on the V+ and V− supply lines can cause conversion errors; the comparator will respond to the noise. The ADC is especially sensitive to any supply spikes that occur during the auto-zero or linearity correction. Low inductance tantalum capacitors of 10 µF or greater paralleled with 0.1 µF monolithic ceramic capacitors are recommended for supply bypassing. Separate bypass capacitors should be used for the V+ and V− supplies and placed as close as possible to these pins.

5.8 GROUNDING

The LM12(H)454/8’s nominal high resolution performance can be maximized through proper grounding techniques. These include the use of separate analog and digital ground planes. The digital ground plane is placed under all components that handle digital signals, while the analog ground plane is placed under all analog signal handling circuitry. The digital and analog ground planes are connected at only one point, the power supply ground. This greatly reduces the occurrence of ground loops and noise.

It is recommended that stray capacitance between the analog inputs or outputs, LM12(H)454: IN0–IN3, MUXOUT+, MUXOUT−, S/H IN+, S/H IN−; LM12(H)458: IN0–IN7, V+ and V−) be reduced by increasing the clearance (6.35mm or 0.25inch) between the analog signal and reference pins and the ground plane.

5.9 CLOCK SIGNAL LINE ISOLATION

The LM12(H)454/8’s performance is optimized by routing the analog input/output and reference signal conductors (pins 34–46) as far as possible from the conductor that carries the clock signal to pin 23. Ground trunks parallel to the clock signal trace can be used on printed circuit boards to reduce clock signal interference on the analog input/output pins.

6.0 Application Circuits

PC EVALUATION INTERFACE BOARD

Figure 16 is the schematic of an evaluation/interface board designed to interface the LM12(H)454 or LM12(H)458 with an XT or AT® style computer. The board can be used to de-
6.0 Application Circuits (Continued)

velop both software and hardware. The board hardwires the BW (Bus Width) pin to a logic high, selecting an 8-bit wide data bus. Therefore, it is designed for an 8-bit expansion slot on the computer's motherboard.

The circuit operates on a single +5V supply derived from the computer's +12V supply using an LM340 regulator. This greatly attenuates noise that may be present on the computer's power supply lines. However, your application may only need an LC filter.

Figure 16 also shows the recommended supply (V+ and V−) and reference input (VREF+, and VREF−) bypassing. The digital and analog supply pins can be connected together to the same supply voltage. However, they need separate, multiplex bypass capacitors. Multiple capacitors on the supply pins and the reference inputs ensures a low impedance bypass path over a wide frequency range.

All digital interface control signals (IOR, IOW, and AEN), data lines (DB0–DB7), address lines (A0–A9), and IRQ (Interrupt request) lines (IRQ2, IRQ3, and IRQ5) connections are made through the motherboard slot connector. All analog signals applied to, or received by, the input multiplexer (IN0–IN7) for the LM12(H)/454, MUXOUT+, MUXOUT−, SH IN+ and SH IN− for the LM12(H)/454, VREF+, VREF−, VREFOUT+ and the SYNC signal input/output are applied through a DB-37 connector on the rear side of the board. Figure 16 shows that there are numerous analog ground connections available on the DB-37 connector.

The voltage applied to VREF− and VREF+ is selected using two jumpers, JP1 and JP2. JP1 selects between the voltage applied to the DB-37's pin 24 or GND and applies it to the LM12(H)/454/8's VREF− input. JP2 selects between the LM12(H)/454/8's internal reference output, VREFOUT+, and the voltage applied to the DB-37's pin 22 and applies it to the LM12(H)/454/8's VREF+ input.

Table 3. LM12(H)/454/8 Evaluation/Interface Board SW DIP-8 Switch Settings for Available I/O Memory Locations

<table>
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<tr>
<th>Hexidecimal</th>
<th>SW DIP-8 Switch Settings for Available I/O Memory Locations</th>
</tr>
</thead>
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<tr>
<td>I/O Memory</td>
<td>SW1 SW2 SW3 SW4</td>
</tr>
<tr>
<td>Base Address</td>
<td>(SEL0) (SEL1) (SEL2) (SEL3)</td>
</tr>
<tr>
<td>100</td>
<td>OFF OFF OFF ON</td>
</tr>
<tr>
<td>120</td>
<td>OFF ON ON ON</td>
</tr>
<tr>
<td>140</td>
<td>ON OFF OFF ON</td>
</tr>
<tr>
<td>160</td>
<td>OFF OFF OFF ON</td>
</tr>
<tr>
<td>180</td>
<td>ON ON ON ON</td>
</tr>
<tr>
<td>1A0</td>
<td>OFF OFF OFF ON</td>
</tr>
<tr>
<td>1C0</td>
<td>ON OFF OFF ON</td>
</tr>
<tr>
<td>200</td>
<td>OFF OFF OFF ON</td>
</tr>
<tr>
<td>220</td>
<td>OFF OFF OFF ON</td>
</tr>
<tr>
<td>240</td>
<td>OFF OFF OFF ON</td>
</tr>
<tr>
<td>260</td>
<td>OFF OFF OFF ON</td>
</tr>
<tr>
<td>280</td>
<td>OFF OFF OFF ON</td>
</tr>
</tbody>
</table>

The board allows the use of one of three Interrupt Request (IRQ) lines (IRQ2, IRQ3, and IRQ5). The individual IRQ line can be selected using switches 5, 6, and 7 of SW DIP-8. When using any of these three IRQs, the user needs to ensure that there are no conflicts between the evaluation board and any other boards attached to the computer's motherboard.

Switches 1–4, along with address lines A5–A9 are used as inputs to GAL16V8 Programmable Gate Array (U2). This device forms the interface between the computer's control and address lines and generates the control signals used by the LM12(H)/454/8 for CS, WR, and RD. It also generates the signal that controls the data buffers. Several address ranges within the computer's I/O memory map are available. Refer to Table 3 for the switch settings that give the desired I/O memory address range. Selection of an address range must be done so that there are no conflicts between the evaluation board and any other boards attached to the computer's motherboard. The GAL equations are shown in Figure 18. The GAL functional block diagram is shown in Figure 19.

Figures 20, 21, 22, 23 show the layout of each layer in the 3-layer evaluation interface board plus the silk-print layout showing parts placement. Figure 21 is the top or component side, Figure 22 is the middle or ground plane layer, Figure 23 is the circuit side, and Figure 24 is the parts layout.
# APPENDIX C: ALPHABETICAL INDEX

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<td>CN3</td>
<td>12</td>
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<td>CN4</td>
<td>11</td>
</tr>
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<td>14</td>
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