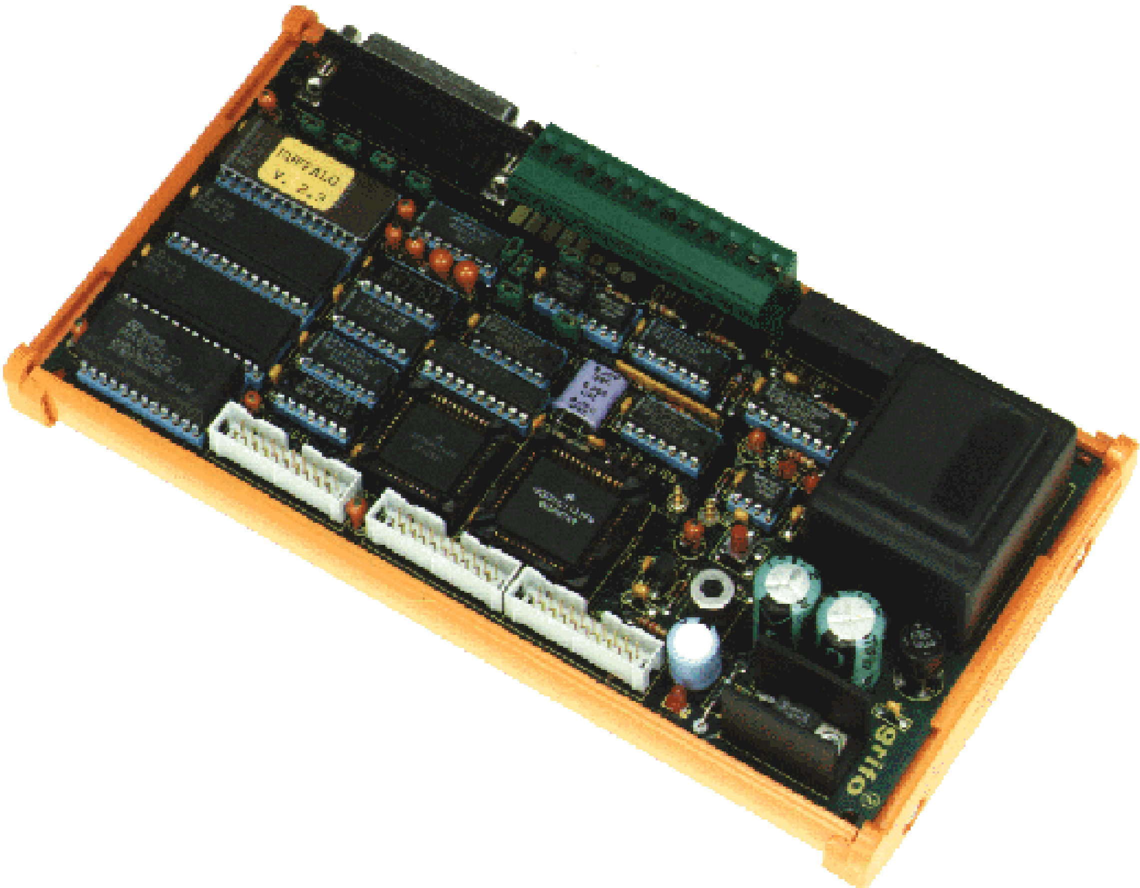
GPC® 11

General Purpose Controller 68 HC 11

TECHNICAL MANUAL



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GPC® 11 Edition 5.00 *Rel. 9 February 1999*

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1**00x195 mm** module format for **DIN 46277-1** and **3** rails. **68HC11A1 CPU** with **8 MHz** crystal. Double **watch dog** circuits. **74K** of memory divided on 4 sockets: 32K **EPROM**; 32K **RAM**, **EEPROM**; 8K RAM, **backed RAM**; 2K RAM, backed RAM and **real time clock**. **32 TTL I/O lines** settable at bit and byte level and completely software manageable. 16 of the said lines are recovered by the microprocessor **I/O ports**, through **68HC24**. One **16 bits timer counter** with compare and capture functions. **512** Bytes of **EEPROM** microprocessor inside. Eight channels of **8 bits A/D** converter lines; **12 μs**; 0÷2.49, 0÷5V or 0÷20 mA range. 1 serial line in **RS 232**, **RS 422**, **RS 485** or **current loop**. Baud rate up to **125 KBaud** (standard 9600 Baud max). Different power supply configuration: **220 Vac** from main; AC or DC **low voltage**; **+5Vdc 50 mA**. Wide range of developement software such as: Monitor, Debugger, Assembler, BASIC interpreter, FORTH, C compilers as: **HTC 11**, **No ICE 11**, **ICC 11**, **CMX RTX**, **DDS micro C**, **Control PASCAL**, **GET 11**, **BASIC 11** and so on.

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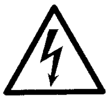
IMPORTANT

Although all the information contained herein have been carefully verified, **grifo®** assumes no responsibility for errors that might appear in this document, or for damage to things or persons resulting from technical errors, omission and improper use of this manual and of the related software and hardware.
grifo® reservs the right to change the contents and form of this document, as well as the features and specification of its products at any time, without prior notice, to obtain always the best product.
For specific informations on the components mounted on the card, please refer to the Data Book of the builder or second sources.

SYMBOLS DESCRIPTION

In the manual could appear the following symbols:


Attention: Generic danger


Attention: High voltage

Trade marks

GENERAL INDEX

FIGURES INDEX

INTRODUCTION

The use of these devices has turned - IN EXCLUSIVE WAY - to specialized personnel.

The purpose of this handbook is to give the necessary information to the cognizant and sure use of the products. They are the result of a continual and systematic elaboration of data and technical tests saved and validated from the manufacturer, related to the inside modes of certainty and quality of the information.

The reported data are destined- IN EXCLUSIVE WAY- to specialized users, that can interact with the devices in safety conditions for the persons, for the machine and for the enviroment, impersonating an elementary diagnostic of breakdowns and of malfunction conditions by performing simple functional verify operations , in the height respect of the actual safety and health norms.

The informations for the installation, the assemblage, the dismantlement, the handling, the adjustment, the reparation and the contingent accessories, devices etc. installation are destined - and then executable - always and in exclusive way from specialized warned and educated personnel, or directly from the TECHNICAL AUTHORIZED ASSISTANCE, in the height respect of the manufacturer recommendations and the actual safety and health norms.

The devices can't be used outside a box. The user must always insert the cards in a container that rispect the actual safety normative. The protection of this container is not threshold to the only atmospheric agents, but specially to mechanic, electric, magnetic, etc. ones.

To be on good terms with the products, is necessary guarantee legibility and conservation of the manual, also for future references. In case of deterioration or more easily for technical updates, consult the AUTHORIZED TECHNICAL ASSISTANCE directly.

To prevent problems during card utilization, it is a good practice to read carefully all the informations of this manual. After this reading, the user can use the general index and the alphabetical index, respectly at the begining and at the end of the manual, to find information in a faster and more easy way.

CARD VERSION

The present handbook is reported to the **GPC® 11** card release **100594** and later. The validity of the bring informations is subordinate to the number of the card release. The user must always verify the correct correspondence among the two denotations. On the card the release number is present in more points both board printed diagram (serigraph) and printed circuit (for example in the right high corner of the component side, near the F1 fuse).

GENERAL FEATURES

The **GPC® 11** card is a powerful control and governing low cost module completely autonomous. It is equipped with a coupled support having quick hook for Omega rails DIN 46277-1 and DIN 46277-3 which allow to put the complete control unit into the electrical panel with no requirements of expensive structure as 3HE rack, back panel and so on. This solution means cheaper costs for the entire economy of the equipment and remarkable praticity of use.
This card supports the powerful MOTOROLA 68HC11A1 monochip that includes a remarkable series of internal resources which enrich the considerable functionality of this card.
The development and setup of applicatives can just start from the **GPC® 11** as it has, on board, the hardware which is needed for a first approach. This card can also counts on many differents software tools which simplify the use of the same; it is sufficient the connection to a P.C. through the on board serial line of the **GPC® 11** for starting to operate in a very friendly way having, at the same time, considerable local resources.
This card it is also equipped with a serie of helpfull **ABACO®** standard pin out connectors. Thanks to these connectors it is very easy to be interfaced to the field by using BLOCK modules or adopting any user's card duly designed for this purpose.

- 1**00x195 mm** module format for **DIN 46277-1** and **3** rails.
- **68HC11A1 CPU** with **8 MHz** crystal.
- Double **watch dog** circuits.
- On board **reset** button.
- **74K** of memory divided on 4 sockets: 32K **EPROM**; 32K **RAM**, **EEPROM**; 8K RAM, **backed RAM**; 2K RAM, backed RAM and **real time clock**.
- **32 TTL I/O lines** settable at bit and byte level and completely software manageable. 16 of the said lines are recovered by the microprocessor **I/O ports**, through **68HC24**.
- One **16 bits timer counter** with compare and capture functions.
- **512** Bytes of **EEPROM** microprocessor inside.
- Eight channels of **8 bits A/D** converter lines; **12** µs; 0÷2.49, 0÷5V or 0÷20 mA range.
- 1 serial line in **RS 232**, **RS 422**, **RS 485** or **current loop**.
- Baud rate up to **125 KBaud** (standard 9600 Baud max).
- Different power supply configuration: **220 Vac** from main; AC or DC **low voltage**; **+5Vdc 50 mA**.
- **Power failure** circuit.
- Wide range of developement software such as: Monitor, Debugger, Assembler, BASIC interpreter, FORTH, C compilers as: **HTC 11**, **No ICE 11**, **ICC 11**, **CMX RTX**, **DDS micro C**, **Control PASCAL**, **GET 11**, **BASIC 11** and so on.

The foolowing pages describe each section of the card in a more detailed mode and figure 1 illustrates the sections interconnections.

CLOCK DEVICE

On **GPC® 11** there is a proper 8 MHz crystal to generate the clock signal for the microprocessor. This frequency is internally divided by the microprocessor to obtain a 2 MHz CPU clock speed, so all the timing calculations must be based on this value. Please remember that the microprocessor clock frequency indirectly defines the baud rate of the serial line, too.

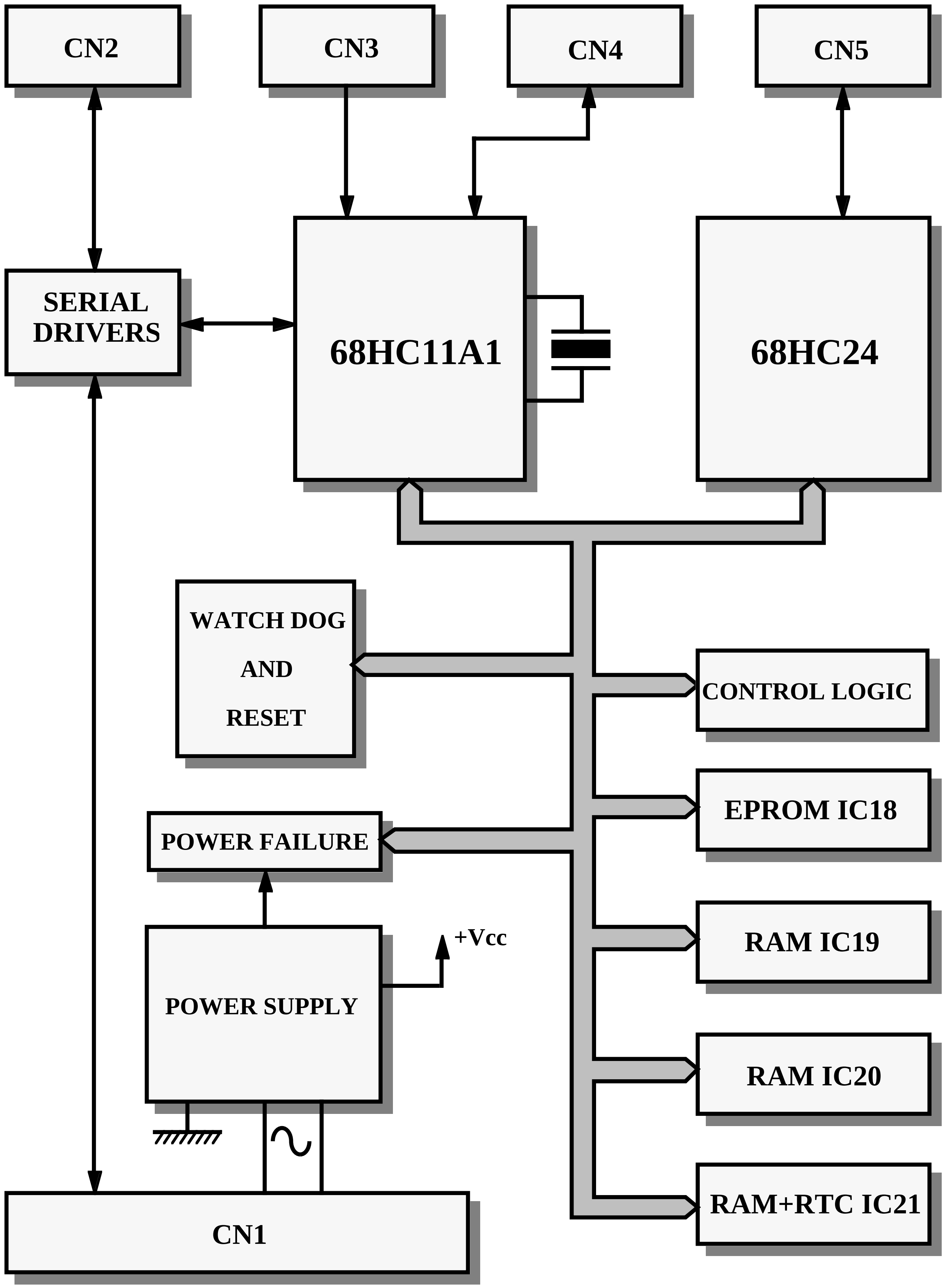


FIGURE 1: BLOCK DIAGRAM

CPU

The **GPC® 11** can use the MC68HC11A1 microprocessor, manufactured by MOTOROLA. This 8 bits microprocessor is code compatible with the world wide used 6801 family and it has an extended instruction set, fast execution time, comfortable use of single I/O lines and an efficient interrupt management. The most important features of the described microprocessor, are:

- 8 bit CPU;
- 12 clocks system cycle;
- 256 bytes of relocatable internal RAM;
- 512 bytes of relocatable internal EEPROM;
- 64K bytes of external code and data memory;
- 16 digital I/O lines;
- One 16 bits timer/counters with capture and compare function;
- 2 priority levels for interrupts and 20 interrupt sources;
- 1 asyncronous serial line (SCI);
- 1 syncronous serial line(SPI);
- Idle mode or power down mode;
- Watch dog circuit driven by software (COP).

For further information, please refer to specific documentation of the manufacturing company.

SERIAL COMMUNICATION

An asyncronous serial line (SCI) is always available on **GPC® 11** and it is completely software configurable for physical protocol (baud rate, stop bits number and lenght of character) by simply programming some microprocessor registers. By hardware the serial line can be buffered in four different electrical protocols: **RS 232**, **RS 422**, **RS 485** or **current loop**, through some on board jumpers.
A syncronous serial line (SPI) is also available on the card. It is always driven by software and it is directly connected to a connector, without any electric driver.
For further information about serial lines, please refer to technical documentation of the manufacturing company and to paragraph "SERIAL COMMUNICATION TYPE SELECTION"

POWER SUPPLY

One of the most important features of **GPC® 11** is its on board power supply; the card can be powered in four different ways as described in the chapter "POWER SUPPLY SELECTION". This section has been designed to reduce the total consumption of the card and it can't supply high current for external system load. The power supply voltage is connected through a proper connector that allows a fast and comfortable installation and it is protected by **TransZorb™** to avoid random damages caused by wrong voltages. When Vac power supply is selected, on the card it is available a power failure circuit that generates an interrupt request, with sufficient advance to execute all the necessary procedures for the upcoming power off management.

WATCH DOG AND RESET

GPC® 11 is provided with a sure reset circuit provided of two different source:

- Two separated watch dog circuits that can reset the card at programmable time intervals, if not retriggered. Watch dog circuits are used when the user want to exit from endless loops or to reset anomalous conditions not estimated by application program. There is a monostable section inside the microprocessor (named COP), with programmable intervention time and an astable section, outside the microprocessor, with 800 ms fixed intervention time. By software the user can set the internal watch dog time, enable or disable the internal watch dog circuit and retrigger both the circuits, using specific registers allocated in microprocessor addressing space.
  The external watch dog intervention time can be modified in response to a specific user request, by modifications of proper RC components; if this modification is necessary, please contact **grifo®**.

- A comfortable reset push button that allows the activation of card reset circuit. By pushing P1, the card restarts execution of the program saved in EPROM and all the on board peripheral devices are reset at the same time. P1 is commonly used to exit from endless loop, especially during debug phase. To recognize P1 location, please refer to figure 11.

A special jumper selects wich one of the reset source is used, as described in paragraph "3 PINS JUMPER".

MEMORY DEVICES

On the card can be mounted 74K of memory divided on four different sockets with JEDECS pin out. The **GPC® 11** memory configuration must be chosen considering the application to realize or the specific requirements of the user. Normally the card is equipped with 32K byte of static RAM and all different configurations must be specified from the user, at the moment of the order (refer to figure 25). By mounting backed RAM module or EEPROM module, there is the possibility to keep data also when power supply is missed; in this way the card is always able to maintain parameters, logged data, system status and configurations, etc. without using expensive external UPS. The backed module can also include a clock calendar capable to self manage day, month, year, hours, minutes, seconds, and day of the week.
The addressing of memory devices is controlled by a specific control logic, that provides to allocate the devices in the microprocessor address space, this control logic automatically manages the different addressing mode and it satisfy the requests of each **GPC® 11** software tools.
For further information about memory configuration, sockets description and jumpers connection, please refer to "ADDRESSES AND MAPS" chapter and to "MEMORY SELECTION" paragraph.

CONTROL LOGIC

The addresses of all peripheral device's registers and of memory devices on **GPC® 11** are assigned from a specific control logic that allocates all these devices in the microprocessor addressing space. For further information please refer to chapter "ADDRESSES AND MAPS" of this manual.

PERIPHERAL DEVICES

GPC® 11 is the right card to solve many control problems in automation fields, in fact it is equipped with some peripheral components that facilitate the connection and the management of external system like probes, switches, relays, motor controllers, etc. These peripherals are:

- **SCI**: it is a microprocessor peripheral device that manages serial communication with any other system provided of RS 232, RS 422, RS 485 or current loop serial line. By software the user can set baud rate, length of character, stop bit number, parity and handshake through a simple programmation of internal microprocessor registers.

- **A/D converter**: it is a CPU internal peripheral device that converts 8 different analog signals with 8 bits resolution. By software the user selects the channel to convert, starts the conversion and controls the end of conversion, through programmation of microprocessor internal registers. The analog inputs can be voltage inputs (0÷2,49V or 0÷5V) or current inputs (0÷20 mA); the full scale value is relative to all inputs while the signal type can be selected for each channel. Both full scale value and signals types must be specified at the moment of the order.

- **Timer counter**: it is a CPU internal peripheral device that include a 16 bits timer counter with interesting automatic campare and capture functions. By software the user can sets any parameters and opearting modes, programming some internal registers.

- **CPU I/O ports**: they are CPU internal peripheral devices that can directly manage 16 digital I/O lines. Some of these lines have double function and they are used by other CPU internal devices. By software the user can set and or acquire the line status thanks to proper CPU register and instructions.

- **PRU**: peripheral device based on MC68HC24 component, that replaces the microprocessor port B and C and restores 16 digital I/O lines. The port B is the same as 8 digital output while port C is equivalent to 8 digital input/output. Some signals of port C are used as serial communication handshakes, too. All the PRU I/O lines are connected to CN5 connector and they are completely managed by software through 7 bytes (or registers) located in microprocessor addressing space. In detail the instructions used for the correspondent CPU ports can be used.

For further information about peripheral device please refer to the technical documentation of the manufacturing company.

TECHNICAL FEATURES

GENERAL FEATURES

Devices:	16 programmable TTL input/output lines (68HC11) 8 programmable TTL input/output lines (68HC24) 8 programmable TTL output lines (68HC24) 1 timer counter 16 bits 1 bidirectional RS 232, RS 422, RS 485, current loop serial line 2 watch dog 8 A/D converter lines 1 real time clock 1 reset push button 1 power failure circuit	
Memory:	IC 18:	From 16K x 8 (27C128) to 32K x 8 (27C256) EPROM
	IC 19:	From 8K x 8 to 32K x 8 RAM, backed RAM 32K x 8 EEPROM
	IC 20:	8K x 8 RAM, backed RAM
	IC 21:	2K x 8 RAM, backed RAM (RTC optional)
CPU:	MOTOROLA MC68HC11A1 (M6801 family)	
Clock frequency:	8 MHz	
A/D resolution:	8 bits	
A/D conversion time:	12 μsec	

PHYSICAL FEATURES

Size:	100 x 195 x 25 mm	(without plastic container)
	110 x 210 x 60 mm	(with plastic container)
Weight:	190 g	(without plastic container, transformer)
	565 g	(complete version)
Connectors:	CN1:	12 pins, quick release, screw terminal connector
	CN2:	25 pins, female, 90°, D connector
	CN3:	20 pins, male, vertical, low profile connector
	CN4:	20 pins, male, vertical, low profile connector
	CN5:	20 pins, male, vertical, low profile connector
Temperature range:	0÷70 °C	
Relative humidity:	20%÷90%	(without condense)
External watch dog time:	800 msec	

ELECTRIC FEATURES

Fuse F1:	100 mA; 250 V; fast type	
Power supply voltage:	+5 Vdc	(without power supply section)
	230 Vac; 50 Hz	(standard power supply)
	6÷10 Vac	(low voltage linear power supply) *
	8÷26 Vac	(low voltage switching power supply)
Consumption on 5 Vdc:	50 mA	
Available current for external load:	350 mA	(standard power supply) *
	950 mA	(low voltage switching power supply) *
	750 mA	(low voltage linear power supply) *
Voltage analog inputs range:	0÷2,49 Vcc or 0÷5,00 V	
Current analog inputs range:	0÷20 mA	
Analog inputs impedance:	10 KΩ	
RS 422-485 line termination:	120 Ω	

***** The listed value are valid only with a + 20 °C room temperature (for further information please refer to "POWER SUPPLY SELECTION" paragraph).

INSTALLATION

In this chapter there are the information for a right installation and correct use of the card. The user can find the location and functions of each connectors, jumpers, LEDs and some diagrams.

CONNECTIONS

The **GPC® 11** module has 5 connectors that can be linkeded to other devices or directly to the field, according to system requirements. In this paragraph there are connectors pin out, a short signals description (including the signals direction), and connectors location (see figure 11).

CN2 - RS 232 SERIAL COMMUNICATION CONNECTOR

CN2 is a 25 pins female D connector.
It can be used to connect the RS 232 serial line to any other compatible system, through standard serial cable. Both DTE and DCE standard pin out can be defined on CN2, in fact the jumpers J10, J11, J12, J13 select which standard must be used, as described in "SERIAL COMMUNICATION TYPE SELECTION" paragraph. The following pin out follows the DTE standard:

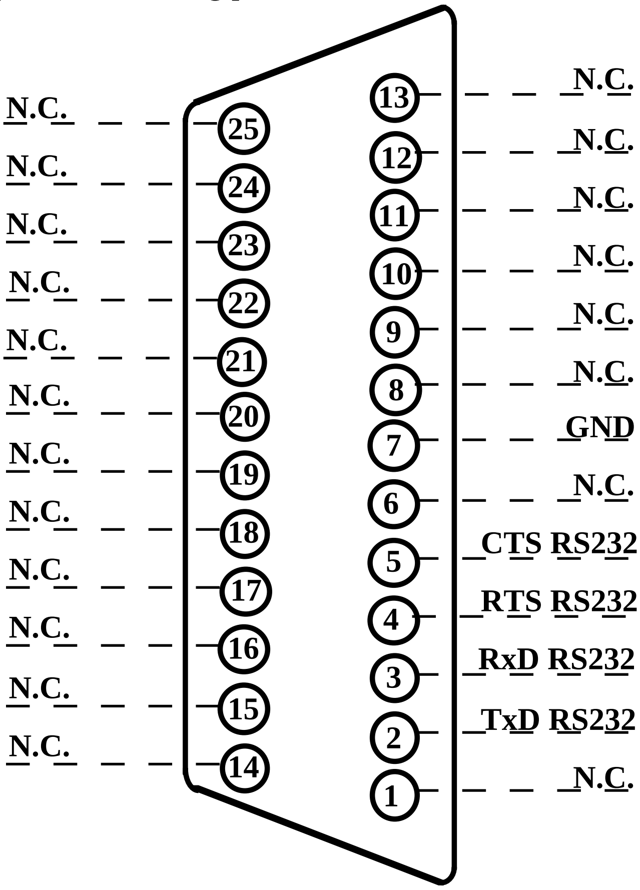


FIGURE 2: RS 232 SERIAL COMMUNICATION CONNECTOR

Signals description:

RxD RS232	=	I	- RS 232 receive signal of serial line.
TxD RS232	=	O	- RS 232 transmit signal of serial line.
CTS RS232	=	I	- RS 232 clear to send handshake of serial line.
RTS RS232	=	O	- RS 232 request to send handshake of serial line.
GND	=		- Ground signal.
N.C.	=		- Not connected.

CN1 - SERIAL LINE AND POWER SUPPLY CONNECTOR

CN1 is a 12 pins, quick release, screw terminal connector.
On CN1 connector can be connected the selected power supply voltage and the asyncronous serial communication line, in all the available electric protocol.

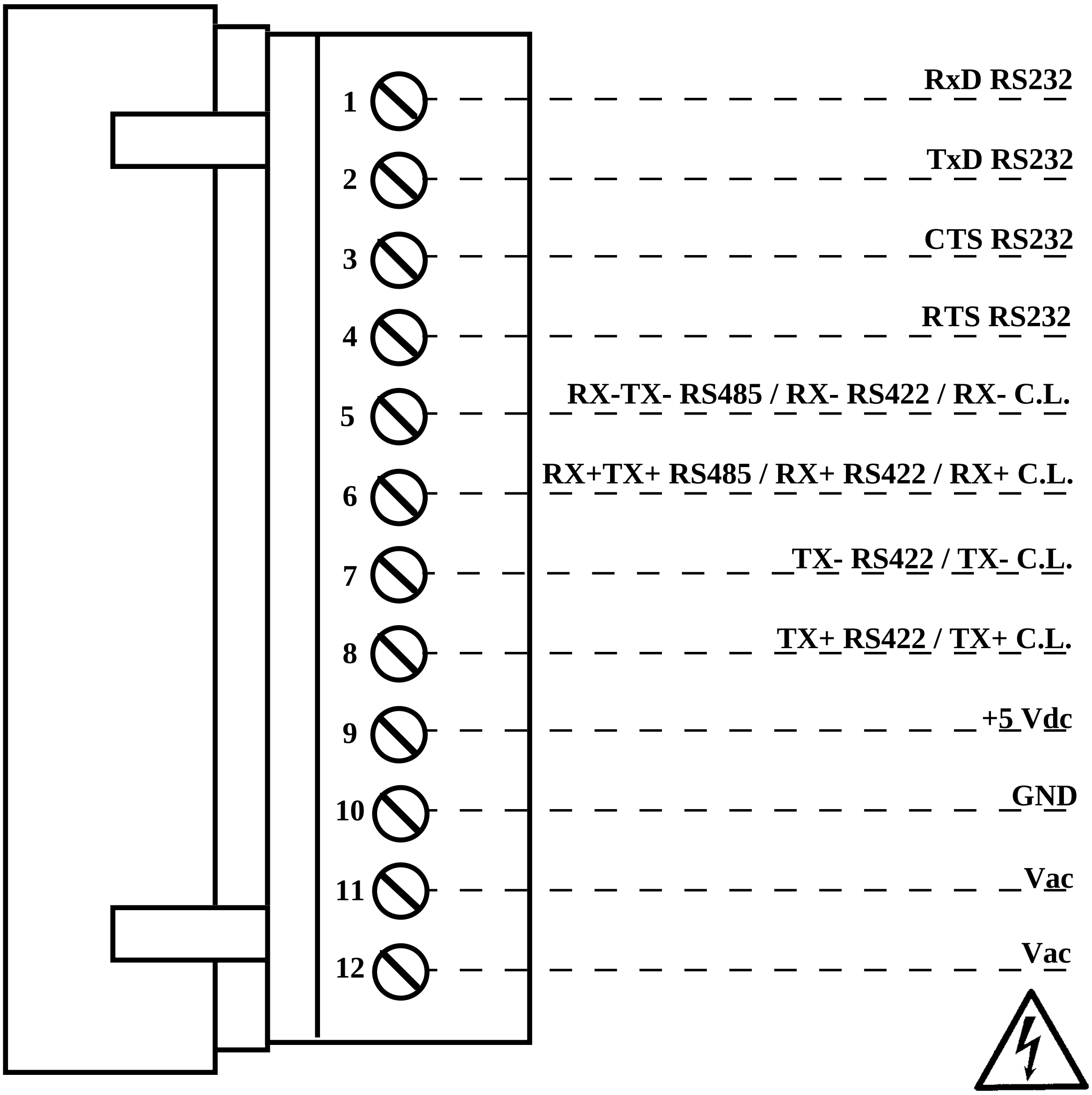


FIGURE 3: CN1 - SERIAL LINE AND POWER SUPPLY CONNECTOR

Signals description:

RxD RS232	=	I	- RS 232 receive signal of serial line.
TxD RS232	=	O	- RS 232 transmit signal of serial line.
CTS RS232	=	I	- RS 232 clear to send handshake of serial line.
RTS RS232	=	O	- RS 232 request to send handshake of serial line.
RX-TX- RS485	=	I/O	- RS 485 receive and transmit data negative of serial line.
RX+TX+ RS485	=	I/O	- RS 485 receive and transmit data positive of serial line.
RX- RS422	=	I	- RS 422 receive data negative of serial line.
RX+ RS422	=	I	- RS 422 receive data positive of serial line.
TX- RS422	=	O	- RS 422 transmit data negative of serial line.
TX+ RS422	=	O	- RS 422 transmit data positive of serial line.

RX- C.L.	=	I	- Current loop receive data negative of serial line.
RX+ C.L.	=	I	- Current loop receive data positive of serial line.
TX- C.L.	=	O	- Current loop transmit data negative of serial line.
TX+ C.L.	=	O	- Current loop transmit data positive of serial line.
+5 Vdc	=	I/O	- +5 Vdc power supply signal.
GND	=		- Ground signal.
Vac	=	I	- Mains or low voltage AC, DC power supply.

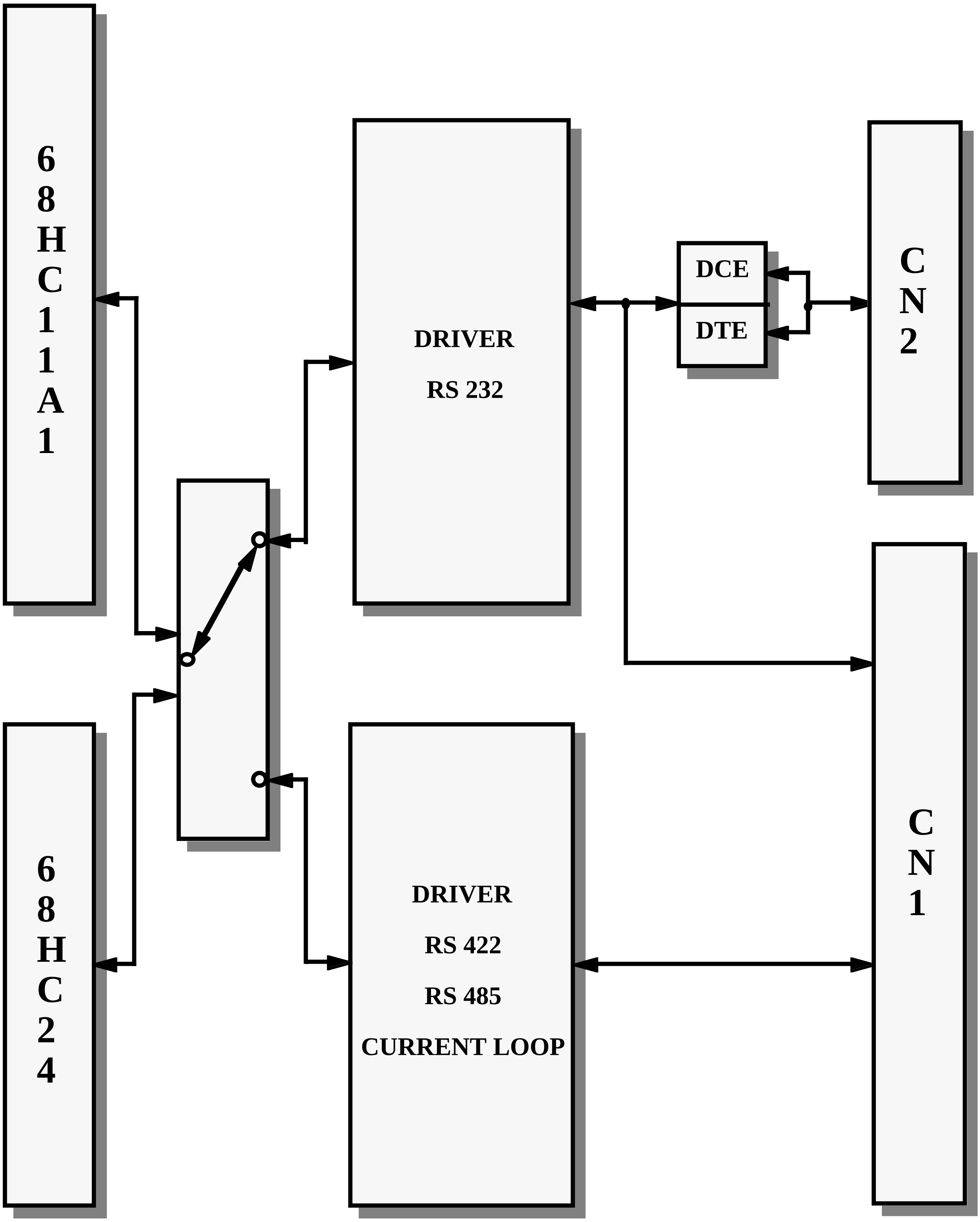


FIGURE 4: SERIAL COMMUNICATION DIAGRAM

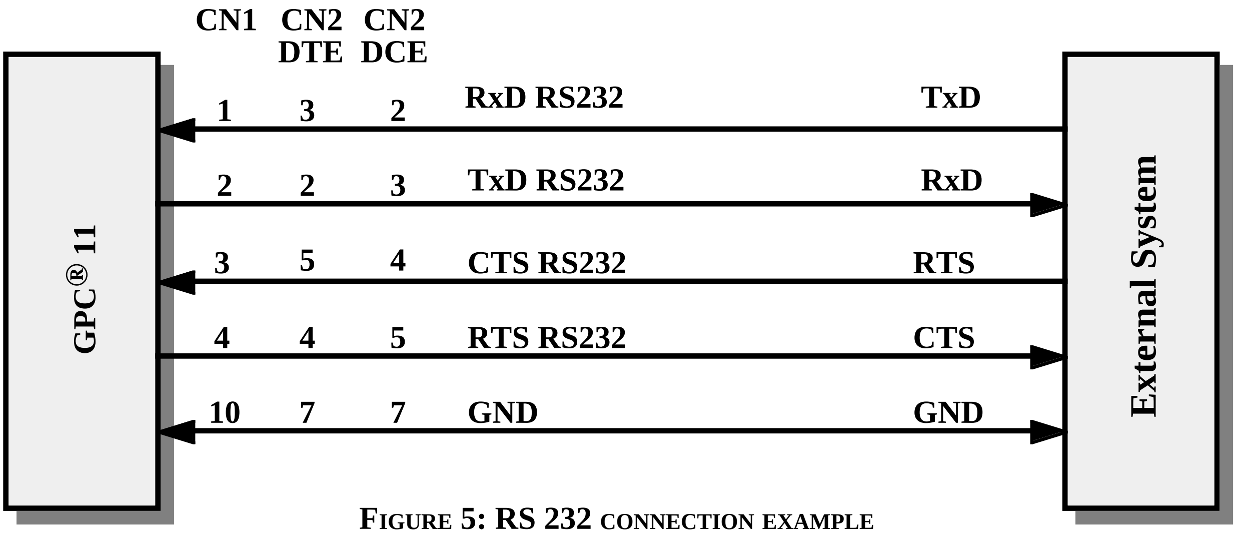


FIGURE 5: RS 232 CONNECTION EXAMPLE

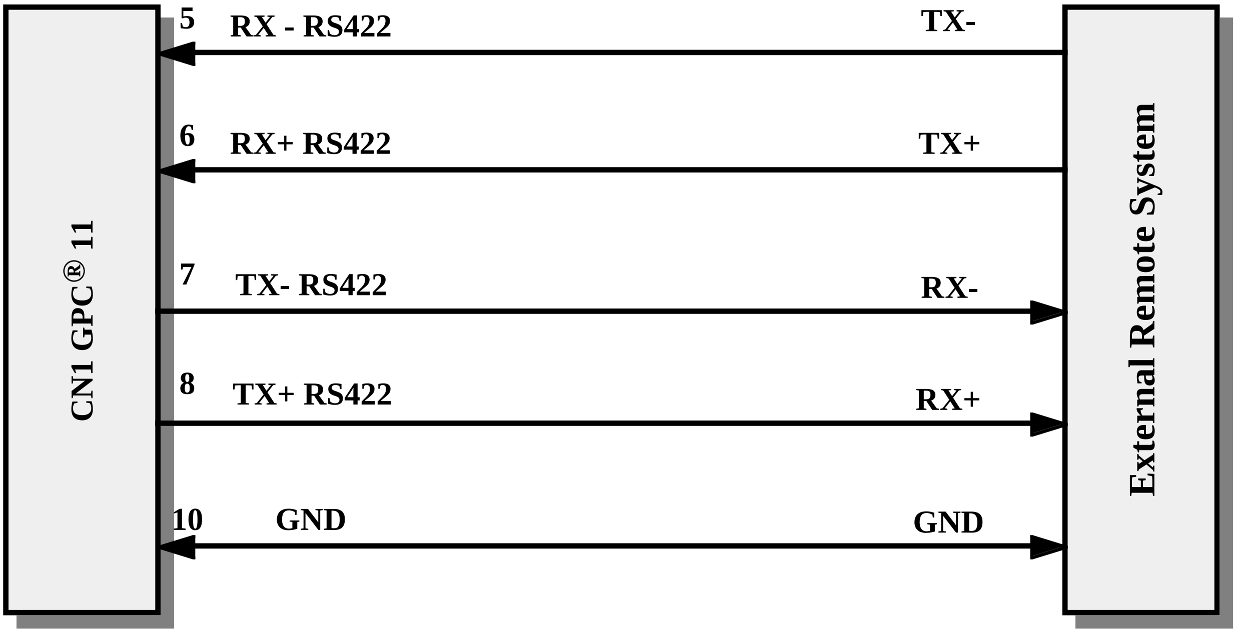


FIGURE 6: RS 422 POINT TO POINT CONNECTION EXAMPLE

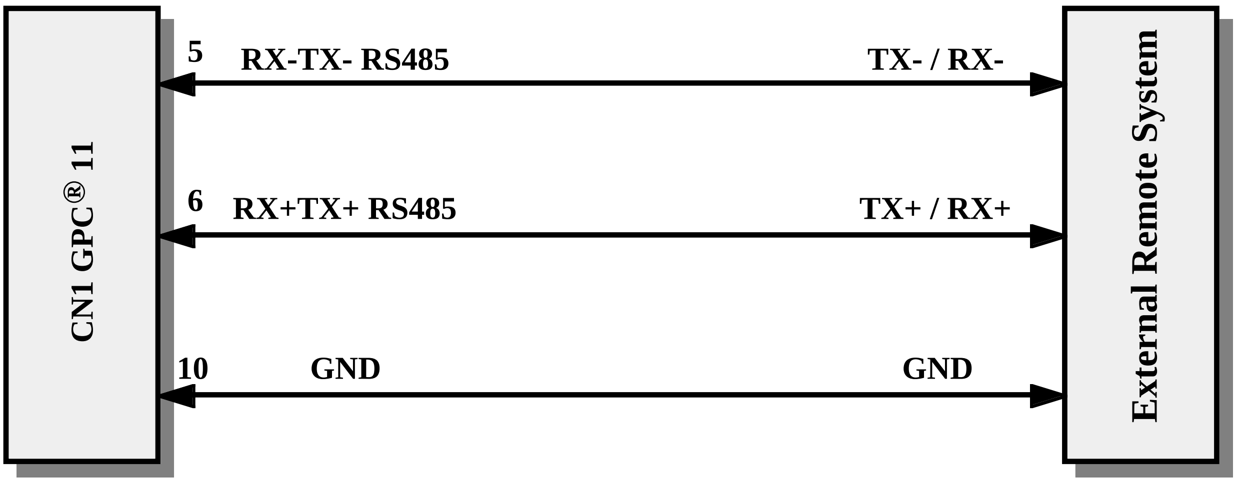


FIGURE 7: RS 485 POINT TO POINT CONNECTION EXAMPLE

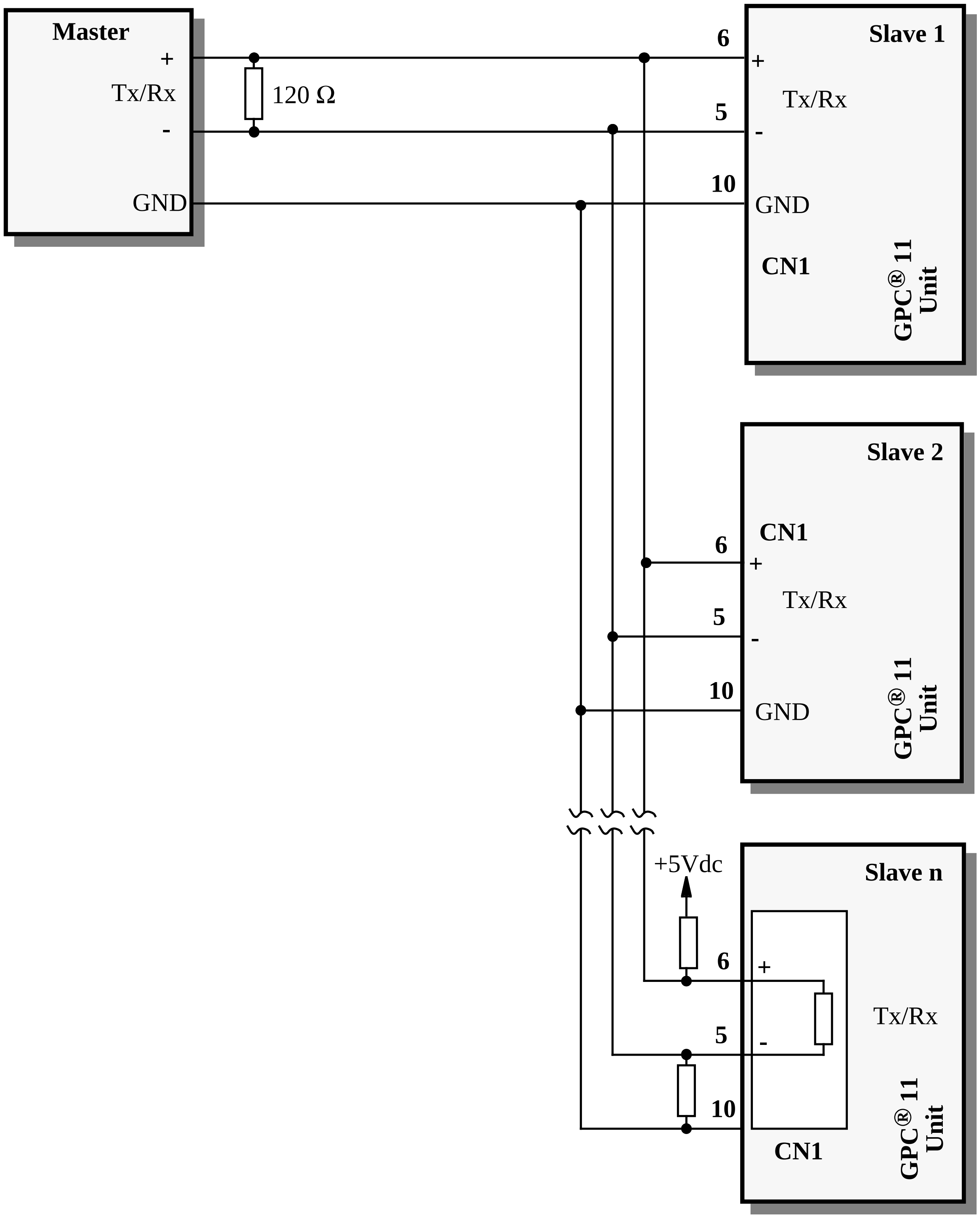


FIGURE 8: RS 485 NETWORK CONNECTION EXAMPLE

The user must always remember to connect at the communication line extremes, 2 line termination resistors (120 Ω) installed respectly near the master unit and near the farthest slave unit. One of the 120 Ω line termination resistor is already available on **GPC® 11**, while the pull up, pull down resistors (3,3 KΩ) must be connected externally, for example on CN1 connector.

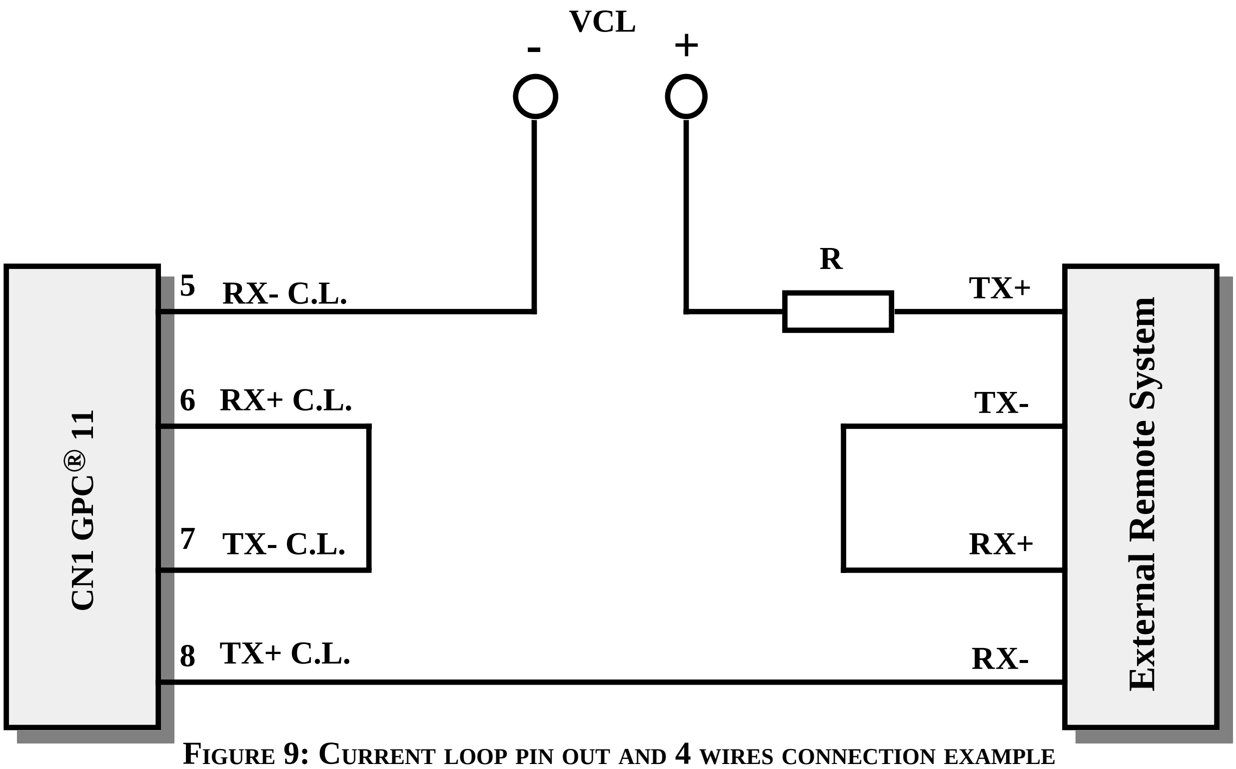


FIGURE 9: CURRENT LOOP PIN OUT AND 4 WIRES CONNECTION EXAMPLE

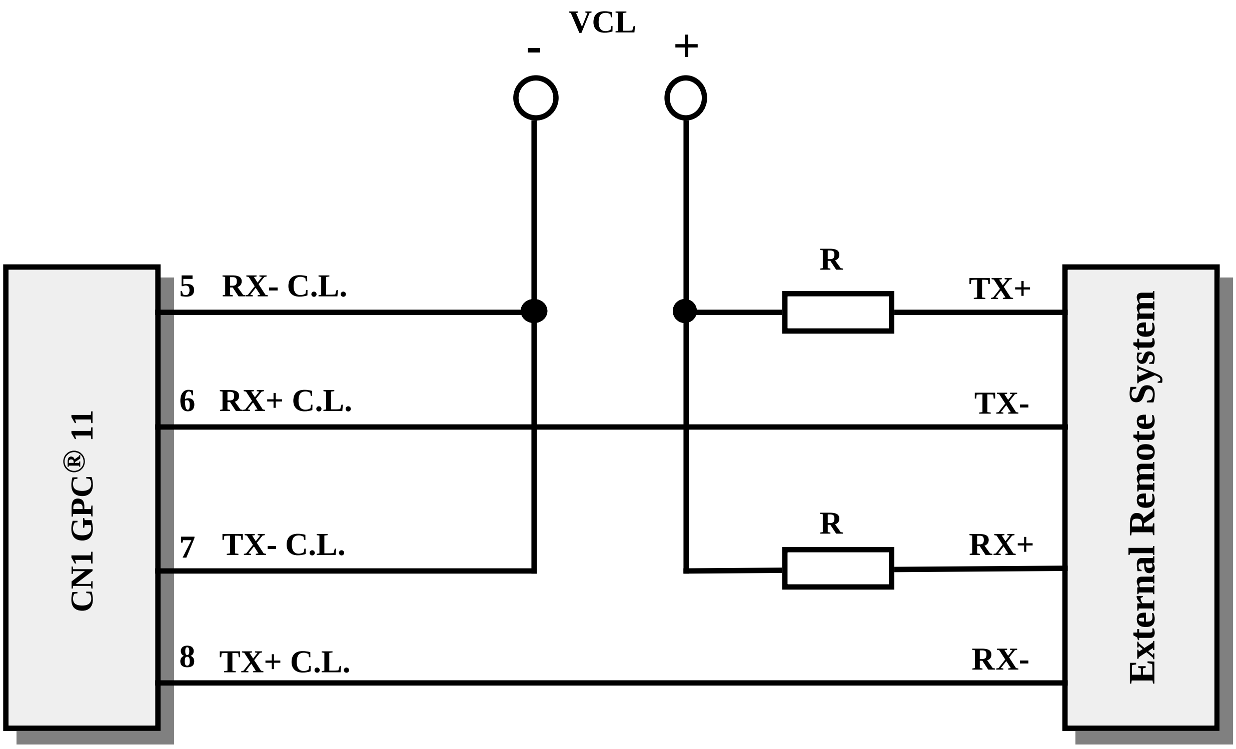


FIGURE 10: CURRENT LOOP PIN OUT AND 2 WIRES CONNECTION EXAMPLE

For current loop connection it is possible to get 2 differents type of connection: 2 and 4 wires. These kind of connections have been shown in the previous two drawings where the supply voltage (**VCL**) and the current limitation resistors (**R**) are reported. The supply voltage vary in compliance with the number of the devices connected. When the maximum of current (**20mA**) runs it must be guaranted that each device dissipates at maximum **125mW** for transmitter and **90mW** for receiver. The R resistor is needed for limiting the maximum of current in case of line short circuit. This is a **220Ω** resistor for a voltage of **VCL = +5 Vdc**.

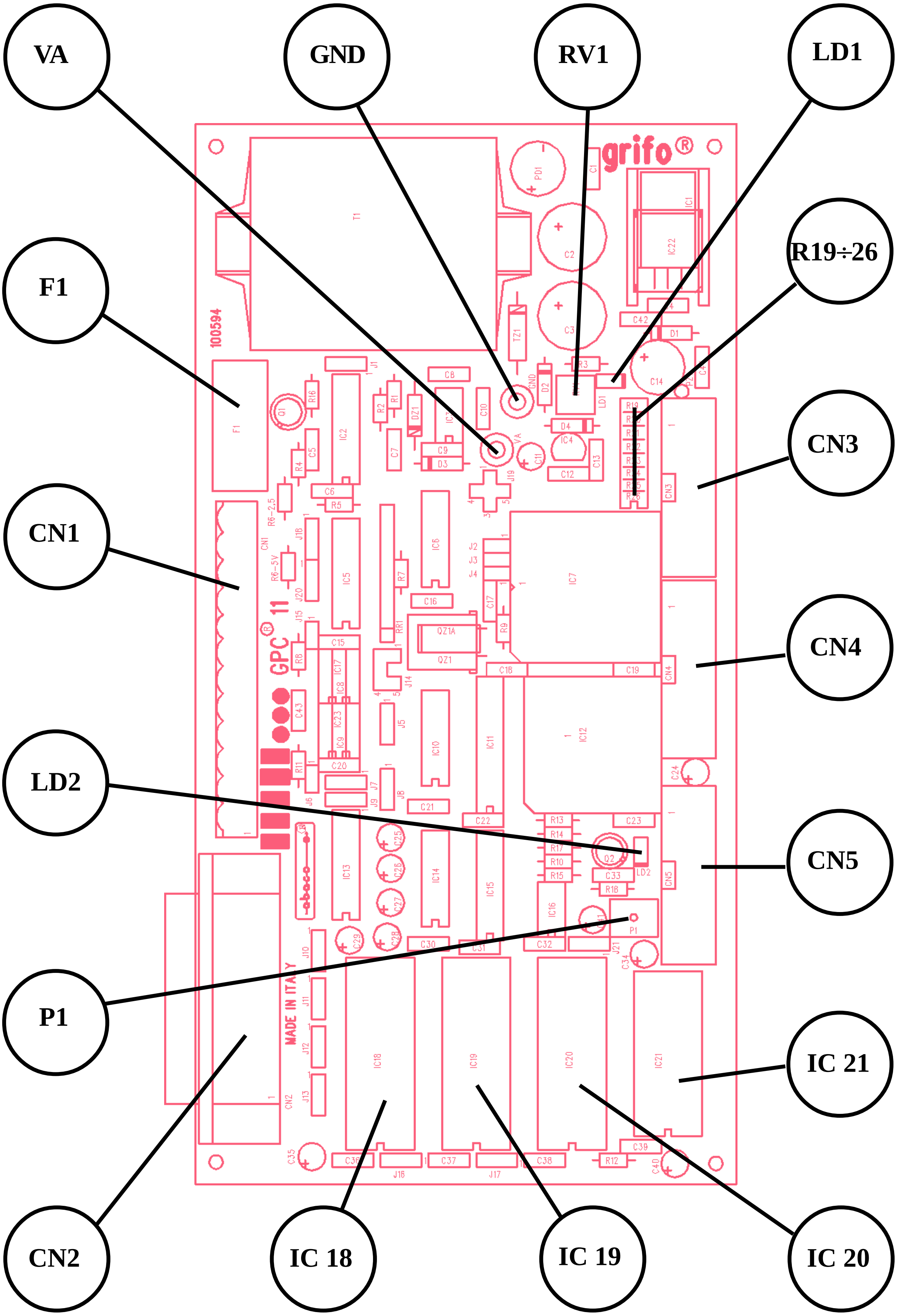


FIGURE 11: LEDS, MEMORIES, CONNECTORS, TEST POINT, ETC. LOCATION

CN3 - A/D CONVERTER CONNECTOR

CN3 is a 20 pins, male, vertical, low profile connector with 2,54 mm pitch.
On CN3 is available microprocessor port E; this port can be connected either to digital TTL inputs or analog signals for A/D converter section , thanks to its double functionality. Between CN3 and port E lines there is an optional current to voltage converter, as described in figure 13.
The analog inputs can be voltage inputs (0÷2,49V or 0÷5V) or current inputs (0÷20 mA or 4÷20 mA).

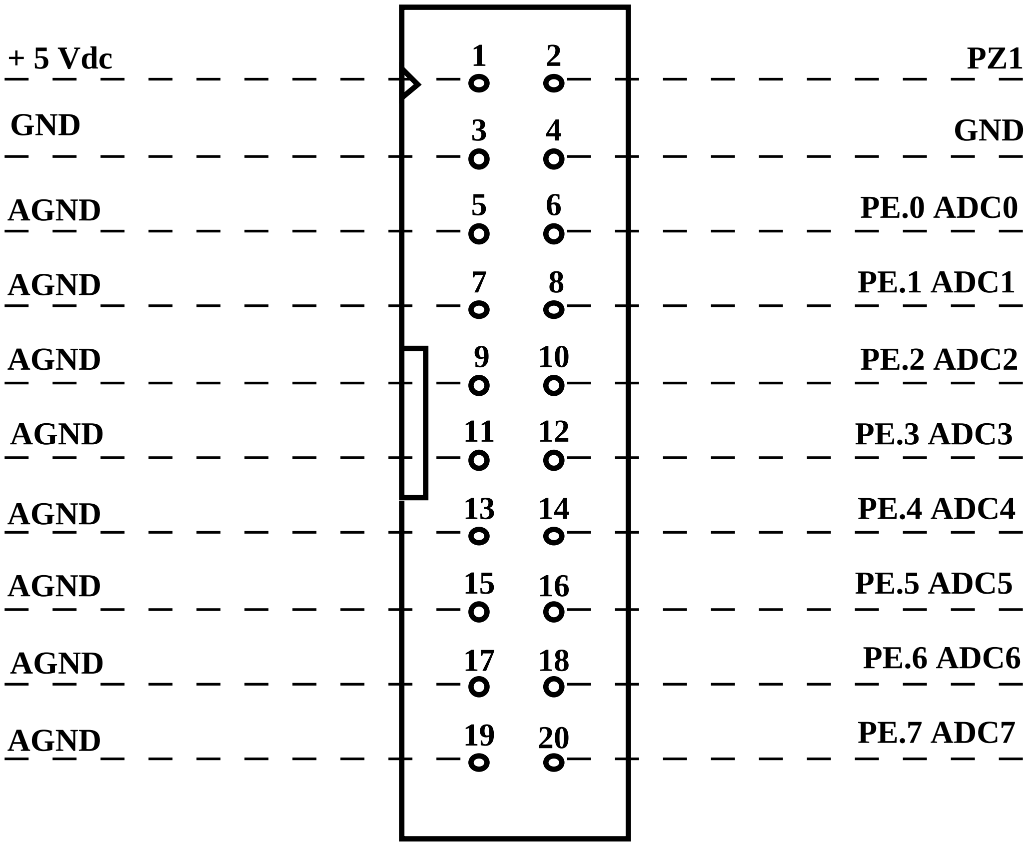


FIGURE 12: CN3- A/D CONVERTER CONNECTOR

Signals description:

PZ1	=		- Signal directly connected to PZ1 pad.
PE.n	=	I	- TTL digital line n of CPU port E.
ADCn	=	I	- Analog inputs n.
AGND	=		- Analog ground signal.
+5 Vdc	=	O	- +5 Vdc power supply.
GND	=		- Ground signal.

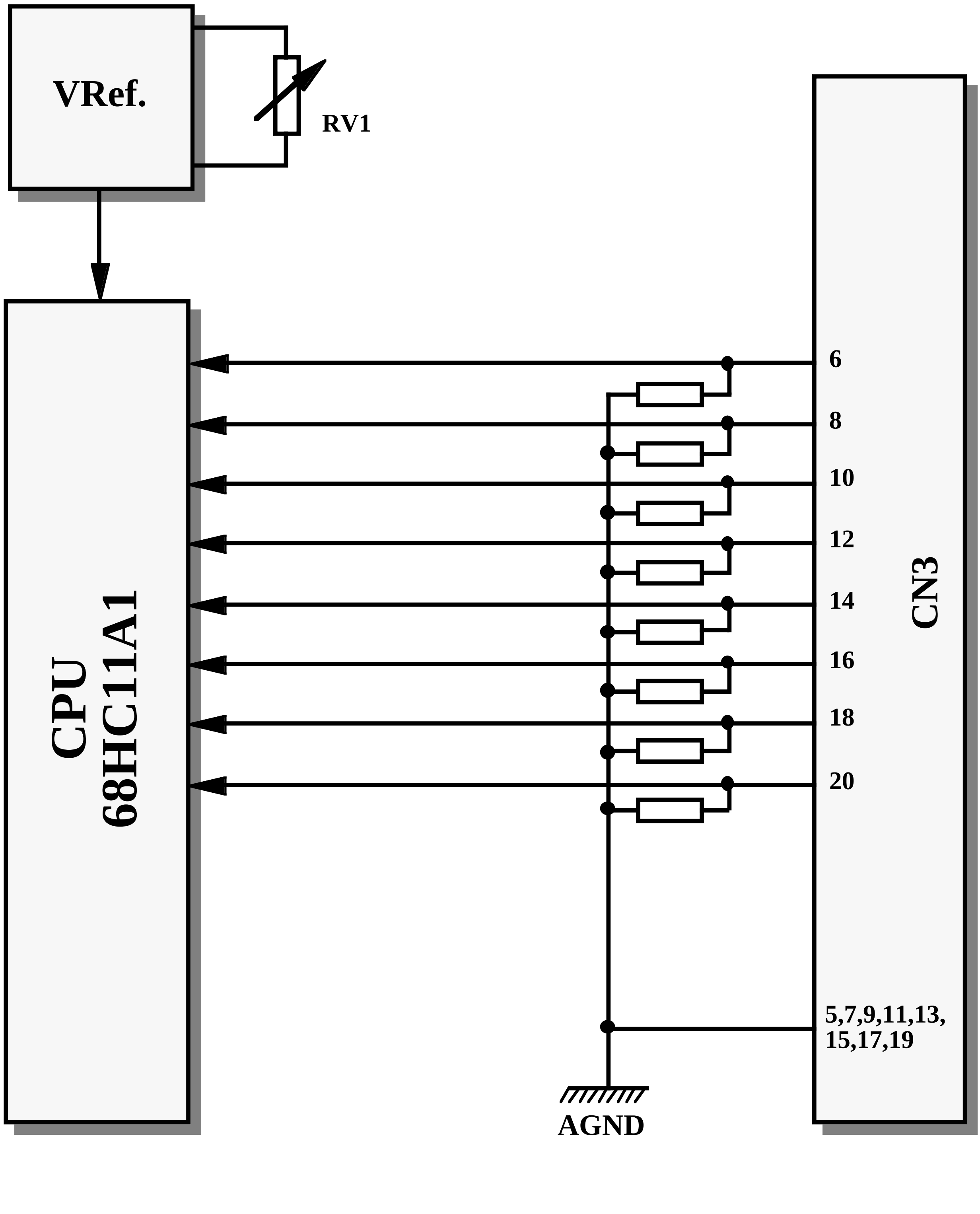


FIGURE 13: A/D CONVERTER INPUTS DIAGRAM

CN4 - 68HC11A1 I/O LINES CONNECTOR

CN4 is a 20 pins, male, vertical, low profile connector with 2,54mm pitch.
On CN4 are available microprocessor ports A and D, equal to 16 digital I/O lines. Please remember that some signals are used on board, in fact they have a double function; these lines are properly indicated in the following figure with two signal names. All the CN4 signals follow TTL standard and I/O **ABACO**® standard pin out.

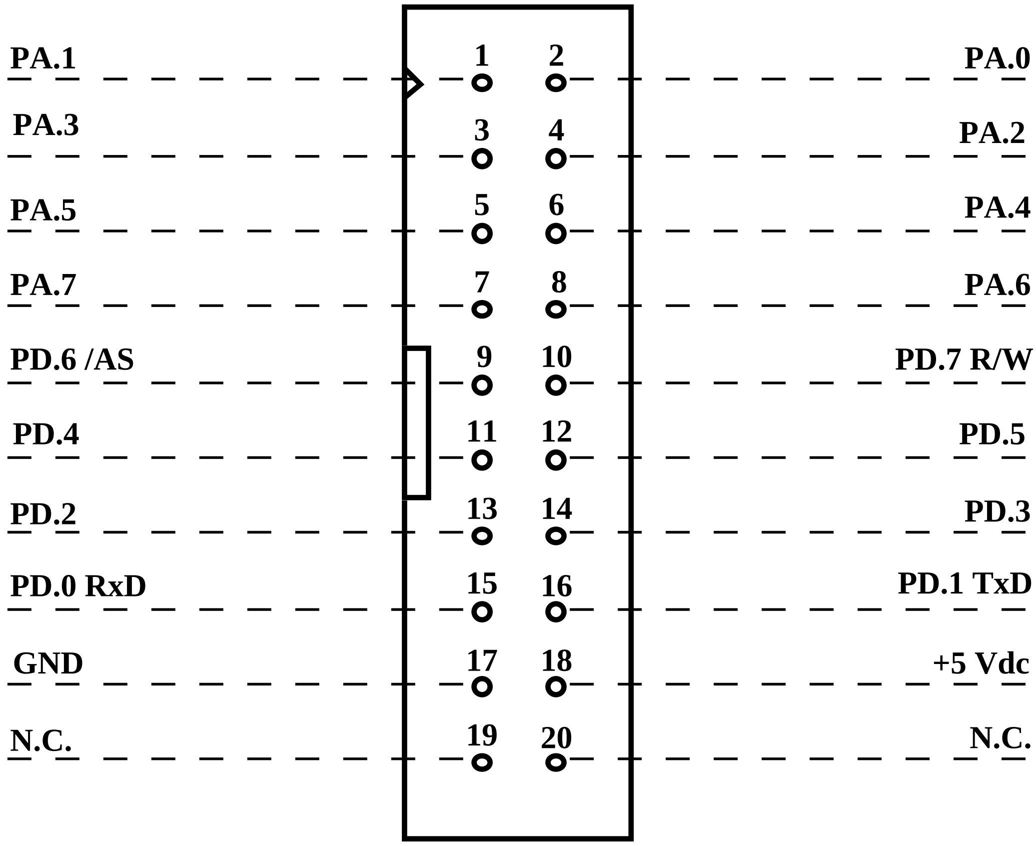


FIGURE 14: CN4 - 68HC11A1 I/O LINES CONNECTOR

Signals description:

PA.n	=	I/O	- Digital line n of CPU port A.
PD.n	=	I/O	- Digital line n of CPU port D.
RxD	=	I	- TTL receive signal of serial line.
TxD	=	O	- TTL transmit signal of serial line.
/AS	=	I	- TTL address strobe signal.
R/W	=	O	- TTL read write signal.
+5 Vdc	=	O	- +5 Vdc power supply.
GND	=		- Ground signal.
N.C.	=		- Not connected.

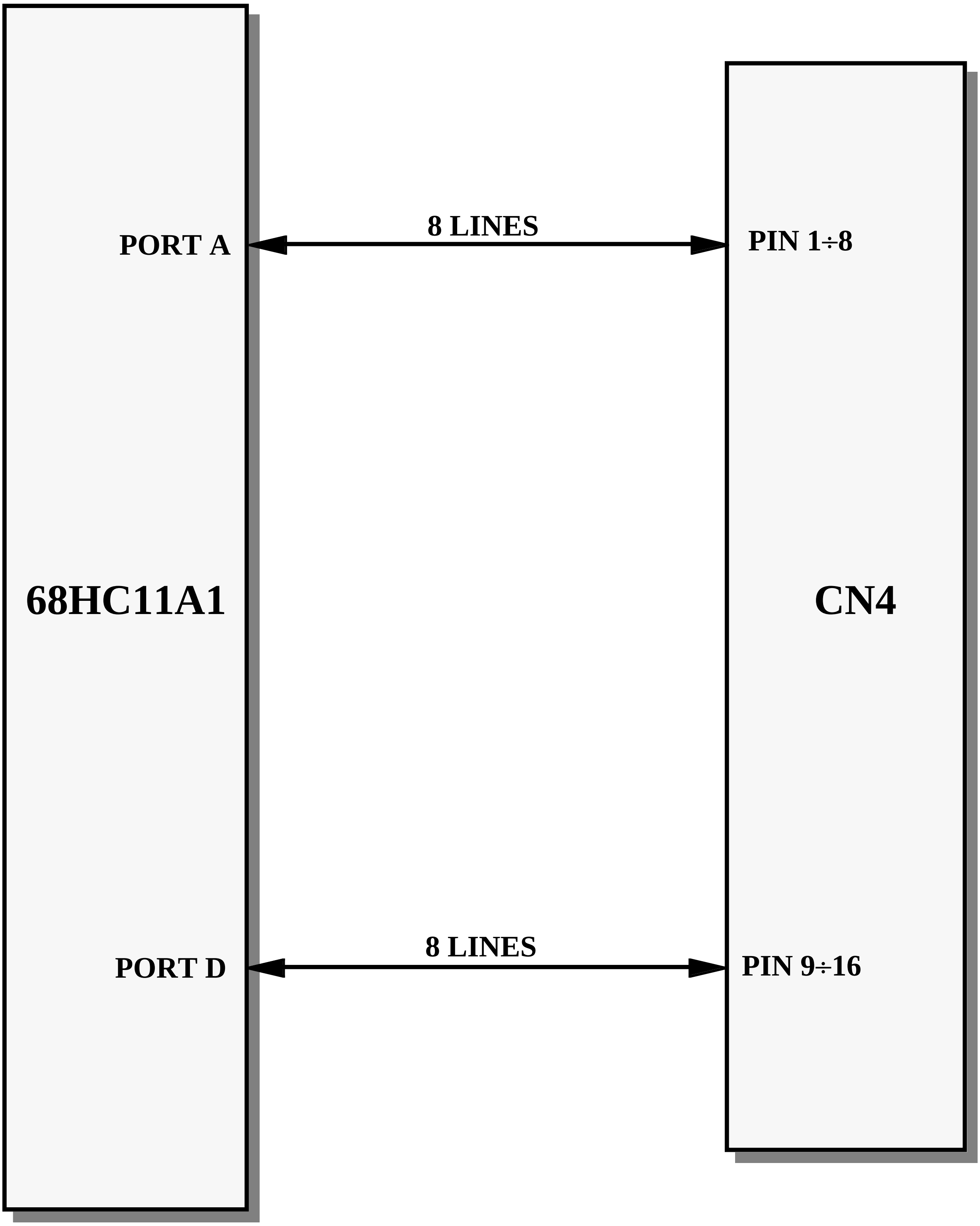


FIGURE 15: 68HC11A1 I/O LINES CONNECTION DIAGRAM

CN5 - 68HC24 I/O LINES CONNECTOR

CN5 is a 20 pins, male, vertical, low profile connector with 2,54mm pitch.
On CN5 are available the 68HC24 ports B and C, equal to 16 digital I/O lines. Please remember that some signals are used on board, in fact they have a double function; these lines are properly indicated in the following figure with two signal names. All the CN5 signals follow TTL standard and I/O **ABACO®** standard pin out.

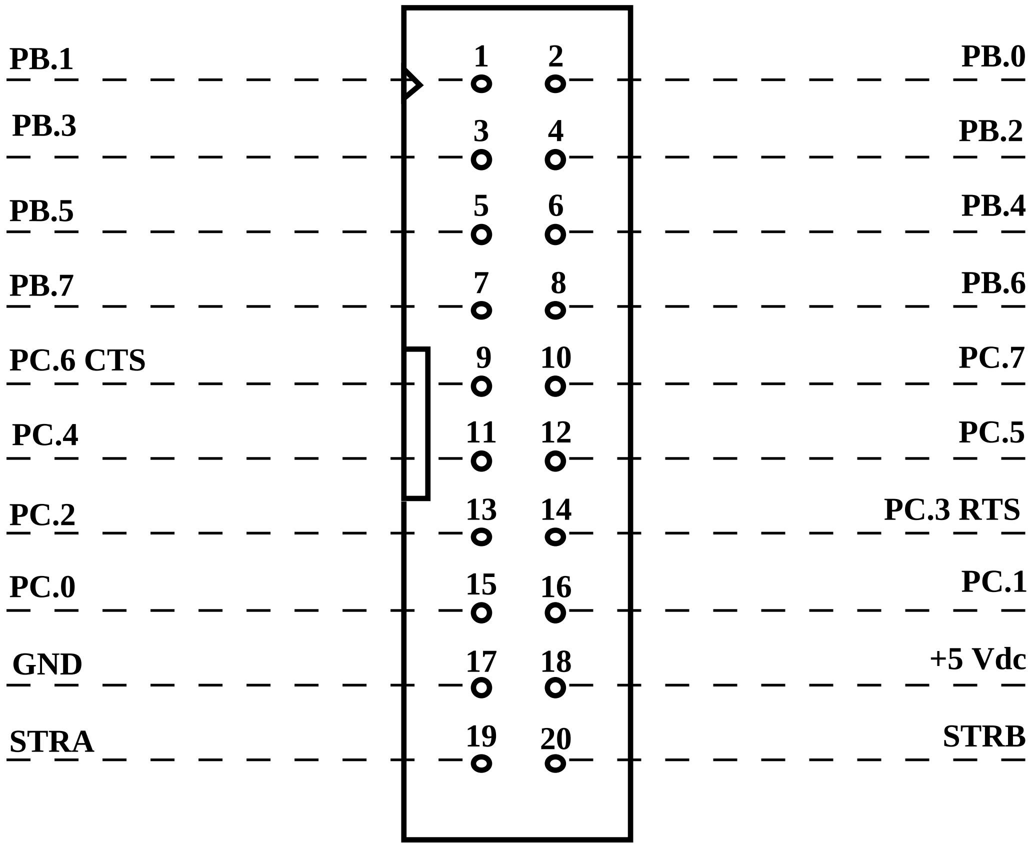


FIGURE 16: CN5 - 68HC24 I/O LINES CONNECTOR

Signals description:

PB.n	=	O	- Digital line n of 68HC24 port B.
PC.n	=	I/O	- Digital line n of 68HC24 port C.
CTS	=	I	- TTL clear to send handshake of serial line.
RTS	=	O	- TTL request to send handshake of serial line.
STRA	=	I	- TTL strobe signal for port C lines.
STRB	=	O	- TTL strobe signal for port B and C lines.
+5 Vdc	=	O	- +5 Vdc power supply.
GND	=		- Ground signal.

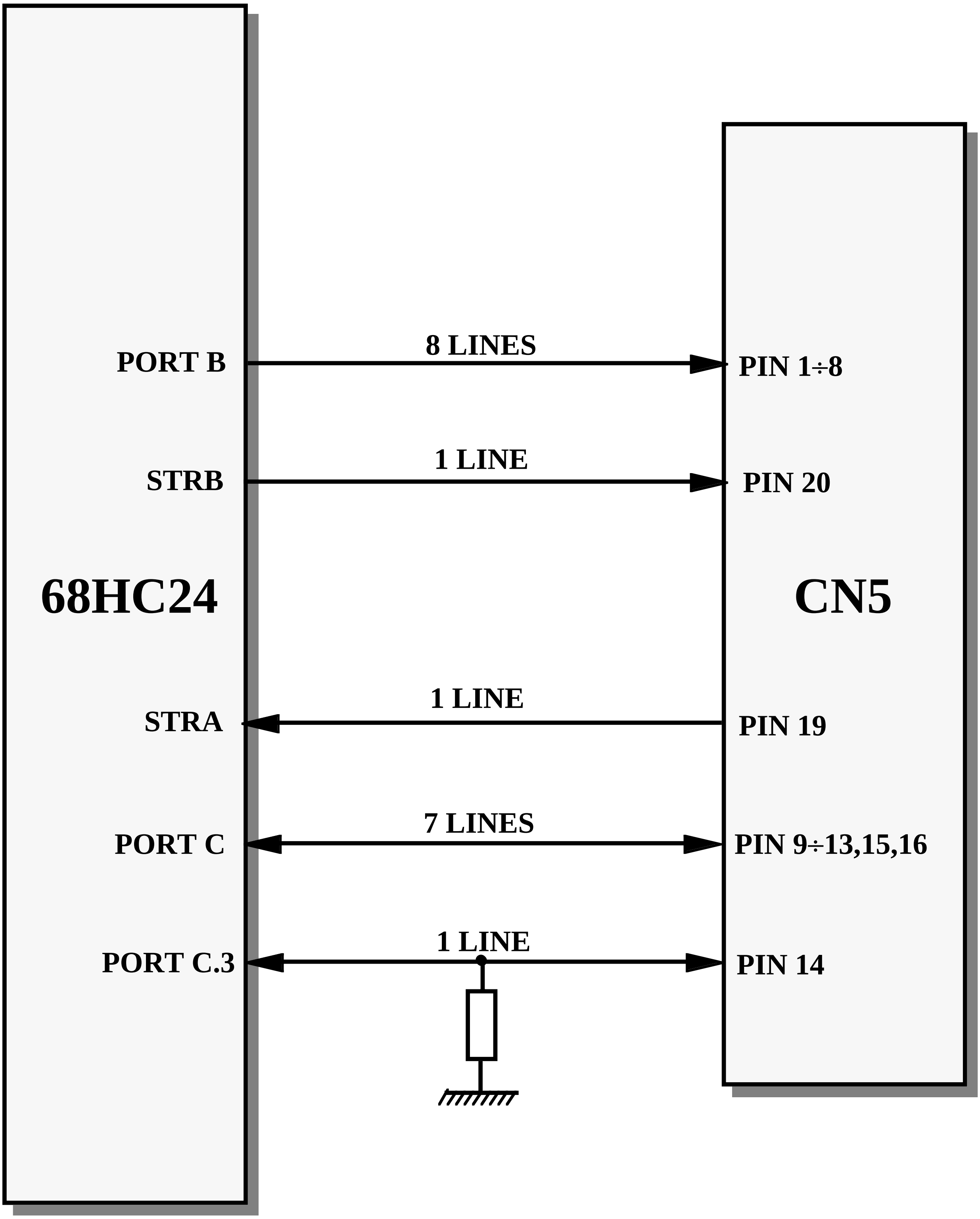


FIGURE 17: 68HC24 I/O LINES CONNECTION DIAGRAM

I/O CONNECTION

To prevent possible connecting problems between **GPC® 11** and the external systems, the user has to read carefully the information of the previous paragraphs and he must follow these instructions:

- For RS 232, RS 422, RS 485 and current loop communication signals the user must follow the standard rules of these protocols.
- For all TTL signals the user must follow the rules of this electric standard. The connected digital signal must be always referred to card digital ground and if an electric insulation is necessary, then an opto coupled interface must be connected. For TTL signals, the 0 Vdc level corresponds to logic state "0", while 5Vdc level corrisponds to logic state "1".
- The analog inputs (A/D section) must be connected to low impedance signals and with the ranges: 0÷2,49 Vdc or 0÷5,00 Vdc or 0÷20 mA according to card configuration.

TRIMMERS AND CALIBRATION

On **GPC® 11** is available a trimmer, named **RV1**, that calibrates the Vref voltage of the A/D converter section. Please refer to figure 11 for RV1 location.
The **GPC® 11** is subjected to a carefull test that verifies and calibrates all the card sections. The calibration is executed in laboratory, with a +20 C° room temperature, following these steps:

- The A/D voltage reference (Vref) is calibrated through RV1 trimmer, by using a 5 digits precision multimeter, to a value of +2,4900 Vdc or +5,0000 Vdc.
- The corrispondance between the analog input signal and the combination read from A/D is verified. This check is performed with a reference signal connected to A/D inputs and testing that the A/D combination and the teoric combination differ at maximum of the A/D section errors sum.
- The trimmer is blocked with paint.

On the card there are two test points, that can be used to measure the A/D reference voltage (Vref) with a tester. In details:

GND	->	Test point connected to VRL
VA	->	Test point connected to VRH

The analog interfaces use high precision components that are selected during mounting phase to avoid complicate and long calibration procedures. After the calibration, all the on board trimmer are blocked with paint to mantain calibration also in presence of mechanic stresses (vibrations, movings, delivery, etc.).
The reference voltage generation circuit defines the full scale value for all the 8 analog inputs, between the two available ranges: 0÷2,49 V or 0÷5,00 V. The full scale value must be specified at the moment of the order, in fact it requires different components and different calibration. If not stated, the standard full scale = 2,49 V is provided.
The user must not modify the card calibration, but if thermic drifts,time drifts, etc. make necessary a new calibration, he must strictly follow the previous described procedure.
To recognize trimmer and test points location on **GPC® 11**, please refer to figure 11.

ANALOG INPUTS SELECTION

One of the **GPC 11** particular features is the possibility to acquire tension and/or current signals for all the 8 A/D inputs. The user can specify the analog input type during the order phase and the current signals can be acquired through proper current to voltage conversion modules (based on high precision resistors) mounted on the card. In details there is the following correspondence:

R26	->	channel 0
R25	->	channel 1
R24	->	channel 2
R23	->	channel 3
R22	->	channel 4
R21	->	channel 5
R20	->	channel 6
R19	->	channel 7

If the resistor is not mounted (default) the channel can acquire a voltage signal in the range 0÷2,49 V (default) or 0÷5 Vdc, instead if the resistor is mounted the channel can acquire a current signal. The resistors value for the current to voltage converter section is calculated with the following formula: ***R = +2,49 V / Imax*** or ***R = +5 V / Imax***
Normaly the precision current to voltage resistor value is **124Ω** or **248Ω** suitable for 0÷20 mA analog inputs. Also the 4÷20 mA analog inputs can be acquired with the described current to voltage resistors but with this signals the resolution is lower than 8 bit, in fact some of the 256 points are lost. On the other hand, this tecnique allows a fast and easy recognition of any signal disconnection or probe break down.
Please refer to figure 11 for the resistors location.

POWER SUPPLY SELECTION

GPC® 11 is equipped with an efficient power supply circuit that makes the card connectable to any standard industrial source like mains, transformer, battery, solar cell, etc. The available power supply types are:

- *Standard power supply* = no option : in this case a 230 Vac, from mains, power supply voltage must be connected to pins 11 and 12 of CN1.
- *Low voltage switching power supply* = **.SW** option : in this case a 8÷26 Vac (or corresponding Vdc, i.e. +24 Vdc) power supply voltage must be connected to pins 11 and 12 of CN1.
- *Low voltage linear power supply* = **.12V** option : in this case a 6÷10 Vac (or corresponding Vdc, i.e. +12 Vdc) power supply voltage must be connected to pins 11 and 12 of CN1.
- *Without power supply* = **.5V** option : in this case a +5 Vdc power supply voltage must be connected to pins 9 and 10 of CN1.

Independently from the power supply type, on **GPC® 11** there is a protection aganist voltage peaks and noise, by **TransZorb**™.
The power supply type must be specified at the moment of the order, using the options before described, as if not stated, the standard configuration (220 Vac) is provided. The user can't change the power supply type in fact this configuration requires an hardware modification that must be performed by specialized **grifo®** technicians.

LEDS

On **GPC® 11** there are 2 LEDs that show some card status, as described in the following table:

LEDs	COLOR	FUNCTION
LD1	Red	Power supply indicator: it shows the presence of +5 Vdc.
LD2	Red	It signals activation of external watch dog circuit.

FIGURE 18: LEDS TABLE

The main function of LEDs is to inform the user about card status, with a simple visual indication and in addition to this, LEDs make easier the debug and test operations of the complete system. To recognize the LED location on the card, please refer to figure 11.

DIGITAL I/O INTERFACES

With CN4 and CN5 (standard **I/O ABACO®**connector) the **GPC® 11** can be connected to some of the numerous **grifo®** boards modules that have the same pin out. The connection of all these external modules is really simple in fact only a 20 ways flat cable (order code FLT.20+20) is necessary, that connects the power supply too. About software the use of digital I/O interfaces is likewise easy in fact **GPC® 11** software tools include proper drivers, library, example, etc.
Below there is a brief description of the supported interfaces:

- **QTP 16P**, **QTP 24P**, **KDx x24**, **DEB 01**, etc.: they are useful local operator panels. These boards already have all the resources (alphanumeric displays, matrix keyboards, LEDs etc) necessary to solve the common man machine communication problems at a short distance from **GPC® 11**. For software the programmer can use the relative procedure contained in all the **GPC® 11** software tools. These procedures normally are software drivers added to the language and they use directly its console instructions (for example INPUT and PRINT for BASIC, PRINTF and SCANF for C etc.), so for the user is very simple to write on displays and to get data from keyboards.
- **MCI 64**: it a large mass memory support that can directly manage the PCMCIA memory cards RAM, FLASH, ROM, etc.) in their available sizes. About software the developed drivers provide procedures to read and write data at a specified addressng, for the selected programming language.
- **IAC 01**, **DEB 01**: it is an interface for CENTRONICS parallel printer that can be connected with a standard printer cable. The printer is managed by software through the high level instructions of the selected programming language (PRINT for BASIC, PRINTF for C, WRITE for PASCAL, etc.).
- **RBO xx**, **TBO xx**, **XBI xx**, **OBI xx**: these are buffer interfaces for I/O TTL signals. With these modules the the TTL input signals are converted in NPN or PNP optoisolated inputs and the TTL output signals are converted in relays or transistor optoisolated outputs.

For further information about the digital I/O interfaces please read "EXTERNAL CARD" chapter and the software tools documentation.

JUMPERS

On **GPC® 11** there are 21 jumpers for card configuration. Connecting these jumpers, the user can define for example the memory type and size, the peripheral devices functionality and so on. Below there is the jumpers list, location and function:

NAME	PIN N°	FUNCTION
J1	3	It selects connection type of power failure circuit.
J2	2	It selects operating mode of PRU (MC68HC24).
J3,J4	2	They select operating mode of CPU (MC68HC11A1).
J5	3	It selects RS 422, RS 485 serial receive driver.
J6	2	It connects termination resistor to RS 422, RS 485 line.
J7	3	It selects connection of RS 232 RTS handshake.
J8	3	It selects connection of RS 232 CTS handshake.
J9	3	It selects electric protocol for serial communication.
J10	3	It selects DTE/DCE interface for CN2 pin 5.
J11	3	It selects DTE/DCE interface for CN2 pin 4.
J12	3	It selects DTE/DCE interface for CN2 pin 3.
J13	3	It selects DTE/DCE interface for CN2 pin 2.
J14	5	It selects RS 422 or RS 485 serial comunication.
J15	2	It connects termination resistor to RS 422 line.
J16	3	It selects size of IC 19 memory device.
J17	3	It selects size of IC 18 memory device.
J18	3	It defines map address of IC 18 memory device.
J19	5	It defines map address of IC 19 memory device.
J20	3	It defines map address of IC 20 memory device.
J21	3	It selects reset source.

FIGURE 19: JUMPERS SUMMARIZING TABLE

The following tables describe all the right connections of **GPC® 11** jumpers with their relative functions. To recognize these valid connections, please refer to the board printed diagram (serigraph) or to figure 26 of this manual, where the pins numeration is listed; for recognizing jumpers location, please refer to figure 22.

The "*" used in the following tables, denotes the default connection, or on the other hand the connection set up at the end of testing phase, that is the configuration the user receives.

2 PINS JUMPERS

JUMPER	CONNECTION	FUNCTION	DEF.
J2	not connected	It connects the MC68HC24 pin 43 to +5 Vdc, to select the "normal mode".	*
	connected	It connects the MC68HC24 pin 43 to GND, to select the "special test mode".	
J3	not connected	It connects the CPU pin 2 (MODB) to +5 Vdc, to define the operating mode.	*
	connected	It connects the CPU pin 2 (MODB) to GND, to define the operating mode.	
J4	not connected	It connects the CPU pin 3 (MODA) to +5 Vdc, to define the operating mode.	*
	connected	It connects the CPU pin 3 (MODA) to GND, to define the operating mode.	
J6	not connected	Termination resistor not connected to RS 422 receive line or RS 485 receive and transmit line.	*
	connected	Termination resistor connected to RS 422 receive line or RS 485 receive and transmit line.	
J15	not connected	Termination resistor not connected to RS 422 transmit line.	*
	connected	Termination resistor connected to RS 422 transmit line.	

FIGURE 20: 2 PINS JUMPERS TABLE

3 PINS JUMPERS

JUMPER	CONNECTION	FUNCTION	DEF.
J1	1-2	Power failure signal connected to CPU /XIRQ interrupt signal.	
	2-3	Power failure signal not connected.	*
J5	1-2	It selects IC 8 as the RS 422, RS 485 receive driver (only for **grifo**® internal use).	
	2-3	It selects IC 9 as the RS 422, RS 485 receive driver.	*
J7	1-2	The handshake RTS RS 232 is maintained active and it is not connected to PC.3=RTS signal.	*
	2-3	The handshake RTS RS 232 is connected to PC.3=RTS signal through an RS 232 driver.	

FIGURE 21: 3 PINS JUMPERS TABLE (1 OF 2)

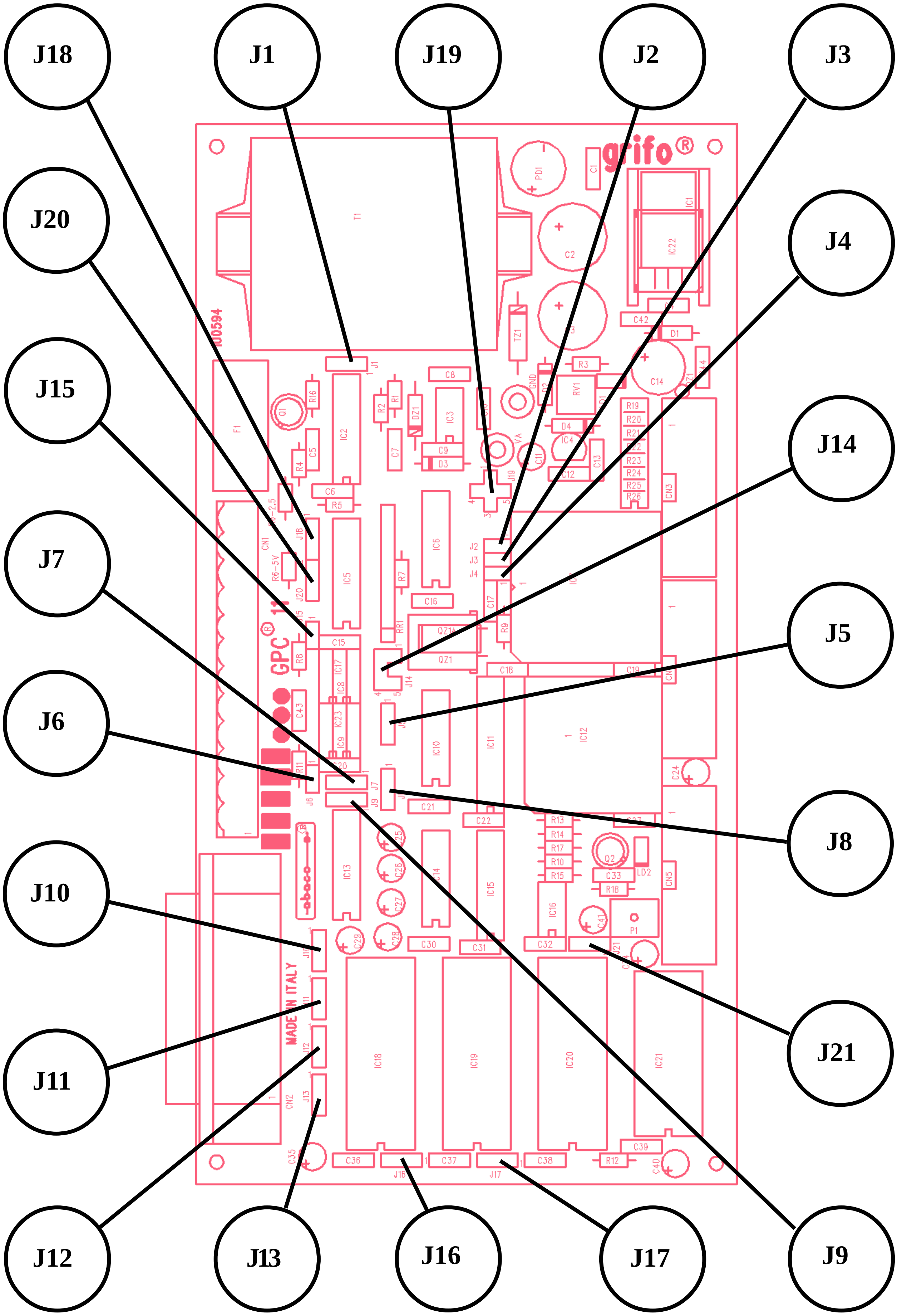


FIGURE 22: JUMPERS LOCATION

JUMPER	CONNECTION	FUNCTION	DEF.
J8	not connected	The PC.6=CTS and CTS RS232 handshake signals are not connected.	*
	1-2	The PC.6=CTS signal is connected to GND, to mantain it active.	
	2-3	The PC.6=CTS is connected to CTS RS232 handshake signal, through an RS 232 driver.	
J9	1-2	It selects an RS 422, RS 485, current loop serial communication.	
	2-3	It selects an RS 232 serial communication.	*
J10	1-2	It connects CN2 pin 5 to RTS RS232 signal (DCE).	
	2-3	It connects CN2 pin 5 to CTS RS232 signal (DTE).	*
J11	1-2	It connects CN2 pin 4 to CTS RS232 signal (DCE).	
	2-3	It connects CN2 pin 4 to RTS RS232 signal (DTE).	*
J12	1-2	It connects CN2 pin 3 to TxD RS232 signal (DCE).	
	2-3	It connects CN2 pin 3 to RxD RS232 signal (DTE).	*
J13	1-2	It connects CN2 pin 2 to RxD RS232 signal (DCE).	
	2-3	It connects CN2 pin 2 to TxD RS232 signal (DTE).	*
J16	1-2	It configures IC 19 for 8 Kbytes memory device.	
	2-3	It configures IC 19 for 32 Kbytes memory device.	*
J17	1-2	It configures IC 18 for 16 Kbytes memory device.	
	2-3	It configures IC 18 for 32 Kbytes memory device.	*
J18	1-2	It defines IC 18 memory addresses from C000H to FFFFH. Please read "MEMORY MAPS" paragraph.	*
	2-3	It defines IC 18 memory addresses from 8000H to FFFFH. Please read "MEMORY MAPS" paragraph.	
J20	1-2	It defines IC 20 memory addresses from 2000H to 3FFFH. Please read "MEMORY MAPS" paragraph.	*
	2-3	It defines IC 20 memory addresses from 0000H to 1FFFH. Please read "MEMORY MAPS" paragraph.	
J21	1-2	P1 button and watch dog circuit are used as reset sources.	
	2-3	Only P1 button is used as reset source.	*

FIGURE 23: 3 PINS JUMPERS TABLE (2 OF 2)

5 PINS JUMPER

JUMPER	CONNECTION	FUNCTION	DEF.
J14	1-2 and 3-4	It configures serial line for RS 422 electric standard (4 wires).	*
	2-3 and 4-5	It configures serial line for RS 485 electric standard (2 wires).	
J19	1-2	It defines IC 19 memory addresses from 4000H to 5FFFH. Please read "MEMORY MAPS" paragraph.	
	3-2	It defines IC 19 memory addresses from 0000H to 7FFFH. Please read "MEMORY MAPS" paragraph.	
	4-2	It defines IC 19 memory addresses from 4000H to BFFFH. Please read "MEMORY MAPS" paragraph.	*
	5-2	It defines IC 19 memory addresses from 4000H to BFFFH. Please read "MEMORY MAPS" paragraph.	

FIGURE 24: 5 PINS JUMPERS TABLE

INTERRUPTS MANAGEMENT

One of the most important **GPC® 11** features is the powerfull interrupts management. The card generates only one interrupt source from its on board power failure circuit and thanks to J1 jumpers this interrupt source can be connected to CPU not maskable interrupt (/XIRQ). The power failure circuit activates the interrupt signal when the first half period of the Vac power voltage is missed; so the /XIRQ signal is always enabled before than 40 msec from the power supply failure and it is kept active. The CPU has a sufficient time period to execute all the necessary procedures for the upcoming power off management, in fact the on board power supply circuit can mantain a valid +5 Vdc for a time longher than 40 msec.
Moreover all the CPU internal peripheral devices (timer counter, serials, port, etc.) can generate interrupts requests. For further information about all internal interrupts and the interrupt mangement by the CPU, please refer to specific documentation of the manufacturing company.

ON BOARD INPUT

GPC® 11 card is equipped with the J6 jumper can be used as on board input acquired by software, in fact it is connected to 68HC24 PC.6 that is mantained low if the jumper is in position 1-2 and viceversa mantained high if it is not connected. This input is normally used for system configuration (operating mode selection, card number programmation inside a network system, fimware configuration, etc.).

MEMORY SELECTION

On **GPC® 11** can be mounted 74K bytes of memory divided in several configurations, as described in the following table:

IC	DEVICE	SIZE	JUMPER CONFIGURATION
18	EPROM	16K Bytes	J17 in 1-2
	EPROM	32K Bytes	J17 in 2-3
19	RAM, backed RAM	8K Bytes	J16 in 1-2
	RAM, backed RAM, EEPROM	32K Bytes	J16 in 2-3
20	RAM, backed RAM	8K Bytes	-
21	RAM, backed RAM	2K Bytes	-

FIGURE 25: MEMORY SELECTION TABLE

All the sockets follow the JEDEC standard, so the mounted memory devices must have JEDEC pin outs. The jumpers configurations described on figure 25 only prearrange the sockets for the indicated memory devices, but there are some other jumpers that set the memory addressing map; for this information, please refer to "MEMORY MAPS" paragraph.
The 2K and 8K Bytes backed RAM modules can also include the real time clock option.
Normally **GPC® 11** is supplied in its default configuration with 32K RAM on IC 19; each different configurations can be defined during order phase or self mounted by the user. Below are reported the abbrevation code of the possible memory options:

.2KMOD	->	2K x 8 backed RAM
.8KMOD	->	8K x 8 backed RAM
.2KRTC	->	2K x 8 backed RAM with real time clock
.8KRTC	->	8K x 8 backed RAM with real time clock
.32KMOD	->	32K x 8 backed RAM
.32EE	->	32K x 8 parallel EEPROM

For further information and prices please contact directly **grifo®**.

POWER ON AND RESET

GPC® 11 has a reset and power on circuit that manages the always hard phase of card power up and start. This circuit has the following features:

- Fixed power on time, defined by a proper on board RC circuit;
- reset source from on board P1 push button;
- reset source from on board watch dog circuit;
- reset circuit output connected to all the card's section;

As before described the J21 jumper let the user define if the watch dog circuit can reset the card or not. This jumper is really usefull during debug phase, in fact the user can disconnect the watch dog when the application program is not running (code download, trace, etc.).

SERIAL COMMUNICATION SELECTION

An asyncronous serial line is available on **GPC® 11** and it can be buffered in RS 232, RS 422, RS 485 or current loop.
By hardware can be selected which one of these electric standards is used, through jumpers connection (as described in the previous tables) and drivers installation. Please refer to APPENDIX A for serial jumpers and serial drivers location.
By software the serial line can be programmed to operate with all the standard physical protocols, in fact the bits per character, parity, stop bits and baud rates can be setted by software.
In the following paragraphs there are all the informations on serial communication configurations.

RS 232 WITH HANDSHAKE

J5	=	don't care	IC8	=	don't care
J7	=	connected in 2-3 position	IC9	=	don't care
J8	=	connected in 2-3 position	IC 13	=	MAX 232 driver
J9	=	connected in 2-3 position	IC 17	=	don't care
J14	=	don't care	IC 23	=	don't care

The handshakes CTS RS232 and RTS RS232 are driven throgh the PC.6=CTS and PC.3=RTS signals of MC68HC24. In this condition this signals on CN5 must be not connected.

RS 232 WITHOUT HANDSHAKE

J5	=	don't care	IC8	=	don't care
J7	=	connected in 1-2 position	IC9	=	don't care
J8	=	not connected	IC 13	=	MAX 232 driver
J9	=	connected in 2-3 position	IC 17	=	don't care
J14	=	don't care	IC 23	=	don't care

In this condition the PC.6 and PC.3 signals on CN5 can be used as normal digital I/O lines.

CURRENT LOOP

J5	=	don't care	IC8	=	no component
J7	=	connected in 1-2 position	IC9	=	no component
J8	=	not connected	IC 13	=	don't care
J9	=	connected in 1-2 position	IC 17	=	HCPL4100 driver
J14	=	don't care	IC 23	=	HCPL4200 driver

In this condition the serial line is connected by using the CN1 pins 5, 6, 7, 8. and the PC.6 and PC.3 signals on CN5 can be used as normal digital I/O lines. The current loop serial line is passive, so during connection the user must provide an external power supply.

RS 485

J5	=	connected in 2-3 position	IC8	=	don't care
J7	=	don't care	IC9	=	SN75176 driver
J8	=	not connected	IC 13	=	don't care
J9	=	connected in 1-2 position	IC 17	=	no component
J14	=	connected in 2-3 and 4-5 position	IC 23	=	no component

The serial line is connected by using the CN1 pins 5, 6 that are either receive or transmit signals, according to PC.3 status, defined by software through the MC68HC24. The RS 485 line is used in 2 wires multipoint communication network in fact :

PC.3 = high level = 1 logic state -> card transmit on RS 485 line
PC.3 = low level = 0 logic state -> card receive from RS 485 line

Furthermore when RS485 is selected all the transmitted characters are, at the same time, received; in this way the line conflict can be immediately recognized by testing the received character after each transmission. In this condition the PC.6 signal on CN5 can be used as normal digital I/O line while the PC.3 signals must be not connected.

RS 422

J5	=	connected in 2-3 position	IC8	=	SN75176 driver
J7	=	don't care	IC9	=	SN75176 driver
J8	=	not connected	IC 13	=	don't care
J9	=	connected in 1-2 position	IC 17	=	no component
J14	=	connected in 1-2 and 3-4 position	IC 23	=	no component

The serial line is connected by using the CN1 pins 5, 6, 7, 8. For point to point connection the PC.3 signal can be kept high, instead for multipoint network the transmit driver must be disabled when the card has no data to send. With PC.3 signal the user enables or disables the transmitter driver, through the MC68HC24, setted by software:

PC.3 = high level = 1 logic state -> RS 422 transmit driver enabled
PC.3 = low level = 0 logic state -> RS 422 transmit driver disabled

In this condition the PC.6 signal on CN5 can be used as normal digital I/O line while the PC.3 signals must be not connected.

After a reset or power on, PC.3 signal is asserted low (0) by a dedicated pull down resistor maintaining enabled RS 485 reception and mantaining disabled the RS 422 transmission; in this way each conflict on the serial network is eliminated.
With jumpers J6 and J15 the RS 422 line or the RS 485 line can be terminated with a suitable resistors. The line termination must be added only at the beginning and at the end of the physical line, by connecting the jumpers. Normally these jumpers must be connected in point to point networks, or on the farthest cards in multipoints networks.

CN2 PIN OUT

The CN2 is a 25 pins female D connector that can be configurated with two different RS 232 standard pin outs. The jumpers J10, J11, J12, J13 selects a DTE (Data Terminal Equipment) or a DCE (Data Communication Equipment) interface as below described:

J10, J11, J12, J13 connected in 1-2 position -> DCE interface
J10, J11, J12, J13 connected in 2-3 position -> DTE interface

Thanks to this standard interfaces, the **GPC® 11** can be directly connected to any RS 232 serial devices (terminal, modem, personal computes, etc.) by using low cost pin to pin communication cable. For further information please refer to "3 PINS JUMPERS" and "CN2 - RS 232 SERIAL COMMUNICATION CONNECTOR" paragraphs.

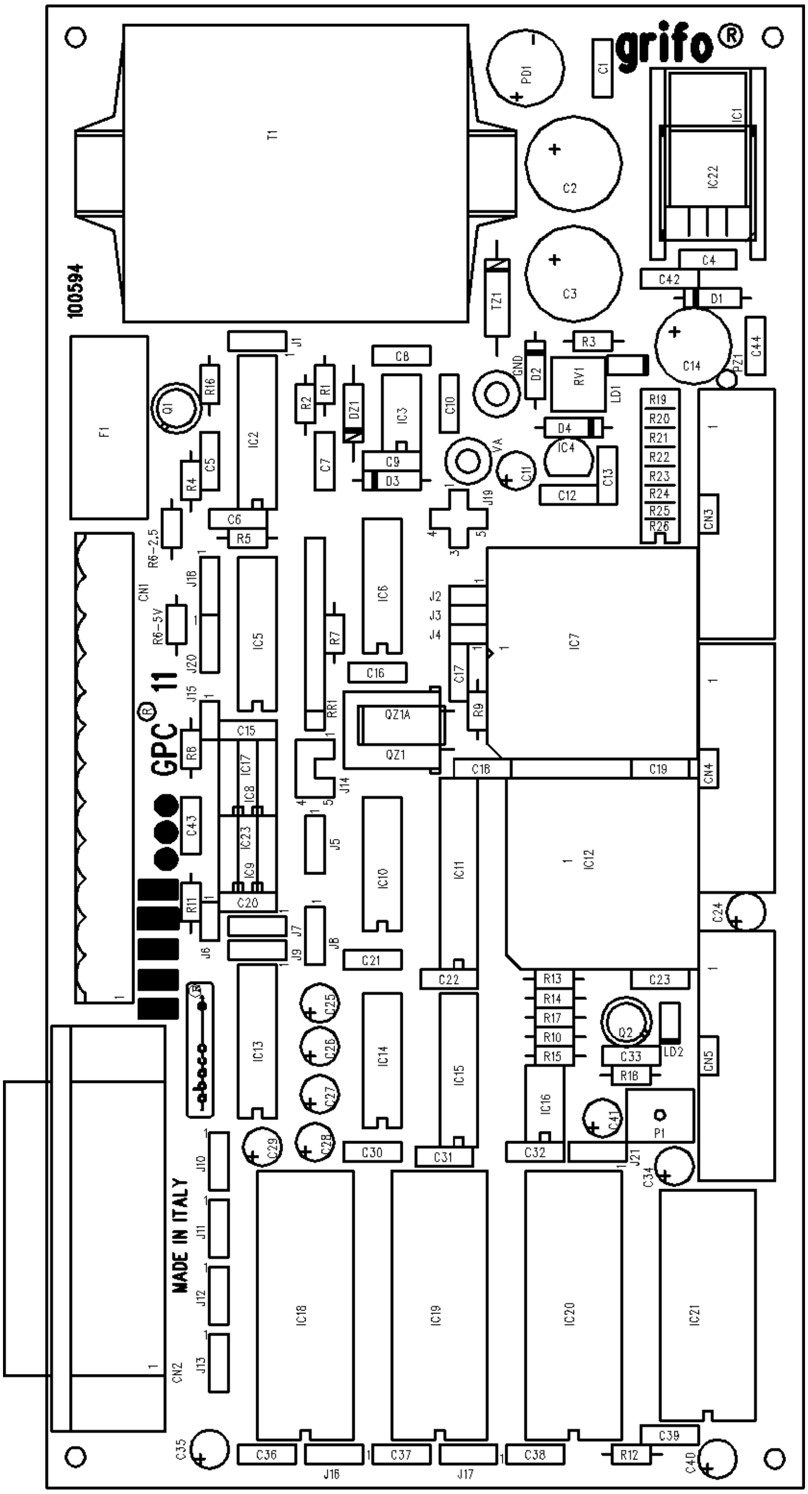


FIGURE 26: COMPONENTS MAP

OPERATING MODE SELECTION

The **GPC® 11** is provided of three jumpers that define the operating mode of some on board components. In details these modes can be selected for the 68HC11A1 CPU and 68HC24 PRU, as described in the following table:

DEVICE	MODE	J2	J3	J4
68HC11A1	Special bootstrap	-	Connected	Connected
	Special test	-	Connected	Not connected
	Single chip	-	Not connected	Connected
	Expanded multiplexed	-	Not connected	Not connected
68HC24	Special test	Connected	-	-
	Normal	Not connected	-	-

FIGURE 27: OPERATING MODE TABLE

When the single chip mode is selected, after a reset or power on the card executes the BUFFALO monitor debugger program, saved on 68HC11A1 inside ROM. It is sufficient to connect a personal computer to RS 232 serial line and use a communication program (i.e. GET11 available on web) at 9600 Baud.
For further information please refer to specific documentation of the manufacturing company.

SOFTWARE

A wide selection of software development tools can be obtained, allowing use of the module as a system for its own development, both in assembler and in other high level languages; in this way the user can easily develop all the requested application programs in a very short time. Generally all software packages available for the mounted microprocessor, or for the '11 family, can be used.

KERNEL: complete development tools for real time, control and data acquisition system. The software tools is saved on EPROM, while the developed application program can be either in RAM (debug phase) or EPROM (final installation). It works with an external communication program, executed on standard personal computer, connected through RS 232 serial line. The software tools is provided of standard function library.

BUFFALO: monitor debugger program ables to work in all the 68HC11 opearting modes and it can load and debug each code written for this microprocessor microprocessor family. It is provided of the standard commands available on hardware in circuit emulator and requires only an external P.C. connected through a serial line. BUFFALO is supplied on EPROM and floppy disk.

ROM BUFFALO: it has the same features of BUFFALO but it is available only on 68HC11A1 microprocessor, in fact it is saved on its internal ROM. For further information please read "OPERATING MODE SELECTION" paragraph.

CONTROL PASCAL: it is a cross compiler that uses a subset of PASCAL instructions, capables to generate code for **GPC® 11**. It is a powerful software tool that includes editor, PASCAL compiler and assembler executed on standard personal computer. The obtained code can be executed directly on the card thanks to a proper interactive program, saved on EPROM, that includes a run time module too.

C I.A.S.: it is a C cross compiler, capables to generate code for **GPC® 11**. It is a powerful software tool that includes editor,translator, C compiler and assembler executed on standard personal computer. The obtained code can be executed directly on the card thanks to a proper interactive program, saved on EPROM, that includes a run time module too. Inside the software tools there are a complete list of library functions that manage the card resource.

BASIC 11: complete development tools for MCS BASIC (interpreted BASIC language for industrial application). It needs a personal computer for console and program saving operations, while the debug, test and program operations are performed on the card. Special instructions which manage the on board peripheral devices have been added.

ICC 11: cross compiler for C source program. It is a powerful software tool that includes editor, C compiler, assembler, linker, library, simulator and remote symbolic debugger (when coupled with NOICE11), included in an easy to use integrated development environment for Windows. Library source are included and floating point is supported.

NO ICE 11: It is a personal computer hosted debugger consists of a target specific DOS program, NOICExxx.EXE, and a target resident monitor program. The two programs comunicate via RS 232. NOICE includes: source level debug; a disassembler; a file viewer; memory display and editing; a virtually unlimited number of breakpoints; hardware free single step; definition of symbols; the ability to record and play back files of commands; on line help.

HI TECH C 11: cross compiler for C source program. It is a powerful software tool that includes editor, C compiler, assembler, optimizer, linker, library, project manager, and remote symbolic debugger, in one easy to use integrated development environment for DOS. Library source are included and floating point is supported.

DDS MICRO C 11: low cost ross compiler for C source program. It is a powerful software tool that includes editor, C compiler, assembler, optimizer, linker, library, and remote debugger, in one easy to use integrated development environment. There are also included the library sources and many utilities programs; floating point is not supported.

GET 11: it is a complete program with editor, communication driver and mass memory management for all '11 family cards. This program developed by **grifo®** allows to operate in the best conditions when BASIC 11, BUFFALO, ROM BUFFALO software tools are used.

All the described software tools can be supplied either on EPROM that must be mounted on **GPC® 11**, or a list of programs directly executable on personal computer and the technical documentation. For further information on this software packages please refer to proper software manual or visit **grifo®** web site, where some demo version are available.
Any software tools requires a suited memory configuration as described in the "MEMORY MAPS" paragraph.

ADDRESSES AND MAPS

INTRODUCTION

In this chapter are reported all information about card use, related to hardware and software. For example, the registers addresses and the memory allocation are described below.

ON BOARD RESOURCES ALLOCATION

The card devices addresses are managed by a specific control logic, realized with CMOS gates. This control logic allocates memory and peripheral devices in a comfortable mode for the user. The microprocessor addresses 64K bytes of memory and the control logic maps the on board memory and peripheral devices, inside these address space. Control logic sets size, type and addresses of memory devices through jumpers J2÷J4 and J16÷J20; at the same time it allocates a fixed address for on board resorce management and it avoids any conflict with the other CPU internal peripheral devices. Summarizing the control logic allocates:

- up to 32K bytes of EPROM on IC 18;
- up to 32K bytes of RAM, EEPROM on IC 19;
- 8K bytes of RAM on IC 20;
- 2K bytes of RAM (with optional RTC) on IC 21;
- external watch dog;

The addresses of all these devices are described in the following paragraphs and can't be set with different value.

MEMORY MAPS

Actually on **GPC® 11** are available many different memory maps, as previously described in the jumpers table figures.
About the most frequently used and most usefull memory configurations, the following paragraphes contain: a graphic description, the J18, J19, J20 jumpers setting, the used software tools, some notes and the addresses used for on board resources. The not described jumpers don't care the memory maps; only the J16 and J17 select memories size and type, as described on figure 25.
It is a good practise to allocate the microprocessor internal resources (registers, RAM, EEPROM, etc.) in the not used areas; please remember that this relocation is allowed only during the first 64 clock cycles, after a reset or power on.

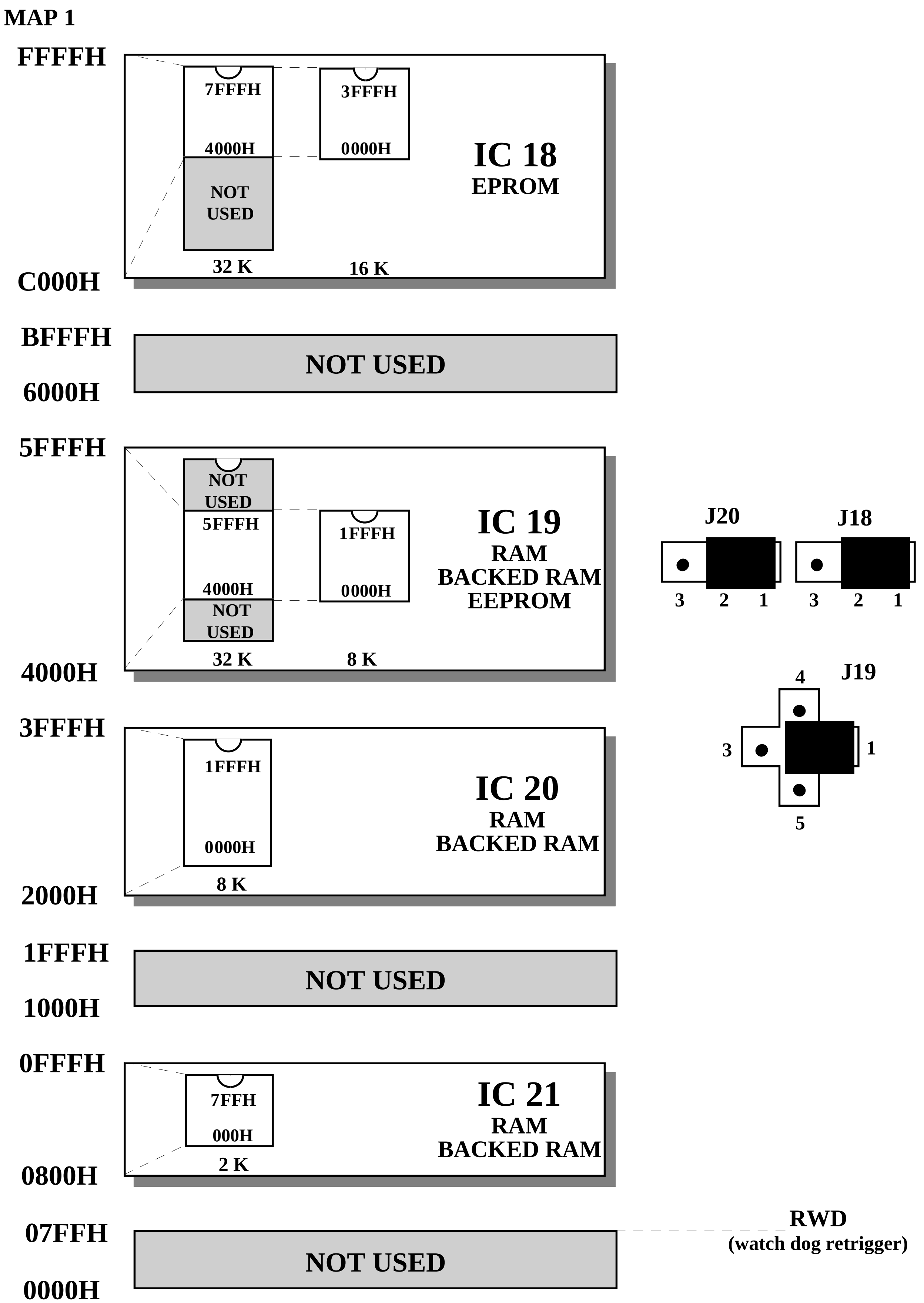


FIGURE 28: MEMORY MAP 1

Used by software tools as: NO ICE11, BUFFALO.
None of the internal microprocessor devices (registers, RAM, EEPROM) must be relocated.

MAP 2

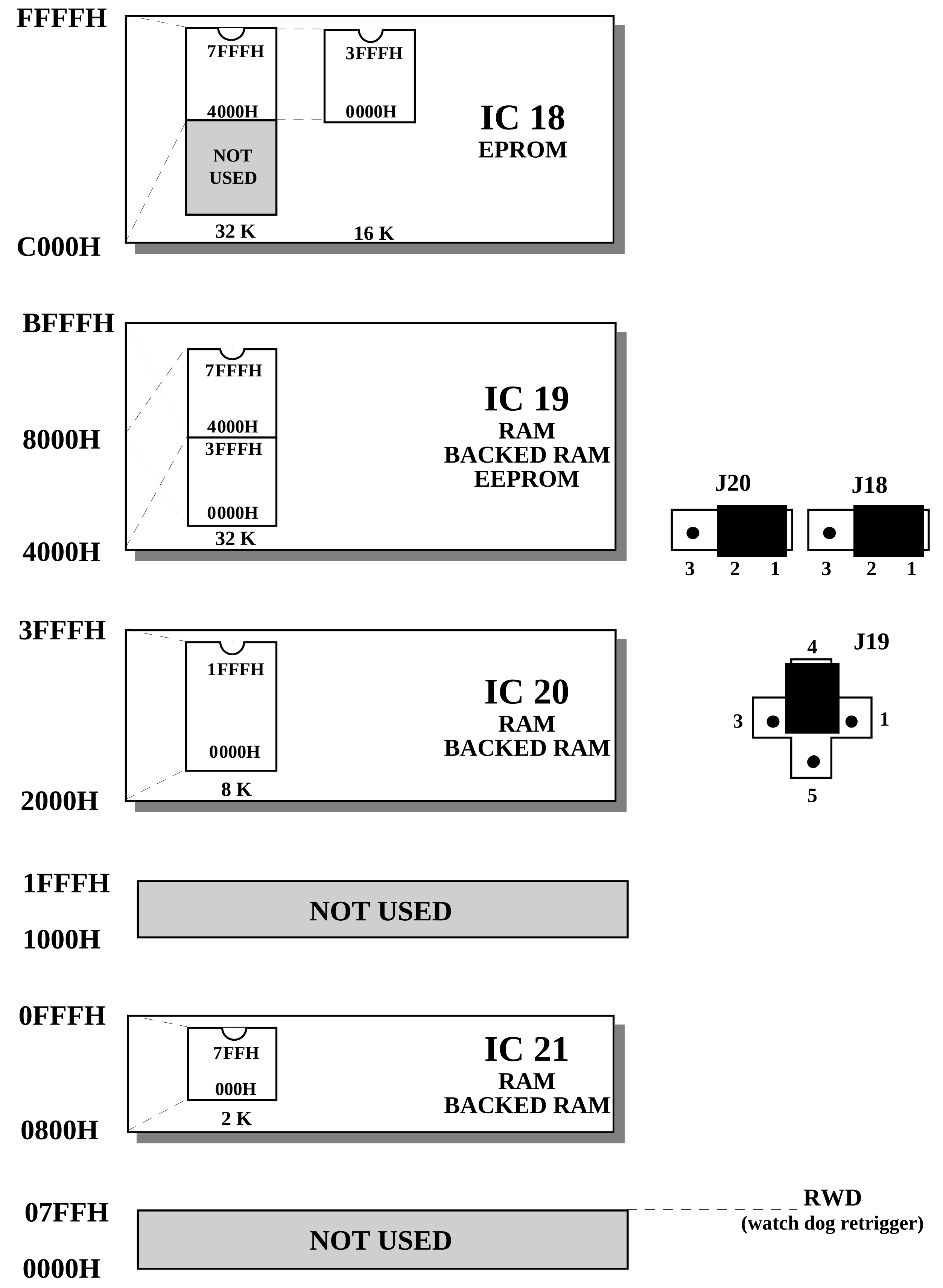


FIGURE 29: MEMORY MAP 2

Used by software tools as: NO ICE11, BUFFALO, BASIC 11.
The internal microprocessor EEPROM must be relocated on the free areas.

MAP 3

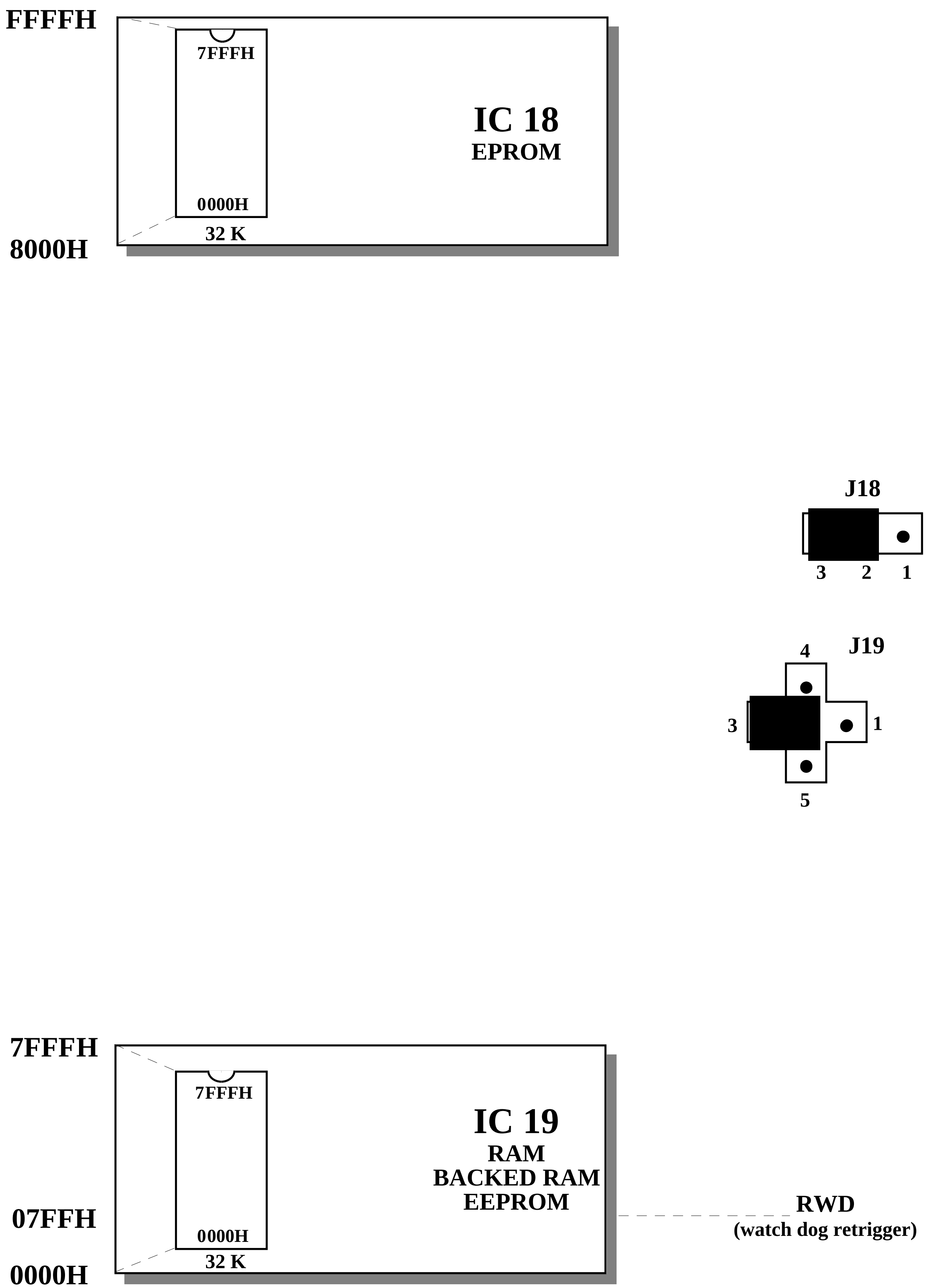


FIGURE 30: MEMORY MAP 3

Used by software tools as: CONTROL PASCAL, HI TECH C 11, ICC 11, DDS MICRO C 11.
All the internal microprocessor devices (registers, RAM, EEPROM) are overlapped.

PERIPHERAL DEVICES SOFTWARE DESCRIPTION

In the previous paragraphes are described the on board devices addresses, while in this one there is a specific description of registers meaning and function. For the microprocessor internal devices, for the MC68HC24 port replacement unit, not described in this chapter, or for any detailed information, please refer to manufacturing company documentation.

EXTERNAL WATCH DOG

Retrigger operation of **GPC® 11** external watch dog circuit is performed with a simple read operation at the address of RWD register (07FFH). This register shares the same address of other on board peripherals, but no conflict are generated in fact retrigger operation is an input operation and the read data has no meaning.
To avoid external watch dog activation it is necessary to retrigger its circuit at regular time periods and the duration of these periods must be smaller than intervention time. If retrigger doesn't happen as before described and J21 is connected in position 1-2, when intervention time is elapsed, the card is reset. The default intervention time is about 800 msec.

BACKED RAM + RTC

This peripheral device is addressed in a 2K or 8K Bytes contiguous area; each bytes inside this area can be either read or write through standard memory operation at the addresses described in the previous chapter.
When the used module is a backed RAM device provided of real time clock, eight internal registers must be used to set and acquire time and data. These registers always are the last eight addresses of the device size, as described in the following table:

REGISTER	ADDRESS
CNT	<LAST ADDRESS> - 7
SEC	<LAST ADDRESS> - 6
MIN	<LAST ADDRESS> - 5
HOU	<LAST ADDRESS> - 4
WEE	<LAST ADDRESS> - 3
DAY	<LAST ADDRESS> - 2
MON	<LAST ADDRESS> - 1
YEA	<LAST ADDRESS> - 0

FIGURE 31: RAM+RTC REGISTERS ADDRESSES TABLE

With these registers the backed RTC can be read (acquisition of actual time and date), wrote (programmation of new time and date), started, stopped, etc. by using simple and fast memory operations.

<reg.>	= D7	D6	D5	D4	D3	D2	D1	D0
YEA	**= Y7**	**Y6**	**Y5**	**Y4**	**Y3**	**Y2**	**Y1**	**Y0**

where: Y7÷Y0 = BCD year value (00-99)

<reg.>	= D7	D6	D5	D4	D3	D2	D1	D0
MON	**= 0**	**0**	**0**	**M4**	**M3**	**M2**	**M1**	**M0**

where: M4÷M0 = BCD month value (01-12)

<reg.>	= D7	D6	D5	D4	D3	D2	D1	D0
DAY	**= 0**	**0**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**

where: D5÷D0 = BCD day of the month value (01-31)

<reg.>	= D7	D6	D5	D4	D3	D2	D1	D0
WEE	**= 0**	**FT**	**0**	**0**	**0**	**W2**	**W1**	**W0**

where:

W2 W1 W0	= Day of the week value:
0 0 1	= Sunday
0 1 0	= Monday
0 1 1	= Tuesday
1 0 0	= Wednesday
1 0 1	= Thursday
1 1 0	= Friday
1 1 1	= Saturday
FT	= Counter frequency test

<reg.>	= D7	D6	D5	D4	D3	D2	D1	D0
HOU	**= KS**	**0**	**H5**	**H4**	**H3**	**H2**	**H1**	**H0**

where:
KS = RTC counter start
H5÷H0 = BCD hour value (00-23)

<reg.>	= D7	D6	D5	D4	D3	D2	D1	D0
MIN	**= 0**	**M6**	**M5**	**M4**	**M3**	**M2**	**M1**	**M0**

where: M6÷M0 = BCD minutes value (00-59)

<reg.>	= D7	D6	D5	D4	D3	D2	D1	D0
SEC	**= ST**	**S6**	**S5**	**S4**	**S3**	**S2**	**S1**	**S0**

where:
S6÷S0 = BCD seconds value (00-59)
ST = RTC counter stop

<reg.>	= D7	D6	D5	D4	D3	D2	D1	D0
CNT	**= W**	**R**	**S**	**C4**	**C3**	**C2**	**C1**	**C0**

where:
W = Write operation selection
R = Read operation selection
S = Sign bit of compensation combination
C4÷C0 = Compensation combination

The right initialization procedure for real time clock, must execute the following steps:

1) Set W bit to 1
2) Reset ST bit to 0
3) Set KS bit to 1
4) Reset W bit to 0
5) Wait 2 second
6) Set W bit to 1
7) Reset KS bit to 0
8) Set the required new data and hour
9) Reset W bit to 0

For further information about RTC use, please refer to manufacturing company documentation.

FIGURE 32: CARD PHOTO

EXTERNAL CARDS

GPC® 11 can be connected to a wide range of **grifo®** cards and to many system of other companies. Hereunder these cards are listed, for further information please call **grifo®** or visit web sites.

OBI 01 - OBI 02
Opto BLOCK Input NPN-PNP
Interface between 16 NPN, PNP optocoupled and displayed input lines, with screw terminal and **ABACO®** standard I/O 20 pins connector; power supply section; connection for DIN Ω rails.

OBI N8 - OBI P8
Opto BLOCK Input NPN-PNP
Interface between 8 NPN, PNP optocoupled and displayed input lines, with screw terminal and **ABACO®** standard I/O 20 pins connector; power supply section; connection for DIN Ω rails.

TBO 01 - TBO 08
Transistor BLOCK Output
Interface for **ABACO®** standard I/O 20 pins connector; 16 or 8 transistor output lines 45 Vdc 3 A open collector; screw terminal; optocoupled and displayed lines; connection for DIN 247277-1 and 3 rails.

RBO 01
Relé BLOCK Output
Interface for **ABACO®** standard I/O 20 pins connector; 8 displayed 5A or 10A relays; screw terminal; connection for DIN Ω rails.

RBO 08 - RBO 16
Relé BLOCK Output
Interface for **ABACO®** standard I/O 20 pins connector; 8 or 16 displayed Relays 3A with MOV; screw terminal; connection for DIN Ctype and Ω rails.

XBI 01
miXed BLOCK Input Output
Interface for **ABACO®** standard I/O 20 pins connector; 8 transistor output lines 45 Vdc 3A; 8 input lines; screw terminal; optocoupled and displayed I/O lines; connection for DIN 247277-1 and 3 rails.

XBI R4 - XBI T4
miXed BLOCK Input-Output
Interface for **ABACO®** standard I/O 20 pins connector; 4 Relays 3A with MOV or 4 optocoupled Transistors 3A open collectors; 4 input lines optocoupled; screw terminal; connection for DIN Ctype and Ω rails.

FBC xxx
Flat Block Contactxxx pins
This interconnection system "wire to board" allows the connection to many type of flat cable connectors to terminal for external connections. Connection for DIN Ω rails.

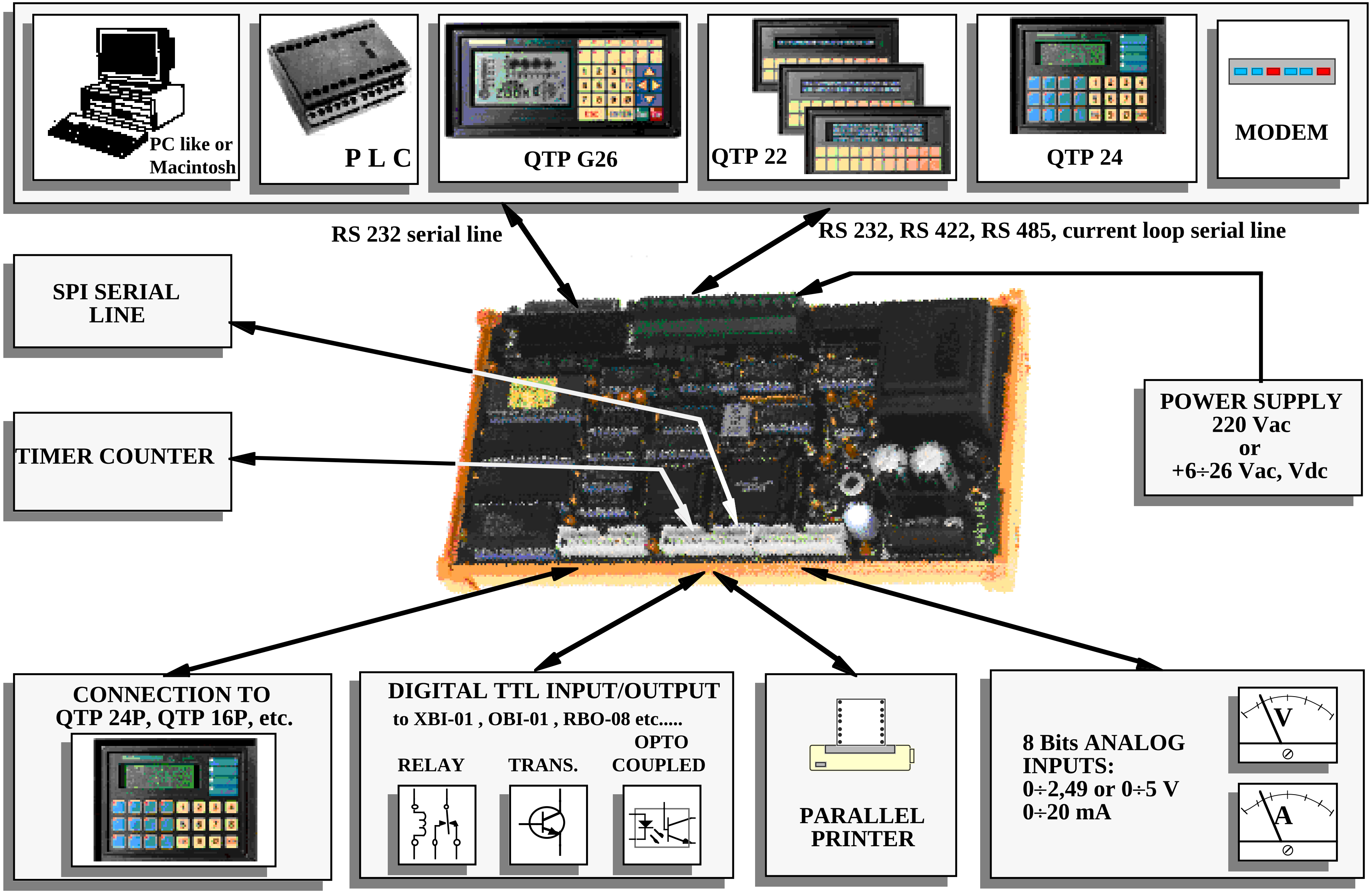


FIGURE 33: GPC® 11 AVAILABLE CONNECTIONS DIAGRAM

IBC 01

Interface Block Comunication

Conversion card for serial communication, 2 RS 232 lines; 1 RS 422-485 line; 1 optical fibre line; selecatble DTE/DCE interface; quick connection for DIN 46277-1 and 3 rails.

MCI 64

Memory Cards Interfaces 64 MBytes

Interfacing card for managing 68 pins PCMCIA memory cards, it is directly driven from any **ABACO®** I/O standard connector; High level languages GDOS supported.

KDL xxx - KDF xxx

Keyboard Display interface - LCD or Fluorescent

Interface with Fluorescent or LCD display, LEDs backlit, 20x2 or 20x4 characters; up to 24 keys matrix keyboard connector. It is directly driven by 16 TTL I/O lines; High level languages supported.

QTP 24 - QTP 24P

Quick Terminal Panel 24 keys with Parallel interface

Intelligent user panel equipped with Fluorescent or LCD display, LEDs backlit, 20x2 or 20x4 characters; RS 232, RS 422, RS 485 or current loop serial line; serial E2 for set up and message. Pssibility of re-naming keys, LEDs and panel name by inserting label with new name into the proper slot; 24 Keys and 16 LEDs with blinking attribute and buzzer manageable by software; built in power supply; RTC option, reader of magnetic badge and relay. The QTP 24P is low cost no intelligent (passive) version. It is directly driven from 16 TTL I/O lines; high level languages supported.

QTP 16 - QTP 16P

Quick Terminal Panel 16 keys with Parallel interface

Intelligent user panel equipped with Fluorescent or LCD display, LEDs backlit, 20x2 or 20x4 characters; RS 232, RS 422, RS 485 or current loop serial line; serial E2 for set up and messages; buzzer manageable by software; 4 readable auxiliary opto in lines; power supply 5 Vdc. The QTP 16P is low cost no intelligent (passive) version. It is directly driven from 16 TTL I/O lines.

QTP G26

Quick Terminal Panel - LCD Graphic, 26 keys

Intelligent user panel equipped with graphic LCD display 240x128 pixel, CFC backlit; optocoupled RS 232 line and additional RS 232, RS 422, RS 485 or current loop serial line. Indipendent optional CAN line controller; serial E2 for set up; RTC and RAM Lithium backed; primary graphic objects; possibility of re-naming keys, LEDs and panel name by inserting label with new name into the proper slot; 26 Keys and 16 LEDs with blinking attribute and buzzer manageable by software; built in power supply; reader of magnetic badge, smart-card and relay option.

CBT 420

Current Block Transmitter 4÷20mA

Interface between 4 input lines 0÷5, 0÷10 Vdc and 4 current output channels 4÷20 mA; signals on screw terminal; 14 bit resolution; quick connection for DIN C type and Ω rails.

IAC 01

Interface Adapter Centronics

Interface between **ABACO®** standard I/O 20 pins connector and D 25 pins connector with Centronics standard pin out.

DEB 01

Didactis Experimental Board

Supporting card for 16 TTL I/O lines use. It includes: 16 keys, 16 LEDs, 4 digits, 16 keys matrix keyboard, Centronics printer interface, LCD display and fluorescent display interface, **GPC® 68** I/O connector, field connection with screw terminal.

IPC 52

Intelligent Peripheral Controller, 24 analogic input

This intelligent peripheral card acquires 24 indipendent analogic input lines: 8 PT 100 or PT 1000 sensors, 8 J,K,S,T termocouples, 8 analog input ±2Vdc or 4÷20mA; 16 bits + sign A/D section; 0.1 °C resolution; 32K RAM for local data logging; buzzer; 16 TTL I/O lines; 5 or 8 conversion per second; facility of networking up to 127 IPC 52 cards using serial line. BUS interfacing or through RS 232, RS 422, RS 485 or current loop line. Only 5Vdc power supply.

UAR 24

Universal Analog Regulator, 2 D/A, 4 Relays

This intelligent peripheral card for temperature PID controls, acquires 2 PT 100 sensors and 2 J,K,S,T termocouples; 16 bits + sign A/D section; 0.1 °C resolution; 32K RAM for local data logging; 4 conversion per second; buzzer; 4 3A relays; 2 12 bits D/A lines, 0÷10Vdc; facility of networking up to 127 UAR 24 cards using serial line. BUS interfacing or through RS 232, RS 422, RS 485 or current loop line. Only 5Vdc power supply.

SBP 01 - xx

Switch BLOCK Power version xx

Switching power suppliers able to generate voltage from -12 to +40 Vdc and current up to 4 A. Input from 12 to 26 Vac; battery backed; power good; status LEDs; comfortable screw terminal connector; quick mounting on DIN 46277-1 and 3 rails.

BIBLIOGRAPHY

In this chapter there is a complete list of technical books, where the user can find all the necessary documentations on the components mounted on **GPC® 11**.

Data book MAXIM:	*New Releases Data Book - Volume 4*
Data book MOTOROLA:	*M68HC11 HCMOS Single-chip Microcomputer*
Data sheets MOTOROLA:	*MC68HC24 Port Replacement Unit (PRU)*
Data book NEC:	*Memory Products*
Data book TEXAS INSTRUMENTS:	*The TTL Data Book - SN54/74 Families*
Data book TEXAS INSTRUMENTS:	*Linear Circuit Data Book - Volume 1 and 3*
Data book TEXAS INSTRUMENTS:	*RS-422 and RS-485 Interface Circuits*
Data book HEWLETT PACKARD	*Optoelectronics Designer's Catalog*
Data book SGS-THOMSON:	*Non Volatile Memories*
Data book NATIONAL SEMICONDUCTOR:	*Linear Data Book - Volume 1*

For further information and upgrades please refer to specific internet web pages of the manufacturing companies.

APPENDIX A: JUMPERS AND DRIVERS LOCATION

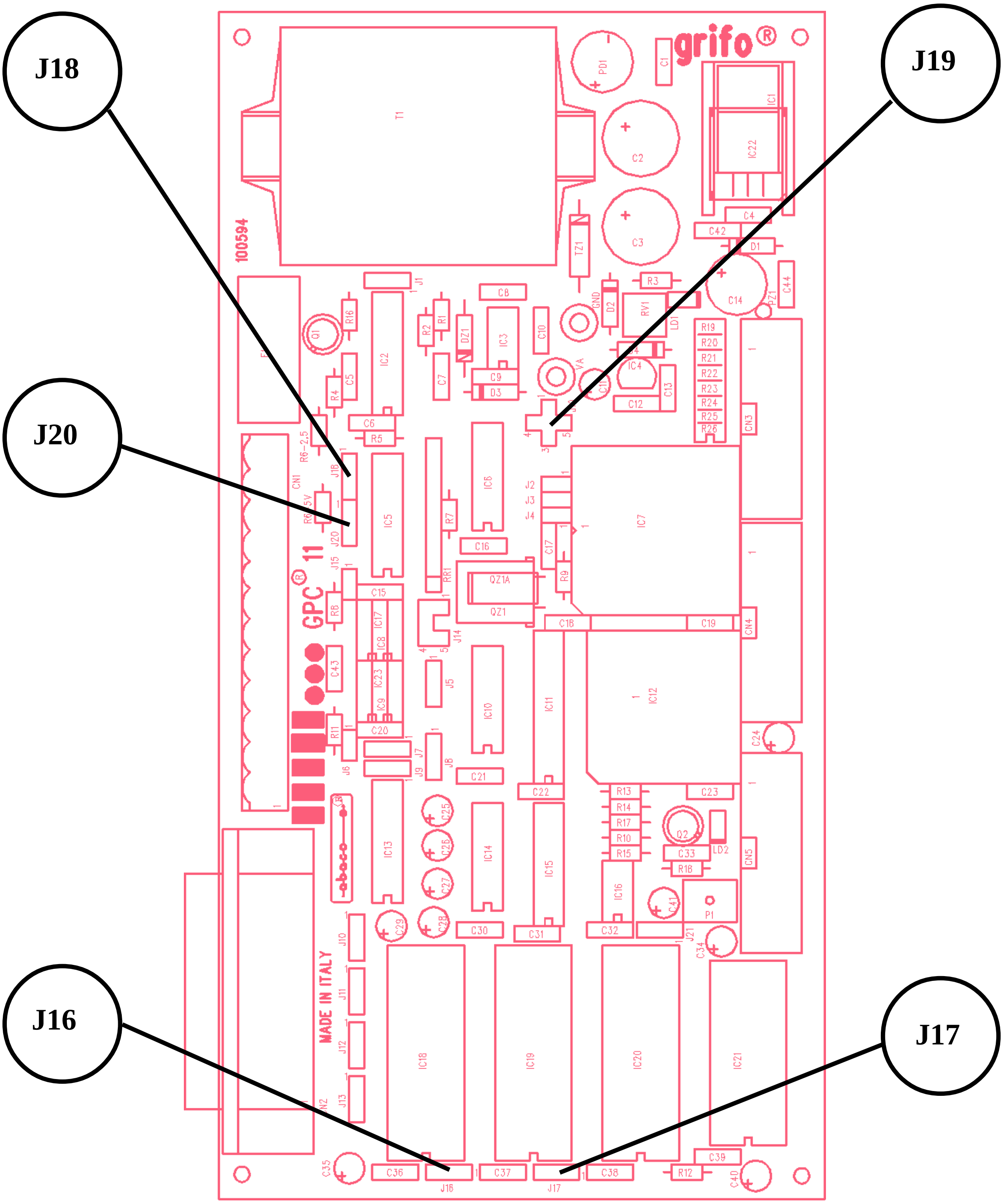


FIGURE A-1: MEMORY JUMPERS LOCATION

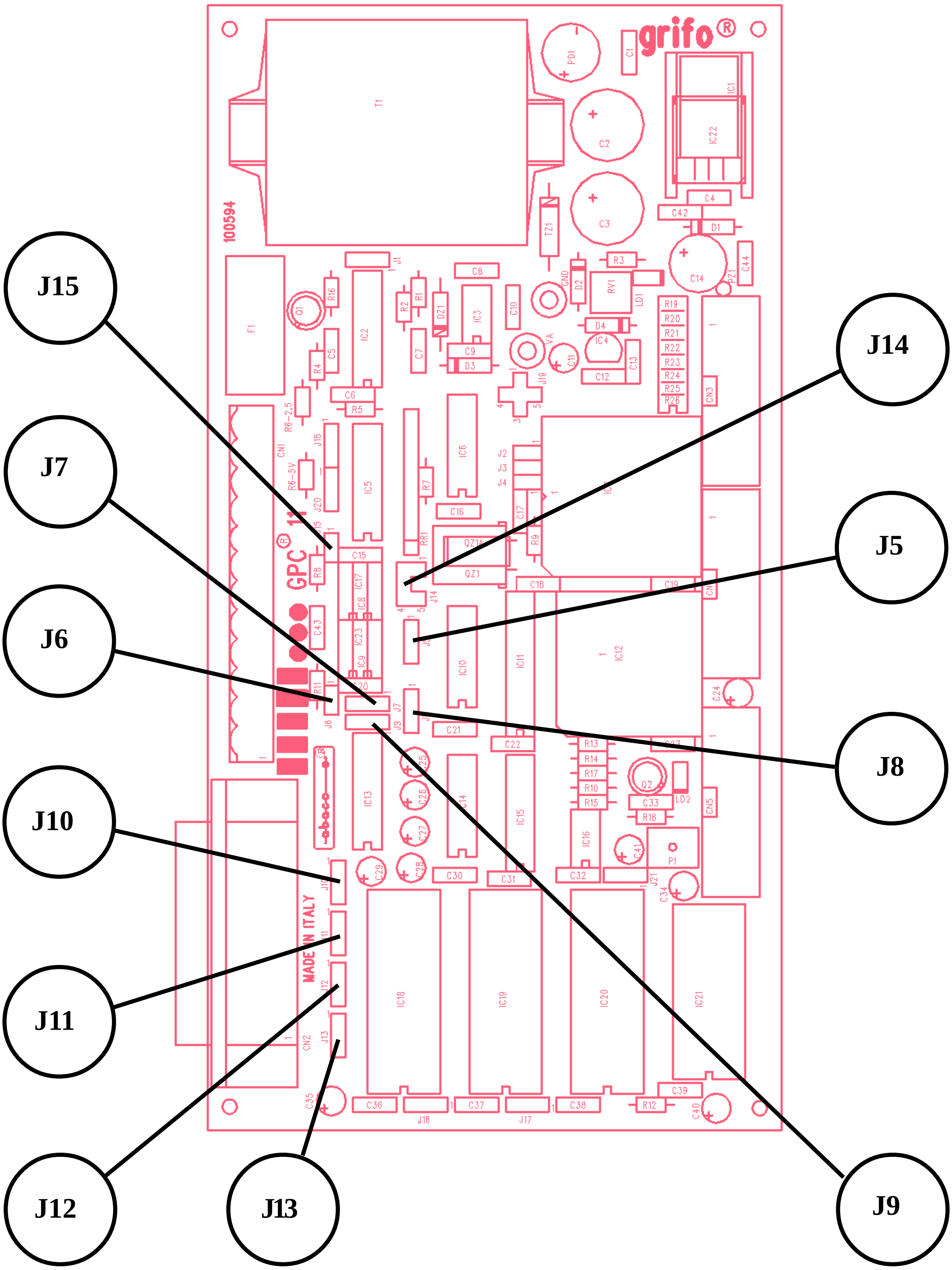
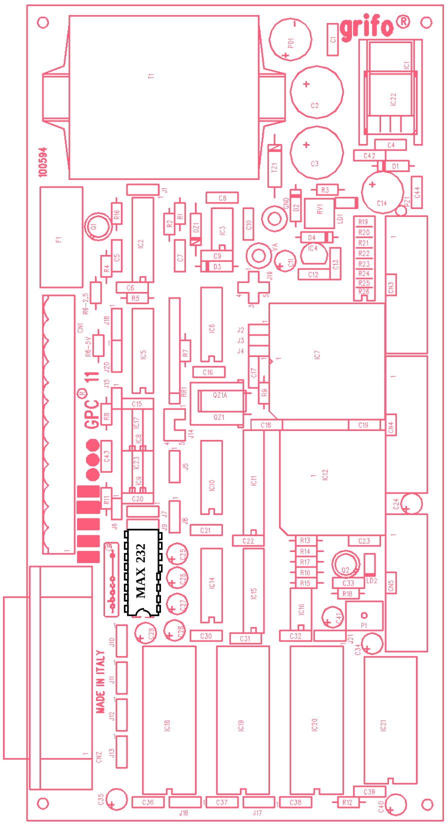
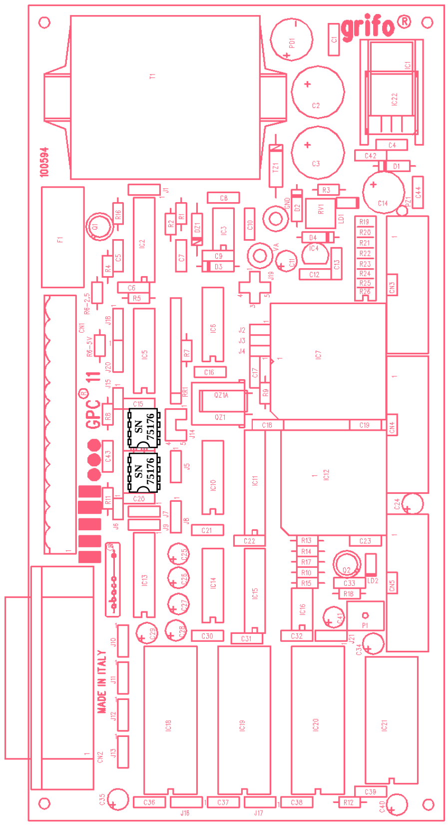


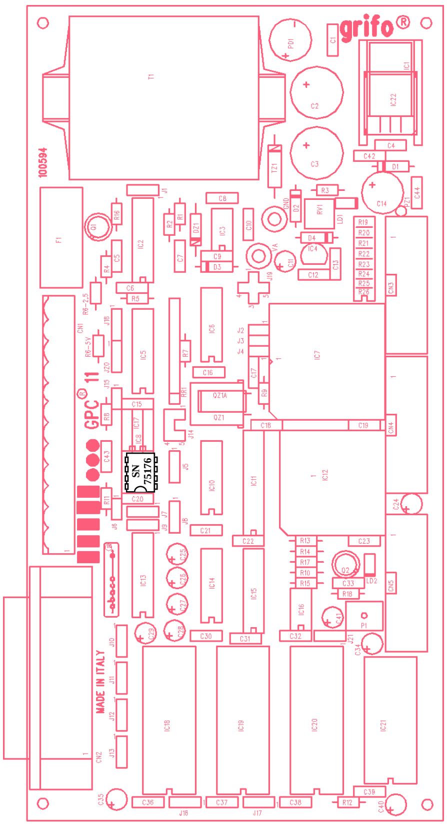
FIGURE A-2: SERIAL COMMUNICATION JUMPERS LOCATION



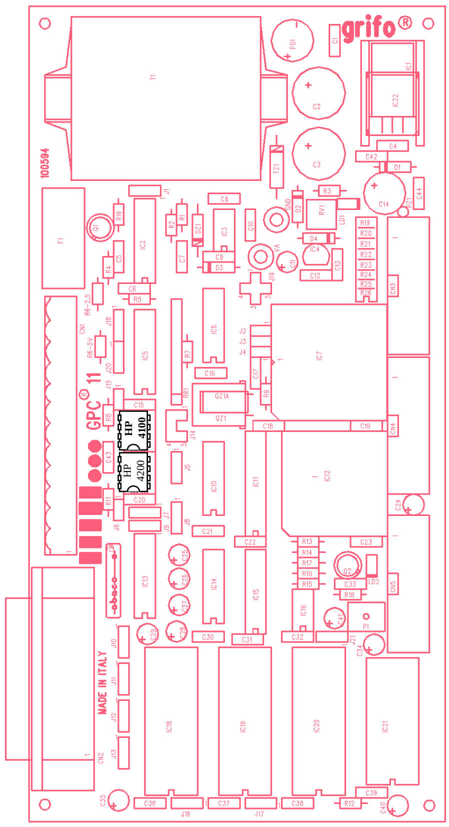
RS 232



RS 422



RS 485



current loop

FIGURE A-3: SERIAL COMMUNICATION DRIVERS LOCATION

APPENDIX B: ON BOARD DEVICE DESCRIPTION

In the following pages are reported the most important technical features of 68HC11A8 microprocessor. This one differs from 68HC11A1, used on **GPC® 11** card, only for the absence of 8K Bytes of internal ROM that are replaced by an internal ROM where ROM BUFFALO monitor debugger program is burned.

1 INTRODUCTION

The HCMOS MC68HC11A8 is an advanced 8-bit microcontroller (MCU) with highly sophisticated on-chip peripheral capabilities. A fully static design and high-density complementary metal-oxide semiconductor (HCMOS) fabrication process allow E-series devices to operate at frequencies from 3 MHz to dc, with very low power consumption.

1.1 Features

The following are some of the hardware and software highlights.

1.1.1 Hardware Features

- 8 Kbytes of ROM
- 512 Bytes of EEPROM
- 256 Bytes of RAM (All Saved During Standby) Relocatable to Any 4K Boundary
- Enhanced 16-Bit Timer System:
  - — Four Stage Programmable Prescaler
  - — Three Input Capture Functions
  - — Five Output Compare Functions
- 8-Bit Pulse Accumulator Circuit
- Enhanced NRZ Serial Communications Interface (SCI)
- Serial Peripheral Interface (SPI)
- Eight Channel, 8-Bit Analog-to-Digital Converter
- Real Time Interrupt Circuit
- Computer Operating Properly (COP) Watchdog System
- Available in Dual-In-Line or Leaded Chip Carrier Packages

1.1.2 Software Features

- Enhanced M6800/M6801 Instruction Set
- 16 x 16 Integer and Fractional Divide Features
- Bit Manipulation
- WAIT Mode
- STOP Mode

1.2 General Description

The high-density CMOS technology (HCMOS) used on the MC68HC11A8 combines smaller size and higher speeds with the low power and high noise immunity of CMOS. On-chip memory systems include 8 Kbytes of ROM, 512 bytes of electrically erasable programmable ROM (EEPROM), and 256 bytes of static RAM.

A block diagram of the MC68HC11A8 is shown in **Figure 1-1**. Major peripheral functions are provided on-chip. An eight channel analog-to-digital (A/D) converter is included with eight bits of resolution. An asynchronous serial communications interface

B MECHANICAL DATA AND ORDERING INFORMATION

B.1 Pin Assignments

The MC68HC11A8 is available in the 52-pin plastic leaded chip carrier (PLCC), the 48-pin dual in-line package (DIP), or the 64-pin quad flat pack (QFP).

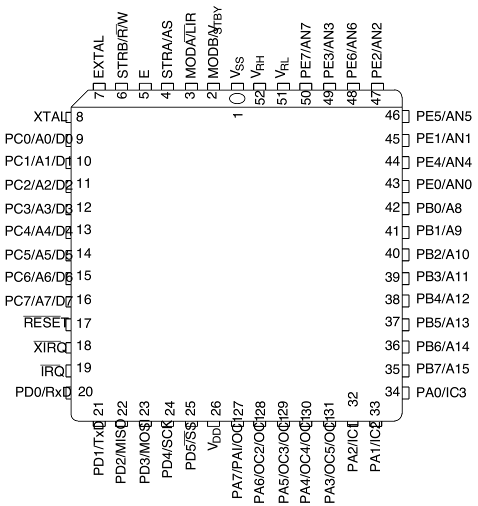


Figure B-1 52-Pin PLCC

(SCI) and a separate synchronous serial peripheral interface (SPI) are included. The main 16-bit free-running timer system has three input capture lines, five output compare lines, and a real-time interrupt function. An 8-bit pulse accumulator subsystem can count external events or measure external periods.

Self monitoring circuitry is included on-chip to protect against system errors. A computer operating properly (COP) watchdog system protects against software failures. A clock monitor system generates a system reset in case the clock is lost or runs too slow. An illegal opcode detection circuit provides a non-maskable interrupt if an illegal opcode is detected.

Two software controlled operating modes, WAIT and STOP, are available to conserve additional power.

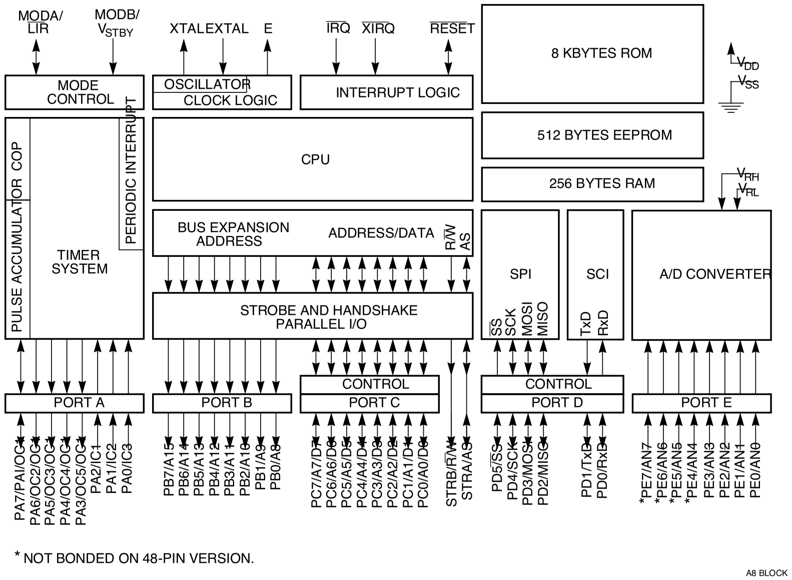


Figure 1-1 Block Diagram

1.3 Programmer's Model

In addition to being able to execute all M6800 and M6801 instructions, the MC68HC11A8 allows execution of 91 new opcodes. **Figure 1-2** shows the seven CPU registers which are available to the programmer.

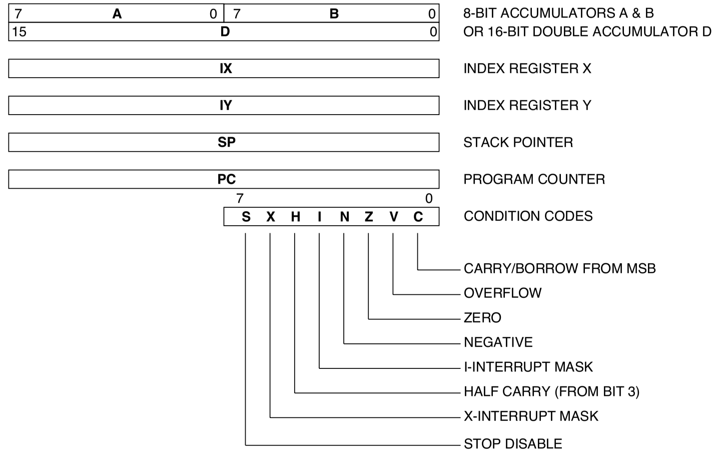


Figure 1-2 Programming Model

1.4 Summary of M68HC11 Family

Table 1-1 and the following paragraphs summarize the current members of the M68HC11 family of MCUs. This technical data book describes the MC68HC11A8 version and can be used as a primary reference for several other versions of the M68HC11 family. However, with the exception of the CPU, some newer members differ greatly from the MC68HC11A8 MCU and their respective technical literature should be referenced.

Several of the device series within the M68HC11 family have ′x1 and ′x0 versions. These are identical to the main member of the series but have some of their on-chip resources disabled. For instance, an MC68HC11A1 is identical to the MC68HC11A8 except that its ROM is disabled. An MC68HC11A0 has disabled EPROM **and** EEPROM arrays. Refer to **Table 1-1**.

Nearly all series within the M68HC11 family have both a ROM version and an EPROM version. Any device in the M68HC11 family that has a 7 preceding the 11 is a device containing EPROM instead of ROM (e.g., MC68HC711E9). These devices operate exactly as the custom ROM-based version (e.g., MC68HC11E9) but can be programmed by the user. EPROM-based devices in a windowed package can be erased and reprogrammed indefinitely. EPROM-based devices in standard packages are one-time-programmable (OTP). Refer to **Table 1-1**.

Table 1-1 M68HC11 Family Devices

Device	RAM	ROM	EPROM	EEPROM	COMMENTS
MC68HC11A8	256	8K	0	512	16-bit timer; 8 channel 8-bit A/D, SCI, SPI
MC68HC11A7	256	8K	0	0	
MC68HC11A1	256	0	0	512	
MC68HC11A0	256	0	0	0	
MC68HC11D3	192	4K	0	0	16-bit timer; SCI, SPI
MC68HC711D3	192	0	4K	0	
MC68HC11D0	192	0	0	0	
MC68HC11ED0	512	0	0	0	16-bit timer; SCI, SPI
MC68HC11E9	512	12K	0	512	16-bit timer; SCI, SPI, 8 channel 8-bit A/D
MC68HC711E9	512	0	12K	512	
MC68HC11E8	512	12K	0	0	
MC68HC11E1	512	0	0	512	
MC68HC11E0	512	0	0	0	
MC68HC811E2	256	0	0	2048	16-bit timer; SCI, SPI, 8 channel 8-bit A/D, 2K EEPROM
MC68HC11E20	768	20K	0	512	16-bit timer; SCI, SPI, 8 channel 8-bit A/D,
MC68HC711E20	768	0	20K	512	20K ROM/EPROM
MC68HC11F1	1024	0	0	512	nonmultiplexed bus, 8 channel 8-bit A/D, 4 chip selects, SCI, SPI
MC68HC11G7	512	24K	0	0	nonmultiplexed bus, 8 channel 10-bit A/D, 4 channel PWM,
MC68HC11G5	512	16K	0	0	SCI, SPI, 66 I/O pins
MC68HC711G5	512	0	16K	0	
MC68HC11G0	512	0	0	0	
MC68HC11K4	768	24K	0	640	nonmultiplexed bus, memory expansion to 1MB,
MC68HC711K4	768	0	24K	640	8 channel 8-bit A/D, 4 channel PWM, 4 chip selects
MC68HC11K3	768	24K	0	0	
MC68HC11K1	768	0	0	640	
MC68HC11K0	768	0	0	0	
MC68HC11KA4	768	24K	0	640	nonmultiplexed bus, 8 channel 8-bit A/D, SCI, SPI,
MC68HC711KA4	768	0	24K	640	4 channel PWM
MC68HC11KA2	1024	32K	0	640	
MC68HC711KA2	1024	0	32K	640	
MC68HC11L6	512	16K	0	512	multiplexed bus, 16-bit timer; 8 channel 8-bit A/D, SCI, SPI
MC68HC711L6	512	0	16K	512	
MC68HC11L5	512	16K	0	0	
MC68HC11L1	512	0	0	512	
MC68HC11L0	512	0	0	0	
MC68HC11M2	1280	32K	0	640	nonmultiplexed bus, 8 channel 8-bit A/D, 4 channel PWM,
MC68HC711M2	1280	0	32K	640	DMA, on-chip math coprocessor, SCI, 2 SPI
MC68HC11N4	768	24K	0	640	nonmultiplexed bus, 12 channel 8-bit A/D, 2 channel 8-bit D/A,
MC68HC711N4	768	0	24K	640	6 channel PWM, on-chip math coprocessor, SCI, SPI
MC68HC11P2	1024	32K	0	640	nonmultiplexed bus, PLL, 8 channel 8-bit A/D, 4 channel PWM,
MC68HC711P2	1024	0	32K	640	3 SCI (2 with MI bus), SPI, 62 I/O pins

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2.1.4 E Clock Output (E)

This is the output connection for the internally generated E clock which can be used as a timing reference. The frequency of the E clock output is actually one fourth that of the input frequency at the XTAL and EXTAL pins. When the E clock output is low an internal process is taking place and, when high, data is being accessed. The E clock signal is halted when the MCU is in STOP mode.

2.1.5 Interrupt Request ($\overline{IRQ}$)

The $\overline{IRQ}$ input provides a means for requesting asynchronous interrupts to the MC68HC11A8. It is program selectable (OPTION register) with a choice of either negative edge-sensitive or level-sensitive triggering, and is always configured to level-sensitive triggering by reset. The $\overline{IRQ}$ pin requires an external pull-up resistor to V_{DD} (typically 4.7K ohm).

2.1.6 Non-Maskable Interrupt ($\overline{XIRQ}$)

This input provides a means for requesting a non-maskable interrupt, after reset initialization. During reset, the X bit in the condition code register is set and any interrupt is masked until MCU software enables it. The $\overline{XIRQ}$ input is level sensitive and requires an external pull-up resistor to V_{DD}.

2.1.7 Mode A/Load Instruction Register and Mode B/Standby Voltage (MODA/$\overline{LIR}$, MODB/V_{STBY})

During reset, MODA and MODB are used to select one of the four operating modes. Refer to **Table 2-1**. Paragraph **2.2 Operating Modes** provides additional information.

Table 2-1 Operating Modes vs. MODA and MODB

MODB	MODA	Mode Selected
1	0	Single Chip
1	1	Expanded Multiplexed
0	0	Special Bootstrap
0	1	Special Test

After the operating mode has been selected, the $\overline{LIR}$ pin provides an open-drain output to indicate that an instruction is starting. All instructions are made up of a series of E clock cycles. The $\overline{LIR}$ signal goes low during the first E clock cycle of each instruction (opcode fetch). This output is provided as an aid in program debugging.

The V_{STBY} signal is used as the input for RAM standby power. When the voltage on this pin is more than one MOS threshold (about 0.7 volts) above the V_{DD} voltage, the internal 256-byte RAM and part of the reset logic are powered from this signal rather than the V_{DD} input. This allows RAM contents to be retained without V_{DD} power applied to the MCU. Reset must be driven low before V_{DD} is removed and must remain low until V_{DD} has been restored to a valid level.

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3 ON-CHIP MEMORY

This section describes the on-chip ROM, RAM, and EEPROM memories. The memory maps for each mode of operation are shown and the RAM and I/O mapping register (INIT) is described. The INIT register allows the on-chip RAM and the 64 control registers to be moved to suit the needs of a particular application.

3.1 Memory Maps

Composite memory maps for each mode of operation are shown in **Figure 3-1**. Memory locations are shown in the shaded areas and the contents of these shaded areas are shown to the right. These modes include single-chip, expanded multiplexed, special bootstrap, and special test.

Single-chip operating modes do not generate external addresses. Refer to **Table 3-1** for a full list of the registers.

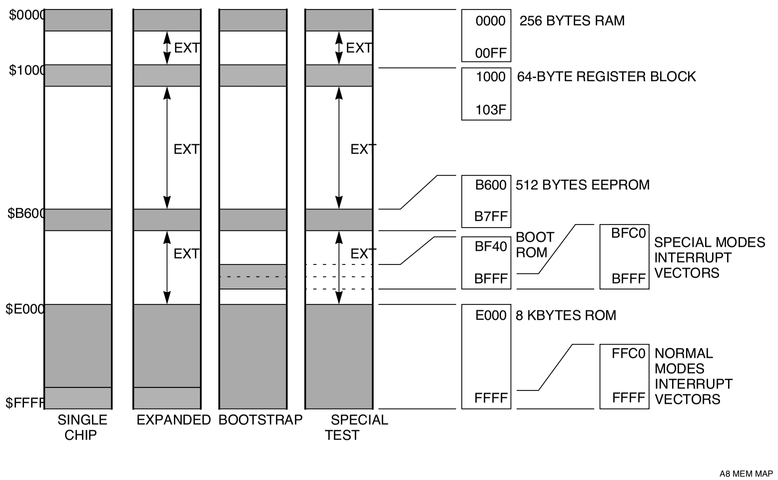

Figure 3-1 Memory Maps

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Table 3-1 Register and Control Bit Assignments (Sheet 1 of 2)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0		
$1000	Bit 7	—	—	—	—	—	—	Bit 0	PORTA	I/O Port A
$1001									Reserved	
$1002	STAF	STAI	CWOM	HNDS	OIN	PLS	EGA	INVB	PIOC	Parallel I/O Control F
$1003	Bit 7	—	—	—	—	—	—	Bit 0	PORTC	I/O Port C
$1004	Bit 7	—	—	—	—	—	—	Bit 0	PORTB	Output Port B
$1005	Bit 7	—	—	—	—	—	—	Bit 0	PORTCL	Alternate Latched Port C
$1006									Reserved	
$1007	Bit 7	—	—	—	—	—	—	Bit 0	DDRC	Data Direction for Port C
$1008			Bit 5	—	—	—	—	Bit 0	PORTD	I/O Port D
$1009			Bit 5	—	—	—	—	Bit 0	DDRD	Data Direction for Port D
$100A	Bit 7	—	—	—	—	—	—	Bit 0	PORTE	Input Port E
$100B	FOC1	FOC2	FOC3	FOC4	FOC5				CFORC	Compare Force Regist
$100C	OC1M7	OC1M6	OC1M5	OC1M4	OC1M3				OC1M	OC1 Action Mask Re
$100D	OC1D7	OC1D6	OC1D5	OC1D4	OC1D3				OC1D	OC1 Action Data Reg
$100E	Bit 15	—	—	—	—	—	—	Bit 8	TCNT	Timer Counter Register
$100F	Bit 7	—	—	—	—	—	—	Bit 0		
$1010	Bit 15	—	—	—	—	—	—	Bit 8	TIC1	Input Capture 1 Register
$1011	Bit 7	—	—	—	—	—	—	Bit 0		
$1012	Bit 15	—	—	—	—	—	—	Bit 8	TIC2	Input Capture 2 Register
$1013	Bit 7	—	—	—	—	—	—	Bit 0		
$1014	Bit 15	—	—	—	—	—	—	Bit 8	TIC3	Input Capture 3 Register
$1015	Bit 7	—	—	—	—	—	—	Bit 0		
$1016	Bit 15	—	—	—	—	—	—	Bit 8	TOC1	Output Compare 1 Register
$1017	Bit 7	—	—	—	—	—	—	Bit 0		
$1018	Bit 15	—	—	—	—	—	—	Bit 8	TOC2	Output Compare 2 Register
$1019	Bit 7	—	—	—	—	—	—	Bit 0		
$101A	Bit 15	—	—	—	—	—	—	Bit 8	TOC3	Output Compare 3 Regi
$101B	Bit 7	—	—	—	—	—	—	Bit 0		
$101C	Bit 15	—	—	—	—	—	—	Bit 8	TOC4	Output Compare 4 Register
$101D	Bit 7	—	—	—	—	—	—	Bit 0		
$101E	Bit 15	—	—	—	—	—	—	Bit 8	TCO5	Output Compare 5 Regi
$101F	Bit 7	—	—	—	—	—	—	Bit 0		

Table 3-1 Register and Control Bit Assignments (Sheet 2 of 2)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0		
$1020	OM2	OL2	OM3	OL3	OM4	OL4	OM5	OL5	TCTL1	Timer Control Register 1
$1021			EDG1B	EDG1A	EDG2B	EDG2A	EDG3B	EDG3A	TCTL2	Timer Control Register 2
$1022	OC1I	OC2I	OC3I	OC4I	OC5I	IC1I	IC2I	IC3I	TMSK1	Timer Interrupt Mask Regi
$1023	OC1F	OC2F	OC3F	OC4F	OC5F	IC1F	IC2F	IC3F	TFLG1	Timer Interrupt Flag Regi
$1024	TOI	RTII	PAOVI	PAII			PR1	PR0	TMSK2	Timer Interrupt Mask Regist
$1025	TOF	RTIF	PAOVF	PAIF					TFLG2	Timer Interrupt Flag Register
$1026	DDRA7	PAEN	PAMOD	PEDGE			RTR1	RTR0	PACTL	Pulse Accumulator Contr
$1027	Bit 7	—	—	—	—	—	—	Bit 0	PACNT	Pulse Accumulator Count Re
$1028	SPIE	SPE	DWOM	MSTR	CPOL	CPHA	SPR1	SPR0	SPCR	SPI Control Register
$1029	SPIF	WCOL		MODF					SPSR	SPI Status Register
$102A	Bit 7	—	—	—	—	—	—	Bit 0	SPDR	SPI Data Register
$102B	TCLR		SCP1	SCP0	RCKB	SCR2	SCR1	SCR0	BAUD	SCI Baud Rate Control
$102C	R8	T8		M	WAKE				SCCR1	SCI Control Register 1
$102D	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK	SCCR2	SCI Control Register 2
$102E	TDRE	TC	RDRF	IDLE	OR	NF	FE		SCSR	SCI Status Register
$102F	Bit 7	—	—	—	—	—	—	Bit 0	SCDR	SCI Data (Read RDR, Write TDR
$1030	CCF		SCAN	MULT	CD	CC	CB	CA	ADCTL	A/D Control Register
$1031	Bit 7	—	—	—	—	—	—	Bit 0	ADR1	A/D Result Register 1
$1032	Bit 7	—	—	—	—	—	—	Bit 0	ADR2	A/D Result Register 2
$1033	Bit 7	—	—	—	—	—	—	Bit 0	ADR3	A/D Result Register 3
$1034	Bit 7	—	—	—	—	—	—	Bit 0	ADR4	A/D Result Register 4
$1035 thru $1038									Reserved	
$1039	ADPU	CSEL	IRQE	DLY	CME		CR1	CR0	OPTION	System Configuration Opti
$103A	Bit 7	—	—	—	—	—	—	Bit 0	COPRST	Arm/Reset COP Timer Circu
$103B	ODD	EVEN		BYTE	ROW	ERASE	EELAT	EEPGM	PPROG	EEPROM Program Control Register
$103C	RBOOT	SMOD	MDA	IRV	PSEL3	PSEL2	PSEL1	PSEL0	HPRIO	Highest Priority I-Bit Int
$103D	RAM3	RAM2	RAM1	RAM0	REG3	REG2	REG1	REG0	INIT	RAM and I/O Mapping R
$103E	TILOP		OCCR	CBYP	DISR	FCM	FCOP	TCON	TEST1	Factory TEST Control Re
$103F	—	—	—	—	NOSEC	NOCOP	ROMON	EEON	CONFIG	COP, ROM, and EEPROI

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In expanded multiplexed operating modes, memory locations are basically the same as the single- chip operating modes; however, the locations between the shaded areas (designated EXT) are for externally addressed memory and I/O. If an external memory or I/O device is located to overlap an enabled internal resource, the internal resource will take priority. For reads of such an address the data (if any) driving the port C data inputs is ignored and will not result in any harmful conflict with the internal read. For writes to such an address data is driven out of the port C data pins as well as to the internal location. No external devices should drive port C during write accesses to internal locations; however, there is normally no conflict since the external address decode and/ or data direction control should incorporate the R/$\overline{W}$ signal in their development. The R/$\overline{W}$, AS, address, and write data signals are valid for all accesses including accesses to internal memory and registers.

The special bootstrap operating mode memory locations are similar to the single-chip operating mode memory locations except that a bootstrap program at memory locations $BF40 through $BFFF is enabled. The reset and interrupt vectors are addressed at $BFC0–$BFFF while in the special bootstrap operating mode. These vector addresses are within the 192 byte memory used for the bootstrap program.

The special test operating mode memory map is the same as the expanded multiplexed operating mode memory map except that the reset and interrupt vectors are located at external memory locations $BFC0–$BFFF.

3.2 RAM and I/O Mapping Register (INIT)

There are 64 internal registers which are used to control the operation of the MCU. These registers can be relocated on 4K boundaries within the memory space, using the INIT register. Refer to **Table 3-1** for a complete list of the registers. The registers and control bits are explained throughout this document.

The INIT register is a special-purpose 8-bit register which may be used during initialization to change the default locations of RAM and control registers within the MCU memory map. It may be written to only once within the initial 64 E clock cycles after a reset and thereafter becomes a read-only register.

	7	6	5	4	3	2	1	0	
$103D	RAM3	RAM2	RAM1	RAM0	REG3	REG2	REG1	REG0	INIT
RESET	0	0	0	0	0	0	0	1	

The default starting address for internal RAM is $0000 and the default starting address for the 64 control registers is $1000 (the INIT register is set to $01 at reset). The upper four bits of the INIT register specify the starting address for the 256 byte RAM and the lower four bits of INIT specify the starting address for the 64 control registers. These four bits are matched to the upper four bits of the 16-bit address.

Throughout this document, the control register addresses will be displayed with the high-order digit shown as a bold "**1**" to indicate that the register block may be relocated to some 4K memory page other than its default position of $1000-$103F.

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Note that if the RAM is relocated to either $E000 or $F000, which is in conflict with the internal ROM, (no conflict if the ROMON bit in the configuration register is zero), RAM will take priority and the conflicting ROM will become inaccessible. Also, if the 64 control registers are relocated so that they conflict with the RAM and/or ROM, then the 64 control registers take priority and the RAM and/or ROM at those locations become inaccessible. No harmful conflicts result, the lower priority resources simply become inaccessible. Similarly, if an internal resource conflicts with an external device no harmful conflict results. Data from the external device will not be applied to the internal data bus and cannot interfere with the internal read.

Note that there are unused register locations in the 64 byte control register block. Reads of these unused registers will return data from the undriven internal data bus and not from another resource that happens to be located at the same address.

3.3 ROM

The internal 8K ROM occupies the highest 8K of the memory map ($E000–$FFFF). This ROM is disabled when the ROMON bit in the CONFIG register is clear. The ROMON bit is implemented with an EEPROM cell and is programmed using the same procedures for programming the on-chip EEPROM. For further information refer to **3.5.3 System Configuration Register (CONFIG)**.

In the single-chip operating mode, internal ROM is enabled regardless of the state of the ROMON bit.

There is also a 192 byte mask programmed boot ROM in the MC68HC11A8. This bootstrap program ROM controls the operation of the special bootstrap operating mode and is only enabled following reset in the special bootstrap operating mode. For more information refer to **2.2.3 Special Bootstrap Operating Mode.**

3.4 RAM

The 256 byte internal RAM may be relocated during initialization by writing to the INIT register. The reset default position is $0000 through $00FF. This RAM is implemented with static cells and retains its contents during the WAIT and STOP modes.

The contents of the 256-byte RAM can also be retained by supplying a low current backup power source to the MODB/V_{STBY} pin. When using a standby power source, V_{DD} may be removed; however, $\overline{RESET}$ must go low before V_{DD} is removed and remain low until V_{DD} has been restored.

3.5 EEPROM

The 512 bytes of EEPROM are located at $B600 through $B7FF and have the same read cycle time as the internal ROM. The write (or programming) mechanism for the EEPROM is controlled by the PPROG register. The EEPROM is disabled when the EEON bit in the CONFIG register is zero. The EEON bit is implemented with an EEPROM cell.

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The erased state of an EEPROM byte is $FF. Programming changes ones to zeros. If any bit in a location needs to be changed from a zero to a one, the byte must be erased in a separate operation before it is reprogrammed. If a new data byte has no ones in bit positions which were already programmed to zero, it is acceptable to program the new data without erasing the EEPROM byte first. For example, programming $50 to a location which was already $55 would change the location to $50.

Programming and erasure of the EEPROM relies on an internal high-voltage charge pump. At E clock frequencies below 2 MHz the efficiency of this charge pump decreases which increases the time required to program or erase a location. The recommended program and erase time is 10 milliseconds when the E clock is 2 MHz and should be increased to as much as 20 milliseconds when E is between 1 MHz and 2 MHz. When the E clock is below 1 MHz, the clock source for the charge pump should be switched from the system clock to an on-chip R-C oscillator clock. This is done by setting the CSEL bit in the OPTION register. A 10 millisecond period should be allowed after setting the CSEL bit to allow the charge pump to stabilize. Note that the CSEL bit also controls a clock to the analog-to-digital converter subsystem.

3.5.1 EEPROM Programming Control Register (PPROG)

This 8-bit register is used to control programming and erasure of the 512-byte EEPROM. Reset clears this register so the EEPROM is configured for normal reads.

	7	6	5	4	3	2	1	0	
$103B	ODD	EVEN	0	BYTE	ROW	ERASE	EELAT	EEPGM	PPROG
RESET	0	0	0	0	0	0	0	0	

ODD — Program Odd Rows (TEST)

EVEN — Program Even Rows (TEST)

Bit 5 — Not implemented.
This bit always reads zero.

BYTE — Byte Erase Select
This bit overrides the ROW bit.
0 = Row or Bulk Erase
1 = Erase Only One Byte

ROW — Row Erase Select
If the BYTE bit is 1, ROW has no meaning.
0 = Bulk Erase
1 = Row Erase

ERASE — Erase Mode Select
0 = Normal Read or Program
1 = Erase Mode

EELAT — EEPROM Latch Control
- 0 = EEPROM Address and Data Configured for Read Mode
- 1 = EEPROM Address and Data Configured for Programming/Erasing

EEPGM — EEPROM Programming Voltage Enable
- 0 = Programming Voltage Switched Off
- 1 = Programming Voltage Turned On

If an attempt is made to set both the EELAT and EEPGM bits in the same write cycle, neither will be set. If a write to an EEPROM address is performed while the EEPGM bit is set, the write is ignored and the programming operation currently in progress is not disturbed. These two safeguards were included to prevent accidental EEPROM changes in cases of program runaway. Mask sets A38P, A49N, and date codes before 86xx did not have these safeguards.

3.5.2 Programming/Erasing Internal EEPROM

The EEPROM programming and erasure process is controlled by the PPROG register. The following paragraphs describe the various operations performed on the EEPROM and include example program segments to demonstrate programming and erase operations.

These program segments are intended to be simple straightforward examples of the sequences needed for basic program and erase operations. There are no special restrictions on the address modes used and bit manipulation instructions may be used. Other MCU operations can continue to be performed during EEPROM programming and erasure provided these operations do not include reads of data from EEPROM (the EEPROM is disconnected from the read data bus during EEPROM program and erase operations). The subroutine DLY10 used in these program segments is not shown but can be any set of instructions which takes ten milliseconds.

3.5.2.1 Read

For the read operation the EELAT bit in the PPROG register must be clear. When this bit is cleared, the remaining bits in the PPROG register have no meaning or effect, and the EEPROM may be read as if it were a normal ROM.

3.5.2.2 Programming

During EEPROM programming, the ROW and BYTE bits are not used. If the E clock frequency is 1 MHz or less, the CSEL bit in the OPTION register must be set. Recall that in this EEPROM, zeros must be erased by a separate erase operation before programming. The following program segment demonstrates how to program an EEPROM byte.

3

```
* On entry, A = data to be programmed and X = EEPROM address
              •
              •
              •
PROG    LDAB   #$02
        STAB   $103B    Set EELAT Bit (EEPGM = 0)
        STAA   0,X      Store Data to EEPROM Address
        LDAB   #$03
        STAB   $103B    Set EEPGM Bit (EELAT = 1)
        JSR    DLY10    Delay 10 ms
        CLR    $103B    Turn Off High Voltage and Set to READ
                        Mode
              •
              •
              •
```

3.5.2.3 Bulk Erase

The following program segment demonstrates how to bulk erase the 512-byte EEPROM. The CONFIG register is not affected in this example.

```
              •
              •
              •
BULKE   LDAB   #$06
        STAB   $103B    Set to Bulk Erase Mode
        STAB   $B600    Write any Data to any EEPROM Address
        LDAB   #$07
        STAB   $103B    Turn On Programming Voltage
        JSR    DLY10    Delay 10 ms
        CLR    $103B    Turn Off High Voltage and Set to READ
                        Mode
              •
              •
              •
```

3.5.2.4 Row Erase

The following program segment demonstrates the row erase function. A ‘row’ is sixteen bytes ($B600-$B60F, $B610-$B61F... $B7F0-$B7FF). This type of erase operation saves time compared to byte erase when large sections of EEPROM are to be erased.

```
*On entry X = any address in the row to be erased
        •
        •
        •
ROWE   LDAB   #$0E
       STAB   $103B   Set to Row Erase Mode
       STAB   0,X     Write any Data to any Address in Row
       LDAB   #$0F
       STAB   $103B   Turn on High Voltage
       JSR    DLY10   Delay 10 ms
       CLR    $103B   Turn Off High Voltage and Set to Read
                      Mode
        •
        •
        •
```

3.5.2.5 Byte Erase

The following program segment shows the byte erase function.

```
*On entry, X = address of byte to be erased
        •
        •
        •
BYTEE  LDAB   #$16
       STAB   $103B   Set to Byte Erase Mode
       STAB   0,X     Write any Data to the Address to Erase
       LDAB   #$17
       STAB   $103B   Turn on High Voltage
       JSR    DLY10   Delay 10 ms
       CLR    $103B   Turn off High Voltage and Set to Read
                      Mode
        •
        •
        •
```

3.5.3 System Configuration Register (CONFIG)

The MC68HC11A8 can be configured to specific system requirements through the use of hardwired options such as the mode select pins, semi-permanent EEPROM control bit specifications (CONFIG register), or by use of control registers. The configuration control register (CONFIG) is implemented in EEPROM cells and controls the presence

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of ROM and EEPROM in the memory map, as well as enabling the COP watchdog system. A security feature to protect data in the EEPROM and RAM is also available on mask programmed MC68HC11A8s.

	7	6	5	4	3	2	1	0	
$103F	0	0	0	0	NOSEC	NOCOP	ROMON	EEON	CONFIG
RESET	(see **3.5.3.2 Operation of the Configuration Mechanism**)								

Bits 7, 6, 5, and 4 — Not Implemented
These bits are always read as zero.

NOSEC — Security Mode Disable Bit
This bit is only implemented if it is specifically requested at the time mask ROM information is submitted. When this bit is not implemented it always reads one.
When RAM and EEPROM security are required, the NOSEC bit can be programmed to zero to enable the software anti-theft mechanism. When clear, the NOSEC bit prevents the selection of expanded multiplexed operating modes. If the MCU is reset in the special bootstrap operating mode while NOSEC is zero, EEPROM, RAM, and CONFIG are erased before the loading process continues.
0 = Enable Security Mode
1 = Disable Security Mode

NOCOP — COP System Disable
0 = COP Watchdog System Enabled
1 = COP Watchdog System Disabled

ROMON — Enable On-Chip ROM
When this bit is clear, the 8K ROM is disabled, and that memory space becomes externally accessed space. In the single-chip operating mode, the internal 8K ROM is enabled regardless of the state of the ROMON bit.

EEON — Enable On-Chip EEPROM
When this bit is clear, the 512-byte EEPROM is disabled, and that memory space becomes externally accessed space.

3.5.3.1 Programming and Erasure of the CONFIG Register

Since the CONFIG register is implemented with EEPROM cells, special provisions must be made to erase and program this register. The normal EEPROM control bits in the PPROG register are used for this purpose. Programming follows the same procedure as programming a byte in the 512-byte EEPROM except the CONFIG register address is used. Erase also follows the same procedure as that used for the EEPROM except that only bulk erase can be used on the CONFIG register. When the CONFIG register is erased, the 512-byte EEPROM array is also erased. Be sure to check the Technical Summary for the particular MC68HC11 Family member you are using.

On mask set B96D and newer, the CONFIG register may only be programmed or erased while the MCU is operating in the test mode or the bootstrap mode. This interlock was added to help prevent accidental changes to the CONFIG register.

The following program segment demonstrates how to program the CONFIG register. This program assumes that the CONFIG register was previously erased.

```
*On entry, A = data to be programmed onto CONFIG
        •
        •
        •
PROGC   LDAB   #$02
        STAB   $103B   Set EELAT Bit (EEPGM = 0)
        STAA   $103F   Store Data to CONFIG Address
        LDAB   #$03
        STAB   $103B   Turn on Programming Voltage
        JSR    DLY10   Delay 10 ms
        CLR    $103B   Turn Off High Voltage and Set to READ
                       Mode
        •
        •
        •
```

The following program segment demonstrates the erase procedure for the CONFIG register.

```
        •
        •
        •
BULKC   LDAB   #$06
        STAB   $103B   Set Bulk Erase Mode
        STAB   $103F   Write any Data to CONFIG
        LDAB   #$07
        STAB   $103B   Turn on Programming Voltage
        JSR    DLY10   Delay 10 ms
        CLR    $103B   Turn Off High Voltage and Set to READ
                       Mode
        •
        •
        •
```


3.5.3.2 Operation of the Configuration Mechanism

The CONFIG register consists of an EEPROM byte and static working latches. This register controls the start-up configuration of the MCU. The contents of the EEPROM CONFIG byte are transferred into static working latches during any reset sequence. The operation of the MCU is controlled directly by these latches and not the actual EEPROM byte. Changes to the EEPROM byte do not affect operation of the MCU until after the next reset sequence. When programming the CONFIG register, the EEPROM byte is being accessed. When the CONFIG register is being read, the static latches are being accessed.

To change the value in the CONFIG register proceed as follows:

1. Erase the CONFIG register.

CAUTION

Do not issue a reset at this time.

2. Program the new value to the CONFIG register.
3. Issue a reset so the new configuration will take effect.

4 PARALLEL I/O

The MC68HC11A8 has 40 I/O pins arranged as five 8-bit ports. All of these pins serve multiple functions depending on the operating mode and data in the control registers. This section explains the operation of these pins only when they are used for parallel I/O.

Ports C and D are used as general purpose input and/or output pins under direct control of their respective data direction registers. Ports A, B, and E, with the exception of port A pin 7, are fixed direction inputs or outputs and therefore do not have data direction registers. Port B, port C, the STRA pin, and the STRB pin are used for strobed and/or handshake modes of parallel I/O, as well as general purpose I/O.

4.1 General-Purpose I/O (Ports C and D)

Each port I/O line has an associated bit in a specific port data register and port data direction register. The data direction register bits are used to specify the primary direction of data for each I/O line. When an output line is read, the value at the input to the pin driver is returned. When a line is configured as an input, that pin becomes a high-impedance input. If a write is executed to an input line, the value does not affect the I/O pin, but is stored in an internal latch. When the line becomes an output, this value appears at the I/O pin. Data direction register bits are cleared by reset to configure I/O pins as inputs.

The AS and R/$\overline{W}$ pins are dedicated to bus control while in the expanded multiplexed operating modes, or parallel I/O strobes (STRA and STRB) while in the single chip operating modes.

4.2 Fixed Direction I/O (Ports A, B, and E)

The lines for ports A, B, and E (except for port A bit 7) have fixed data directions. When port A is being used for general purpose I/O, bits 0, 1, and 2 are configured as input only and writes to these lines have no effect. Bits 3, 4, 5, and 6 of port A are configured as output only and reads of these lines return the levels sensed at the input to the line drivers. Port A bit 7 can be configured as either a general-purpose input or output using the DDRA7 bit in the pulse accumulator control register. When port B is being used for general purpose output, it is configured as output only and reads of these lines will return the levels sensed at the input of the pin drivers. Port E contains the eight A/D channel inputs, but these lines may also be used as general purpose digital inputs. Writes to the port E address have no effect.

4

4.3 Simple Strobed I/O

The simple strobed mode of parallel I/O is invoked and controlled by the parallel I/O control register (PIOC). This mode is selected when the handshake bit (HNDS) in the PIOC register is clear. Port C becomes a strobed input port with the STRA line as the edge-detecting latch command input. Also, port B becomes a strobed output port with the STRB line as the output strobe. The logic sense of the STRB output is selected by the invert strobe B bit (INVB) in the PIOC register.

4.3.1 Strobed Input Port C

In this mode, there are two addresses where port C may be read, the PORTC data register and the alternate latched port C register (PORTCL). The data direction register still controls the data direction of all port C lines. Even when the strobed input mode is selected, any or all of the port C lines may still be used for general purpose I/O.

The STRA line is used as an edge-detecting input, and the edge-select for strobe A (EGA) bit in the PIOC register defines either falling or rising edge as the significant edge. Whenever the selected edge is detected at the STRA pin, the current logic levels at port C lines are latched into the PORTCL register and the strobe A flag (STAF) in the PIOC register is set. If the strobe A interrupt enable (STAI) bit in PIOC is also set, an internal interrupt sequence is requested. The strobe A flag (STAF) is automatically cleared by reading the PIOC register (with STAF set) followed by a read of the PORTCL register. Data is latched in the PORTCL register whether or not the STAF flag was previously clear.

4.3.2 Strobed Output Port B

In this mode, the STRB pin is a strobe output which is pulsed for two E clock periods each time there is a write to port B. The INVB bit in the PIOC register controls the polarity of the pulse on the STRB line.

4.4 Full Handshake I/O

The full handshake modes of parallel I/O involve port C and the STRA and STRB lines. There are two basic modes (input and output) and an additional variation on the output handshake mode that allows three-stated operation of port C. In all handshake modes, STRA is an edge-detecting input, and STRB is a handshake output line.

When full input handshake protocol is specified, both general purpose input and/or general purpose output can coexist at port C. When full output handshake protocol is specified, general purpose output can coexist with the handshake outputs at port C, but the three-state feature of the output handshake mode interferes with general purpose input in two ways. First, in full output handshake, the port C lines are outputs whenever STRA is at its active level regardless of the data direction register bits. This potentially conflicts with any external device trying to drive port C unless that external device has an open-drain type output driver. Second, the value returned on reads of port C is the state of the outputs of an internal port C output latch regardless of the states of the data direction register bits, so that the data written for output handshake can be read even if the pins are in a three-state condition.

4.4.1 Input Handshake Protocol

In the input handshake protocol, port C is a latching input port, STRA is an edge-sensitive latch command from the external system that is driving port C, and STRB is a "ready" output line controlled by logic in the MCU.

When a "ready" condition is recognized, the external device places data on the port C lines, then pulses the STRA line. The active edge on the STRA line latches the port C data into the PORTCL register, sets the STAF flag (optionally causing an interrupt), and deasserts the STRB line. Deassertion of the STRB line automatically inhibits the external device from strobing new data into port C. Reading the PORTCL latch register (independent of clearing the STAF flag) asserts the STRB line, indicating that new data may now be applied to port C.

The STRB line can be configured (with the PLS control bit) to be a pulse output (pulse mode) or a static output (interlocked mode).

The port C data direction register bits should be cleared for each line that is to be used as a latched input line. However, some port C lines can be used as latched inputs with the input handshake protocol while, at the same time, using some port C lines as static inputs, and some port C lines as static outputs. The input handshake protocol has no effect on the use of port C lines as static inputs or as static outputs. Reads of the PORTC data register always return the static logic level at the port C lines (for lines configured as inputs). Writes to either the PORTC data register or the alternate latched port C register (PORTCL) send information to the same port C output register without affecting the input handshake strobes.

4.4.2 Output Handshake Protocol

In the output handshake protocol, port C is an output port, STRB is a "ready" output, and STRA is an edge-sensitive acknowledge input signal, used to indicate to the MCU that the output data has been accepted by the external device. In a variation of this output handshake protocol, STRA is also used as an output-enable input, as well as an edge-sensitive acknowledge input.

The MCU places data on the port C output lines and then indicates stable data is available by asserting the STRB line. The external device then processes the available data and pulses the STRA line to indicate that new data may be placed on the port C output lines. The active edge on the STRA line causes the STRB line to be deasserted and the STAF status flag to be set. In response to the STAF bit being set, the program transfers new data out of port C as required. Writing data to the PORTCL register causes the data to appear on port C lines and asserts the STRB line.

There is a variation to the output handshake protocol that allows three-state operation on port C. It is possible to directly connect this 8-bit parallel port to other three-state devices with no additional parts.

While the STRA input line is inactive, all port C lines obey the data direction specified by the data direction register so that lines which are configured as inputs are high impedance. When the STRA line is activated, all port C lines are forced to outputs regardless of the data in the data direction register. Note that in output handshake

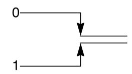
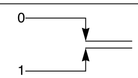
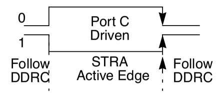
protocol, reads of port C always return the value sensed at the input to the output buffer regardless of the state of the data direction register bits because the lines would not necessarily have meaningful data on them in the three-state variation of this protocol. This operation makes it impractical to use some port C lines as static inputs, while using others as handshake outputs, but does not interfere with the use of some port C lines as static outputs. Port C lines intended as static outputs or normal handshake outputs should have their corresponding data direction register bits set, and lines intended as three-state handshake outputs should have their corresponding data direction register bits clear.

4.5 Parallel I/O Control Register (PIOC)

The parallel handshake I/O functions are available only in the single-chip operating mode. The PIOC is a read/write register except for bit 7 which is read only. **Table 4-1** shows a summary of handshake I/O operations.

Table 4-1 Handshake I/O Operations Summary

	STAI	CWOM	INVB
0	STAF Interrupts Inhibited	Port C Outputs Normal	STRB Active Low
1	STAF Interrupts Enabled	Port C Outputs Open-Drain	STRB Active High

	STAF Clearing Sequence[1]	HNDS	OIN	PLS	EGA	Port C	Port B
Simple Strobe Mode	Read PIOC with STAF = 1 then Read PORTCL	0	X	X		Inputs latched into PORTCL on any active edge on STRA.	STRB pulses on writes to port B.
Full Input Handshake	Read PIOC with STAF = 1 then Read PORTCL	1	0	0 = STRB Active Level 1 = STRB Active Pulse		Inputs latched into PORTCL on any active edge on STRA.	Normal output port. Unaffected in handshake modes
Full Output Handshake	Read PIOC with STAF = 1 then Write to PORTCL	1	1	0 = STRB Active Level 1 = STRB Active Pulse		Driven as outputs if STRA at active level. Follows DDRC if STRA not at active level.	Normal output port. Unaffected in handshake modes

NOTE:
1. Set by active edge on STRA

	7	6	5	4	3	2	1	0	
$1002	STAF	STAI	CWOM	HNDS	OIN	PLS	EGA	INVB	PIOC
RESET	0	0	0	0	0	U	1	1	

STAF — Strobe A Interrupt Status Flag
This bit is set when a selected edge occurs on strobe A. Clearing it depends on the state of HNDS and OIN bits. In simple strobed mode or in full input handshake mode, STAF is cleared by reading the PIOC register with STAF set followed by reading the PORTCL register. In output handshake, STAF is cleared by reading the PIOC register with STAF set followed by writing to the PORTCL register.

STAI — Strobe A Interrupt Enable Mask
When the I bit in the condition code register is clear and STAI is set, STAF (when set) will request an interrupt.

CWOM — Port C Wire-OR Mode
CWOM affects all eight port C pins together
- 0 = Port C outputs are normal CMOS outputs
- 1 = Port C outputs act as open-drain outputs

HNDS — Handshake Mode
When clear, strobe A acts as a simple input strobe to latch data into PORTCL, and strobe B acts as a simple output strobe which pulses after a write to port B. When set, a handshake protocol involving port C, STRA, and STRB is selected (see the definition for the OIN bit).
- 0 = Simple strobe mode
- 1 = Full input or output handshake mode

OIN — Output or Input Handshaking
This bit has no meaning when HNDS = 0.
- 0 = Input handshake
- 1 = Output handshake

PLS — Pulse/Interlocked Handshake Operation
This bit has no meaning if HNDS = 0. When interlocked handshake operation is selected, strobe B, once activated, stays active until the selected edge of strobe A is detected. When pulsed handshake operation is selected, strobe B is pulsed for two E cycles.
- 0 = Interlocked handshake select
- 1 = Pulsed handshake selected

EGA — Active Edge for Strobe A
- 0 = Falling edge of STRA is selected. When output handshake is selected, port C lines obey the data direction register while STRA is low, but port C is forced to output when STRA is high.
- 1 = Rising edge of STRA is selected. When output handshake is selected, port C lines obey the data direction register while STRA is high, but port C is forced to output when STRA is low.

INVB — Invert Strobe B
- 0 = Active level is logic zero
- 1 = Active level is logic one

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5.8.2 Serial Communications Control Register 1 (SCCR1)

The serial communications control register 1 (SCCR1) provides the control bits which: (1) determine the word length, and (2) select the method used for the wake-up feature.

	7	6	5	4	3	2	1	0	
$102C	R8	T8	0	M	WAKE	0	0	0	SCCR1
RESET	U	U	0	0	0	0	0	0	

R8 — Receive Data Bit 8
If the M bit is set, this bit provides a storage location for the ninth bit in the receive data character.

T8 —Transmit Data Bit 8
If the M bit is set, this bit provides a storage location for the ninth bit in the transmit data character. It is not necessary to write to this bit for every character transmitted, only when the sense is to be different than that for the previous character.

Bit 5 — Not Implemented
This bit always reads zero.

M — SCI Character Length
- 0 = 1 start bit, 8 data bits, 1 stop bit
- 1 = 1 start bit, 9 data bits, 1 stop bit

WAKE — Wake Up Method Select
- 0 = Idle Line
- 1 = Address Mark

Bits 2-0 — Not Implemented
These bits always read zero.

5.8.3 Serial Communications Control Register 2 (SCCR2)

The serial communications control register 2 (SCCR2) provides the control bits which enable/disable individual SCI functions.

	7	6	5	4	3	2	1	0	
$102D	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK	SCCR2
RESET	0	0	0	0	0	0	0	0	

TIE — Transmit Interrupt Enable
- 0 = TDRE interrupts disabled
- 1 = SCI interrupt if TDRE = 1

TCIE — Transmit Complete Interrupt Enable
0 = TC interrupts disabled
1 = SCI Interrupt if TC = 1

RIE — Receive Interrupt Enable
0 = RDRF and OR interrupts disabled
1 = SCI interrupt if RDRF or OR = 1

ILIE — Idle Line Interrupt Enable
0 = IDLE interrupts disabled
1 = SCI interrupt if IDLE = 1

TE — Transmit Enable
When the transmit enable bit is set, the transmit shift register output is applied to the TxD line. Depending on the state of control bit M (SCCR1), a preamble of 10 (M = 0) or 11 (M = 1) consecutive ones is transmitted when software sets the TE bit from a cleared state. After loading the last byte in the serial communications data register and receiving the TDRE flag, the user can clear TE. Transmission of the last byte will then be completed before the transmitter gives up control of the TxD pin. While the transmitter is active, the data direction register control for port D bit 1 is overridden and the line is forced to be an output.

RE — Receive Enable
When the receive enable bit is set, the receiver is enabled. When RE is clear, the receiver is disabled and all of the status bits associated with the receiver (RDRF, IDLE, OR, NF, and FE) are inhibited. While the receiver is enabled, the data direction register control for port D bit 0 is overridden and the line is forced to be an input.

RWU — Receiver Wake Up
When the receiver wake-up bit is set by the user's software, it puts the receiver to sleep and enables the "wake up" function. If the WAKE bit is cleared, RWU is cleared by the SCI logic after receiving 10 (M = 0) or 11 (M = 1) consecutive ones. If the WAKE bit is set, RWU is cleared by the SCI logic after receiving a data word whose MSB is set.

SBK — Send Break
If the send break bit is toggled set and cleared, the transmitter sends 10 (M = 0) or 11 (M = 1) zeros and then reverts to idle or sending data. If SBK remains set, the transmitter will continually send whole blocks of zeros (sets of 10 or 11) until cleared. At the completion of the break code, the transmitter sends at least one high bit to guarantee recognition of a valid start bit. If the transmitter is currently empty and idle, setting and clearing SBK is likely to queue two character times of break because the first break transfers almost immediately to the shift register and the second is then queued into the parallel transmit buffer.

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5.8.4 Serial Communications Status Register (SCSR)

The serial communications status register (SCSR) provides inputs to the interrupt logic circuits for generation of the SCI system interrupt.

	7	6	5	4	3	2	1	0	
$102E	TDRE	TC	RDRF	IDLE	OR	NF	FE	0	SCSR
RESET	1	1	0	0	0	0	0	0	

TDRE — Transmit Data Register Empty
The transmit data register empty bit is set to indicate that the content of the serial communications data register have been transferred to the transmit serial shift register. This bit is cleared by reading the SCSR (with TDRE = 1) followed by a write to the SCDR.

TC — Transmit Complete
The transmit complete bit is set at the end of a data frame, preamble, or break condition if:

1. TE = 1, TDRE = 1, and no pending data, preamble, or break is to be transmitted; or
2. TE = 0, and the data, preamble, or break in the transmit shift register has been transmitted.

The TC bit is a status flag which indicates that one of the above conditions have occurred.
The TC bit is cleared by reading the SCSR (with TC set) followed by a write to the SCDR.

RDRF — Receive Data Register Full
The receive data register full bit is set when the receiver serial shift register is transferred to the SCDR. The RDRF bit is cleared when the SCSR is read (with RDRF set) followed by a read of the SCDR.

IDLE — Idle Line Detect
The idle line detect bit, when set, indicates the receiver has detected an idle line. The IDLE bit is cleared by reading the SCSR with IDLE set followed by reading SCDR. Once the IDLE status flag is cleared, it will not be set again until after the RxD line has been active and becomes idle again.

OR — Overrun Error
The overrun error bit is set when the next byte is ready to be transferred from the receive shift register to the SCDR which is already full (RDRF bit is set). When an overrun error occurs, the data which caused the overrun is lost and the data which was already in SCDR is not disturbed. The OR is cleared when the SCSR is read (with OR set), followed by a read of the SCDR.

NF — Noise Flag

The noise flag bit is set if there is noise on any of the received bits, including the start and stop bits. The NF bit is not set until the RDRF flag is set. The NF bit is cleared when the SCSR is read (with NF set), followed by a read of the SCDR.

FE — Framing Error

The framing error bit is set when no stop bit was detected in the received data character. The FE bit is set at the same time as the RDRF is set. If the byte received causes both framing and overrun errors, the processor will only recognize the overrun error. The framing error flag inhibits further transfer of data into the SCDR until it is cleared. The FE bit is cleared when the SCSR is read (with FE equal to one) followed by a read of the SCDR.

Bit 0 — Not Implemented

This bit always reads zero.

5.8.5 Baud Rate Register (BAUD)

The baud rate register selects the different baud rates which may be used as the rate control for the transmitter and receiver. The SCP[0:1] bits function as a prescaler for the SCR[0:2] bits. Together, these five bits provide multiple baud rate combinations for a given crystal frequency.

	7	6	5	4	3	2	1	0	
$102B	TCLR	0	SCP1	SCP0	RCKB	SCR2	SCR1	SCR0	BAUD
RESET	0	0	0	0	0	U	U	U	

TCLR — Clear Baud Rate Counters (Test)

This bit is used to clear the baud rate counter chain during factory testing. TCLR is zero and cannot be set while in normal operating modes.

SCP1 and SCP0 — SCI Baud Rate Prescaler Selects

The E clock is divided by the factors shown in **Table 5-1**. This prescaled output provides an input to a divider which is controlled by the SCR2-SCR0 bits.

Table 5-1 First Prescaler Stage

SCP1	SCP0	Internal Processor Clock Divided By
0	0	1
0	1	3
1	0	4
1	1	13

SCR2, SCR1, and SCR0 — SCI Baud Rate Selects

These three bits select the baud rates for both the transmitter and the receiver. The prescaler output described above is further divided by the factors shown in **Table 5-2**.

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Table 5-2 Second Prescaler Stage

SCR2	SCR1	SCR0	Prescaler Output Divide By
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

RCKB — SCI Baud Rate Clock Check (Test)

This bit is used during factory testing to enable the exclusive-OR of the receiver clock and transmitter clock to be driven out the TxD pin. RCKB is zero and cannot be set while in normal operating modes.

The diagram shown in **Figure 5-7** and the data given in **Table 5-3** and **Table 5-4** illustrate the divider chain used to obtain the baud rate clock. Note that there is a fixed rate divide-by-16 between the receive clock (RT) and the transmit clock (Tx). The actual divider chain is controlled by the combined SCP[1:0] and SCR[2:0] bits in the baud rate register as illustrated.

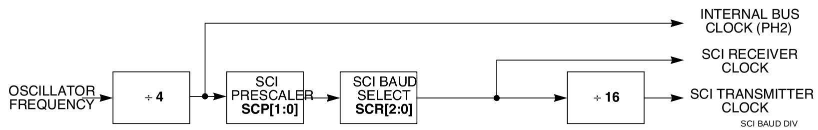

Figure 5-7 Rate Generator Division

Table 5-3 Prescaler Highest Baud Rate Frequency Output

SCP Bit		Clock* Divided By	Crystal Frequency (MHz)					
1	0		12.0	8.3886	8.0	4.9152	4.0	3.6864
0	0	1	187.50 K Baud	131.072 K Baud	125.000 K Baud	76.80 K Baud	62.50 K Baud	57.60 K Baud
0	1	3	62.50 K Baud	43.690 K Baud	41.666 K Baud	25.60 K Baud	20.833 K Baud	19.20 K Baud
1	0	4	46.875 K Baud	32.768 K Baud	31.250 K Baud	19.20 K Baud	15.625 K Baud	14.40 K Baud
1	1	13	14.423 K Baud	10.082 K Baud	9600 Baud	5.907 K Baud	4800 Baud	4430 Baud

*The clock in the "Clock Divided By" column is the internal processor clock

NOTE

The divided frequencies shown in **Table 5-3** represent baud rates which are the highest transmit baud rate (Tx) that can be obtained by a specific crystal frequency and only using the prescaler division. Lower baud rates may be obtained by providing a further division using the SCI rate select bits as shown below for some representative prescaler outputs.

Table 5-4 Transmit Baud Rate Output for a Given Prescaler Output

SCR Bit			Divided	Representative Highest Prescaler Baud Rate Output					
2	**1**	**0**	**By**	**131.072 K Baud**	**32.768 K Baud**	**76.80 K Baud**	**19.20 K Baud**	**9600 Baud**	**4800 Baud**
0	0	0	1	131.072 K Baud	32.768 K Baud	76.80 K Baud	19.20 K Baud	9600 Baud	4800 Baud
0	0	1	2	65.536 K Baud	16.384 K Baud	38.40 K Baud	9600 Baud	4800 Baud	2400 Baud
0	1	0	4	32.768 K Baud	8.192 K Baud	19.20 K Baud	4800 Baud	2400 Baud	1200 Baud
0	1	1	8	16.384 K Baud	4.096 K Baud	9600 Baud	2400 Baud	1200 Baud	600 Baud
1	0	0	16	8.192 K Baud	2.048 K Baud	4800 Baud	1200 Baud	600 Baud	300 Baud
1	0	1	32	4.096 K Baud	1.024 K Baud	2400 Baud	600 Baud	300 Baud	150 Baud
1	1	0	64	2.048 K Baud	512 Baud	1200 Baud	300 Baud	150 Baud	75 Baud
1	1	1	128	1.024 K Baud	256 Baud	600 Baud	150 Baud	75 Baud	—

NOTE

Table 5-4 illustrates how the SCI select bits can be used to provide lower transmitter baud rates by further dividing the prescaler output frequency. The five examples are only representative samples. In all cases, the baud rates shown are transmit baud rates (transmit clock) and the receiver clock is 16 times higher in frequency than the actual baud rate.

7 ANALOG-TO-DIGITAL CONVERTER

The MC68HC11A8 includes an 8-channel, multiplexed-input, successive approximation, analog-to-digital (A/D) converter with sample and hold to minimize conversion errors caused by rapidly changing input signals. Two dedicated lines (V_{RL}, V_{RH}) are provided for the reference voltage inputs. These pins may be connected to a separate or isolated power supply to ensure full accuracy of the A/D conversion. The 8-bit A/D converter has a total error of ±1 LSB which includes ± 1/2 LSB of quantization error and accepts analog inputs which range from V_{RL} to V_{RH}. Smaller analog input ranges can also be obtained by adjusting V_{RH} and V_{RL} to the desired upper and lower limits. Conversion is specified and tested for V_{RL} = 0 V and V_{RH} = 5 V ± 10%; however, laboratory characterization over the full temperature range indicates little or no degradation with V_{RH}-V_{RL} as low as 2.5 to 3 V. The A/D system can be operated with V_{RH} below V_{DD} and/or V_{RL} above V_{SS} as long as V_{RH} is above V_{RL} by enough to support the conversions (2.5 to 5.0 V). Each conversion is accomplished in 32 MCU E clock cycles, provided the E clock rate is greater than 750 kHz. For systems which operate at clock rates less than 750 kHz, an internal R-C oscillator must be used to clock the A/D system. The internal R-C oscillator is selected by setting the CSEL bit in the OPTION register.

NOTE

Only four A/D input channels are available in the 48-pin version.

7.1 Conversion Process

The A/D converter is ratiometric. An input voltage equal to V_{RL} converts to $00 and an input voltage equal to V_{RH} converts to $FF (full scale), with no overflow indication. For ratiometric conversions, the source of each analog input should use V_{RH} as the supply voltage and be referenced to V_{RL}.

Figure 7-1 shows the detailed sequence for a set of four conversions. This sequence begins one E clock cycle after a write to the A/D control/status register (ADCTL). **Figure 7-2** shows a model of the port E A/D channel inputs. This model is useful for understanding the effects of external circuitry on the accuracy of A/D conversions.

7.2 Channel Assignments

A multiplexer allows the single A/D converter to select one of sixteen analog signals. Eight of these channels correspond to port E input lines to the MCU, four of the channels are for internal reference points or test functions, and four channels are reserved for future use. **Table 7-1** shows the signals selected by the four channel select control bits.

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7.3 Single-Channel Operation

There are two variations of single-channel operation. In the first variation (SCAN = 0), the single selected channel is converted four consecutive times with the first result being stored in A/D result register 1 (ADR1) and the fourth result being stored in register ADR4. After the fourth conversion is complete, all conversion activity is halted until a new conversion command is written to the ADCTL register. In the second variation (SCAN = 1), conversions continue to be performed on the selected channel with the fifth conversion being stored in register ADR1 (overwriting the first conversion result), the sixth conversion overwrites ADR2, and so on.

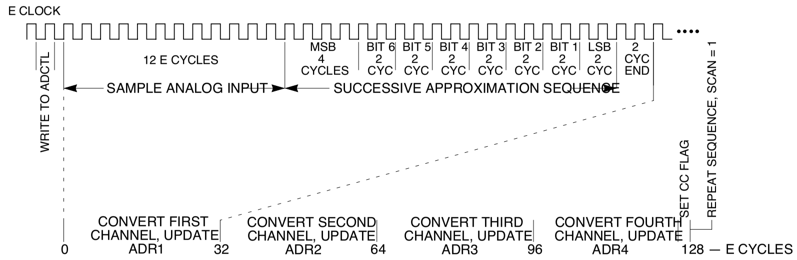
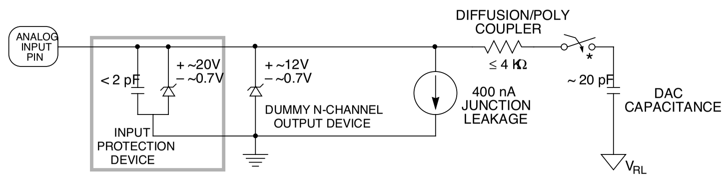


Figure 7-1 A/D Conversion Sequence



* THIS ANALOG SWITCH IS CLOSED ONLY DURING THE 12-CYCLE SAMPLE TIME.

Figure 7-2 A/D Pin Model

7.4 Multiple-Channel Operation

There are two variations in multiple-channel operation. In the first variation (SCAN = 0), the selected group of four channels are converted, one time each, with the first result being stored in register ADR1 and the fourth result being stored in register ADR4. After the fourth conversion is complete, all conversion activity is halted until a new conversion command is written to the ADCTL register. In the second variation (SCAN = 1), conversions continue to be performed on the selected group of channels with the fifth conversion being stored in register ADR1 (replacing the earlier conversion result for the first channel in the group), the sixth conversion overwrites ADR2, and so on.

7.5 Operation in STOP and WAIT Modes

If a conversion sequence is still in process when either the STOP or WAIT mode is entered, the conversion of the current channel is suspended. When the MCU resumes normal operation, that channel will be re-sampled and the conversion sequence resumed. As the MCU exits the WAIT mode, the A/D circuits are stable and valid results can be obtained on the first conversion. However, in STOP mode, all analog bias currents are disabled and it becomes necessary to allow a stabilization period when leaving the STOP mode. If the STOP mode is exited with a delay, there will be enough time for these circuits to stabilize before the first conversion. If the STOP mode is exited with no delay (DLY bit in OPTION register equal to zero), sufficient time must be allowed for the A/D circuitry to stabilize to avoid invalid results (see **7.8 A/D Power-Up and Clock Select**).

7.6 A/D Control/Status Register (ADCTL)

All bits in this register may be read or written, except bit 7 which is a read-only status indicator and bit 6 which always reads as a zero.

	7	6	5	4	3	2	1	0	
$1030	CCF	0	SCAN	MULT	CD	CC	CB	CA	ADCTL
RESET	0	0	U	U	U	U	U	U	

CCF — Conversions Complete Flag

This read-only status indicator is set when all four A/D result registers contain valid conversion results. Each time the ADCTL register is written, this bit is automatically cleared to zero and a conversion sequence is started. In the continuous modes, conversions continue in a round-robin fashion and the result registers continue to be updated with current data even though the CCF bit remains set.

NOTE

The user must write to register ADCTL to initiate conversion. To abort a conversion in progress, write to the ADCTL register and a new conversion sequence is initiated immediately.

Bit 6 — Not Implemented

This bit always reads zero.

SCAN — Continuous Scan Control

When this control bit is clear, the four requested conversions are performed once to fill the four result registers. When this control bit is set, conversions continue in a round-robin fashion with the result registers being updated as data becomes available.

MULT — Multiple-Channel/Single Channel Control

When this bit is clear, the A/D system is configured to perform four consecutive conversions on the single channel specified by the four channel select bits CD through CA (bits [3:0] of the ADCTL register). When this bit is set, the A/D system is configured to perform a conversion on each of four channels where each result register corresponds to one channel.

CAUTION

When the multiple channel continuous scan mode is used, extra care is needed in the design of circuitry driving the A/D inputs. Refer to the A/D Pin Model and A/D Conversion Sequence figures in addition to the following discussion. The charge on the capacitive DAC array prior to the sample time is related to the voltage on the previously converted channel. A charge share situation exists between the internal DAC capacitance and the external circuit capacitance. Although the amount of charge involved is small the rate at which it is repeated is every 64 microseconds for an E clock of 2 MHz. The RC charging rate of the external circuit must be balanced against this charge sharing effect to avoid accuracy errors.

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CD — Channel Select D
CC — Channel Select C
CB — Channel Select B
CA — Channel Select A

These four bits are used to select one of 16 A/D channels (see **Table 7-1**). When a multiple channel mode is selected (MULT = 1), the two least-significant channel select bits (CB and CA) have no meaning and the CD and CC bits specify which group of four channels are to be converted. The channels selected by the four channel select control bits are shown in **Table 7-1**.

Table 7-1 Analog-to-Digital Channel Assignments

CD	CC	CB	CA	Channel Signal	Result in ADRx if MULT=1
0	0	0	0	AN0	ADR1
0	0	0	1	AN1	ADR2
0	0	1	0	AN2	ADR3
0	0	1	1	AN3	ADR4
0	1	0	0	AN4*	ADR1
0	1	0	1	AN5*	ADR2
0	1	1	0	AN6*	ADR3
0	1	1	1	AN7*	ADR4
1	0	0	0	Reserved	ADR1
1	0	0	1	Reserved	ADR2
1	0	1	0	Reserved	ADR3
1	0	1	1	Reserved	ADR4
1	1	0	0	V_{RH} Pin**	ADR1
1	1	0	1	V_{RL} Pin**	ADR2
1	1	1	0	$(V_{RH})/2$**	ADR3
1	1	1	1	Reserved**	ADR4

*Not available in 48-pin package versions.
**This group of channels used during factory test.

7.7 A/D Result Registers 1, 2, 3, and 4 (ADR1, ADR2, ADR3, and ADR4)

The A/D result registers are read-only registers used to hold an 8-bit conversion result. Writes to these registers have no effect. Data in the A/D result registers is valid when the CCF flag bit in the ADCTL register is set, indicating a conversion sequence is complete. If conversion results are needed sooner refer to **Figure 7-1**. For example the ADR1 result is valid 33 cycles after an ADCTL write. Refer to the A/D channel assignments in **Table 7-1** for the relationship between the channels and the result registers.

7.8 A/D Power-Up and Clock Select

A/D power-up is controlled by bit 7 (ADPU) of the OPTION register. When ADPU is cleared, power to the A/D system is disabled. When ADPU is set, the A/D system is enabled. A delay of as much as 100 microseconds is required after turning on the A/D converter to allow the analog bias voltages to stabilize.

Clock select is controlled by bit 6 (CSEL) of the OPTION register. When CSEL is cleared, the A/D system uses the system E clock. When CSEL is set, the A/D system uses an internal R-C clock source, which runs at about 1.5 MHz. The MCU E clock is not suitable to drive the A/D system if it is operating below 750 kHz, in which case the R-C internal clock should be selected. A delay of 10 ms is required after changing CSEL from zero to one to allow the R-C oscillator to start and internal bias voltages to settle. Refer to **9.1.5 Configuration Options Register (OPTION)** for additional information. Note that the CSEL control bit also enables a separate R-C oscillator to drive the EEPROM charge pump.

When the A/D system is operating with the MCU E clock, all switching and comparator operations are synchronized to the MCU clocks. This allows the comparator results to be sampled at quiet clock times to minimize noise errors. The internal R-C oscillator is asynchronous to the MCU clock so noise will affect A/D results more while CSEL = 1.

8 PROGRAMMABLE TIMER, RTI, AND PULSE ACCUMULATOR

This section describes the 16-bit programmable timer, the real time interrupt, and the pulse accumulator system.

8.1 Programmable Timer

The timer has a single 16-bit free-running counter which is clocked by the output of a four-stage prescaler (divide by 1, 4, 8, or 16), which is in turn driven by the MCU E clock. Input functions are called input captures. These input captures record the count from the free-running counter in response to a detected edge on an input line. Output functions, called output compares, cause an output action when there is a match between a 16-bit output-compare register and the free-running counter. This timer system has three input capture registers and five output compare registers.

8.1.1 Counter

The key element in the timer system is a 16-bit free-running counter, or timer counter register. After reset, the MCU is configured to use the E clock as the input to the free-running counter. Initialization software may optionally reconfigure the system to use one of the three prescaler values. The prescaler control bits can only be written once during the first 64 cycles after a reset. Software can read the counter at any time without affecting its value because it is clocked and read during opposite phases of the E clock.

A counter read should first address the most significant byte. An MPU read of this address causes the least significant byte to be transferred to a buffer. This buffer is not affected by reset and is accessed when reading the least significant byte of the counter. For double byte read instructions, the two accesses occur on consecutive bus cycles.

The counter is cleared to $0000 during reset and is a read-only register with one exception. In test modes only, any MPU write to the most significant byte presets the counter to $FFF8 regardless of the value involved in the write.

When the count changes from $FFFF to $0000, the timer overflow flag (TOF) bit is set in timer interrupt flag register 2 (TFLG2). An interrupt can be enabled by setting the interrupt enable bit (TOI) in timer interrupt mask register 2 (TMSK2).

8.1.2 Input Capture

The input capture registers are 16-bit read-only registers which are not affected by reset and are used to latch the value of the counter when a defined transition is sensed by the corresponding input capture edge detector. The level transition which triggers counter transfer is defined by the corresponding input edge bits (EDGxB, EDGxA) in TCTL2.

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The result obtained by an input capture corresponds to the value of the counter one E clock cycle after the transition which triggered the edge-detection logic. The selected edge transition sets the ICxF bit in timer interrupt flag register 1 (TFLG1) and can cause an interrupt if the corresponding ICxI bit(s) is (are) set in the timer interrupt mask register 1 (TMSK1). A read of the input capture register's most significant byte inhibits captures for one E cycle to allow a double-byte read of the full 16-bit register.

8.1.3 Output Compare

All output compare registers are 16-bit read/write registers which are initialized to $FFFF by reset. They can be used as output waveform controls or as elapsed time indicators. If an output compare register is not used, it may be used as a storage location.

All output compare registers have a separate dedicated comparator for comparing against the free-running counter. If a match is found, the corresponding output compare flag (OCxF) bit in TFLG1 is set and a specified action is automatically taken. For output compare functions two through five the automatic action is controlled by pairs of bits (OMx and OLx) in the timer control register 1 (TCTL1). Each pair of control bits are encoded to specify the output action to be taken as a result of a successful OCx compare. The output action is taken on each successful compare regardless of whether or not the OCxF flag was previously clear.

An interrupt can also accompany a successful output compare, provided that the corresponding interrupt enable bit (OCxI) is set in TMSK1.

After a write cycle to the most significant byte, output compares are inhibited for one E cycle in order to allow writing two consecutive bytes before making the next comparison. If both bytes of the register are to be changed, a double-byte write instruction should be used in order to take advantage of the compare inhibit feature.

Writes can be made to either byte of the output compare register without affecting the other byte.

A write-only register, timer compare force (CFORC), allows forced compares. Five of the bit positions in the CFORC register correspond to the five output compares. To force a compare, or compares, a write is done to CFORC register with the associated bits set for each output compare that is to be forced. The action taken as a result of a forced compare is the same as if there was a match between the OCx register and the free-running counter, except that the corresponding interrupt status flag bits are not set. Output actions are synchronized to the prescaled timer clock so there could be as much as 16 E clock cycles of delay between the write to CFORC and the output action.

8.1.4 Output Compare 1 I/O Pin Control

Unlike the other four output compares, output compare 1 can automatically affect any or all of the five output pins (bits 3-7) in port A as a result of a successful compare between the OC1 register and the 16-bit free-running counter. The two 5-bit registers used in conjunction with this function are the output compare 1 mask register (OC1M) and the output compare 1 data register (OC1D).

Register OC1M is used to specify the bits of port A (I/O and timer port) which are to be affected as a result of a successful OC1 compare. Register OC1D is used to specify the data which is to be stored to the affected bits of port A as the result of a successful OC1 compare. If an OC1 compare and another output compare occur during the same E cycle and both attempt to alter the same port A line, the OC1 compare prevails.

This function allows control of multiple I/O pins automatically with a single output compare.

Another intended use for the special I/O pin control on output compare 1 is to allow more than one output compare to control a single I/O pin. This allows pulses as short as one E clock cycle to be generated.

8.1.5 Timer Compare Force Register (CFORC)

The timer compare force register is used to force early output compare actions. The CFORC register is an 8-bit write-only register. Reads of this location have no meaning and always return logic zeros. Note that the compare force function is not generally recommended for use with the output toggle function because a normal compare occurring immediately before or after the force may result in undesirable operation.

	7	6	5	4	3	2	1	0	
$100B	FOC1	FOC2	FOC3	FOC4	FOC5	0	0	0	CFORC
RESET	0	0	0	0	0	0	0	0	

FOC1-FOC5 — Force Output Compare x Action
- 0 = Has no meaning
- 1 = Causes action programmed for output compare x, except the OCxF flag bit is not set.

Bits 2-0 — Not Implemented
These bits always read zero.

8.1.6 Output Compare 1 Mask Register (OC1M)

This register is used in conjunction with output compare 1 to specify the bits of port A which are affected as a result of a successful OC1 compare.

	7	6	5	4	3	2	1	0	
$100C	OC1M7	OC1M6	OC1M5	OC1M4	OC1M3	0	0	0	OC1M
RESET	0	0	0	0	0	0	0	0	

The bits of the OC1M register correspond bit-for-bit with the lines of port A (lines 7 through 3 only). For each bit that is affected by the successful compare, the corresponding bit in OC1M should be set to one.

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Note that the pulse accumulator function shares line 7 of port A. If the DDRA7 bit in the pulse accumulator control register (PACTL) is set, then port A line 7 is configured as an output and OC1 can obtain access by setting OC1M bit 7. In this condition if the PAEN bit in the PACTL register is set, enabling the pulse accumulator input, then OC1 compares cause a write of OC1D bit 7 to an internal latch, and the output of that latch drives the pin and the pulse accumulator input. This action can then cause the pulse accumulator to take the appropriate action (pulse count or gate modes).

8.1.7 Output Compare 1 Data Register (OC1D)

This register is used in conjunction with output compare 1 to specify the data which is to be stored to the affected bits of port A as the result of a successful OC1 compare.

	7	6	5	4	3	2	1	0	
$100D	OC1D7	OC1D6	OC1D5	OC1D4	OC1D3	0	0	0	OC1D
RESET	0	0	0	0	0	0	0	0	

The bits of the OC1D register correspond bit-for-bit with the lines of port A (lines 7 thru 3 only). When a successful OC1 compare occurs, for each bit that is set in OC1M, the corresponding data bit in OC1D is stored in the corresponding bit of port A. If there is a conflicting situation where an OC1 compare and another output compare function occur during the same E cycle with both attempting to alter the same port A line, the OC1 action prevails.

8.1.8 Timer Control Register 1 (TCTL1)

	7	6	5	4	3	2	1	0	
$1020	OM2	OL2	OM3	OL3	OM4	OL4	OM5	OL5	TCTL1
RESET	0	0	0	0	0	0	0	0	

OM2, OM3, OM4, and OM5 — Output Mode
OL2, OL3, OL4, and OL5 — Output Level
These two control bits (OMx and OLx) are encoded to specify the output action taken as a result of a successful OCx compare.

OMx	OLx	Action Taken Upon Successful Compare
0	0	Timer disconnected from output pin logic
0	1	Toggle OCx output line
1	0	Clear OCx output line to zero
1	1	Set OCx output line to one

8.1.9 Timer Control Register 2 (TCTL2)

	7	6	5	4	3	2	1	0	
$1021	0	0	EDG1B	EDG1A	EDG2B	EDG2A	EDG3B	EDG3A	TCTL2
RESET	0	0	0	0	0	0	0	0	

Bits 7-6 — Not Implemented
These bits always read zero.

EDGxB and EDGxA — Input Capture x Edge Control.
These two bits (EDGxB and EDGxA) are cleared to zero by reset and are encoded to configure the input sensing logic for input capture x as follows:

EDGxB	EDBxA	Configuration
0	0	Capture disabled
0	1	Capture on rising edges only
1	0	Capture on falling edges only
1	1	Capture on any (rising or falling) edge

8.1.10 Timer Interrupt Mask Register 1 (TMSK1)

	7	6	5	4	3	2	1	0	
$1022	OC1I	OC2I	OC3I	OC4I	OC5I	IC1I	IC2I	IC3I	TMSK1
RESET	0	0	0	0	0	0	0	0	

OCxI — Output Compare x Interrupt
If the OCxI enable bit is set when the OCxF flag bit is set, a hardware interrupt sequence is requested.

ICxI — Input Capture x Interrupt
If the ICxI enable bit is set when the ICxF flag bit is set, a hardware interrupt sequence is requested.

8.1.11 Timer Interrupt Flag Register 1 (TFLG1)

Timer interrupt flag register 1 is used to indicate the occurrence of timer system events, and together with the TMSK1 register allows the timer subsystem to operate in a polled or interrupt driven system. For each bit in TFLG1, there is a corresponding bit in TMSK1 in the same bit position. If the mask bit is set, each time the conditions for the corresponding flag are met, a hardware interrupt sequence is requested as well as the flag bit being set.

These timer system status flags are cleared by writing a one to the bit positions corresponding to the flag(s) which are to be cleared. Bit manipulation instructions would be inappropriate for flag clearing because they are read-modify-write instructions. Even though the instruction mask implies that the programmer is only interested in some of the bits in the manipulated location, the entire location is actually read and rewritten which may clear other bits in the register.

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	7	6	5	4	3	2	1	0	
$1023	OC1F	OC2F	OC3F	OC4F	OC5F	IC1F	IC2F	IC3F	TFLG1
RESET	0	0	0	0	0	0	0	0	

OCxF — Output Compare x Flag
This flag bit is set each time the timer counter matches the output compare register x value. A write of a zero does not affect this bit. A write of a one causes this bit to be cleared.

ICxF — Input Capture x Flag
This flag is set each time a selected active edge is detected on the ICx input line. A write of a zero does not affect this bit. A write of a one causes this bit to be cleared.

8.1.12 Timer Interrupt Mask Register 2 (TMSK2)

Timer interrupt mask register 2 is used to control whether or not a hardware interrupt sequence is requested as a result of a status bit being set in timer interrupt flag register 2. In addition, two timer prescaler bits are included in this register. For each of the four most significant bits in timer flag register 2, (TFLG2), there is a corresponding bit in the timer mask register 2 (TMSK2) in the same bit position.

	7	6	5	4	3	2	1	0	
$1024	TOI	RTII	PAOVI	PAII	0	0	PR1	PR0	TMSK2
RESET	0	0	0	0	0	0	0	0	

TOI — Timer Overflow Interrupt Enable
0 = TOF interrupts disabled
1 = Interrupt requested when TOF = 1

RTII — RTI Interrupt Enable
0 = RTIF interrupts disabled
1 = Interrupt requested when RTIF = 1

PAOVI — Pulse Accumulator Overflow Interrupt Enable
0 = PAOVF interrupts disabled
1 = Interrupt requested when PAOVF = 1

PAII — Pulse Accumulator Input Interrupt Enable
0 = PAIF interrupts disabled
1 = Interrupt requested when PAIF = 1

Bits 3 and 2 — Not Implemented
These bits always read zero.

PR1 and PR0 — Timer Prescaler Selects

These two bits may be read at any time but may only be written during initialization. Writes are disabled after the first write or after 64 E cycles out of reset. If the MCU is in special test or special bootstrap mode, then these two bits may be written any time.

These two bits specify the timer prescaler divide factor.

PR1	PR0	Prescaler
0	0	÷ 1
0	1	÷ 4
1	0	÷ 8
1	1	÷ 16

8.1.13 Timer Interrupt Flag Register 2 (TFLG2)

Timer interrupt flag register 2 is used to indicate the occurrence of timer system events and, together with the TMSK2 register, allows the timer subsystems to operate in a polled or interrupt driven system. For each bit in timer flag register 2 (TFLG2), there is a corresponding bit in timer mask register 2 (TMSK2) in the same bit position. If the enable bit is set each time the conditions for the corresponding flag are met, a hardware interrupt sequence is requested as well as the flag bit being set.

The timer system status flags are cleared by writing a one to the bit positions corresponding to the flag(s) which are to be cleared. Bit manipulation instructions would be inappropriate for flag clearing because they are read-modify-write instructions. Even though the instruction mask implies that the programmer is only interested in some of the bits in the manipulated location, the entire location is actually read and rewritten which may clear other bits in the register.

	7	6	5	4	3	2	1	0	
$1025	TOF	RTIF	PAOVF	PAIF	0	0	0	0	TFLG2
RESET	0	0	0	0	0	0	0	0	

TOF — Timer Overflow

This bit is cleared by reset. It is set to one each time the 16-bit free-running counter advances from a value of $FFFF to $0000. This bit is cleared by a write to the TFLG2 register with bit 7 set.

RTIF — Real Time Interrupt Flag

This bit is set at each rising edge of the selected tap point. This bit is cleared by a write to the TFLG2 register with bit 6 set.

PAOVF — Pulse Accumulator Overflow Interrupt Flag

This bit is set when the count in the pulse accumulator rolls over from $FF to $00. This bit is cleared by a write to the TFLG2 register with bit 5 set.

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PAIF — Pulse Accumulator Input Edge Interrupt Flag

This bit is set when an active edge is detected on the PAI input pin. This bit is cleared by a write to the TFLG2 register with bit 4 set.

Bits 3-0 — Not Implemented

These bits always read zero.

8.2 Real-Time Interrupt

The real-time interrupt feature on the MCU is configured and controlled by using two bits (RTR1 and RTR0) in the PACTL register to select one of four interrupt rates. The RTII bit in the TMSK2 register enables the interrupt capability. Every timeout causes the RTIF bit in TFLG2 to be set, and if RTII is set, an interrupt request is generated. After reset, one entire real time interrupt period elapses before the RTIF flag is set for the first time.

8.3 Pulse Accumulator

The pulse accumulator is an 8-bit read/write counter which can operate in either of two modes (external event counting or gated time accumulation) depending on the state of the PAMOD control bit in the PACTL register. In the event counting mode, the 8-bit counter is clocked to increasing values by an external pin. The maximum clocking rate for the external event counting mode is E clock divided by two. In the gated time accumulation mode, a free-running E clock/64 signal drives the 8-bit counter, but only while the external PAI input pin is enabled.

The pulse accumulator uses port A bit 7 as its PAI input, but this pin also shares function as a general purpose I/O pin and as a timer output compare pin. Normally port A bit 7 would be configured as an input when being used for the pulse accumulator. Note that even when port A bit 7 is configured for output, this pin still drives the input to the pulse accumulator.

8.3.1 Pulse Accumulator Control Register (PACTL)

Four bits in this register are used to control an 8-bit pulse accumulator system and two other bits are used to select the rate for the real time interrupt system.

	7	6	5	4	3	2	1	0	
$1026	DDRA7	PAEN	PAMOD	PEDGE	0	0	RTR1	RTR0	PACTL
RESET	0	0	0	0	0	0	0	0	

DDRA7 — Data Direction for Port A Bit 7

0 = Input only
1 = Output

PAEN — Pulse Accumulator System Enable

0 = Pulse accumulator off
1 = Pulse accumulator on

PAMOD — Pulse Accumulator Mode
0 = External event counting
1 = Gated time accumulation

PEDGE — Pulse Accumulator Edge Control
This bit has different meanings depending on the state of the PAMOD bit.

PAMOD	PEDGE	Action on Clock
0	0	PAI Falling Edge Increments the Counter
0	1	PAI Rising Edge Increments the Counter
1	0	A zero on PAI Inhibits Counting
1	1	A one on PAI Inhibits Counting

Bits 3-2 — Not Implemented
These bits always read zero.

RTR1 and RTR0 — RTI Interrupt Rate Selects
These two bits select one of four rates for the real time periodic interrupt circuit (see **Table 8-1**). Reset clears these two bits and after reset, a full RTI period elapses before the first RTI interrupt.

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Table 8-1 Real Time Interrupt Rate versus RTR1 and RTR0

RTR1	RTR0	Rate	XTAL = 12.0 MHz	XTAL = 2^{23}	XTAL = 8.0 MHz	XTAL = 4.9152 MHz	XTAL = 4.0 MHz	XTAL = 3.6864 MHz
0	0	$2^{13} \div E$	8.192 ms	3.91 ms	4.10 ms	6.67 ms	8.19 ms	8.89 ms
0	1	$2^{14} \div E$	16.384 ms	7.81 ms	8.19 ms	13.33 ms	16.38 ms	17.78 ms
1	0	$2^{15} \div E$	32.768 ms	15.62 ms	16.38 ms	26.67 ms	32.77 ms	35.56 ms
1	1	$2^{16} \div E$	65.536 ms	31.25 ms	32.77 ms	53.33 ms	65.54 ms	71.11 ms
		E =	**3.0 MHz**	**2.1 MHz**	**2.0 MHz**	**1.2288 MHz**	**1.0 MHz**	**921.6 kHz**

of reset. The DLY control bit is set to specify that an oscillator start-up delay is imposed upon recovery from STOP mode. The clock monitor system is disabled by CME equal zero.

9.1.3 Computer Operating Properly (COP) Reset

The MCU includes a computer operating properly watchdog system to help protect against software failures. To use a COP watchdog timer, a watchdog timer reset sequence must be executed on a regular periodic basis so that the watchdog timer is never allowed to time out.

The internal COP function includes special control bits which permit specification of one of four time out periods and even allows the function to be disabled completely. The COP system has a separate reset vector.

The NOCOP control bit, which determines whether or not a watchdog timeout causes a system reset, is implemented in an EEPROM cell in the CONFIG register. Once programmed, this bit remains set (or cleared) even when no power is applied, and the COP function is enabled or disabled independent of resident software. The NOCOP control bit may be preempted while in special modes to prevent the COP system from causing a hardware reset.

Two other control bits in the OPTION register select one of four timeout durations for the COP timer. The actual timeout period is dependent on the system E clock frequency, but for reference purposes, **Table 9-1** shows the relationship between the CR1 and CR0 control bits and the COP timeout period for various system clock frequencies.

Table 9-1 COP Timeout Period versus CR1 and CR0

CR1	CR0	Rate	XTAL = 12.0 MHz Timeout −0/+10.9 ms	XTAL = 2^{23} Timeout – 0/+15.6 ms	XTAL = 8.0 MHz Timeout – 0/+16.4 ms	XTAL = 4.9152 MHz Timeout – 0/+26.7 ms	XTAL = 4.0 MHz Timeout – 0/+32.8 ms	XTAL = 3.6864 MHz Timeout – 0/+35.6 ms
0	0	$2^{15} \div E$	10.923 ms	15.625 ms	16.384 ms	26.667 ms	32.768 ms	35.556 ms
0	1	$2^{17} \div E$	43.691 ms	62.5 ms	65.536 ms	106.67 ms	131.07 ms	142.22 ms
1	0	$2^{19} \div E$	174.76 ms	250 ms	262.14 ms	426.67 ms	524.29 ms	568.89 ms
1	1	$2^{21} \div E$	699.05 ms	1 s	1.049 s	1.707 s	2.1 s	2.276 s
		E =	**3.0 MHz**	**2.1 MHz**	**2.0 MHz**	**1.2288 MHz**	**1.0 MHz**	**921.6 kHz**

The default reset condition of the CR1 and CR0 bits is cleared which corresponds to the shortest timeout period.

The sequence required to reset the watchdog timer is:

1. Write $55 to the COP reset register (COPRST) at $103A, followed by
2. Write $AA to the same address.

Both writes must occur in correct order prior to timeout but, any number of instructions may be executed between the writes. The elapsed time between adjacent software reset sequences must never be greater than the COP time out period. Reading the COPRST register does not return meaningful data and does not affect the watchdog timer.

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9.1.4 Clock Monitor Reset

The clock monitor function is enabled by the CME control bit in the OPTION register. When CME is clear, the monitor function is disabled. When the CME bit is set, the clock monitor function detects the absence of an E clock for more than a certain period of time. The timeout period is dependent on processing parameters and will be between 5 and 100 microseconds. This means that an E-clock rate of 200 kHz or more will never cause a clock monitor failure and an E-clock rate of 10 kHz or less will definitely cause a clock monitor failure. This implies that systems operating near or below an E-clock rate of 200 kHz should not use the clock monitor function.

Upon detection of a slow or absent clock, the clock monitor circuit will cause a system reset. This reset is issued to the external system via the bidirectional $\overline{\text{RESET}}$ pin. The clock monitor system has a separate reset vector.

Special considerations are needed when using a STOP function and clock monitor in the same system. Since the STOP function causes the clocks to be halted, the clock monitor function will generate a reset sequence if it is enabled at the time the STOP mode is entered.

The clock monitor is useful as a backup for the COP watchdog timer. Since the watchdog timer requires a clock to function, it will not indicate any failure if the system clocks fail. The clock monitor would detect such a failure and force the MCU to its reset state. Note that clocks are not required for the MCU to reach its reset configuration, although clocks are required to sequence through reset back to the run condition.

9.1.5 Configuration Options Register (OPTION)

This is a special purpose 8-bit register that is used (optionally) during initialization to configure internal system configuration options. With the exception of bits 7, 6, and 3 (ADPU, CSEL, and CME) which may be read or written at any time, this register may be written to only once after a reset and thereafter is a read-only register. If no write is performed to this location within 64 E-clock cycles after reset, then bits 5, 4, 1, and 0 (IRQE, DLY, CR1, and CR0) will become read-only to minimize the possibility of any accidental changes to the system configuration (writes will be ignored). While in special test modes, the protection mechanism on this register is preempted and all bits in the OPTION register may be written repeatedly.

	7	6	5	4	3	2	1	0	
$1039	ADPU	CSEL	IRQE	DLY	CME	0	CR1	CR0	OPTION
RESET	0	0	0	1	0	0	0	0	

ADPU — A/D Power-up

This bit controls operations of the on-chip analog-to-digital converter. When ADPU is clear, the A/D system is powered down and conversion requests will not return meaningful information. To use the A/D system, this bit should be set. A 100 microsecond delay is required after ADPU is turned on to allow the A/D system to stabilize.

CSEL — A/D/EE Charge Pump Clock Source Select

This bit determines the clocking source for the on-chip A/D and EEPROM charge pump. When this bit is zero, the MCU E clock drives the A/D system and the EEPROM charge pump. When CSEL is one, on-chip separate R-C oscillators are enabled and clock the systems at about 2 MHz. When running with an E clock below 1 MHz, CSEL must be high to program or erase EEPROM. When operating below 750 kHz E clock rate, CSEL should be high for A/D conversions. A delay of 10 milliseconds is required after CSEL is turned on to allow the A/D system to stabilize.

IRQE — IRQ Edge/Level Sensitive

This bit may only be written under special circumstances as described above. When this bit is clear, the $\overline{IRQ}$ pin is configured for level sensitive wired-OR operation (low level) and when it is set, the $\overline{IRQ}$ pin is configured for edge-only sensitivity (falling edges).

DLY — STOP Exit Turn-On Delay

This bit may only be written under special circumstances as described above. This bit is set during reset and controls whether or not a relatively long turn-on delay will be imposed before processing can resume after a STOP period. If an external clock source is supplied this delay can be inhibited so that processing can resume within a few cycles of a wake up from STOP mode. When DLY is set, a 4064 E clock cycle delay is imposed to allow oscillator stabilization and when DLY is clear, this delay is bypassed.

CME — Clock Monitor Enable

This control bit may be read or written at any time and controls whether or not the internal clock monitor circuit will trigger a reset sequence when a slow or absent system clock is detected. When it is clear, the clock monitor circuit is disabled and when it is set, the clock monitor circuit is enabled. Systems operating at or below 200 kHz should not use the clock monitor function. Reset clears the CME bit.

Bit 2 — Not Implemented

This bit always reads zero.

CR1 and CR0 — COP Timer Rate Selects

These bits may only be written under special circumstances as described above. Refer to **Table 9-1** for the relationship between CR1:CR0 and the COP timeout period.

9.2 Interrupts

When an external or internal (hardware) interrupt occurs, the interrupt is not serviced until the current instruction being executed is completed. Until the current instruction is complete, the interrupt is considered pending. After completion of current instruction execution, unmasked interrupts may be serviced in accordance with an established fixed hardware priority circuit; however, one I-bit related interrupt source may be dynamically elevated to the highest I bit priority position in the hierarchy (see **9.2.5 Highest Priority I Interrupt Register (HPRIO)**).

Seventeen hardware interrupts and one software interrupt (excluding reset type interrupts) can be generated from all of the possible sources. The interrupts can be divided

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into two basic categories, maskable and non-maskable. In the MC68HC11A8 fifteen of the interrupts can be masked using the condition code register I bit. In addition to being maskable by the I bit in the condition code register, all of the on-chip interrupt sources are individually maskable by local control bits.

Table 9-2 IRQ Vector Interrupts

Interrupt Cause	Local Mask
External Pin	None
Parallel I/O Handshake	STAI

The software interrupt (SWI instruction) is a non-maskable instruction rather than a maskable interrupt source. The illegal opcode interrupt is a non-maskable interrupt. The last interrupt source, external input to the $\overline{XIRQ}$ pin, is considered a non-maskable interrupt because once enabled, it cannot be masked by software; however, it is masked during reset and upon receipt of an interrupt at the $\overline{XIRQ}$ pin. **Table 9-2**, **Table 9-3**, and **Table 9-4** provide a list of each interrupt, its vector location in memory, and the actual condition code and control bits that mask it. A discussion of the various interrupts is provided below. **Figure 9-3** shows the interrupt stacking order.

Table 9-3 Interrupt Vector Assignments

Vector Address	Interrupt Source	CC Register Mask	Local Mask
FFC0, C1	Reserved	—	—
•	•		
•	•		
FFD4, D5	Reserved	—	—
FFD6, D7	SCI Serial System	I Bit	See Table 9-3
FFD8, D9	SPI Serial Transfer Complete	I Bit	SPIE
FFDA, DB	Pulse Accumulator Input Edge	I Bit	PAII
FFDC, DD	Pulse Accumulator Overflow	I Bit	PAOVI
FFDE, DF	Timer Overflow	I Bit	TOI
FFE0, E1	Timer Output Compare 5	I Bit	OC5I
FFE2, E3	Timer Output Compare 4	I Bit	OC4I
FFE4, E5	Timer Output Compare 3	I Bit	OC3I
FFE6, E7	Timer Output Compare 2	I Bit	OC2I
FFE8, E9	Timer Output Compare 1	I Bit	OC1I
FFEA, EB	Timer Input Capture 3	I Bit	OC3I
FFEC, ED	Timer Input Capture 2	I Bit	OC2I
FFEE, EF	Timer Input Capture 1	I Bit	OC1I
FFF0, F1	Real Time Interrupt	I Bit	RTII
FFF2, F3	$\overline{IRQ}$ (External Pin or Parallel I/O)	I Bit	See Table 9-4
FFF4, F5	$\overline{XIRQ}$ Pin (Pseudo Non-Maskable Interrupt)	X Bit	None
FFF6, F7	SWI	None	None
FFF8, F9	Illegal Opcode Trap	None	None
FFFA, FB	COP Failure (Reset)	None	NOCOP
FFFC, FD	COP Clock Monitor Fail (Reset)	None	CME
FFFE, FF	$\overline{RESET}$	None	None

Table 9-4 SCI Serial System Interrupts

Interrupt Cause	Local Mask
Receive Data Register Full	RIE
Receiver Overrun	RIE
Idle Line Detect	ILIE
Transmit Data Register Empty	TIE
Transmit Complete	TCIE

9.2.1 Software Interrupt (SWI)

The software interrupt is executed in the same manner as any other instruction and will take precedence over interrupts only if the other interrupts are masked (I and X bits in the condition code register set). The SWI instruction is executed in a manner similar to other maskable interrupts in that it sets the I bit, CPU registers are stacked, etc.

NOTE

The SWI instruction will not be fetched if an interrupt is pending. However, once an SWI instruction has begun, no interrupt can be honored until the SWI vector has been fetched.

	7 … 0	
SP	PCL	— SP BEFORE INTERRUPT
SP–1	PCH	
SP–2	IYL	
SP–3	IYH	
SP–4	IXL	
SP–5	IXH	
SP–6	ACCA	
SP–7	ACCB	
SP–8	CCR	
SP–9		— SP AFTER INTERRUPT

Figure 9-3 Interrupt Stacking Order

9.2.2 Illegal Opcode Trap

Since not all possible opcodes or opcode sequences are defined, an illegal opcode detection circuit has been included. When an illegal opcode is detected, an interrupt is requested to the illegal opcode vector. The illegal opcode vector should never be left uninitialized. It is a good idea to reinitialize the stack pointer as a result of an illegal opcode interrupt so repeated execution of illegal opcodes does not cause stack overruns.

9.2.3 Interrupt Mask Bits in Condition Code Register

Upon reset, both the X bit and the I bit are set to inhibit all maskable interrupts and $\overline{XIRQ}$. After minimum system initialization, software may clear the X bit by a TAP instruction, thus enabling $\overline{XIRQ}$ interrupts. Thereafter software cannot set the X bit so an $\overline{XIRQ}$ interrupt is effectively a nonmaskable interrupt. Since the operation of the I

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bit related interrupt structure has no effect on the X bit, the external $\overline{XIRQ}$ pin remains effectively non-masked. In the interrupt priority logic, the $\overline{XIRQ}$ interrupt is a higher priority than any source that is maskable by the I bit. All I bit related interrupts operate normally with their own priority relationship. When an I bit related interrupt occurs, the I bit is automatically set by hardware after stacking the condition code register byte, but the X bit is not affected. When an X bit related interrupt occurs, both the X bit and the I bit are automatically set by hardware after stacking the condition code register. An RTI (return from interrupt) instruction restores the X and I bits to their pre-interrupt request state.

9.2.4 Priority Structure

Interrupts obey a fixed hardware priority circuit to resolve simultaneous requests; however, one I bit related interrupt source may be elevated to the highest I bit priority position in the resolution circuit. The first six interrupt sources are not masked by the I bit in the condition code register and have the fixed priority interrupt relationship of: reset, clock monitor fail, COP fail, illegal opcode, and $\overline{XIRQ}$. (SWI is actually an instruction and has highest priority other than reset in the sense that once the SWI opcode is fetched, no other interrupt can be honored until the SWI vector has been fetched). Each of these sources is an input to the priority resolution circuit. The highest I bit masked priority input to the resolution circuit is assigned under software control (of the HPRIO register) to be connected to any one of the remaining I bit related interrupt sources. In order to avoid timing races, the HPRIO register may only be written while the I bit related interrupts are inhibited (I bit in condition code register is a logic one). An interrupt that is assigned to this high priority position is still subject to masking by any associated control bits or the I bit in the condition code register. The interrupt vector address is not affected by assigning a source to this higher priority position.

Figure 9-4, **Figure 9-5**, and **Figure 9-6** illustrate the interrupt process as it relates to normal processing. **Figure 9-4** shows how the CPU begins from a reset and how interrupt detection relates to normal opcode fetches. **Figure 9-5** is an expansion of a block in **Figure 9-4** and shows how interrupt priority is resolved. **Figure 9-6** is an expansion of the SCI interrupt block in **Figure 9-5**. **Figure 9-6** shows the resolution of interrupt sources within the SCI subsystem.

9.2.5 Highest Priority I Interrupt Register (HPRIO)

This register is used to select one of the I bit related interrupt sources to be elevated to the highest I bit masked position in the priority resolution circuit. In addition, four miscellaneous system control bits are included in this register.

	7	6	5	4	3	2	1	0	
$103C	RBOOT	SMOD	MDA	IRV	PSEL3	PSEL2	PSEL1	PSEL0	HPRIO
RESET	—	—	—	—	0	1	0	1	

RBOOT — Read Bootstrap ROM

The read bootstrap ROM bit only has meaning when the SMOD bit is a one (special bootstrap mode or special test mode). At all other times, this bit is clear and may not be written.

When set, upon reset in bootstrap mode only, the small bootstrap loader program is enabled. When clear, by reset in the other three modes, this ROM is disabled and accesses to this area are treated as external accesses.

SMOD — Special Mode

The special mode bit reflects the inverse of the MODB input pin at the rising edge of reset. It is set if the MODB pin is low during reset. If MODB is high during reset, it is cleared. This bit may be cleared under software control from the special modes, thus, changing the operating mode of the MCU, but may never be set by software.

MDA — Mode Select A

The mode select A bit reflects the status of the MODA input pin at the rising edge of reset. While the SMOD bit is set (special bootstrap or special test mode in effect) the MDA bit may be written, thus, changing the operating mode, of the MCU. When the SMOD bit is clear, the MDA bit is a read-only bit and the operating mode cannot be changed without going through a reset sequence.

Table 9-5 summarizes the relationship between the SMOD and MDA bits and the MODB and MODA input pins at the rising edge of reset.

Table 9-5 Mode Bits Relationship

Inputs		Mode Description	Latched at Reset	
MODB	MODA		SMOD	MDA
1	0	Single Chip	0	0
1	1	Expanded Multiplexed	0	1
0	0	Special Bootstrap	1	0
0	1	Special Test	1	1

1 = Logic High   0 = Logic Low

IRV — Internal Read Visibility

The internal read visibility bit is used in the special modes (SMOD = 1) to affect visibility of internal reads on the expansion data bus. IRV is writeable only if SMOD = 1 and returns to zero if SMOD = 0. If IRV is clear, visibility of internal reads is blocked. If the bit is set, internal reads are visible on the external bus.

PSEL3, PSEL2, PSEL1, and PSEL0 — Priority Select

These four priority select bits are used to specify one I bit related interrupt source which becomes the highest priority I bit related source (**Table 9-6**). These bits may be written only while the I bit in CCR = 1 (interrupts masked).

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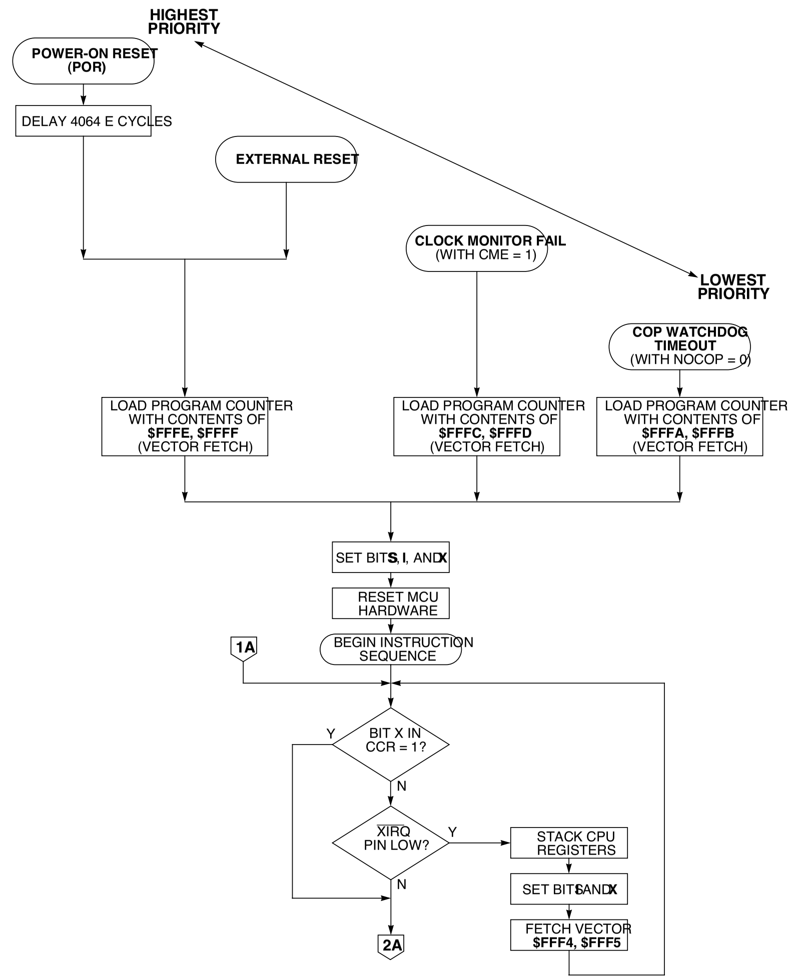

Figure 9-4 Processing Flow Out of Resets (Sheet 1 of 2)

Table 9-6 Highest Priority I Interrupt versus PSEL[3:0]

PSEL3	PSEL2	PSEL1	PSEL0	Interrupt Source Promoted
0	0	0	0	Timer Overflow
0	0	0	1	Pulse Accumulator Overflow
0	0	1	0	Pulse Accumulator Input Edge
0	0	1	1	SPI Serial Transfer Complete
0	1	0	0	SCI Serial System
0	1	0	1	Reserved (Default to $\overline{IRQ}$)
0	1	1	0	$\overline{IRQ}$ (External Pin or Parallel I/O)
0	1	1	1	Real Time Interrupt
1	0	0	0	Timer Input Capture 1
1	0	0	1	Timer Input Capture 2
1	0	1	0	Timer Input Capture 3
1	0	1	1	Timer Output Compare 1
1	1	0	0	Timer Output Compare 2
1	1	0	1	Timer Output Compare 3
1	1	1	0	Timer Output Compare 4
1	1	1	1	Timer Output Compare 5

NOTE:
During reset, PSEL3, PSEL2, PSEL1, and PSEL0 are initialized to 0:1:0:1 which corresponds to "Reserved (default to $\overline{IRQ}$)" being the highest priority I-bit-related interrupt source.

9.3 Low-Power Modes

The MCU contains two programmable low power consumption modes; WAIT and STOP. These two instructions are discussed below. **Table 9-7** summarizes the activity on all pins of the MCU for all operating conditions.

9.3.1 WAIT Instruction

The WAI instruction puts the MCU in a low power consumption mode, keeping the oscillator running. Upon execution of a WAI instruction, the machine state is stacked and program execution stops. The wait state can be exited only by an unmasked interrupt or $\overline{RESET}$. If the I bit is set (interrupts masked) and the COP is disabled, the timer system will be turned off to additionally reduce power consumption. The amount of power savings is application dependent and depends upon circuitry connected to the MCU pins as well as which subsystems (i.e., timer, SPI, SCI) are active when the WAIT mode is entered. Turning off the A/D subsystem by clearing ADPU further reduces WAIT mode current.

9.3.2 STOP Instruction

The STOP instruction places the MCU in its lowest power consumption mode provided the S bit in the condition code register is clear. If the S bit is set, the STOP mode is disabled and STOP instructions are treated as NOPs (no operation). In the STOP mode, all clocks including the internal oscillator are stopped causing all internal processing to be halted. Recovery from the STOP mode may be accomplished by $\overline{RESET}$, $\overline{XIRQ}$, or an unmasked $\overline{IRQ}$. When the $\overline{XIRQ}$ is used, the MCU exits from the STOP mode regardless of the state of the X bit in the condition code register; however,

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the actual recovery sequence differs depending on the state of the X bit. If the X bit is clear, the MCU starts up with the stacking sequence leading to normal service of the $\overline{XIRQ}$ request. If the X bit is set, then processing will continue with the instruction immediately following the STOP instruction and no $\overline{XIRQ}$ interrupt service routine is requested. A reset will always result in an exit from the STOP mode, and the start of MCU operation is determined by the reset vector.

Table 9-7 Pin State Summary for RESET, STOP, and WAIT

Pins	Single Chip Modes			Expanded Modes		
	RESET	WAIT	STOP	RESET	WAIT	STOP
Output Only						
E	Active E	Active E	0	Active E	Active E	0
XTAL!!!	Active	Active	1	Active	Active	1
STRB/RW	0	SS	SS	1	1	1
PA3-PA6	0	SS	SS	0	SS	SS
PB0-PB7	0	SS	SS	HI ADD	HI ADD	HI ADD
Input/Output						
RESET	I (0)	I	I	I (0)	I	I
MODA/LIR	I (0)	OD (1)	OD (1)	I (1)	OD (1)	OD (1)
MODB/V_{STBY}	I (MODB)	I (V_{STBY})	I (V_{STBY})	I (MODES)	I (V_{STBY})	I (V_{STBY})
STRA/AS	I (STRA)	I (STRA)	I (STRA)	Active AS	Active AS	0
PA7	I	I/O	I/O	I	I/O	I/O
PC0-PC7	I	I/O	I/O	ADD/DATA	SP-8/DATA	LO ADD
PD0-PD5	I	I/O	I/O	I	I/O	I/O
Input Only						
EXTAL	Input Clock or Connect to Crystal with XTAL					
$\overline{IRQ}$	Terminate Unused Inputs to V_{DD}					
$\overline{XIRQ}$	Terminate Unused Inputs to V_{DD}					
PA0-PA2	Terminate Unused Inputs to V_{DD} or V_{SS}					
PE0-PE7	If Not Used, External Drive Not Required					
V_{RH}-V_{RL}	If Not Used, External Drive Not Required					

SYMBOLS:
- DATA =Current data present.
- I =Input pin, if ( ) associated then this is required input state.
- I/O =Input/output pin, state determined by data direction register.
- HI ADD =High byte of the address.
- LO ADD =Low byte of the address.
- ADD/DATA =Low byte of the address multiplexed with data.
- OD =Open drain output, ( ) current output state.
- SS =Steady state, output pin stays in current state.
- SP-8 =Address output during WAI period following WAI instruction, stack pointer value, at time of WAI, minus 8.
- !!! =XTAL is output but not normally usable for any output function beyond crystal drive.

Since the oscillator is stopped in the STOP mode, a restart delay of 4064 clock cycle times may be required to allow oscillator stabilization. If the internal oscillator is being used, this delay is required; however, if a stable external oscillator is being used, a control bit in the OPTION register may be used (DLY = 0) to give a delay of four cycles.

APPENDIX C: ELECTRIC DIAGRAM

In this appendix are available some electric diagrams of the most frequently used **GPC® 11** interfaces. All these interface can be yourself produced and some of them are standard **grifo®** cards and, if required, they can be directly ordered.

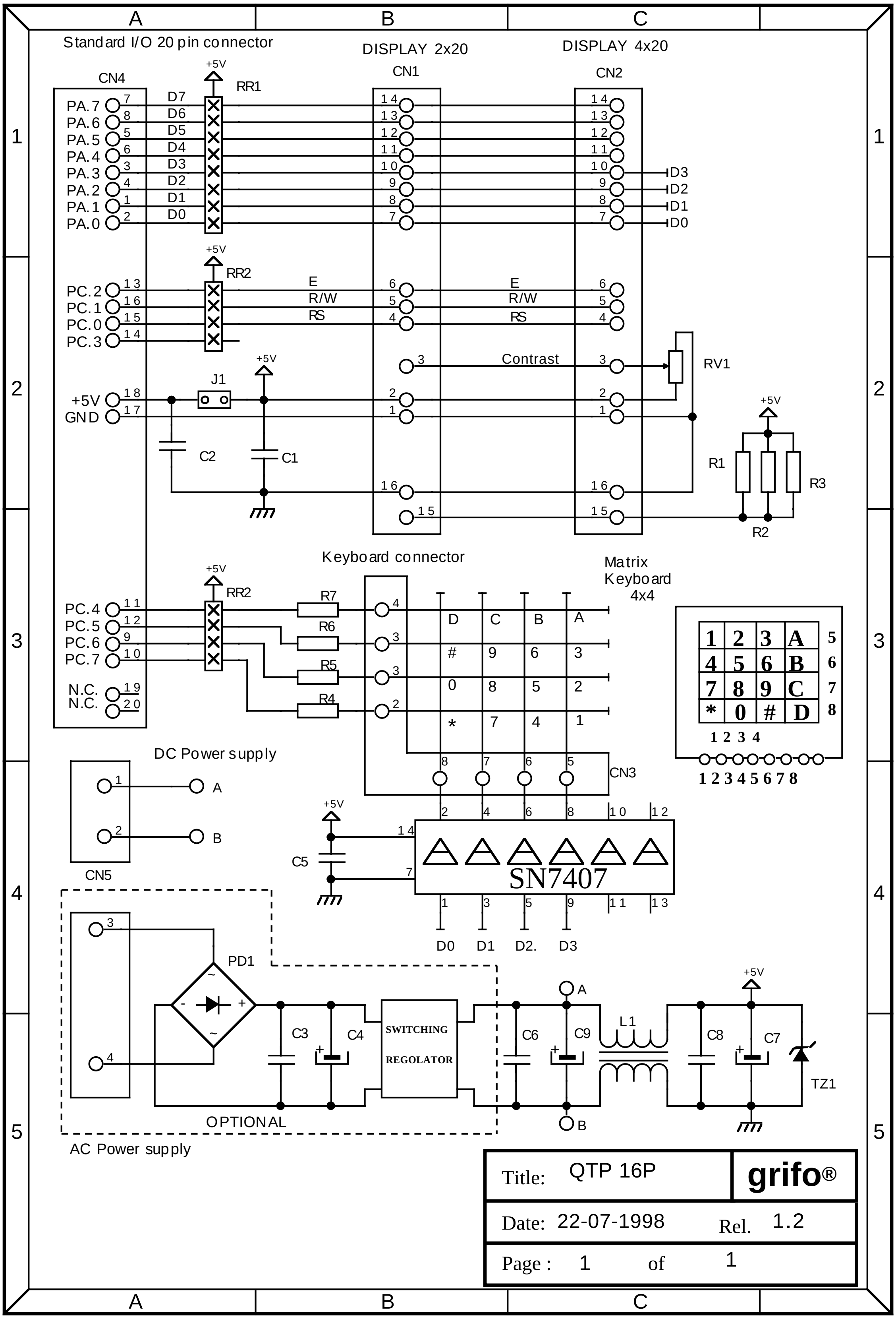

FIGURE C1: QTP 16P ELECTRIC DIAGRAM

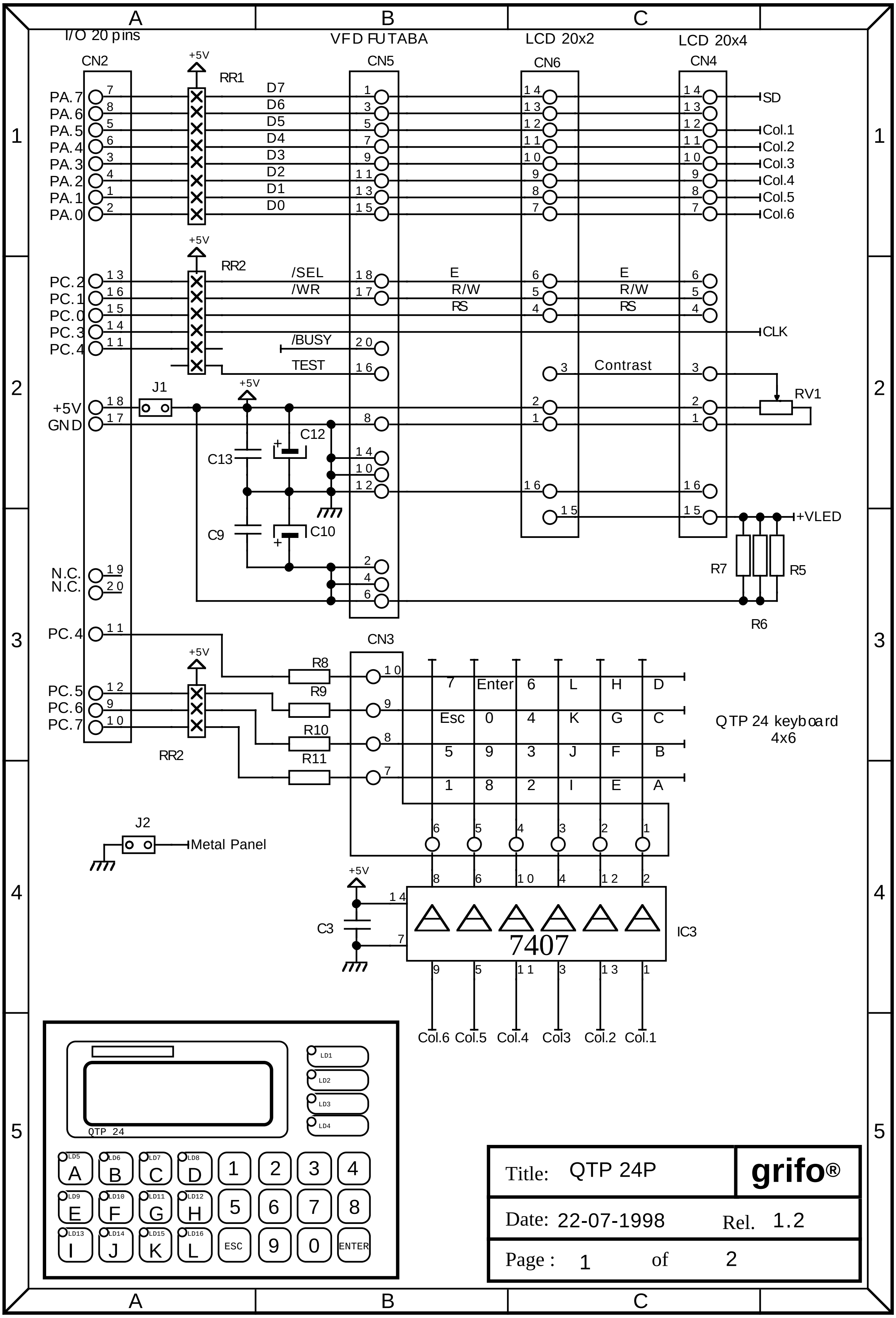

FIGURE C2: QTP 24P ELECTRIC DIAGRAM (1 OF 2)

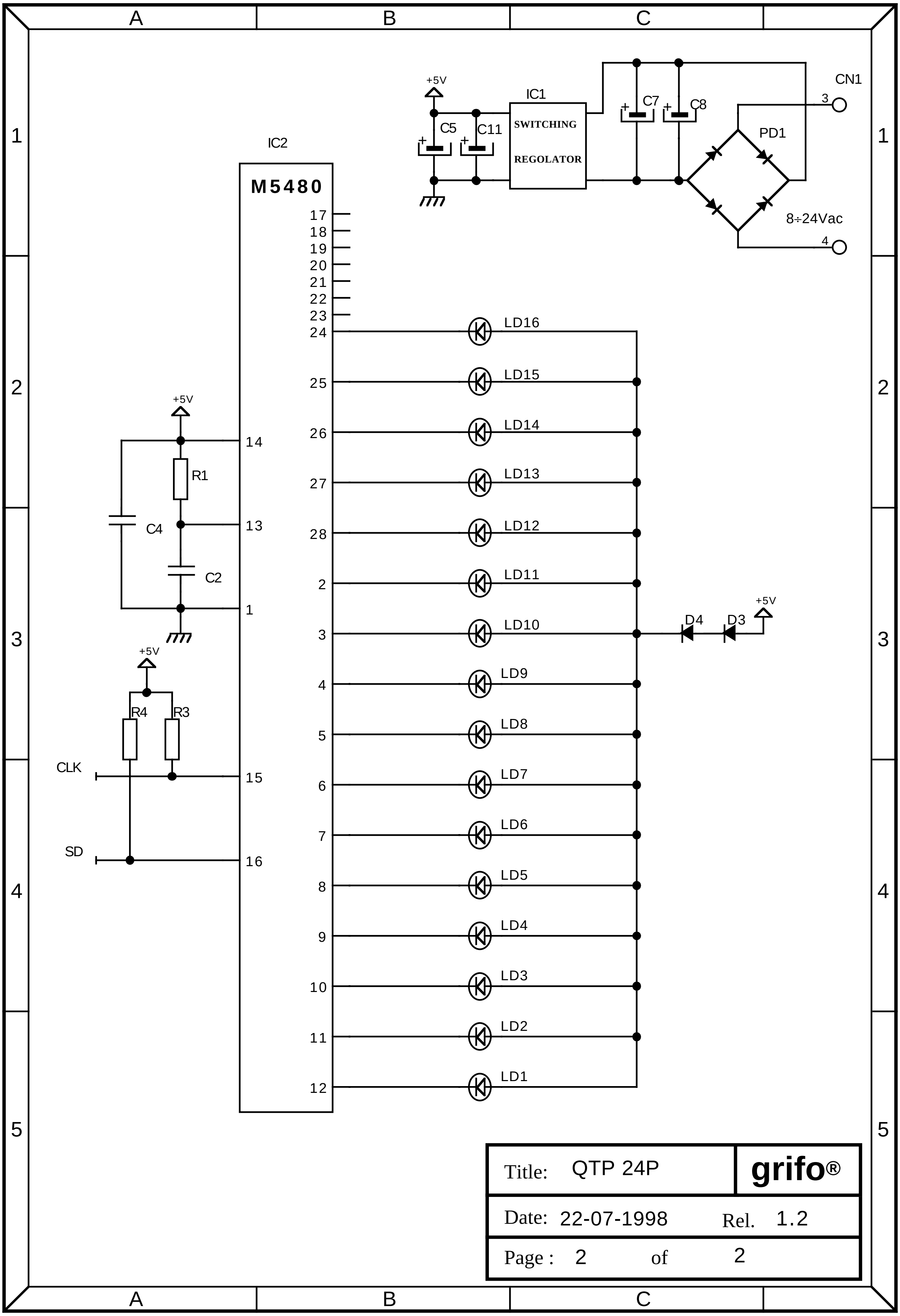

FIGURE C3: QTP 24P ELECTRIC DIAGRAM (2 OF 2)

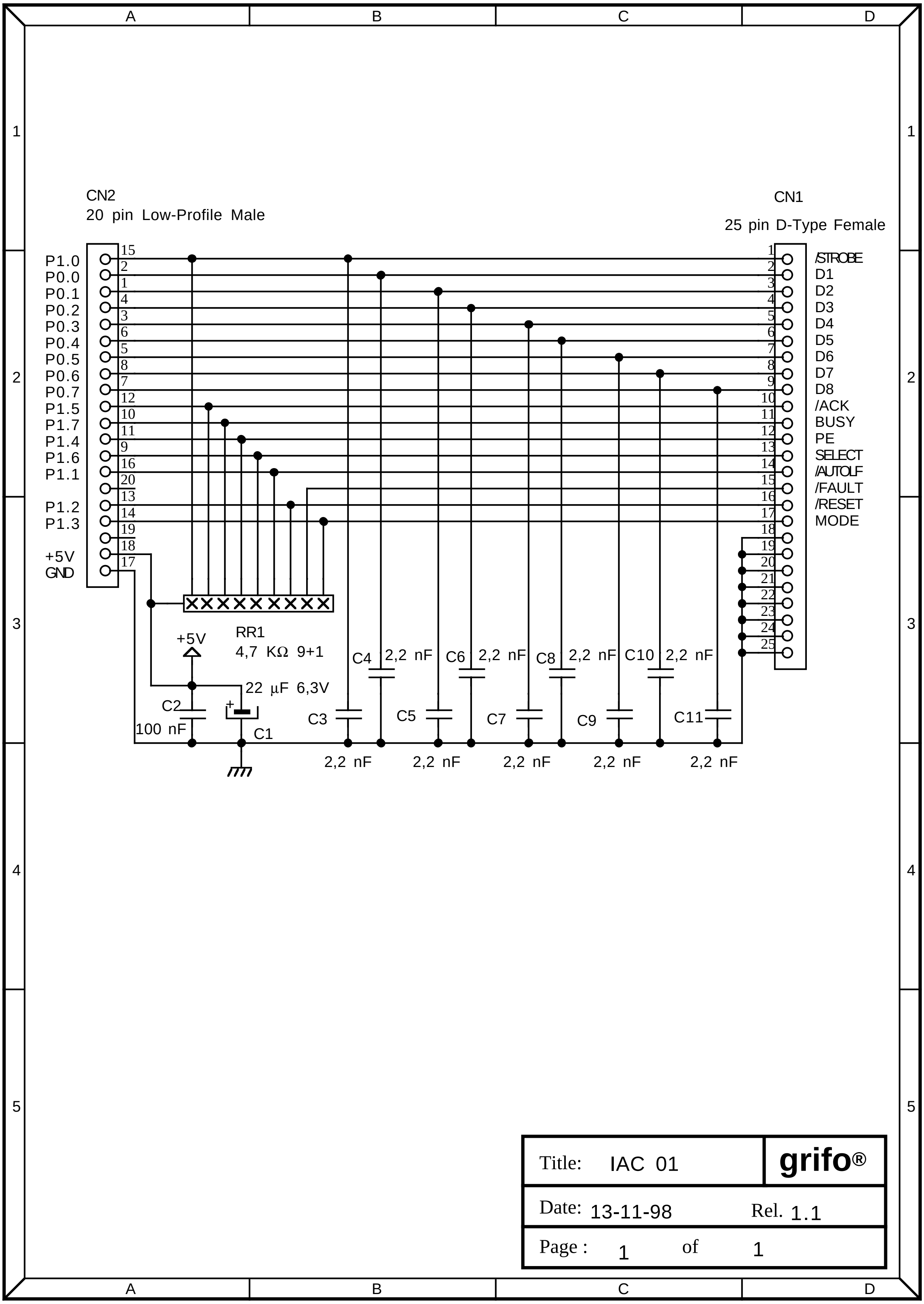

FIGURE C4: IAC 01 ELECTRIC DIAGRAM

APPENDIX D: ALPHABETICAL INDEX