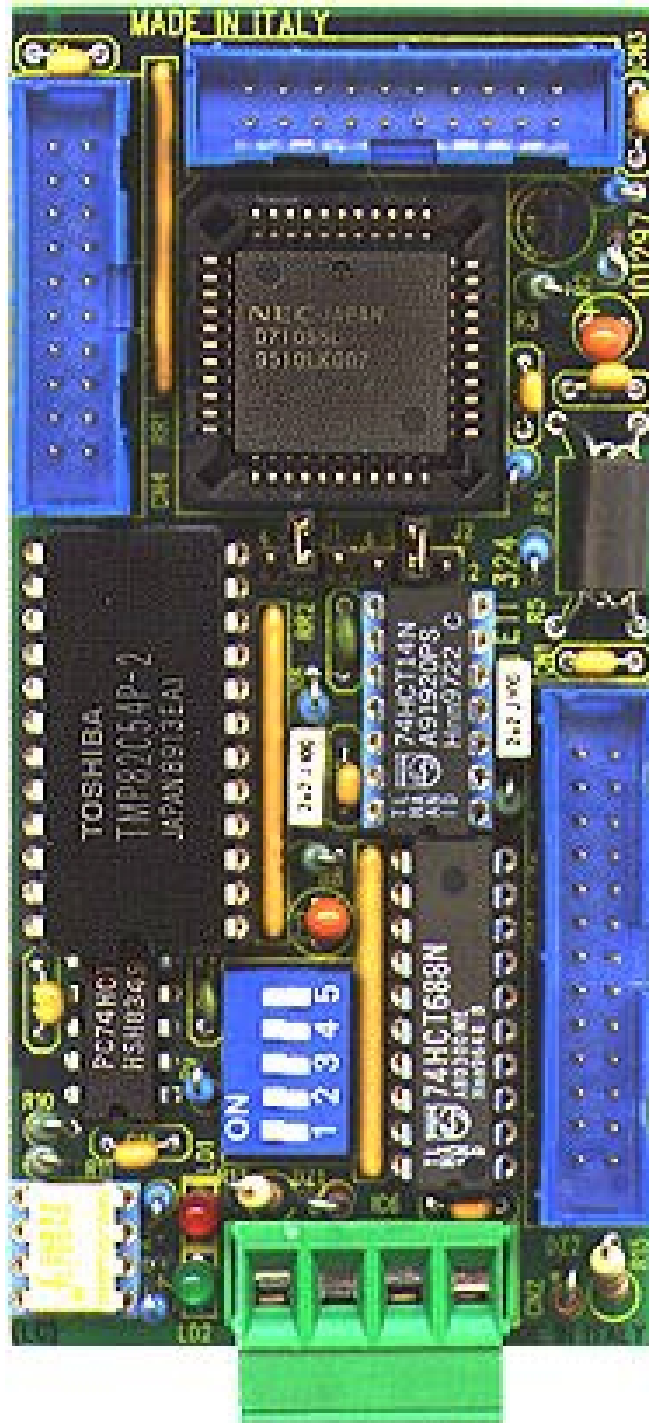


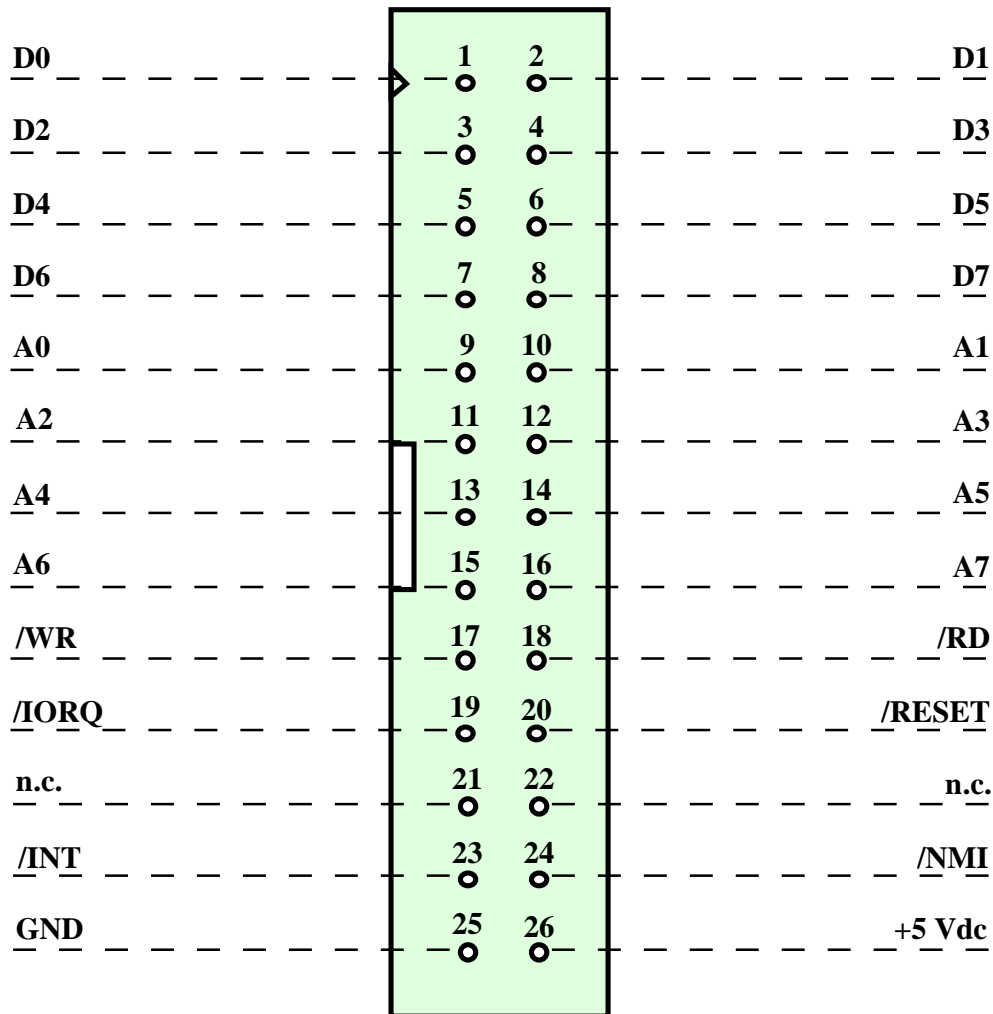
PRELIMINARY ETI 324



CN1 - ABACO® I/O BUS CONNECTOR

CN1 is a 26 pins, male, vertical, low profile connector with 2.54 mm pitch.

Through CN1 ETI 324 can be connected via **ABACO®** I/O BUS to external the **GPC®** card which controls the application. All this connector signals are at TTL level.



CN1 - ABACO® I/O BUS CONNECTOR

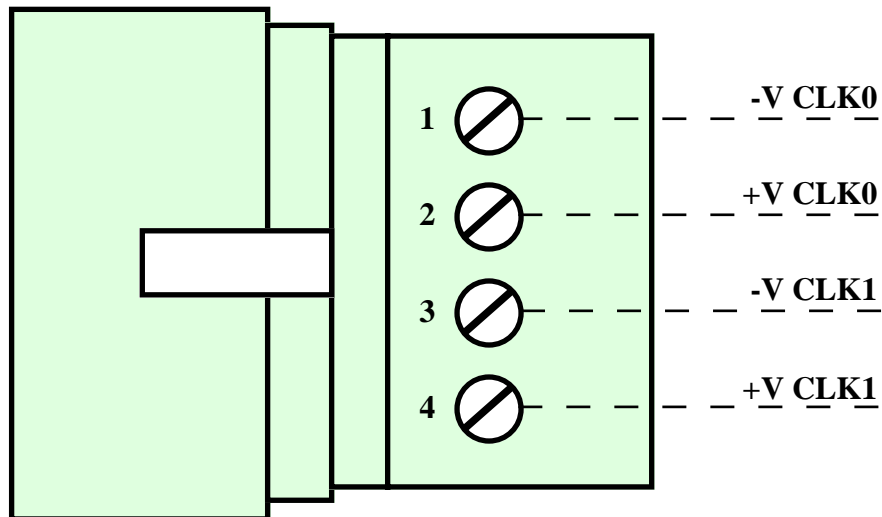
Signals description:

A0÷A7	= I - Address BUS.
D0÷D7	= I/O - Data BUS.
/INT BUS	= O - Interrupt request (open collector type).
/NMIBUS	= O - Non mascable interrupt.
/IORQ	= I - Input output request.
/RD	= I - Read cycle status.
/WR	= I - Write cycle status.
/RESET	= I - Reset.
+5 Vdc	= I - +5 Vdc power supply.
GND	= - Ground signal.
N.C.	= - Not connected.

CN2 - TIMER/COUNTER OPTOCOUPLED INPUTS CONNECTOR

CN2 is a 4 pins quick release screw terminal connector. CN2 allows to connect the two optocoupled inputs connected to on board COUNTER count signals.

The connector features optocoupled inputs each of which accepts a signal of 12 Vdc.



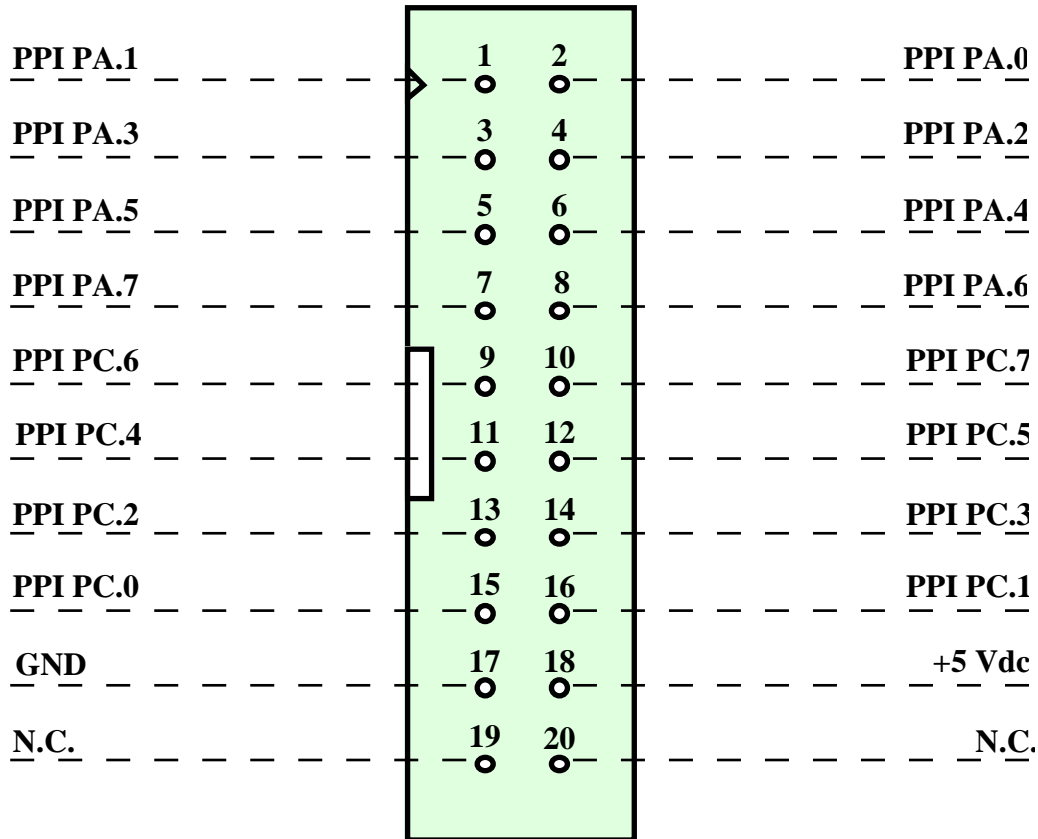
CN2 - TIMER/COUNTER OPTOCOUPLED INPUTS

Signals description:

$\underline{+V\ CLH\ n}$ = I - n-th channell CLK positive input
 $\underline{-V\ CLH\ n}$ = - - n-th channell CLK negative input

CN3 - PPI 82C55 PORT A AND C I/O CONNECTOR

CN3 is a 20 pins, male, vertical, low profile connector, 2.54 mm pitch. Through CN3 two parallel 8 bits ports out of three (ports A and C) of programmable peripheral PPI 82C55 are connected to external world. All this connector's signals are at TTL level.


CN3 - PPI 82C55 PORT A AND C I/O CONNECTOR

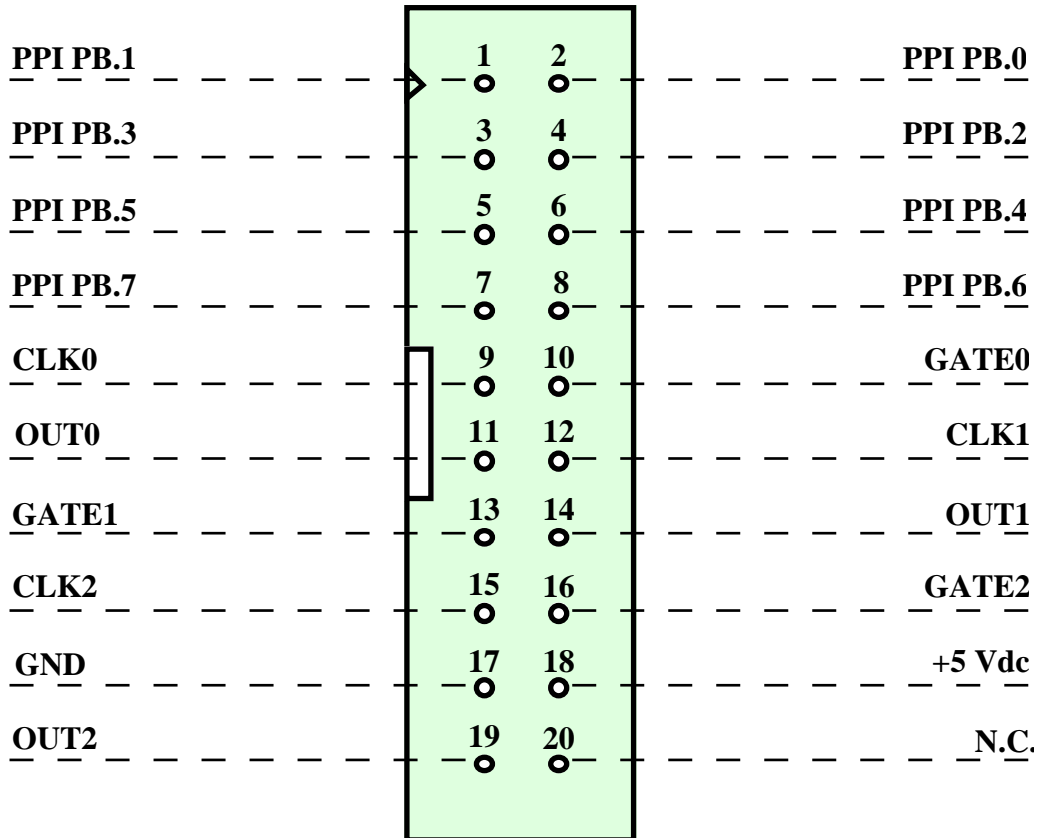
Signals description:

PPI PA.n	=	I/O	-	PPI 82C55 port A n-th digital signal
PPI PC.n	=	I/O	-	PPI 82C55 port C n-th digital signal
GND	=	-	-	Ground signal
+5 Vdc	=	O	-	+5 Vdc signal
N.C.	=	-	-	Not connected

CN4 - PPI 82C55 PORT B I/O CONNECTOR AND COUNTER SIGNAL

CN4 is a 20 pins, male, vertical, low profile connector, 2.54 mm pitch. Through CN4 one of the three programmable peripheral PPI 82C55 8 bits parallel ports (port B) is connected to external world. All this connector's signals are at TTL level.

CN4 performs also the connection for the three programmable counters provided by 8254.



CN4- PPI 82C55 PORT B I/O AND COUNTERS

Signals description:

- PPI PB.n** = I/O - PPI 82C55 port B n-th digital signal
- GND** = - Ground signal
- OUTn** = - n-th Counter Output digital signal
- GATEn** = - n-th Counter Gate Input digital signal
- +5 Vdc** = O - +5 Vdc signal
- N.C.** = - Not connected

JUMPERS

The board is provided with two jumpers, called J1 and J2, here is the description of their function:

J1	pos.1-2	Connects input CLK 0 to galvanically isolated section on CN2
	pos.1-3	Connects input CLK 0 to encoder direction discriminator on CN2
	pos.1-4	Connects input CLK 0 to connector CN4
J2	pos.1-2	Connects input CLK 1 to connector CN4
	pos.1-3	Connects input CLK 1 to encoder direction discriminator on CN2
	pos.1-4	Connects input CLK 1 to galvanically isolated section on CN2

VISUAL SIGNALATIONS

The board is provided with two visualization LEDs, called LD1 and LD2, the first (red) indicates the status of counter 0 input, while the other (green) indicates the status of counter 1 input.

BOARD MAPPING

ETI 324 is mapped into a 8 bytes I/O addressing space, that can be allocated starting from different base addresses according to how the board is configured. This feature allows to use several **ETI 324** cards on the same **ABACO®** I/O BUS or **ABACO®** BUS, or to install them on a BUS where other peripheral modules are installed obtaining a structure that can be expanded without any difficulty or modifications to the application software. These bytes allow the complete control of board settings and status and the complete flow of input and output data.

The base address can be defined through the specific BUS interface circuitry on the board itself; this circuitry uses the eight pins dip switch called **DSW1**, from which it reads the address set by the user. Here follows the correspondance between configuration dyps and address signals.

DSW1.1	->	address A3
DSW1.2	->	address A4
DSW1.3	->	address A5
DSW1.4	->	address A6
DSW1.5	->	address A7

These dyps are driven in complemented logic, this means that if a switch is **ON** generates a **logic zero**, viceversa if a switch is **OFF** generates a **logic one**.

As an example, dip configuration to set address 080H is repored here:

DSW1.1 -> ON
 DSW1.2 -> ON
 DSW1.3 -> ON
 DSW1.4 -> ON
 DSW1.5 -> OFF

The on board control logic manages the allocation of the 8 registers that completely manage on board peripherals.

Indication <baseadd> means the base address of the board decided with DSW1, as previously described.

REGISTER	ADDRESS	R/W	MEANING
PDA	<baseadd>+00	R/W	PPI 8255 PORT A data register.
PDB	<baseadd>+01	R/W	PPI 8255 PORT B data register.
PDC	<baseadd>+02	R/W	PPI 8255 PORT C data register.
CNT	<baseadd>+03	R/W	PPI 8255 control and command register.
COUNTER0	<baseadd>+04	R/W	PIT 8254 counter 0 register.
COUNTER1	<baseadd>+05	R/W	PIT 8254 counter 1 register.
COUNTER2	<baseadd>+06	R/W	PIT 8254 counter 2 register.
CONTROLLO	<baseadd>+07	R/W	PIT 8254 control and command register.

PERIPHERAL DEVICES SOFTWARE DESCRIPTION

In the previous paragraphs are described the external registers addresses, while in this one there is a specific description of registers meaning and function (please refer to I/O addressing tables, for the registers name and addresses values). For microprocessor internal peripheral devices, not described in this paragraph, or for further information, please refer to manufacturing company documentation.

PPI 82C55

Questa periferica è vista in 4 registri: uno di stato (CNT) e tre dei dati (PDA, PDB, PDC) con cui si
 eThis external peripheral device is managed through 4 registers: one status register (CNT) and three data registers (PDA, PDB, PDC). The data registers are available both for read operation (to obtain signal status) and for write operation (to set signal status) with the correspondence described in figure 23. The PPI 82C55 can work in three different modes:

MODE 0 = it provides two 8 bits bidirectional ports (A,B) and two 4 bits bidirectional ports (C LOW, C HIGH); output signals are latched and input signals are not latched; no handshake signals are provided.

MODE 1 = it provides two 12 bits ports (A+C LOW and B+C HIGH) where ports A and B are used as 8 I/O lines and port C are used as 4 handshake lines. Both inputs and outputs are latched.

MODE 2 = it provides a 13 bits port (A+C3÷7) where port A is used as 8 I/O lines and the 5 bits of port C are used as handshake, and a 11 bits port (B+C0÷2) where port B is used as 8 I/O lines and the 3 bits of port C are used as handshakes. Both inputs and outputs are latched.

The device is programmed writing an 8 bits word in the status register CNT, with the following bit meaning:

CNT = SF M1 M2 A CH M3 B CL

where

SF = mode Set Flag: if activated (1) the device is enabled for standard I/O operation

M1 M2 = mode selection:

0 0 = mode 0

0 1 = mode 1

1 X = mode 2

A = port A direction: 1=input; 0=output

CH = port C HIGH direction: 1=input; 0=output

M3 = mode selection: 1=mode 1; 0=mode 0

B = port B direction: 1=input; 0=output

CL = port C LOW direction: 1=input; 0=output

After Reset or power on PPI 82C55 is programmed in mode 0 with all three ports in input; in this way any connection of PPI 82C55 signals can be used without conflict problems.

TIMER/COUNTER 8254

This peripheral is mapped in 4 registers (one status register and three data registers) that allow to program and control it completely. Data register are used both for write operations (loading of count combination in the counters) and for read operations (combination reached during count). Each data register reports the combination of its matched counter
The peripheral can work in 5 different modes:

MODE 0 = output is normally low; after writing data n in counter data register, the output will remain low for n CLK periods then goes high. GATE input can keep output low for a longer time after writing to counter register.

MODE 1 = output is normally high; after writing data n in counter data register, the output will go low after the first pulse on GATE and remains low for n CLK periods then goes high. Successive GATE pulses reset the count of CLK periods.

MODE = 2 output is normally high; after writing data n in counter data register output goes periodically low for a CLK period. The time between two low outputs is n CLK periods. GATE input can keep output low for a longer time.

MODE 3 = output is normally high; after writing data n in counter data register output goes low for $n/2$ CLK periods then returns high for the remaining $n/2$ CLK periods, continuing forever. If n is odd the output remains high for one CLK period longer than it remains low. GATE input can keep longer both status.

MODE 4 = output is normally high; after writing data n in counter data register output keeps high for n CLK periods, then it goes low for one CLK period. GATE input can keep output high for a longer time after writing to counter register.

MODE 5 = output is normally high; after writing data n in counter data register output remains high when first GATE pulse is received for n CLK periods, then it goes low for one CLK period. Successive GATE pulses reset the count of CLK periods.

Programming the peripherals is performed writing an 8 bit byte in control and status register, where:

CONTROL = S1 S0 R1 R0 M2 M1 M0 BCD

S1 S0

0 0	Select internal counter 0
0 1	Select internal counter 1
1 0	Select internal counter 2

R1 R0

0 0	R/W operation on latched counters
0 1	R/W operation on M.S.Byte only
1 0	R/W operation on L.S.Byte only
1 1	R/W operation on L.S.Byte first, M.S.Byte next

These commands are essential because counter word length is 16 bit, while data register length is 8 bit.

M2 M1 M0

0 0 0	Select Mode 0
0 0 1	Select Mode 1
X 1 0	Select Mode 2
X 1 1	Select Mode 3
1 0 0	Select Mode 4
1 0 1	Select Mode 5

BCD

If active (1) counters are are 4 figures BCD counters, viceversa are pure binary counters.