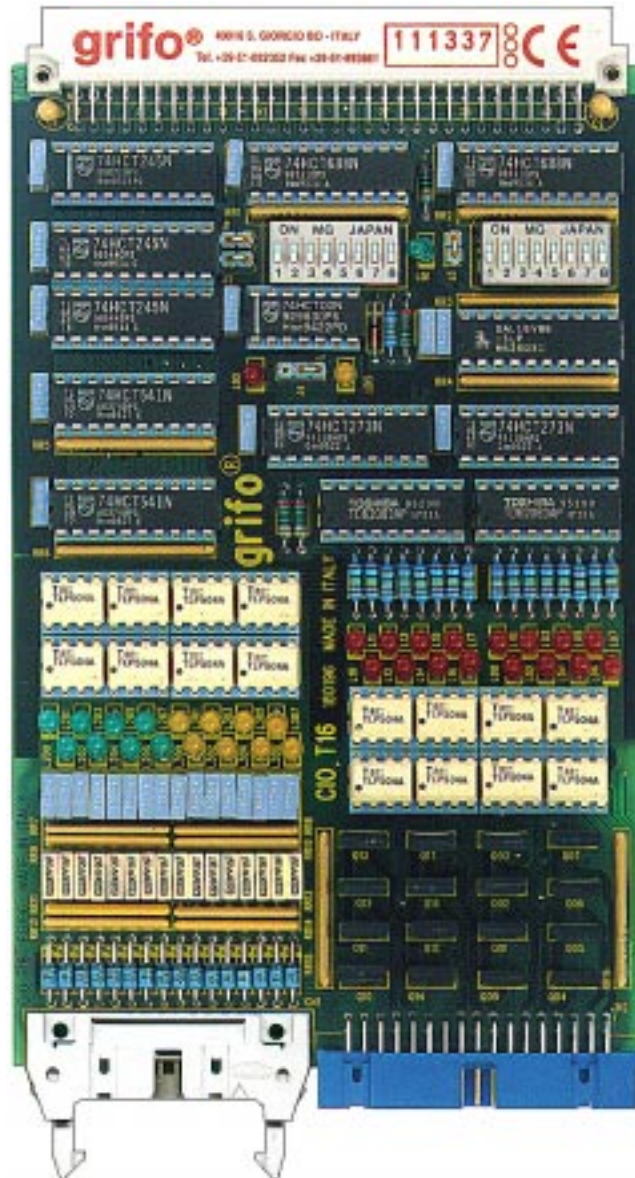


CI/O T16

Coupled Input Output NPN Transistors

TECHNICAL MANUAL



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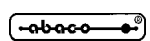
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CI/O T16

Edition 5.00

Rel. 01 September 2000

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CI/O T16

Coupled Input Output NPN Transistors

TECHNICAL MANUAL

Single Europe format size 100x160 mm; **ABACO**[®] BUS industrial interface; 16 digital output signals with 4A 45Vdc Darlington NPN open collector, without heat sink; 16 LEDs to visualize the transistors' status; anti-activation during the power on circuitry; 16 digital optocoupled NPN input signals with π filter on each input; 16 LEDs to visualize the logic status of each optocoupled input; I/O mapping selection through on board Dip Switch; addressing space needed as low as 2 bytes contiguous; BUS data and addresses path can be 8 or 16 bits; BUS configuration visualized through 3 LEDs; possibility to connect or disconnect BUS /RESET signal; 20 pins standard input connector and 34 pins standard output connector; direct connection to interfaces for the external world **FBC 34**, **FBC L34**, etc.; unique power supply for the on board logic +5Vdc; power supply for optocoupled input 12÷24 Vdc.

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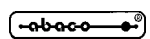
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For specific informations on the components mounted on the card, please refer to the Data Book of the builder or second sources.

SYMBOLS DESCRIPTION

In the manual could appear the following symbols:

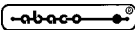


Attention: Generic danger



Attention: High voltage

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INTRODUCTION

The use of these devices has turned - IN EXCLUSIVE WAY - to specialized personnel.

The purpose of this handbook is to give the necessary information to the cognizant and sure use of the products. They are the result of a continual and systematic elaboration of data and technical tests saved and validated from the manufacturer, related to the inside modes of certainty and quality of the information.

The reported data are destined- IN EXCLUSIVE WAY- to specialized users, that can interact with the devices in safety conditions for the persons, for the machine and for the environment, impersonating an elementary diagnostic of breakdowns and of malfunction conditions by performing simple functional verify operations , in the height respect of the actual safety and health norms.

The informations for the installation, the assemblage, the dismantlement, the handling, the adjustment, the reparation and the contingent accessories, devices etc. installation are destined - and then executable - always and in exclusive way from specialized warned and educated personnel, or directly from the TECHNICAL AUTHORIZED ASSISTANCE, in the height respect of the manufacturer recommendations and the actual safety and health norms.

The devices can't be used outside a box. The user must always insert the cards in a container that respect the actual safety normative. The protection of this container is not threshold to the only atmospheric agents, but specially to mechanic, electric, magnetic, etc. ones.

To be on good terms with the products, is necessary guarantee legibility and conservation of the manual, also for future references. In case of deterioration or more easily for technical updates, consult the AUTHORIZED TECHNICAL ASSISTANCE directly.

To prevent problems during card utilization, it is a good practice to read carefully all the informations of this manual. After this reading, the user can use the general index and the alphabetical index, respectly at the begining and at the end of the manual, to find information in a faster and more easy way.

CARD VERSION

The present manual is reported to the **CI/O T16** version **290398** .

The validity of the bring informations is subordinate to the number of the card release. The user must always verify the correct correspondence among the two denotations. Version number is printed on the boards in several positions both in serigraph and in printed circuit (for example centered amongst the optocouplers on the component side).

GENERAL INFORMATION

La **CI/O T16** (Coupled Input Output **16 Transistors** and **16 NPN** inputs) is a powerful digital I/O module that provides on one only board the features normally available on two boards. This extreme compactness, distinctive feature of **grifo**[®] boards, allows to optimize room and cost of the final application. The board uses only as low as two bytes of addressing space, distinguishing the two locations for read or write operations. No software initialization is needed to use the board. When a Power on or Reset occur **CI/O T16** disables the 16 outputs through a specific circuitry (if it has not been excluded by moving a jumper) warranting so the absence of any kind of inconsistency of the initial status.

Only after a write operation to one of its two registers the protection circuitry allows the activation of the relays and awarns that the board is working properly by lighting the **LED** corresponding to the register.

All the output transistors are provided with a LED to indicate if the transistor is activated or not.

The sixteen input signals, galvanically isolated and NPN type, are provided with a π filter and a LED to indicate the status of each single input.

The connection with the external world is performed through two comfortable standard I/O connectors located on the front of the board. One of the connectors is dedicated to inputs, the other one is dedicated to outputs. This separation increases the safety in the working of the board.

To simplify the connection of the several signals to the external world, the BLOCK modules of FBC series are available. These modules have been designed to unravel the signals coming from the two flat cables to comfortable quick release screw terminal connectors. The best choices are **FBC 34**, **FBC 20**, **FBC 120**, **FBC L34** e **FBC L20**. The latter two **FBC**, **L34** and **L20**, allow to visualize the signals status through LEDs, making easier the task to control the correct cables connections even when the board is already in a Rack.

A remarkable feature of **CI/O T16** is the possibility to have a BUS data path of 8 or 16 bits and a BUS addresses path of 8 or 16 bits. Selection of operational mode (Byte or Word) and addressing range is performed through comfortable jumpers and visualized through LEDs.

- Single Europe format size 100x160 mm
- **ABACO**[®] BUS industrial interface
- **16** optocoupled digital output signals with 4A 45Vdc **Darlington NPN** open collector transistor, without heat sink
- **16** LEDs to visualize the transistors' status
- Anti-activation during the power on circuitry
- **16** digital **optocoupled NPN** input signals with π filter on each input
- **16** LEDs to visualize the logic status of each optocoupled input
- I/O mapping selection through on board **Dip Switch**
- Addressing space needed as low as 2 bytes contiguous
- BUS data and addresses path can be **8** or **16** bits
- BUS configuration visualized through **3 LEDs**
- Possibility to connect or disconnect BUS /RESET signal
- **20 pins** standard input connector and **34 pins** standard output connector
- Direct connection to interfaces for the external world **FBC 34**, **FBC L34**, etc.
- Unique power supply for the on board logic **+5Vdc**
- Power supply for optocoupled input **12÷24 Vdc**

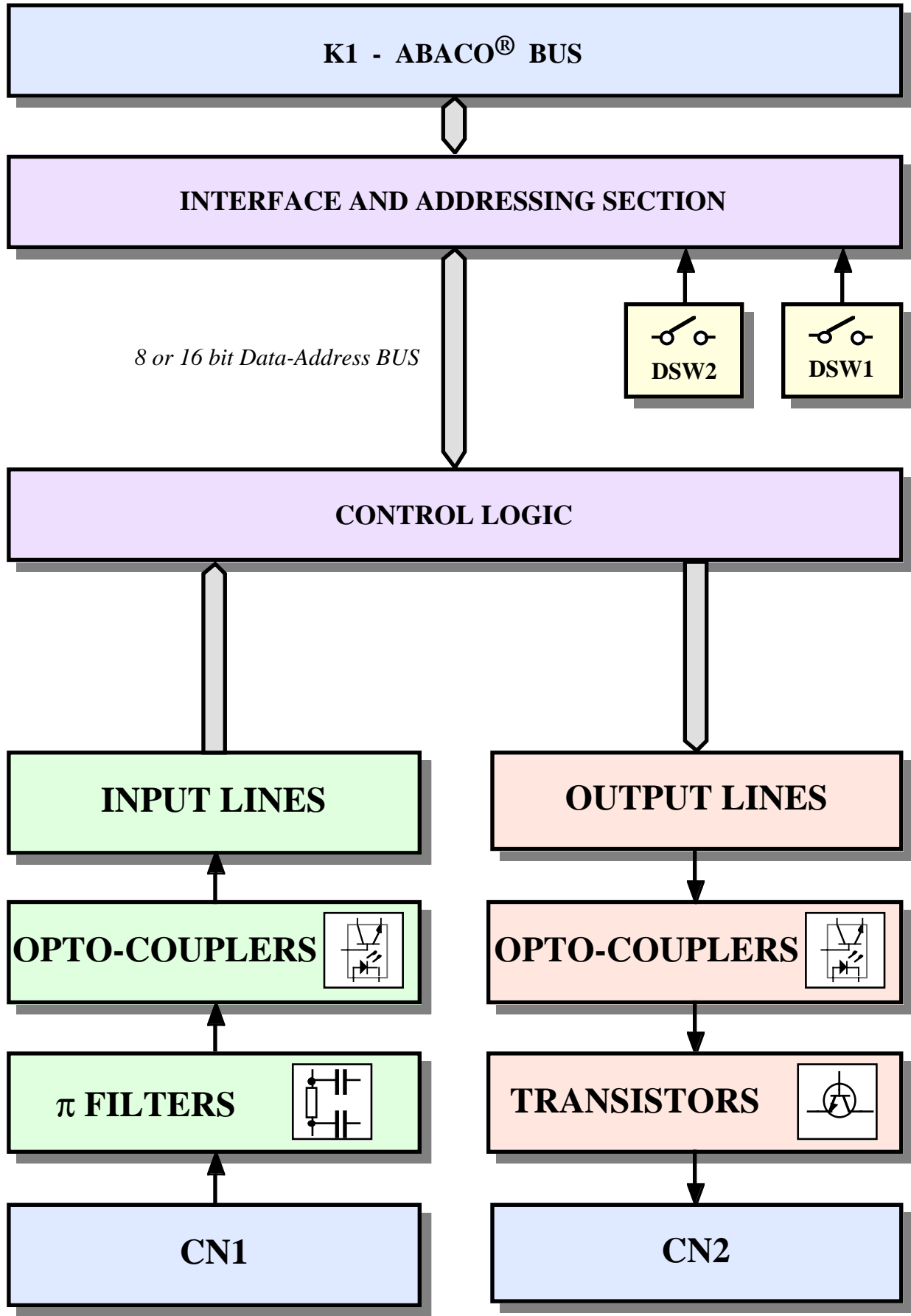


FIGURE 1: BLOCK DIAGRAM

Here follows a description of **CI/O T16** board's functional blocks, with an indication of the operations performed by each one. To easily locate these blocks and verify their connections please refer to figure 1.

INTERFACING AND ADDRESSING SECTION

This section manages the data exchange between control logic and command board through **ABACO® BUS**. In particular, all written or read data transit across this section that, in addition, provides the board I/O management, by setting the dip switched **DSW1** and **DSW2**. Please remark that this section can be configured to make **CI/O T16** addressable in a physical space of 256 or 64 Kbytes.

ABACO® industrial BUS supports both 8 bits and 16 bits addressing mode.

For further informations please refer to the chapter dedicated to board's software description.

CONTROL LOGIC

This section generates all the chip select signals needed to access the several peripherals on **CI/O T16** boards. Using this section the programmer can interact to the board's several sections, verifying their status, reading digital input configurations, setting output signals, etc.

All this can be done through a simple software management based on **ABACO® BUS**, to which the control logic connects through the interfacing and addressing section. For further informations please refer to the chapter dedicated to board's software description.

OUTPUT SECTION

This section features 16 Output signals driven by one or more latches. These components are managed through specific read/write registers, according to the informations contained in the chapters dedicated to board's hardware and software description. Any Output signal, optocoupled and visualized through its own LED, controls a 4A (not continuative), 45 Vdc open collector Darlington NPN transistor. The power supply is +5 Vdc, which supplies the on board logic circuits. This solution allows to have a unique stabilized voltage to supply the whole system.

INPUT SECTION

This section features 16 Input signals, acquired through input buffers. These components are managed by specific read/write registers, according to the informations contained in the chapters dedicated to board's hardware and software description. Any Input signal is galvanically isolated, NPN type and visualized through its own LED. Optocouplers of this section are supplied through +24 Vdc voltage that must be provided by means of a specific connector. All the input signals are protected by a π filter, that warrants a high immunity against the disturbs from the external world.

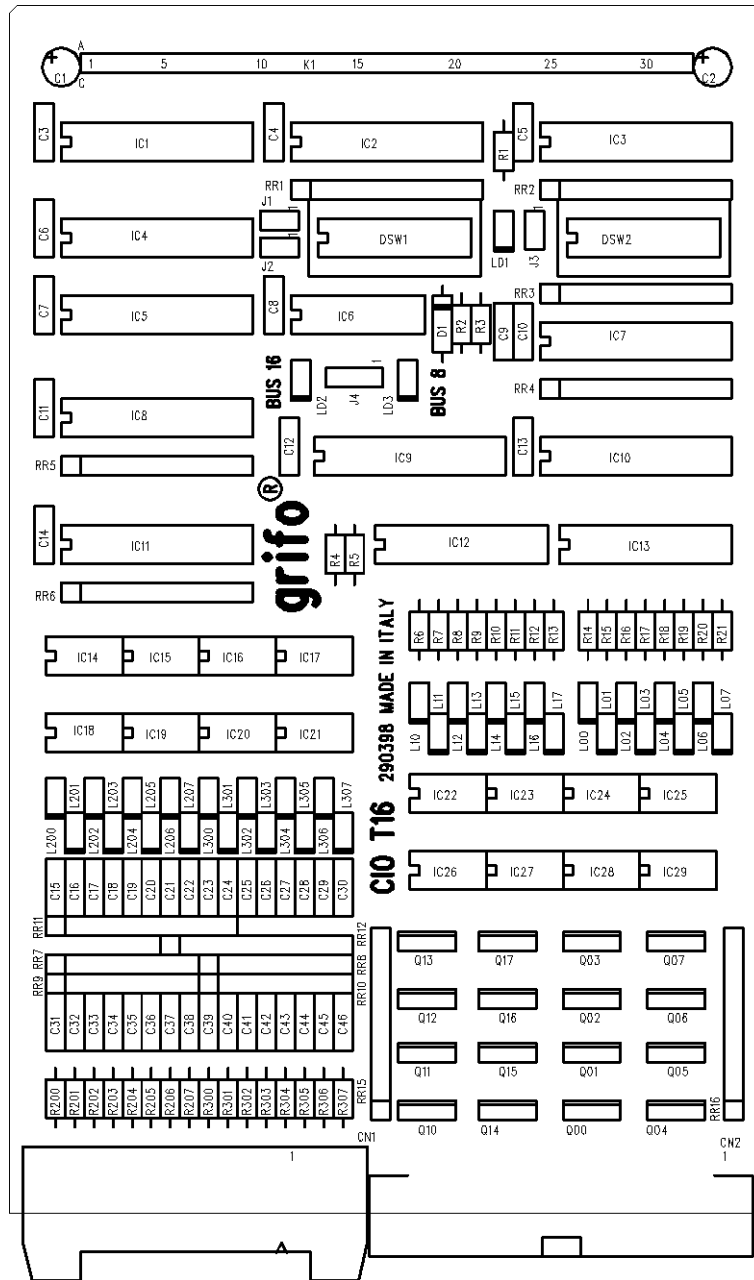


FIGURE 2: COMPONENTS MAP

TECHNICAL FEATURES

GENERAL FEATURES

On board resources:	16 Input optocoupled NPN 16 Output open collector Darlington NPN transistor 2 Dip switches with 8 pins to set the I/O addressing
BUS type:	ABACO [®] Industrial 8 or 16 bits data and addresses
N. addressable bytes:	256 bytes or 64 Kbytes
N. bytes occupied:	2 / 1

ELECTRIC FEATURES

Power supply:	+5 Vdc (logic circuits and relays) + 12÷24 Vdc (Vopto: optocoupled inputs)
Current consumption:	420 mA (+5 Vdc) 192 mA (Vopto = +24 Vdc)
Max current on transistor:	4 A non continuative (*) 600 mA continuative, supplying a resistive load at +24 Vdc (*)
Max voltage on transistors:	45 Vdc (*)
Max power each transistor:	1.25 W (*)
Filter on NPN inputs:	π filter
Minimum current on NPN inputs:	1.6 mA

(*) Values referred to a working temperature of 20 °C

PHYSICAL FEATURES

Size:	Standard EUROPE format 100x160 mm
Weight:	170 g
Connectors:	K1: DIN 41612 64 pins M 90° A+C type C CN1: Low profile 20 pins M 90° strain relief clamp CN2: Low profile 34 pins M 90°
Temperature range:	from 0 to 70 centigrad degrees
Relative humidity:	20% up to 90% (without condense)

INSTALLATION

In this chapter there are the information for a right installation and correct use of **CI/O T16** card. The User can find the location and functions of each connectors, jumpers and some explanatory diagrams.

CONNECTIONS

The **CI/O T16** card has 3 connectors that can be linkeded to other devices or directly to the field, according to system requirements. In this paragraph there are connectors pin outs, a short signals description (including the signals direction) and connectors location (please see figure 9), plus some figures that describe how the interface signals are connected on the card.

CN1 - CONNECTOR FOR OPTOCOUPLED INPUTS

The connector for optocoupled NPN inputs, called CN1, is a low profile, 2.54 mm pitch, 90 degrees, 20 pins connector.

The connector features the 16 inputs of **CI/O T16** and the lines to supply the optocouplers.

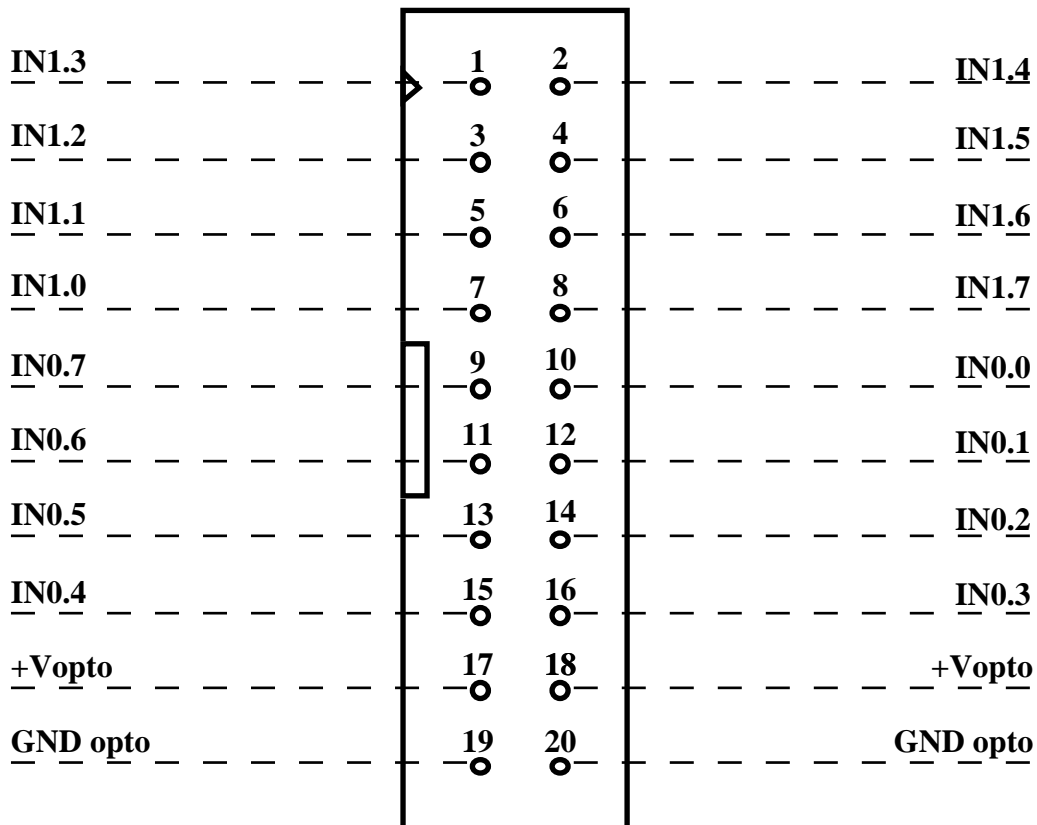


FIGURE 3: CN1 - CONNECTOR FOR OPTOCOUPLED INPUTS

Signals description:

- IN0.n** = I - n-th optocoupled NPN input n of section IN0.
- IN1.n** = I - n-th optocoupled NPN input n of section IN1.
- +Vopto** = I - Optocouplers power supply for sections IN0 and IN1.
- GND opto** = - Common terminal of optocouplers power supply for sections IN0 and IN1.

The NPN input signals available on **CI/O T16** are optocoupled and provided with π filter to warrant a high degree of protection against noise and disturbs from the external world. Each signal is provided with a LED for visual feed back (the LED will light whenever the input will have the potential of GND opto signal); this means that the inputs are going to support normally open contacts. These contacts are suitable to be connected to NPN drivers. In case the User would want to connect PNP drivers then he/she will have to put a **PBI 01** BLOCK module between the drivers and the card.

The interface circuitry for the 16 lines of the input section is shown in the following diagram.

The supply voltage of the optocouplers must be in the range **+12÷24 Vdc** and must be provided through the specific pins of CN1.

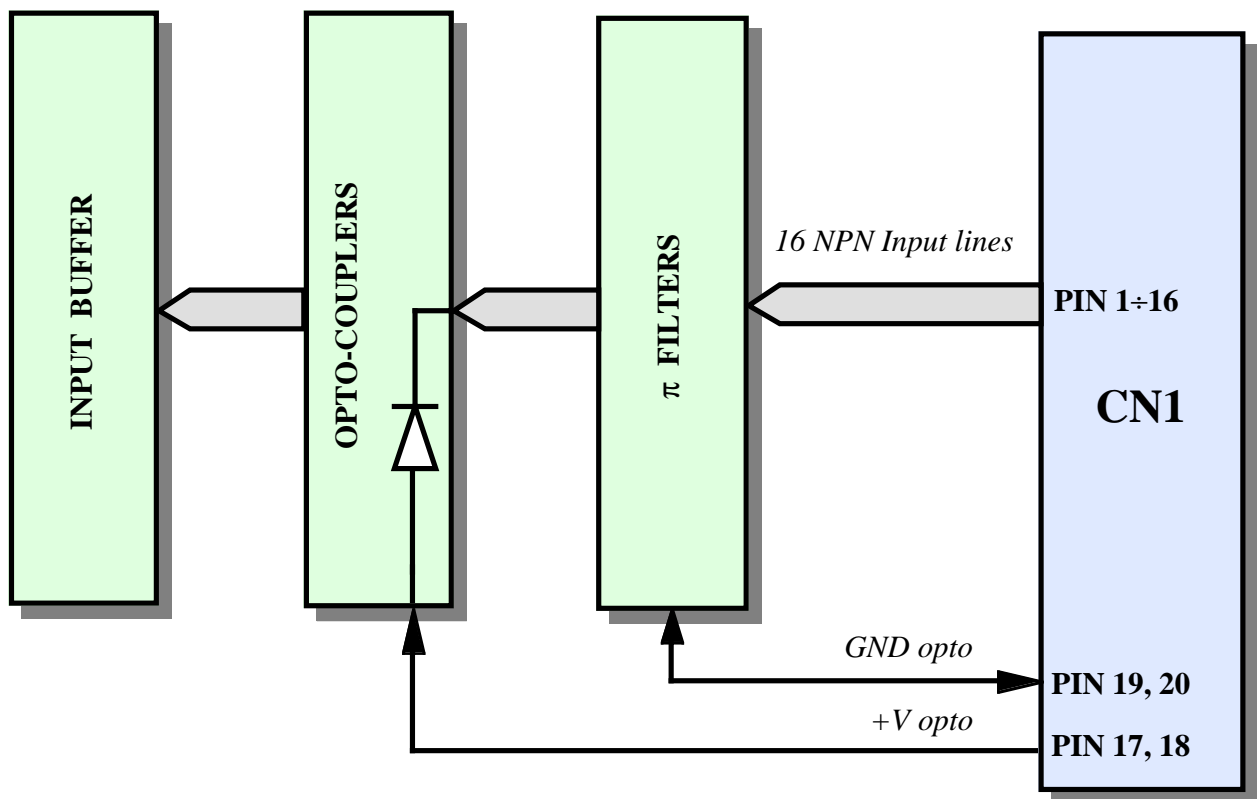


FIGURE 4: OPTOCOUPLED INPUTS BLOCK DIAGRAM

CN2 - CONNECTOR FOR TRANSISTOR OUTPUTS

The connector for NPN transistor outputs, called CN2, is a low profile, 2.54 mm pitch, 90 degrees, 34 pins connector. Open collector contacts of each output transistor and two common terminals related to two output groups OUT0 and OUT1 are present; please remark that the maximum current for each transistor is 4 A non continuative, maximum voltage is +45 Vdc.

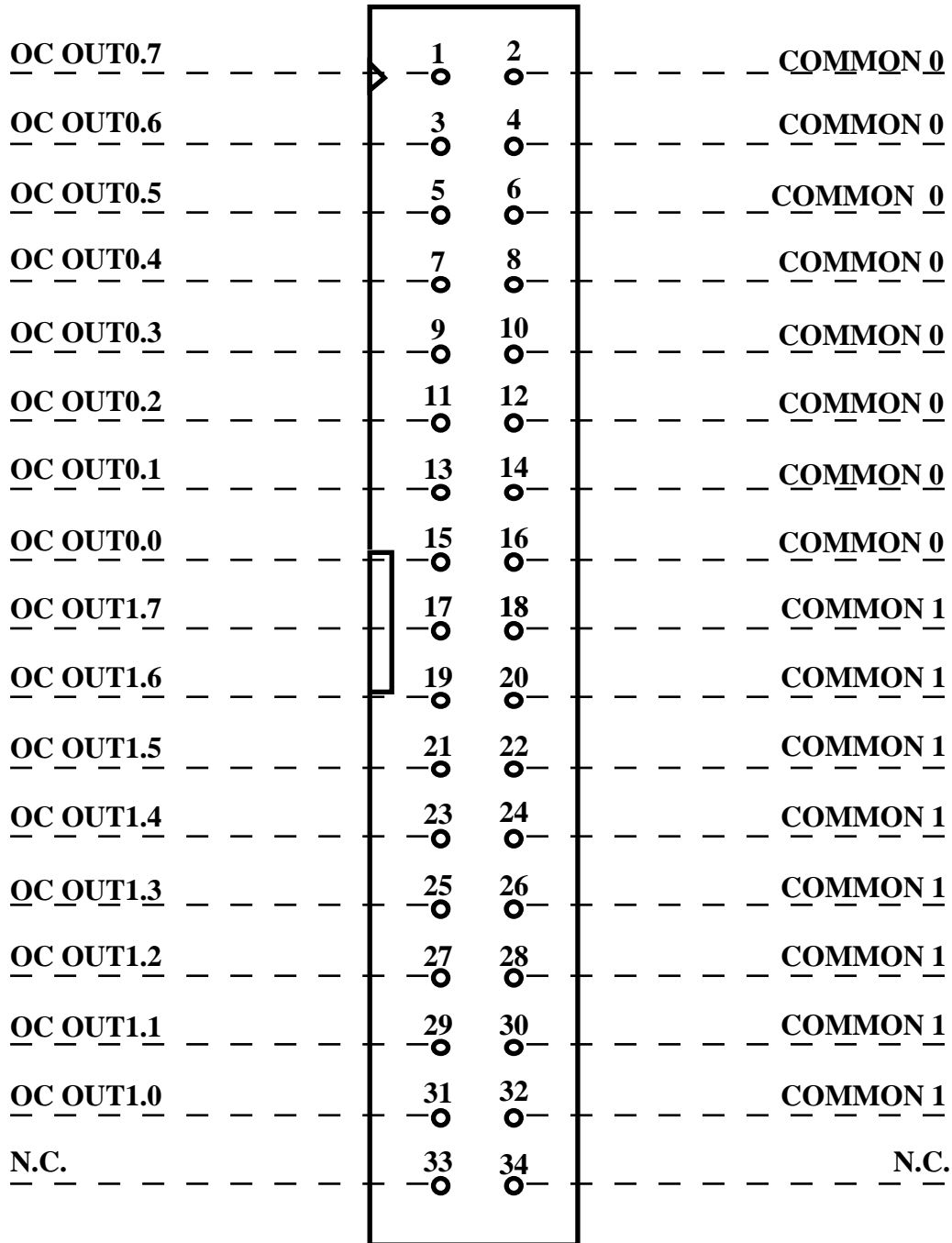


FIGURE 5: CN2 - TRANSISTOR OUTPUTS CONNECTOR

Signals description:

OC OUT0.n	= O - Contact of n-th open collector output in section OUT0.
COMMON 0	= - Common contact of the 8 transistors of section OUT0.
OC OUT1.n	= O - Contact of n-th open collector output in section OUT1.
COMMON 1	= - Common contact of the 8 transistor of section OUT1.
N.C.	= - Not connected.

The transistor output signals available on **CI/O T16** are provided with a LED for visual feed back (the LED will light whenever the transistor is conducting); in addition they are optocoupled, to warrant galvanic separation between internal electronics and external world.

The final stage of the outputs is made by a Darlington **NPN** open collector transistor, capable to bear a maximum current of **4 A non continuative** or a tension that can be as high as **+45 Vdc**.

Please remark that this component, being without heat sink, can drive in continuative way a resistive load absorbing a maximum current of **600 mA** at a tension of **+24 Vdc**, at a working temperature of 20 centigrad degrees.

The interface circuitry for this 16 transistors output section is shown in the following diagram.

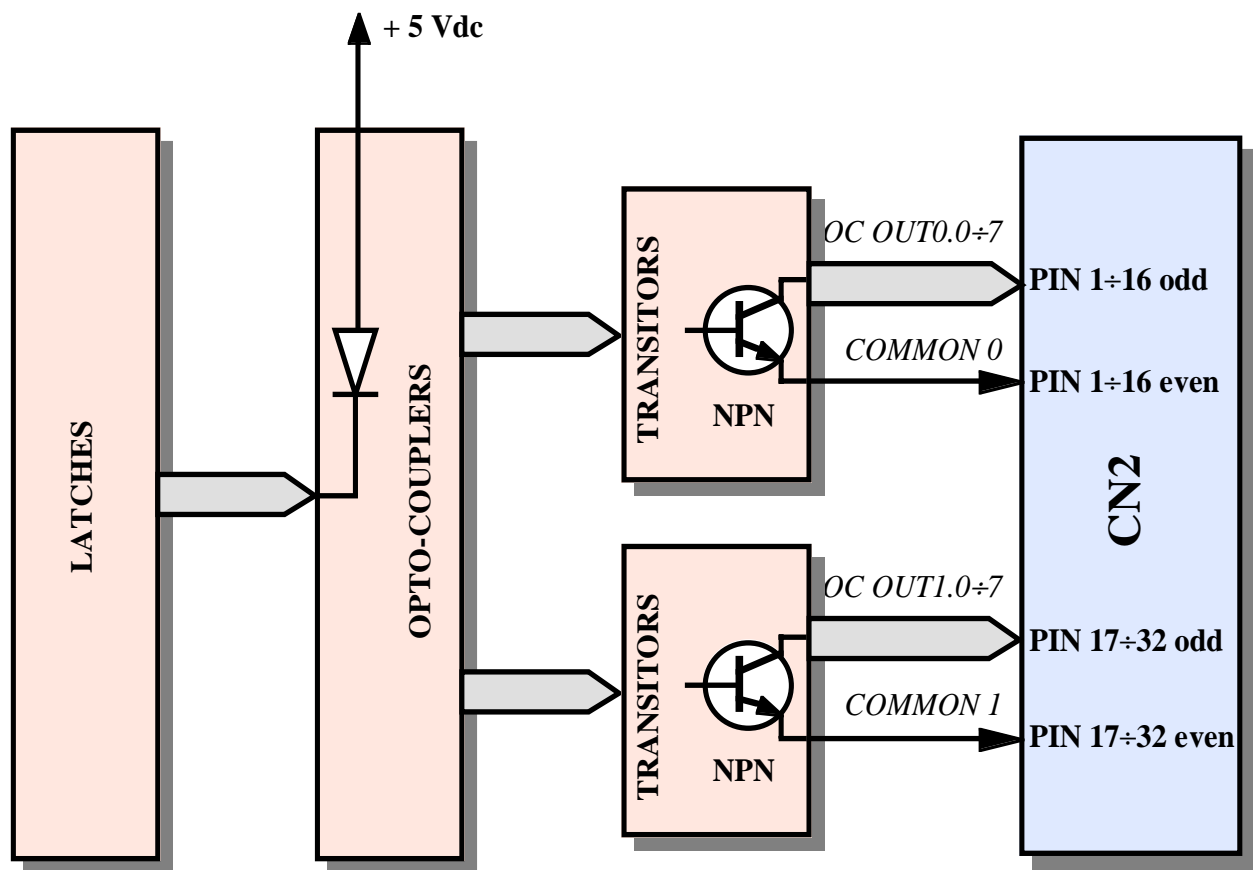


FIGURE 6: TRANSISTOR OUTPUTS BLOCK DIAGRAM

K1 - CONNECTOR FOR ABACO® BUS

The connector for **ABACO® industrial BUS**, called K1 on the board, is a DIN 41612, male, a 90 degree, type C, A+C.

Here follows the pin-out of the connector installed on **CI/O T16**, in addition there is the standard 8 bits and 16 bits **ABACO® BUS** pin-out.

Please remark that all the signals here described are TTL, except for the power supplies.

A BUS a 16 bit	A BUS a 8 bit	A CI/O T16	PIN	C CI/O T16	C BUS a 8 bit	C BUS a 16 bit
GND	GND	GND	1	GND	GND	GND
+5 Vdc	+5 Vdc	+5 Vdc	2	+5 Vdc	+5 Vdc	+5 Vdc
D0	D0	D0	3	D8		D8
D1	D1	D1	4	D9		D9
D2	D2	D2	5	D10		D10
D3	D3	D3	6	N.C.	/INT	/INT
D4	D4	D4	7	N.C.	/NMI	/NMI
D5	D5	D5	8	D11	/HALT	D11
D6	D6	D6	9	N.C.	/MREQ	/MREQ
D7	D7	D7	10	/IORQ	/IORQ	/IORQ
A0	A0	A0	11	/RD	/RD	/RD LDS
A1	A1	A1	12	/WR	/WR	/WR LDS
A2	A2	A2	13	D12	/BUSAK	D12
A3	A3	A3	14	N.C.	/WAIT	/WAIT
A4	A4	A4	15	D13	/BUSRQ	D13
A5	A5	A5	16	/RESET	/RESET	/RESET
A6	A6	A6	17	/M1	/M1	/IACK
A7	A7	A7	18	D14	/RFSH	D14
A8	A8	A8	19	N.C.	/MEMDIS	/MEMDIS
A9	A9	A9	20	N.C.	VDUSEL	A22
A10	A10	A10	21	D15	/IEI	D15
A11	A11	A11	22	N.C.		
A12	A12	A12	23	N.C.	CLK	CLK
A13	A13	A13	24	/RDUDS		/RDUDS
A14	A14	A14	25	/WRUDS		/WRUDS
A15	A15	A15	26	N.C.		A21
A16		N.C.	27	N.C.		A20
A17		N.C.	28	N.C.		A19
A18		N.C.	29	N.C.	/R.T.	/R.T.
+12 Vdc	+12 Vdc	N.C.	30	N.C.	-12 Vdc	-12 Vdc
+5 Vdc	+5 Vdc	+5 Vdc	31	+5 Vdc	+5 Vdc	+5 Vdc
GND	GND	GND	32	GND	GND	GND

FIGURE 7: K1 - CONNECTOR FOR ABACO® BUS

Signals description:

8 bits CPU

A0-A15	=	O	- Address BUS
D0-D7	=	I/O	- Data BUS
INT	=	I	- Interrupt request
NMI	=	I	- Non Maskable Interrupt
HALT	=	O	- Halt state
MREQ	=	O	- Memory Request
IORQ	=	O	- Input Output Request
RD	=	O	- Read cycle status
WR	=	O	- Write cycle status
BUSAK	=	O	- BUS Acknowledge
WAIT	=	I	- Wait
BUSRQ	=	I	- BUS Request
RESET	=	O	- Reset
M1	=	O	- Machine cycle one
RFSH	=	O	- Refresh for dynamic RAM
MEMDIS	=	I	- Memory Display
VDUSEL	=	O	- VDU Selection
IEI	=	I	- Interrupt Enable Input
CLK	=	O	- System clock
R.B.	=	I	- Reset button
+5 Vdc	=	I	- Power supply at +5 Vdc
+12 Vdc	=	I	- Power supply at +12 Vdc
-12 Vdc	=	I	- Power supply at -12 Vdc
GND	=		- Ground signal

16 bits CPU

A16-A22	=	O	- Address BUS
D8-D15	=	I/O	- Data BUS
RD UDS	=	O	- Read Upper Data Strobe
WR UDS	=	O	- Write Upper Data Strobe
IACK	=	O	- Interrupt Acknowledge
RD LDS	=	O	- Read Lower Data Strobe
WR LDS	=	O	- Write Lower Data Strobe

N.B.

Directionality indications as above stated are referred to a master (**CPU** or **GPC®**) board and have been kept untouched to avoid ambiguity in case of multi-boards systems.

VISUAL SIGNALATIONS

CI/O T16 card is provided with signalation LEDs to show several status informations, as described in the following table:

LED	COLOUR	PURPOSE
LD1	Green	If lighting, indicates that the 64 Kbytes addressing mode is used.
LD2	Red	If lighting, indicates that the 16 bits BUS data path mode is used.
LD3	Yellow	If lighting, indicates that the 8 bits BUS data path mode is used.
L00÷L07	Red	Visualize the status of the eight outputs of section OUT0, respectively OUT0.0÷OUT0.7. A LED on indicates an active output (open collector transistor conducting).
L10÷L17	Red	Visualize the status of the eight outputs of section OUT1, respectively OUT1.0÷OUT1.7. A LED on indicates an active output (open collector transistor conducting).
L200÷L207	Green	Visualize the status of the eight otocoupled input signals IN0, respectively IN0.0÷IN0.7. A LED on indicates an input contact closed.
L300÷L307	Yellow	Visualize the status of the eight otocoupled input signals IN0, respectively IN1.0÷IN1.7. A LED on indicates an input contact closed.

FIGURE 8: VISUAL SIGNALATIONS TABLE

The main purpose of LEDs is to show a visual indication about the card's status, making so easier debug and verify operations. To easily locate these visual signalations please refer to the figure 9.

POWER SUPPLY

CI/O T16 is provided with an efficient circuitry that solves in a comfortable and simple way the problem of the board's supply, under any condition of use.

Here follow the voltages needed:

V_{opto}: Supplies the optocouplers of the input section; must be in the range +12÷24 Vdc and must be provided through pins 17-18 and pins 19-20 of CN1.

+5 Vdc: Supplies the on board logic; must be in the range +5 Vdc ± 5% and must be provided through the specific pins of connector K1 (ABACO® BUS).

To warrant great immunity to external noise and so a correct working of the board, it is essential that **V_{opto}** tension is galvanically isolated.

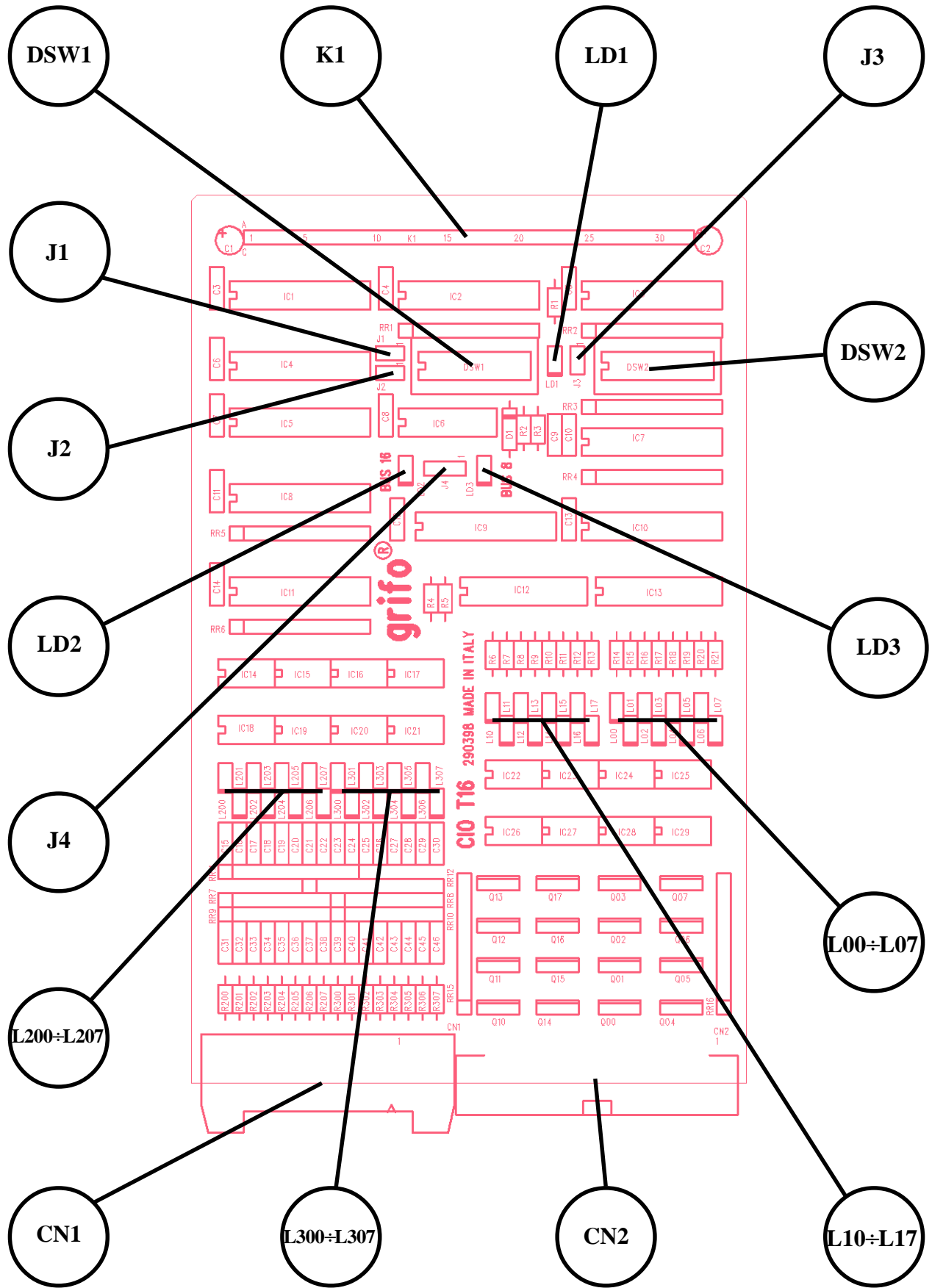


FIGURE 9: CONNECTORS, DIP SWITCH, LEDs AND JUMPERS LOCATION

JUMPERS

On **CI/O T16** board there are 4 jumpers for card configuration. Below there is the jumpers list, location and function.

JUMPER	N. PINS	PURPOSE
J1	2	It selects the connectio of signal /M1, coming from ABACO [®] BUS, to the specific circuitry installed on the board.
J2	2	It selects the connectio of signal /RESET, coming from ABACO [®] BUS, to the specific circuitry installed on the board.
J3	2	It selects between 256 bytes normal addressing mode or 64 Kbytes exteded addressing mode.
J4	3	Selects BUS addresses path between 8 or 16 bits.

FIGURE 10: JUMPERS SUMMARIZING TABLE

These tables describe all the right connections of the three jumpers with their relative functions. For recognizing jumpers location, please refer to the figure 9.

The "*" used in the following tables, denotes the default connection, or on the other hand the connection set up at the end of testing phase, that is the configuration the user receives.

2 PINS JUMPERS

JUMPER	CONNECTION	PURPOSE	DEF.
J1	not connected	Parallel interface does not manage signal /M1 coming from ABACO [®] BUS.	
	connected	Parallel interface manages signal /M1 coming from ABACO [®] BUS.	*
J2	not connected	It does not connect the signal /RESET, coming from ABACO [®] BUS, to the specific circuitry installed on the board.	
	connected	It connects the signal /RESET, coming from ABACO [®] BUS, to the specific circuitry installed on the board.	*
J3	not connected	Selects the board's 256 bytes normal addressing mode.	*
	connected	Selects the board's 64 Kbytes extended addressing mode.	

FIGURE 11: 2 PINS JUMPERS TABLE

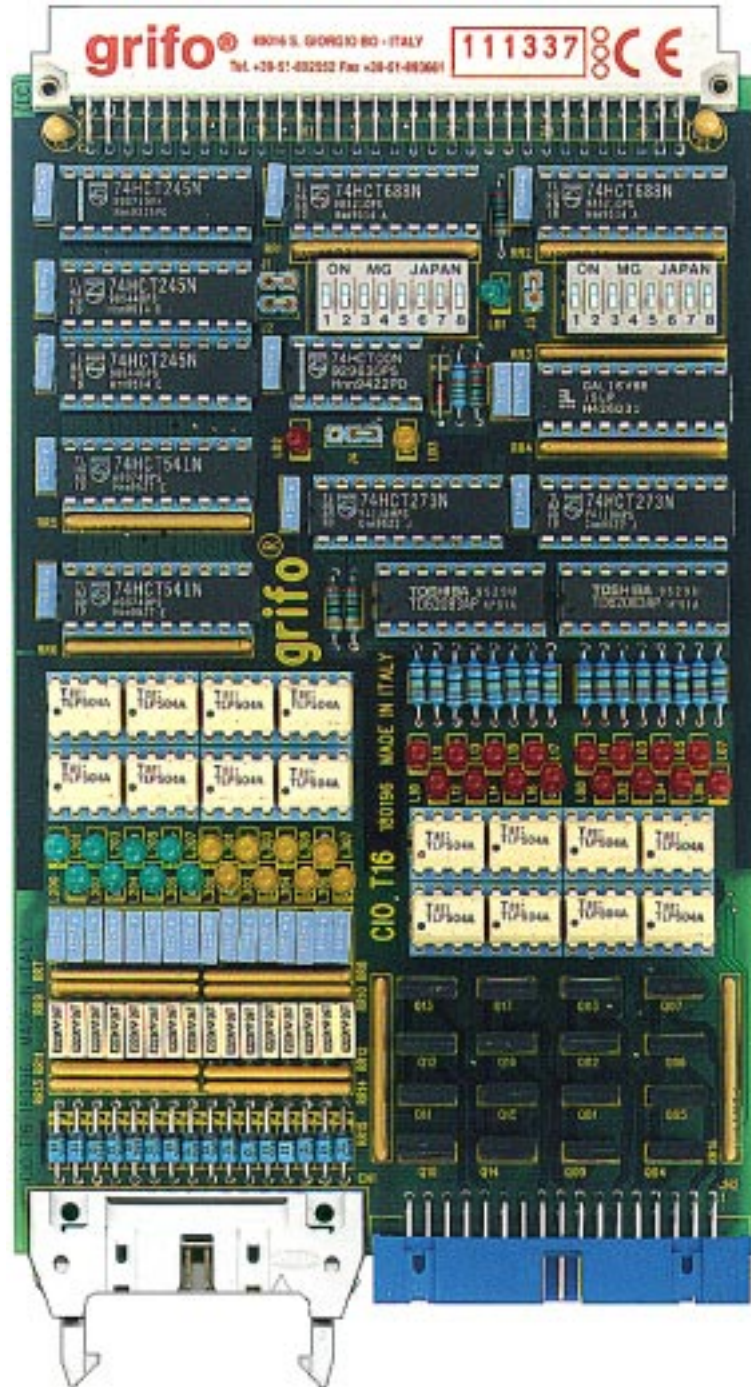


FIGURE 12: CARD PHOTO

3 PINS JUMPERS

JUMPER	CONNECTION	PURPOSE	DEF.
J4	position 1-2	Configures the board to be managed through an 8 bits wide BUS data path.	*
	position 2-3	Configures the board to be managed through a 16 bits wide BUS data path.	

FIGURE 13: 3 PINS JUMPER TABLE

RESET CIRCUITRY CONFIGURATION

Through jumper **J2**, as described in the next paragraph, the User may select whether to connect or not the /RESET signal coming from **ABACO® BUS** to the specific circuitry on the board **CI/O T16**; if the jumper is **connected**, when the /RESET is active the board's outputs are **disabled**. Viceversa if the jumper is **not connected**, /RESET signal **doesn't affect** the status of the outputs, that are disabled whenever a Power-On occurs. This feature is essential when, for example, the outputs must not change status for a control board's reset due to, for example, an intervent of its on board Watch Dog circuitry.

I/O CONNECTIONS

To prevent possible connecting problems between **CI/O T16** board and the external systems, the User has to read carefully the information of the previous paragraphs and he must follow these instructions:

- To connect to the optocoupled input signals, only the contacts to acquire must be connected from the external system(s). These contacts (relays, switches, etc.) must connect or not connect the input signal INx.y to GND opto. About the correspondance between logic signals and contact status, an open contact generates a logic **1**, a closed contact generates a logic **0**, following the NPN standard.
- The NPN Darlington transistors output signals must be connected directly to the load to drive (power relays, etc.). The board provides the open collector outputs called NO OUTx.y, capable to bear a maximum current of **4 A non continuative** with a tension that can be **+45 Vdc**. Being without heat sink, they can drive in continuative way a resistive load absorbing a maximum current of **600 mA** at a tension of **+24 Vdc**, at a working temperature of 20 centigrad degrees. To allow the User to drive several loads having different power supplies, each output section is provided with two differnt COMMON terminals connected to two groups of eight relays.
- The TTL output signals can be connected directly only to a device featuring the same type of interface. About the correspondance between logic signals and TTL output status, remember that a logic **0** generates a TTL 0 Vdc, while a logic **1** generates a TTL +5 Vdc.

HARDWARE DESCRIPTION

This chapter provides all the hardware informations needed to use **CI/O T16** board. Here the User will find informations about I/O card mapping and on board peripheral devices addressing.

BOARD MAPPING

CI/O T16 board is mapped into a 2 bytes I/O addressing space (or one word in 16 bits addressing mode), that can be mapped starting from different base addresses according to how the board is configured. This feature allows to use several **CI/O T16** cards on the same **ABACO® BUS**, or to install them on a BUS where other peripheral modules are installed obtaining a structure that can be expanded without any difficulty or modifications to the application software.

The base address can be defined through the specific BUS interface circuitry on the board itself; this circuitry uses the 2 eight pins dip switched called **DSW1** and **DSW2**, from which it reads the address set by the User. Here follows the corrispondance between dips configuration and address signals.

DSW1.1	->	<i>Don't care</i>	<u>8 bits BUS data path (J4 in position 1-2)</u>
		<i>Address A0</i>	<u>16 bits BUS data path (J4 in position 2-3)</u>
DSW1.2	->	Address A1	
DSW1.3	->	Address A2	
DSW1.4	->	Address A3	
DSW1.5	->	Address A4	
DSW1.6	->	Address A5	
DSW1.7	->	Address A6	
DSW1.8	->	Address A7	
DSW2.1	->	Address A8	
DSW2.2	->	Address A9	
DSW2.3	->	Address A10	
DSW2.4	->	Address A11	
DSW2.5	->	Address A12	
DSW2.6	->	Address A13	
DSW2.7	->	Address A14	
DSW2.8	->	Address A15	

These dips are driven in complemented logic, this means that if a jumper is **CONNECTED** generates a **logic zero**, viceversa if a jumper is **NOT CONNECTED** generates a **logic one**.

Jumper J3 selects the number of bytes addressed amongst which the allocation address can be chosen. If the 256 bytes (from 00H to FFH) normal addressing mode is selected, only DSW1 is significant (switches configuration on DSW2 is indifferent); if the 64Kbytes (from 00H to FFFFH) extended addressing mode is selected, then both DSW1 and DSW2 must be configured correctly.

Also jumper J1, described in the previous paragraph, affects the addressing logic and must be connected according to the type of control card (**GPC**[®] serie) is used. In detail if the control card is provided with signal /M1 on the **ABACO**[®] BUS connector, then jumper J1 must be connected and viceversa.

NOTE

When allocating the mapping address of the boards, please be careful not to allocate more than one device in the same addressing space (count also the number of bytes occupied by the card). If this condition will not be respected, a BUS conflict will happen; such conflict will compromise the correct working of the whole system.

As an example, possible mappings are reported here.

- 1) Address used to map **C/IO T16**: 04AH with 256 bytes addressing mode.
Control board used: data and addresses bus path are 8 bits wide;
provided with signal /M1.

J1	->	Connected
J3	->	Not connected
J4	->	Position 1-2
DSW1.1	->	Don't care
DSW1.2	->	OFF
DSW1.3	->	ON
DSW1.4	->	OFF
DSW1.5	->	ON
DSW1.6	->	ON
DSW1.7	->	OFF
DSW1.8	->	ON
DSW2	->	Don't care

- 2) Address used to map **C/IO T16**: 14F8H with 64Kbytes addressing mode.
Control board used: data bus path is 8 bits wide;
addresses bus path is 16 bits wide;
not provided with signal /M1.

J1	->	Not connected
J3	->	Connected
J4	->	Position 1-2
DSW1.1	->	Don't care
DSW1.2	->	ON
DSW1.3	->	ON
DSW1.4	->	OFF
DSW1.5	->	OFF
DSW1.6	->	OFF
DSW1.7	->	OFF
DSW1.8	->	OFF

DSW2.1	->	ON
DSW2.2	->	ON
DSW2.3	->	OFF
DSW2.4	->	ON
DSW2.5	->	OFF
DSW2.6	->	ON
DSW2.7	->	ON
DSW2.8	->	ON

3) Address used to map C/IO T16:

Control board used:

F680H with 64Kbytes addressing mode.
data and addresses bus path are 16 bits wide;
not provided with signal /M1.

J1	->	Not connected
J3	->	Connected
J4	->	Position 2-3

DSW1.1	->	ON
DSW1.2	->	ON
DSW1.3	->	ON
DSW1.4	->	ON
DSW1.5	->	ON
DSW1.6	->	ON
DSW1.7	->	ON
DSW1.8	->	OFF

DSW2.1	->	ON
DSW2.2	->	OFF
DSW2.3	->	OFF
DSW2.4	->	ON
DSW2.5	->	OFF
DSW2.6	->	OFF
DSW2.7	->	OFF
DSW2.8	->	OFF

To easily locate jumpers and dip switches please refer to figures 2 and 9.

INTERNAL REGISTERS ADDRESSING

Indicating the board base address with **<baseaddr>**, that is the address set using Dip Switches DSW1 and DSW2, as indicated in the previous paragraph **CI/O T16** internal registers are addressable as explained in the following tables, respectively when addressing mode is 8 bit and 16 bit.

NOTE

If using several boards on the same **ABACO® BUS**, when setting the boards mapping address the User should be careful not to allocate more than one board in the same addressing space (consider the base address plus the bytes taken by the board addressing). If this condition is not satisfied a BUS conflict situation will occur, prejudicing the correct working of the whole system.

INTERNAL REGISTERS ADDRESSING FOR 8 BIT ADDRESSING MODE

DEVICE	REG.	ADDRESS	R/W	PURPOSE
OUTPUT 0	OUT0	<baseaddr>+00H	W	Register to set the status of the 8 relay outputs in section OUT0.
OUTPUT 1	OUT1	<baseaddr>+01H	W	Register to set the status of the 8 relay outputs in section OUT1.
INPUT 0	IN0	<baseaddr>+00H	R	Register to read the status of the 8 optocoupled inputs in section IN0.
INPUT 1	IN1	<baseaddr>+01H	R	Register to read the status of the 8 optocoupled inputs in section IN1.

FIGURE 14: INTERNAL REGISTERS ADDRESSING TABLE FOR 8 BIT ADDRESSING MODE

INTERNAL REGISTERS ADDRESSING FOR 16 BIT ADDRESSING MODE

DEVICE.	REG.	ADDRESS	R/W	PURPOSE
OUTPUT	OUT	<baseaddr>+00H	W	Register to set the status of the 16 relay outputs in section OUT0 and OUT1.
INPUT	IN	<baseaddr>+00H	R	Registro to read the status of the 16 optocoupled inputs in section IN0 and IN1.

FIGURE 15: INTERNAL REGISTERS ADDRESSING TABLE FOR 16 BIT ADDRESSING MODE

PERIPHERAL DEVICES SOFTWARE DESCRIPTION

In the previous paragraph allocation addresses of all the peripherals have been reported, here follows a detailed description of function and meaning of internal registers (please always refer to the peripheral mapping tables to understand completely the following informations). Should the present documentaion be inadequate please refer to the component's manufacturer documentation.

In the following paragraphs the indications D0÷D7 or D0÷D15 are used to refer the bits of the byte or word involved in the I/O operations.

RELAY OUTPUTS

Input/Output registers (called OUT1 and OUT2 if BUS data path is 8 bits wide and called OUT if BUS data path is 16 bits wide) are used to perform the output management on **CI/O T16** board. The bits of these registers have the following meaning:

8 bits data BUS

OUT1.D7 -> OC OUT1.7
 OUT1.D6 -> OC OUT1.6
 OUT1.D5 -> OC OUT1.5
 OUT1.D4 -> OC OUT1.4
 OUT1.D3 -> OC OUT1.3
 OUT1.D2 -> OC OUT1.2
 OUT1.D1 -> OC OUT1.1
 OUT1.D0 -> OC OUT1.0

OUT0.D7 -> OC OUT0.7
 OUT0.D6 -> OC OUT0.6
 OUT0.D5 -> OC OUT0.5
 OUT0.D4 -> OC OUT0.4
 OUT0.D3 -> OC OUT0.3
 OUT0.D2 -> OC OUT0.2
 OUT0.D1 -> OC OUT0.1
 OUT0.D0 -> OC OUT0.0

16 bits data BUS

OUT.D15 -> OC OUT1.7
 OUT.D14 -> OC OUT1.6
 OUT.D13 -> OC OUT1.5
 OUT.D12 -> OC OUT1.4
 OUT.D11 -> OC OUT1.3
 OUT.D10 -> OC OUT1.2
 OUT.D9 -> OC OUT1.1
 OUT.D8 -> OC OUT1.0

OUT.D7 -> OC OUT0.7
 OUT.D6 -> OC OUT0.6
 OUT.D5 -> OC OUT0.5
 OUT.D4 -> OC OUT0.4
 OUT.D3 -> OC OUT0.3
 OUT.D2 -> OC OUT0.2
 OUT.D1 -> OC OUT0.1
 OUT.D0 -> OC OUT0.0

The indication **OC OUTn.?** stands for OUT0 and OUT1 sections, whose output signals are available on connector CN2.

Performing an output operation at the address of OUT0, OUT1 or OUT the corresponding outputs are set by the output data.

The correspondance between status of an output and value of a bit is:

Bit at logic 0 -> Output disabled = Realy contact open
 Bit at logic 1 -> Output enabled = Realy contact closed

All registers are reset (all bits are 0) when a Reset or a Power On occur if **J2** is connected, this disables all the outputs and disabmes all the open collector transistors.

OPTOCOUPLED INPUTS

Input registers (called IN1 and IN2 if BUS data path is 8 bits wide and called IN if BUS data path is 16 bits wide) are used to perform the input management on **CI/O T16** board. The bits of these registers have the following meaning:

8 bits data BUS

IN1.D7	->	IN1.7
IN1.D6	->	IN1.6
IN1.D5	->	IN1.5
IN1.D4	->	IN1.4
IN1.D3	->	IN1.3
IN1.D2	->	IN1.2
IN1.D1	->	IN1.1
IN1.D0	->	IN1.0

IN0.D7	->	IN0.7
IN0.D6	->	IN0.6
IN0.D5	->	IN0.5
IN0.D4	->	IN0.4
IN0.D3	->	IN0.3
IN0.D2	->	IN0.2
IN0.D1	->	IN0.1
IN0.D0	->	IN0.0

16 bits data BUS

IN.D15	->	IN1.7
IN.D14	->	IN1.6
IN.D13	->	IN1.5
IN.D12	->	IN1.4
IN.D11	->	IN1.3
IN.D10	->	IN1.2
IN.D9	->	IN1.1
IN.D8	->	IN1.0

IN.D7	->	IN0.7
IN.D6	->	IN0.6
IN.D5	->	IN0.5
IN.D4	->	IN0.4
IN.D3	->	IN0.3
IN.D2	->	IN0.2
IN.D1	->	IN0.1
IN.D0	->	IN0.0

The indication **INn.?** stands for IN1 and IN2 sections, whose input signals are available on connector CN1.

Performing an input operation at the address of IN1, IN2 or IN the corresponding optocoupled input signals are acquired.

The correspondance between status of an input and value of a bit is:

Bit at logic 0	->	Input disabled	=	Input contact open
Bit at logic 1	->	Input enabled	=	Input contact closed

EXTERNAL CARDS

CI/O T16 board can interface to most of **grifo**® industrial boards. Their main purpose is to perform a digital Input/Output interfacement between CPU (**GPC**®) cards and the external world.

Here is reported an illustrative list of cards capable to interact with **CI/O T16** board with a short description of their features; for further informations please request the specific documentation.

MB3 01-MB4 01-MB8 01

Mother Board 3, 4, 8 slots

Motherboard featuring 3, 4 or 8 slots of **ABACO**® industrial BUS; pitch 4 TE; standard power supply connectors; LEDs for visual feed-back of power supply; holes for rack docking.

SPB 04-SPB 08

Switch Power BUS 4-8 slots

Motherboard featuring 4-8 slots of **ABACO**® industrial BUS; pitch 4 TE; standard power supply connectors; termination resistances; connector type F for **SPC xxx** supply ; holes for rack docking.

ABB 03

ABACO® Block BUS 3 slots

3 slots **ABACO**® mother board; 4 TE pitch connectors; **ABACO**® I/O BUS connector; screw terminal for power supply; connection for DIN C type and Ω rails.

ABB 05

ABACO® Block BUS 5 slots

5 slots **ABACO**® mother board with power supply. Double power supply built in; 5Vdc 2,5A section for powering the on board logic; second section at 24Vdc 400mA galvanically coupled, for the optocoupled input lines. Auxiliary connector for **ABACO**® I/O BUS. Connection for DIN Ω rails.

SBP 02-xx

Switch BLOCK Power xx version

Low cost switching power supply able to generate voltage from +5 to +40 Vdc and current up to 2.5 A; Input from 12 to 24 Vac; Connection for DIN C Type and Ω rails.

SPC 03.5S

Switch Power Card +5 Vdc

Europe format switching power supply capable to provide +5 Vdc to a load of 4 A; input voltage 12÷24 Vac; power-failure; connector for back-up battery; standard connector for mother board **SPB 0x**.

SPC 512

Switch Power Card +5 Vdc +12 Vdc

Europe format switching power supply capable to provide +5 Vdc 5A and +12 Vdc 2.5 A; input voltage 12÷24 Vac; power-failure; connector for back-up battery; standard connector for mother board **SPB 0x**.

GPC® 51

General Purpose Controller fam. 51

Microprocessor family 51 INTEL including the masked BASIC chip; the board features: 16 I/O TTL lines; dip switch; 3 timer/counter; RS 232; 4 A/D converter signals resolution 11 bit; buzzer; on board EPROM programmer; RTC and 32K SRAM with Lithium battery back up; controller for display and keyboard.

GPC® 188F

General Purpose Controller 80C188

80C188 μ P 20MHz; 1 RS 232 line; 1 RS 232, RS 422-485 or Current Loop line; 24 TTL I/O lines; 1MEPROM or 512K FLASH; 1MRAMLithium battery backed; 8K serial EEPROM; RTC; Watch Dog; 8 Dip switch; 3 Timer Counter; 8 13 bit A/D lines; Power failure; activity LEDs; single power supply +5Vdc.

GPC® 15A

General Purpose Controller 84C15

Full CMOS card, 10÷20 MHz 84C15 CPU; 512K EPROM or FLASH; 128K RAM; 8K RAM and RTC backed; 8K serial EEPROM; 1 RS 232 line; 1 RS 232 line or RS 422-485 or Current Loop line; 32 or 40 TTL I/O lines; CTC; Watch dog; 2 Dip switches; Buzzer.

GPC® 150

General Purpose Controller 84C15

Microprocessor Z80 at 16 MHz; implementation completely CMOS; 512K EPROM or FLASH; 512K SRAM; RTC; Back-Up through external Lithium battery; 4M serial FLASH; 1 serial line RS 232 plus 1 RS 232 or RS 422-485 or current loop; 40 I/O TTL; 2 timer/counter; 2 watch dog; dip switch; EEPROM; A/D converter with resolution 12 bit; activity LED.

GPC® 15R

General Purpose Controller 84C15

84C15 μ P, 10÷16 MHz; 1 RS 232 line; 1 RS 232 or RS 422-485 or C. L. line; 16÷24 TTL I/O lines; 16 Opto-in; 8 Relays; 4 Opto Coupled Timers Counters; 512K EPROM or FLASH; 512K RAM and RTC backed; 8K serial EEPROM; 8K Backed RAM modul; Buzzer; 1 Activity LED; Watch dog; 4÷12 readable DIPs; LCD Interface.

GPC® 323

General Purpose Controller 51 family

80C32 μ P, 14 MHz; Full CMOS; 1 RS 232 line (software); 1 RS 232 or RS 422-485 or Current Loop line; 24 TTL I/O lines; 11 A/D 12 bits lines; 3 Timers Counters; 64K EPROM; 64K RAM; 32K RAM and RTC backed; 32K DIL EEPROM; 8K serial EEPROM; Buzzer; 2 Activity LED; Watch dog; 5 readable DIPs; LCD Interface.

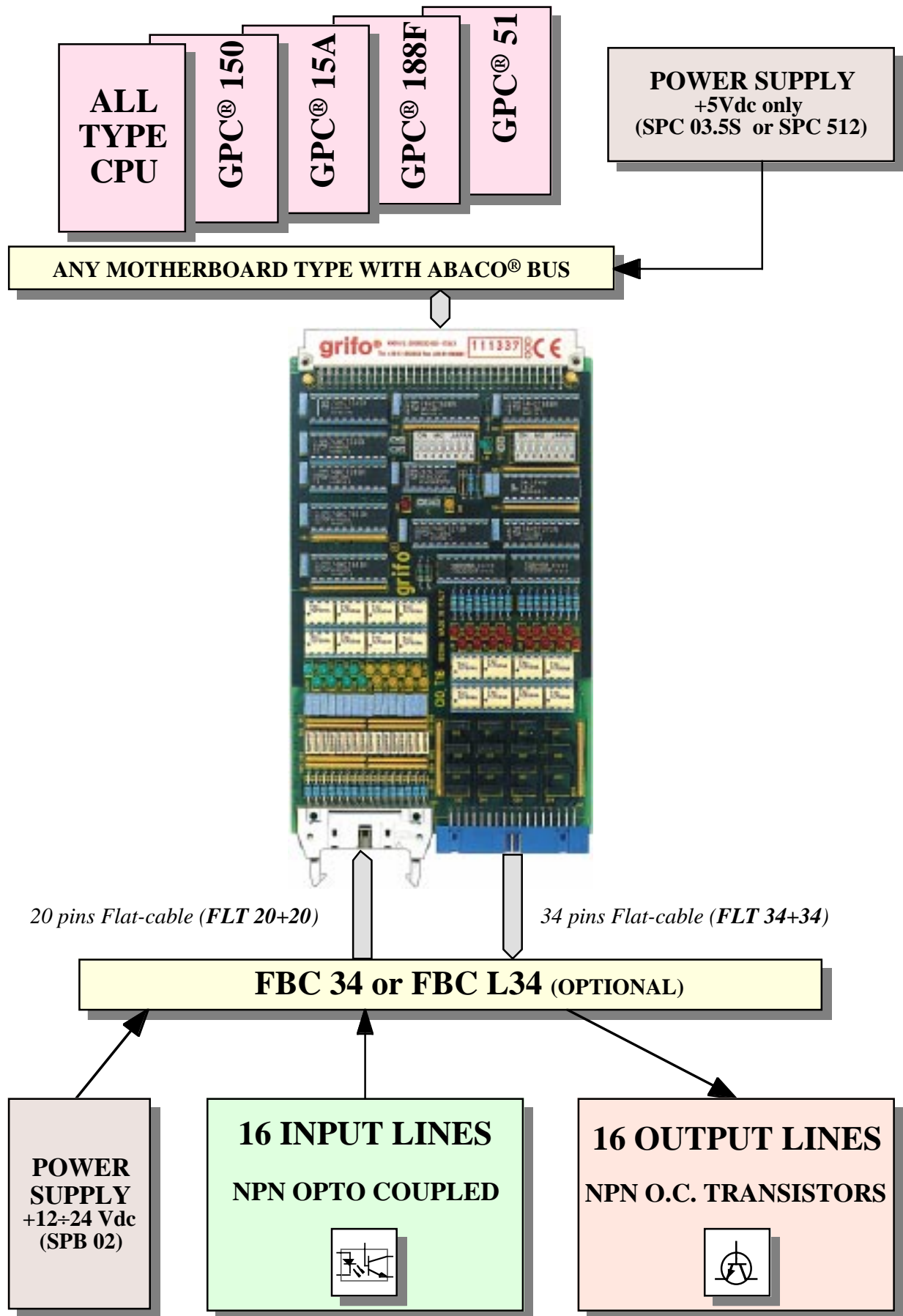


FIGURE 16: POSSIBLE CONNECTIONS DIAGRAM

GPC® 553

General Purpose Controller 80C552

80C552 μ P, 22÷33 MHz; 1 RS 232 line (software); 1 RS 232 or RS 422-485 or Current Loop line; 16 TTL I/O lines; 8 A/D 10 bits lines; 3 Timers Counters; 64K EPROM; 64K RAM; 32K RAM and RTC backed; 32K DIL EEPROM; 8K serial EEPROM; 2 PWM lines; 1 Activity LED; Watch dog; 5 readable DIPs; LCD Interface.

GPC® 153

General Purpose Controller Z80

84C15 μ P, 10÷16 MHz; Full CMOS; 1 RS 232 line; 1 RS 232 or RS 422-485 or Current Loop line; 16 TTL I/O lines; 8 A/D 12 bits lines; 2÷4 Timers Counters; 512K EPROM or FLASH; 512K RAM and RTC backed; 8K serial EEPROM; Buzzer; 1 Activity LED; Watch dog; 8 readable DIPs; LCD Interface.

GPC® 183

General Purpose Controller Z180

Z180 μ P, 10÷16 MHz; Full CMOS; 1 RS 232 line; 1 RS 232 or RS 422-485 or Current Loop line; 24 TTL I/O lines; 11 A/D 12 bits lines; 2 Timers Counters; 512K EPROM or FLASH; 512K RAM and RTC backed; 8K serial EEPROM; Buzzer; 2 Activity LED; Watch dog; 4 readable DIPs; LCD Interface.

GPC® 324/D

“4” Type General Purpose Controller 80C32/320

80C32 or 80C320 μ P, 14÷22 MHz; Full CMOS; 1 RS 232 line; 1 RS 232 or RS 422-485 or Current Loop line; 4÷16 TTL I/O lines; 3 Timers Counters; 64K EPROM; 64K RAM; 32K RAM backed; 32K DIL E2; 8K serial EEPROM; Watch dog; 1 readable DIP; LCD Interface; Abaco® I/O BUS; 5Vdc Power supply; Size: 100x50 mm.

GPC® 554

General Purpose Controller 80C552

Microprocessor 80C552 at 22 MHz; implementation completely CMOS; 32K EPROM; 32 K SRAM; 32 K EEPROM or SRAM; EEPROM; 2 RS 232 serial lines; 16 I/O TTL; 2 PWM lines; 16 bits Timer/Counter; Watch Dog; 6 signals A/D converter with resolution 10 bit; interface for **ABACO®** I/O BUS.

GPC® 154

“4” Type General Purpose Controller Z80

84C15 μ P, 10÷16 MHz; Full CMOS; 1 RS 232 line; 1 RS 232 or RS 422-485 line; 16 TTL I/O lines; 2÷4 Timers Counters; 512K EPROM or FLASH; 512K RAM and RTC backed; 8K serial EEPROM; Watch dog; 2 readable DIPs; LCD Interface; Abaco® I/O BUS; 5Vdc Power supply; Size: 100x50 mm.

GPC® 884

General Purpose Controller Am188ES

Microprocessor AMD Am188ES up to 40 MHz; 16 bits; implementation completely CMOS; serie 4 format; 512K EPROM or FLASH; 512K SRAM backed with Lithium battery; RTC; 1 RS 232 serial line + 1 RS 232 or RS 422-485 or current loop; 16 I/O TTL; 3 timer/counter; watch dog; EEPROM; 11 signals A/D converter with 12 bit resolution; interface for **ABACO®** I/O BUS.

GPC® 114

General Purpose Controller 68HC11

Microprocessor 68HC11A1 at 8 MHz; implementation completely CMOS; serie 4 format; 32K EPROM; 32K SRAM backed with Lithium battery; 32K EPROM, SRAM, EEPROM; RTC; 1 serial line RS 232 or RS 422-485; 10 I/O TTL; 3 timer/counter; watch dog; 8 signals A/D converter with resolution 8 bit; 1 asynchronous serial line; extremely low power consumption; interface for **ABACO®** I/O BUS.

PBI 01

PNP BLOCK Input

Interface for PNP drivers through NPN inputs; 16 inputs for driver PNP, visualized by LEDs; 16 NPN outputs on **ABACO®** standard input connector; Plastic mount for rails DIN 46277-1 and 3.

FBC 20-120

Flat Block Contact 20 vie

Interface for 2 or 1 mounting cable connectors (low profile 20 pins male) and quick release screw terminal connectors; Plastic mount for rails DIN 46277-1 and 3.

FBC 34

Flat Block Contact 34 vie

Interface for 2 mounting cable connector (low profile 34 pins male) and quick release screw terminal connectors; Plastic mount for rails DIN 46277-1 and 3.

FBC L20

Flat Block Contact LED 20 vie

Interface for 1 mounting cable connector (low profile 20 pins male, featuring **ABACO®** standard Input pin out, and quick release screw terminal connectors; All the signals are visualized through LEDs; Plastic mount for rails DIN 46277-1 and 3.

FBC L34

Flat Block Contact LED 34 vie

Interface for 2 mounting cable connectors (low profile 34 and 20 pins male) and quick release screw terminal connectors; featuring **ABACO®** standard Input and Output pin out; All the signals are visualized through LEDs; Plastic mount for rails DIN 46277-1 and 3.

BIBLIOGRAPHY

Here follows a list of manuals and technical notes that the User can read to acquire more informations about **CI/O T16** board.

Manual SGS-THOMSON: *Industrial and Computer Peripheral ICs - Data Book*

Manual SGS-THOMSON: *Programmable logic manual - GAL Products*

Manual TEXAS INSTRUMENTS: *The TTL data Book - SN54/74 Families*

Manual TOSHIBA: *Photo Couplers - Data Book*

Manual MOTOROLA: *Bipolar Power Transistor Data*

Please connect to the manufactures Web sites to get the latest version of all manuals and data sheets.

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