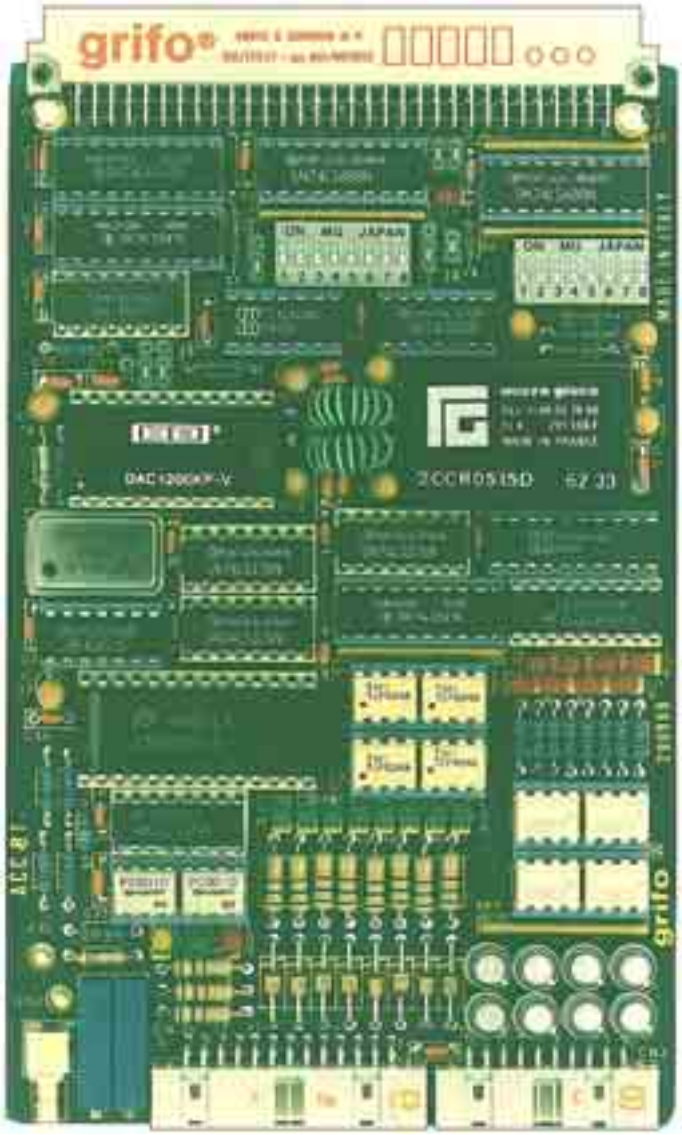
ACC 01

Axis Control Card 1 axis

TECHNICAL MANUAL



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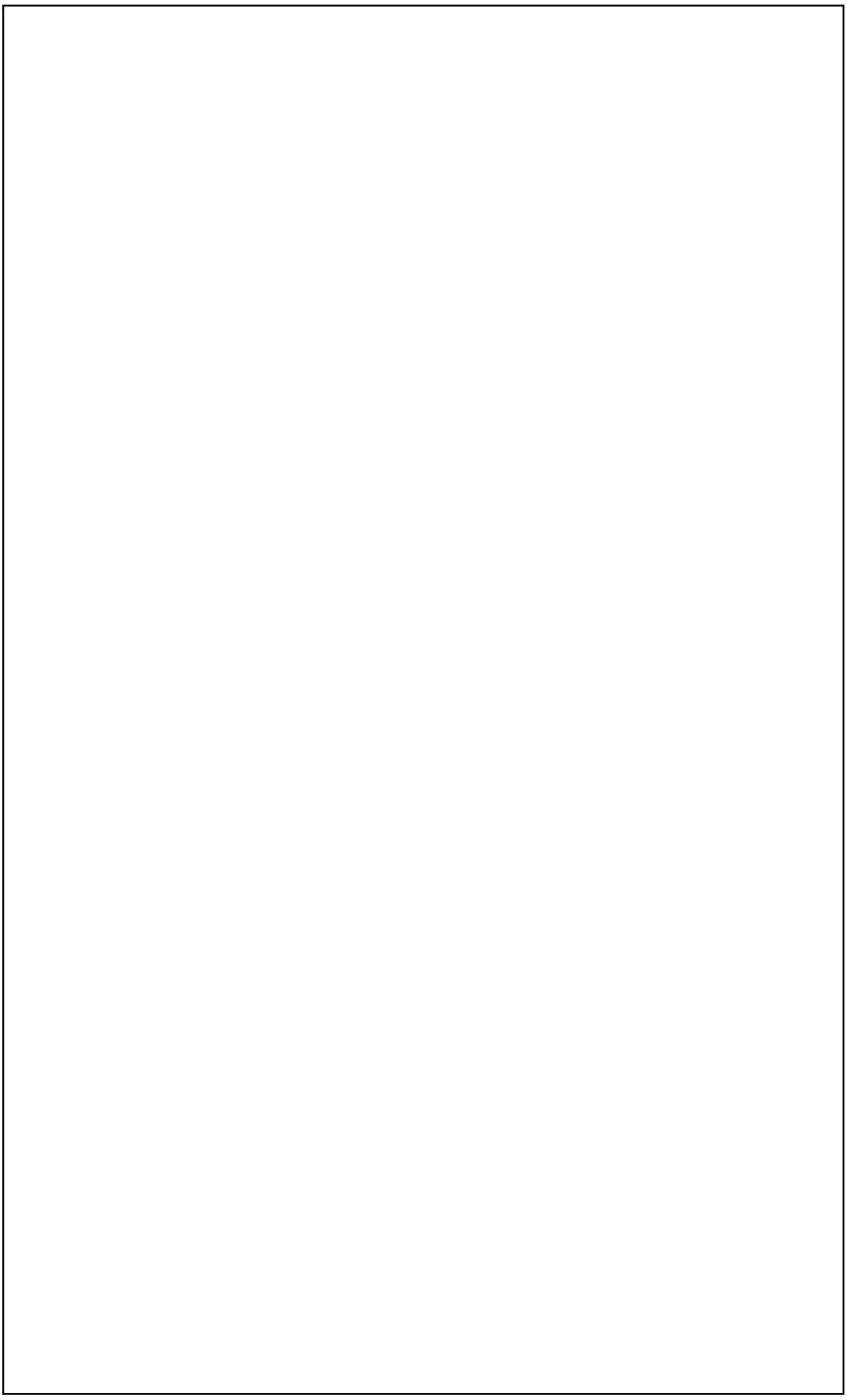

ACC 01

Axis Control Card 1 axis

TECHNICAL MANUAL

Eurocard format board: size: **100** x **160 mm**; interface to industrial **ABACO®** BUS; interface for **bidirectional encoder** with **zero count** signal; encoder acquisition signals, visualized through LEDs, available as: **optocoupled NPN input** for encoder with **open collector** output or **differential** input for encoder with **line drivers** outputs (option **.LD**); decoding **4 quadrature** encoder signals decoded with four-to-one resolution gain of advantage from encoder resolution; maximum encoder speed acquisition **187.5 KHz**; **12 bit** D/A converter with output selectable amongst: ±10; ±5; ±2.5; 0÷5; 0÷10 V; on board **DC/DC** converter to supply **D/A** section; sampling range is **341 µs**; internal **trapezoidal** velocity profile generator; **32 bit** position, velocity and acceleration registers; programmable digital PID filter with **16 bit** coefficients; velocity, target position and filter parameters may be changed **during motion**; real time programmable host **interrupts**, visualized through LED and connectable to interrupt signals of CPU control card; **position** and **velocity** modes of operation; **8 digital optocoupled inputs** visualized through LEDs, supply from **12 to 24 Vdc**; **8 digital optocoupled outputs**, visualized and buffered through open collector transistors, capable to drive a load of **500 mA, 40 Vdc**; **low profile and UHF connectors** to connect field interfacement signals; a total of 20 status LEDs for card visual control; 8 bits data bus, addressing selectable amongst normal (**256 Bytes**), extended (**64 KBytes**) and super extended (**256 KBytes**); unique power supply **+5Vdc** ±5%, **600 mA** max; provided with demo programs that simplify and make faster development of applications with any external system.

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IMPORTANT

Although all the information contained herein have been carefully verified, **grifo®** assumes no responsability for errors that might appear in this document, or for damage to things or persons resulting from technical errors, omission and improper use of this manual and of the related software and hardware.
grifo® reserves the right to change the contents and form of this document, as well as the features and specification of its products at any time, without prior notice, to obtain always the best product.
For specific informations on the components mounted on the card, please refer to the Data Book of the builder or second sources.

SYMBOLS DESCRIPTION

In the manual could appear the following symbols:

Attention: Generic danger

Attention: High voltage

Trade Marks

GENERAL INDEX

FIGURES INDEX

INTRODUCTION

The use of these devices has turned - IN EXCLUSIVE WAY - to specialized personnel.

The purpose of this handbook is to give the necessary information to the cognizant and sure use of the products. They are the result of a continual and systematic elaboration of data and technical tests saved and validated from the manufacturer, related to the inside modes of certainty and quality of the information.

The reported data are destined- IN EXCLUSIVE WAY- to specialized users, that can interact with the devices in safety conditions for the persons, for the machine and for the enviroment, impersonating an elementary diagnostic of breakdowns and of malfunction conditions by performing simple functional verify operations , in the height respect of the actual safety and health norms.

The informations for the installation, the assemblage, the dismantlement, the handling, the adjustment, the reparation and the contingent accessories, devices etc. installation are destined - and then executable - always and in exclusive way from specialized warned and educated personnel, or directly from the TECHNICAL AUTHORIZED ASSISTANCE, in the height respect of the manufacturer recommendations and the actual safety and health norms.

The devices can't be used outside a box. The User must always insert the cards in a container that rispect the actual safety normative. The protection of this container is not threshold to the only atmospheric agents, but specially to mechanic, electric, magnetic, etc. ones.

To be on good terms with the products, is necessary guarantee legibility and conservation of the manual, also for future references. In case of deterioration or more easily for technical updates, consult the AUTHORIZED TECHNICAL ASSISTANCE directly.

To prevent problems during card utilization, it is a good practice to read carefully all the informations of this manual. After this reading, the User can use the general index and the alphabetical index, respectly at the begining and at the end of the manual, to find information in a faster and more easy way.

CARD VERSION

This handbook make reference to card ACC 01 printed circuit version **110293**.
The validity of the information contained in this manual is subordinated to the printerd circuit release number, so the user must always verify the correct correspondence beetween the notations.
Hardware version is printed in several places, for example on the external edge on the component side, near the red LEDs.

GENERAL INFORMATION

ACC 01 is a sophisticated card capable to perform the task to control the velocity profile of an axis through a DC, AC or BRUSHLESS motor actuator.
Communication and programming are made through BUS by one of the several CPU cards compliant with **ABACO®** Industrial BUS and it is reduced to a simple initialization sequence that sets the internal registers and a handy loop that waits the end of the trajectory.
Once the **ACC 01** has been programmed and the Start command has been sent, it is capable to perform the movement profile that has been specified. This is done in complete autonomy and without any intervent from the **CPU** card: the card controls and regulates automatically the acceleration, the speed, the position and the deceleration along the complete movement profile.
The sophisticated on board circuitery allows even to change the parameters of the velocity profile also when **ACC 01** is busy in controllng the axis.
It is possible to decide to change the working conditions, switching to new data, in any moment. This way becomes possible to perform very elaborate velocity profiles assuring the maximum safety about the final results.
Furthermore a group of coefficients, always programmable, allows the activation of a PID control which is capable to mantain the real movement really near to the theoretic one, even if there are external variable elements as the motor loads, the axis inertia, the vibrations, etc.
The tipical use of **ACC 01**, also for its low cost, ranges from the employ in simple positioners to much more complicted industrial numeric controlled systems (CNC).
A great amount of **optocoupled** and **buffered** digital **I/O** resources are already installed on the board. This reduces the minimun number of boards involved in the hardware system that resolves the application even when the common problems related to axis control must be satisfied (i.e. start and stop axis travel, allarms and commands for motor actuator, electric brakes, etc.).
In order to make easy the **ACC 01** interface to the field, there is a serie of **BLOCK** modules **FBC** type which allow to connect the various flat cables to the easy quick screw terminal connectors.

- **Single Eurocard** format size, 100x160 mm.
- Interface to **ABACO®** industrial BUS.
- Interface for **bidirectional encoder** with **zero index** signal.
- Encoder acquisition lines, visualized through **LEDs**, are available as:
  NPN optocpupled inputs for encoder with **open collector** outputs
  differential inputs for encoder with with **line drivers** outputs (**.LD** option)
- **4 quadratures** counting of the encoder pulses equal to a multiplication factor 4 of the encoder resolution
- Maximum encoder acquisition speed **750 KHz** max
- **D/A converter** resolution **12 bit** with selectable output: ±10; ±5; ±2.5; 0÷5; 0÷10 V.
- **DC/DC** converter for D/A section.
- Sample time of **341 μs**.
- Internal **trapezoidal** velocity profile generator.
- **32 bit** registers to decide postion, speed and accelleration.
- **PID** filter (**P**roportional **I**ntegral **D**erivative) with **16 bit** coefficents to optimize the movement profile control.
- Velocity, target position and filter parameters may be changed **during motion**.
- Real time programmable **interrupt**, displayed by LED and connectable to each source of the host control card.
- **Position** range:
  -1.073.741.824 ÷ +1.073.741.823 counts, resolution 1 count.

- **Velocity** range:
  0 ÷ 16.383 counts/sample, resolution of 1/65536 counts/sample.
- **Acceleration** range:
  0 ÷ 16.383 counts/sample/sample, resolution of 1/65536 counts/sample/sample.
- **Derivative sampling** interval unit:
  1 ÷ 256 sample, resolution 1 sample.
- **Proportional** and **integral sampling** interval unit:
  1 sample.
- Two operating modes: **position** and **velocity**.
- **8** digital optocoupled inputs, visualized through **LEDs**, from **12** to **24 Vdc**.
- **8** digital optocoupled outputs, displayed and buffered through open collector transistors capable to drive **500 mA**, **40 Vdc** loads.
- **Low profile** and **miniature UHF** connectors on front side, for a direct interfe to all the external signals.
- **20** status **LEDs** for visual feedback of right card functionality.
- 8 bits data BUS and selectable addressing mode among normal (**256 Bytes**), expanded (**64 KBytes**) and super expanded (**256 KBytes**).
- Single power supply voltage: **5 Vdc ±5%, 600 mA** max.
- Supplied with **demo programs** that simplify and speed the card use with each programmable external systems.

Here follows a description of the board's functional blocks, with an indication of the operations performed by each one.

CLOCK DEVICE

ACC 01 is provided with an on board clock circuitery section capable to generate the synchronization signal required by the peripherals.
This allows to use the board matched to any CPU card regardless of its speed.
This circuitery is based on a 24 MHz oscillator used to generate a 6 MHz frequency for controller LM 628.

CONTROL LOGIC

This section generates all the chip select signals essential to access the **ACC 01** on board peripherals. It allows the programmer to reach the board devices and check their status, read the digital inputs and outputs, use the motion controller LM 628, etc.
The control logic interfaces to **ABACO® Industrial BUS** through the addressing and interfacement section, the BUS connection allows an easy software management of al the sections.
For further information please refer to chapter “SOFTWARE DESCRIPTION”.

ADDRESSING AND INTERFACEMENT SECTION

This section manages the information interchange between control logic and external **GPC®** control cards. In detail, it controls I/O mapping through two comfortable dip switches (DIP1 and DIP2), each byte read or written passes through this section.
In fact this section can be configured to address **ACC 01** in a 256 bytes up to 256Kbytes I/O addressing range.
The **ABACO® Industrial BUS** interfacement has been designed anticipating an 8 bits data path.
For further information please refer to chapter "ADDRESSES AND MAPS".

MOTION CONTROLLER LM 628

Thia is the core section of **ACC 01**; it generates the velocity profile required by the user for the axis to control.
The contol loop takes the trajectory as input, uses D/A as actuative output and takes the encoder output as feedback input.
Velocity profile can be completely programmed by software by providing the following parameters: acceleration, speed, position and deceleration that are the theorical target control values to obtain.
Since when motion starts, LM 628 performs sampling at regualar intervals (341 μsec) to decide in which point of trajectory the system is, detects the real point through encoder and calculates the error.
Such error, after filtering and elaboration, is used to set the D/A output that generates the real trajectory.
Error is elaborated and filtered with a PID, parametrized with coefficents that can be programmed by software.
In addition, LM 628 can operate in two different modalities that fulfil all requirements of industrial systems: position (trajectory is controlled through positions that must be reached) and velocity (trajectory is controlled through speed that must be kept).
Management of LM 628 is software managed through two bytes addressed as decided by the user according to instructions in chapter "ADDRESSES AND MAPS".
For further information about parameters, controller initialization, correction coefficents, theory of operation, interrupt, etc. please refer to manufacturer documentation, as indicated in "APPENDIX A" of this manual.

D/A CONVERTER

This section features one D/A Converter signal, based on as many **DAC80P**, warranting a high linearity and a remarkable driving capability.
Analog circuitry is capable to generate the signal that controls the motor motion.
Of course, this signal can't be connected directly to the motor, it must be provided to an interface card (continuous current, brushless, inverter, etc.) compliant to the kind of motor that drives the axis.
ACC 01 in fact, does not provide power outputs but the control signal.
Voltage of this signal can be set in one of 5 different ranges up to ±10 V through a specific 7 pins jumper.
This peripheral is managed directly by the LM 628 motion controller so the user interacts with it indirectly through the speed and acceleration parameters of this latter.

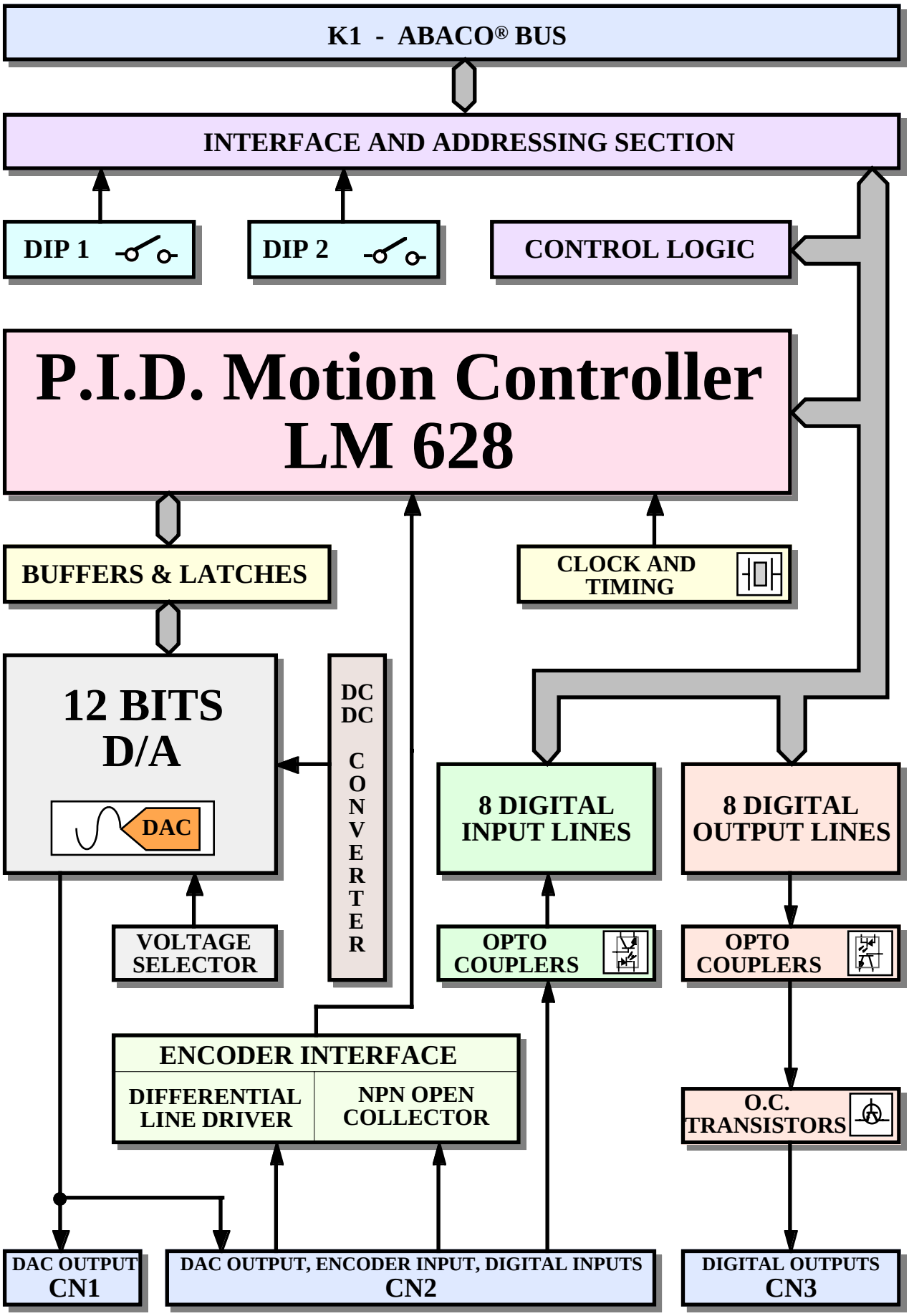


FIGURE 1: BLOCK DIAGRAM

DC/DC CONVERTER SECTION

ACC 01 features an on board positive booster whose task is to provide all the supply voltages needed by the digital-to-analog conversion section.
This component generates two ±15 V voltages from the unique +5 Vdc board supply voltage and needs no software management.

ENCODER INTERFACE

This section features a circuitery that acquires, conditions and transforms the three signals provided by and incremental bidirectional encoder (phase A, phase B and an optional index count).
Electrically, the section can be configured in two different standard modes: for encoders with NPN open collector outputs, which provided optocoupled inputs and visualized through LEDs, or for encoders with line driver outputs, which provided optocoupled differential inputs.
The modalities mutually exclude, so only one can be installed, but in both cases encoder outputs must fetaure the typical 90° phase displacement and the optional index count signal must be active low.
The user can choose the best encoder for one's application always verifying the parameters in chapter "TECHNICAL FEATURES" are respected.
Please remark that differential interface is optional, this means not installed if not specified in order phase. In detail, the card can be:

default version	->	open collector encoder interface
.LD version	->	line driver encoder interface

DIGITAL INPUTS

This section features 4 digital input lines, software acquirable through a specific butter, allocated on a specific address accoding to the instructions of chapter "ADDRESSES AND MAPS".
Each input signal is galvanically isolated and type NPN, it is visualized by its own green LED, power supply for optocouplers can vary in the range +12÷24 Vdc.
Typical applications of digital inputs are: start and stop buttons acquisition, alarm signals from motor interface card, axis stroke end signal, etc.

DIGITAL OUTPUTS

This section features 8 digital output signals, software settable, through a specific latch allocated on a specific address accoding to the instructions of chapter "ADDRESSES AND MAPS".
Each output signal is galvanically isolated, visualized by its own red LED and drives an open collector transistor that can bear a maximum resistive load of +40 Vdc, 500 mA.
Typical applications are: motor interface card control, electric brakes control, etc.

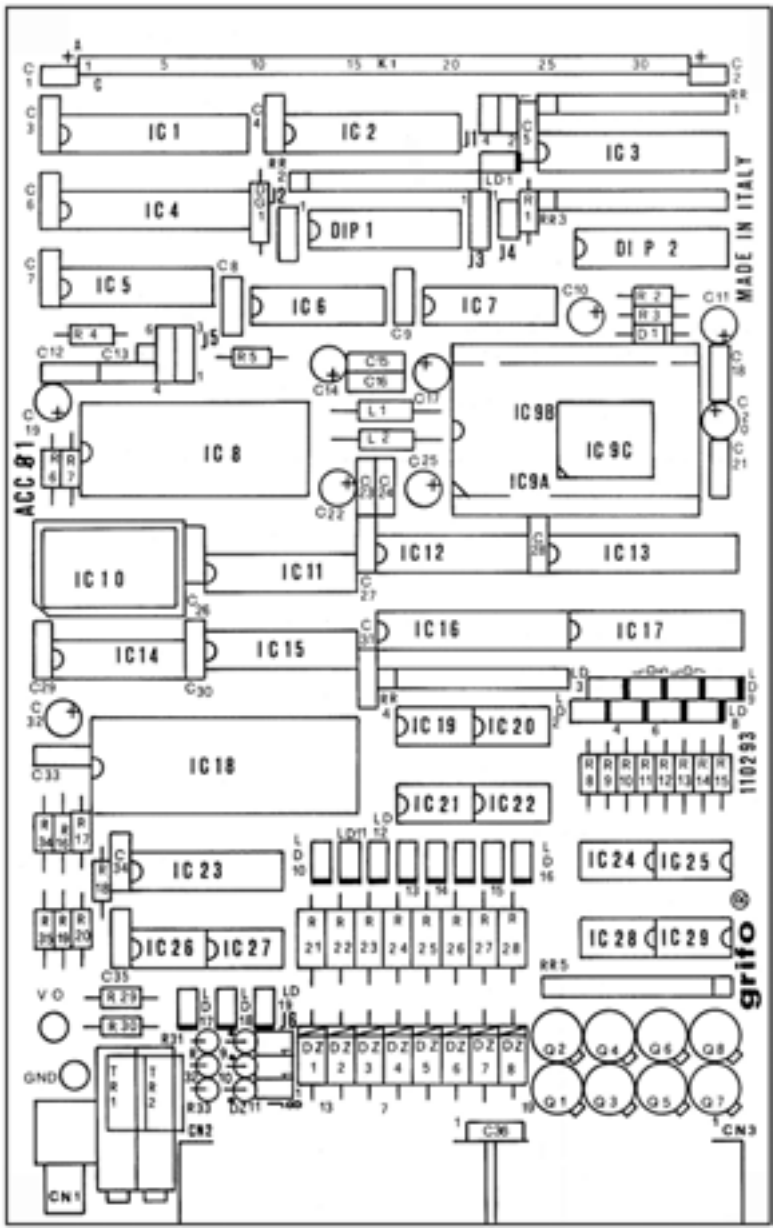


FIGURE 2: COMPONENTS MAP (COMPONENTS SIDE)

TECHNICAL FEATURES

GENERAL FEATURES

BUS type:	**ABACO®**
Addressable Range:	256 (normal) 64 K (extended) 256 K (super extended)
Bytes taken:	4
On Board Resources:	1 motion controller PID, LM 628 1 input for bidirectional incremental encoder 1 analogic output with range selectable up to ±10 V 8 digital optocoupled inputs 4 transistor digital optocoupled outputs 2 dip switch for mapping with 8 dips 20 status LEDs
Clock frequency of LM 628:	6 MHz
Sampling time:	341 μsec
Reset time:	1 msec
Power on time:	40 msec
Precision on position:	1/4 encoder impuls
D/A settling time:	4 μsec

PHYSICAL FEATURES

Size:	Eurocard standard format 100 x 160 mm
Weight:	180 g max
Connectors:	K1: DIN 41612, 64 pins, male, 90 degreeses, A+C type C CN1: Mini UHF, male, 90 degreeses (type SMB) CN2: low profile 26 pins, male, 90 degreeses CN3: low profile 20 pins, male, 90 degreeses
Temperature range:	From 0 to 70 °C
Relative humidity:	20% up to 90% (without condense)

ELECTRIC FEATURES

Power supply:	+5 Vdc ±5%.	
Current consumption:	600 mA max	
Open collector encoder input voltage:	+V opto ENC = +12 or +24 Vdc	(*)
Open collector encoder input current:	15 mA +V opto ENC=+12 or +24 Vdc	(*)
Open collector encoder input cut-off frequency:	112 KHz	(*)
Line driver encoder input voltage:	±7 Vdc	
Line driver encoder input current:	±1,5 mA	(*)
Line driver encoder input cut-off frequency:	187,5 KHz	
D/A output voltage ranges:	±2.5; ±5; ±10; 0÷5; 0÷10 V	
D/A output current:	±5 mA	
Digital transistor outputs maximum current:	500 mA	(*)
Digital transistor outputs maximum voltage:	40 Vdc	(*)
Digital transistor outputs maximum power:	0.5 W	(*)
Digital inputs voltage:	+V opto = +12÷24 Vdc	(*)
Digital inputs current:	5 mA +V opto=+12 Vdc 12 mA +V opto=+24 Vdc	(*) (*)
Digital inputs cut-off frequency:	7 KHz	(*)

(*) Values referred to 20 °C working temperature

INSTALLATION

In this chapter there are the information for a right installation and correct use of **ACC 01**.
In detail there are the locations and functions of each connector, of the user settable jumpers and dip switches, etc.

CONNECTIONS

ACC 01 has 4 connectors that can be linkeded to other devices or directly to the field, according to system requirements.
In this paragraph there are connectors pin out, a short signals description (including the signals direction) and connectors location (see figure 8).

D/A SHIELDED ANALOG OUTPUT CONNECTOR

The D/A analog output connector is a coaxial UHF sub miniature gold plated male 90° connector, belonging to **SMB** serie.
This kind of connector, matched to its female part, assures a strong mechanical connections and a very low contact resistance.
The connector features analog output and its ground, which acts also as shielding.

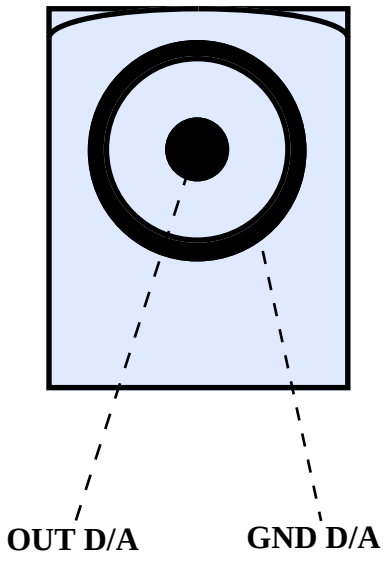


FIGURE 3: CN1 - D/A ANALOG OUTPUT CONNECTOR

Signals description:

OUT D/A = O - Digital to analog converter output signal.
D/A GND = - Ground and shileding of analog output signal.

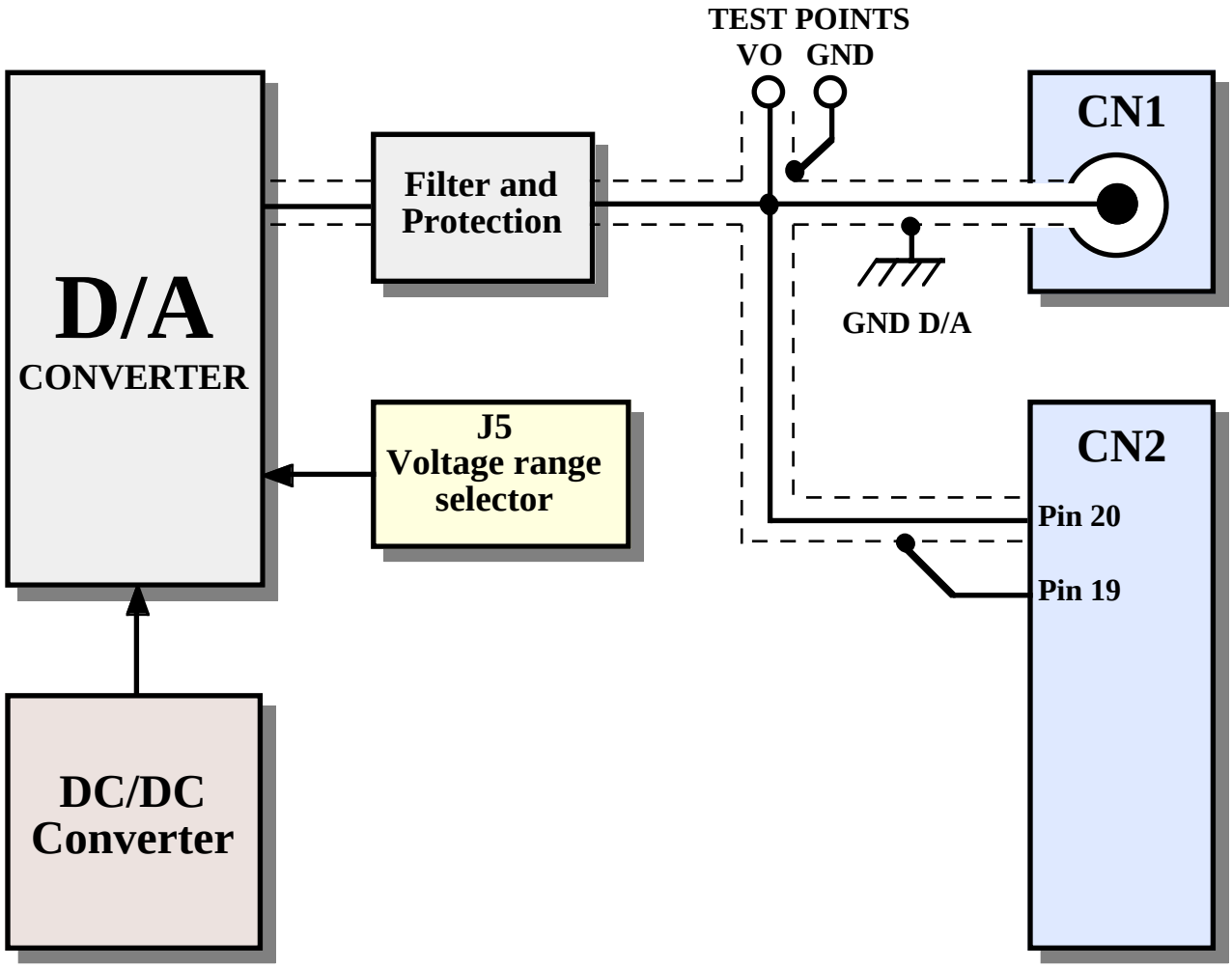


FIGURE 4: D/A SECTION BLOCK DIAGRAM

CN2 - ENCODER, ANALOG OUTPUT AND DIGITAL INPUS CONNECTOR

CN2 is a 26 pins, low profile, 90 degreeses, male connector with 2.54 mm pitch.
CN2 connects **ACC 01** to the incremental bidirectional encoder (both open collector and line driver), the motor interface card (through D/A converter analog output) and the eventual 8 optocoupled digital inputs.
CN2 signal displacement has been designed to reduce interferences and to easy external cabling; this latter can be made using module **FBC 126**, to interface this connector via comfortable quick release screw terminal connectors.

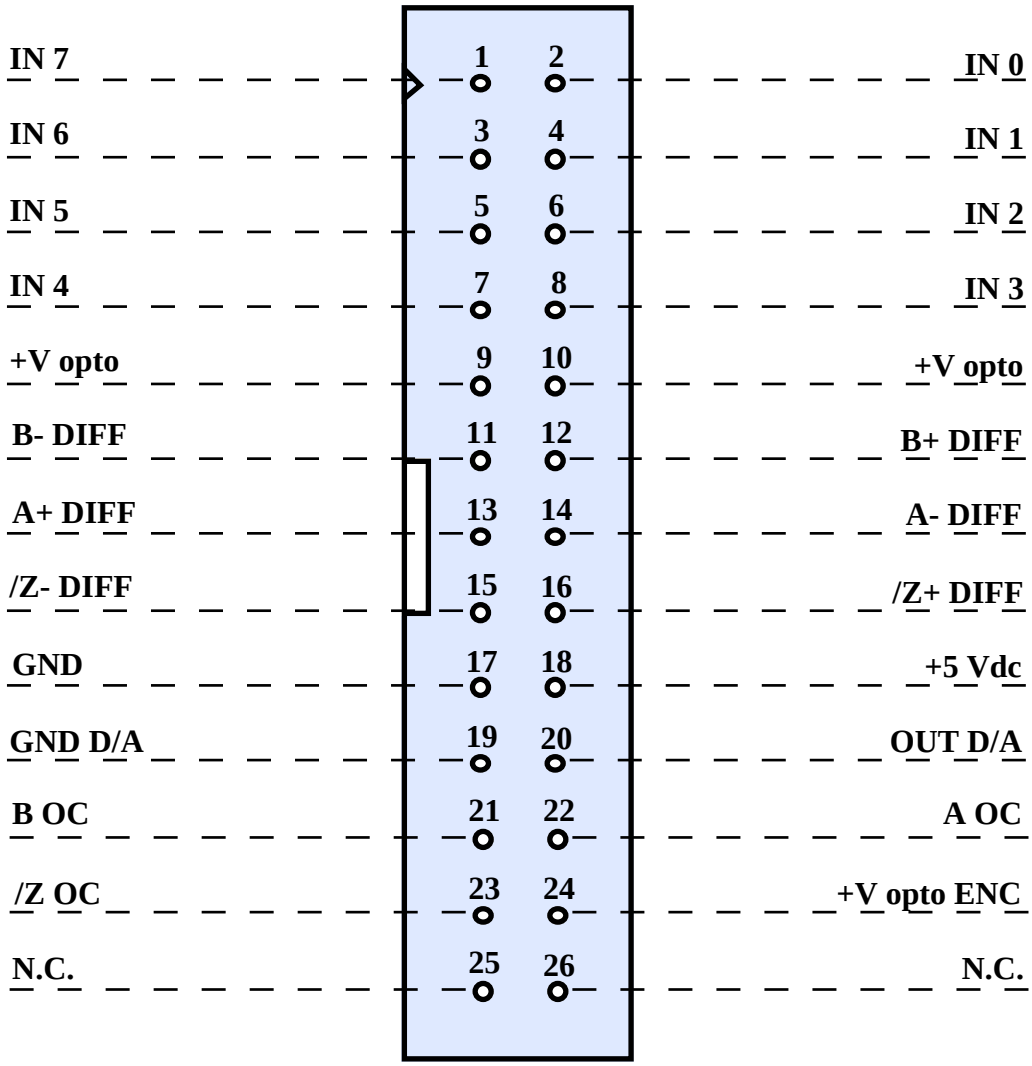


FIGURE 5: CN2 - ENCODER, ANALOG OUTPUT AND DIGITAL INPUTS CONNECTOR

Signals description:

IN n	=	I - n-th, optocoupled NPN digital input
+V opto	=	I - NPN optocoupled digital input power supply
B- DIFF	=	I - Negative differential signal of line driver phase B of encoder
B+ DIFF	=	I - Positive differential signal of line driver phase B of encoder
A- DIFF	=	I - Negative differential signal of line driver phase A of encoder
A+ DIFF	=	I - Positive differential signal of line driver phase A of encoder
/Z- DIFF	=	I - Negative differential signal of line driver eventual zero index of encoder

/Z+ DIFF	=	I	- Positive differential signal of line driver eventual zero index of encoder
B OC	=	I	- Optocoupled signal of phase B of encoder
A OC	=	I	- Optocoupled signal of phase A of encoder
/Z OC	=	I	- Optocoupled signal of eventual zero index of encoder
+V opto ENC	=	I	- Power supply of open collector encoder signals
OUT D/A	=	O	- D/A converter analog output signal
GND D/A	=		- Ground of analog output signals
+5 Vdc	=	O	- Power supply +5 Vdc
GND	=		- Ground of digital signals
N.C.	=		- Not connected

Digital inputs available on the card are optocoupled and are provided with an amplitude cut-off circuitery that warrants internal electionic protection against noise from external world and allow to acquire both inputs supplied with +12 and +24 Vdc.
Each line features a LED for visual signalation (LED is ON when input IN is connected to opto GND, the ground of galvanically isolated voltage +Vopto).
Inputs support normally open **NPN** contacts, an opportune converions module must be used to support **PNP** contacts.

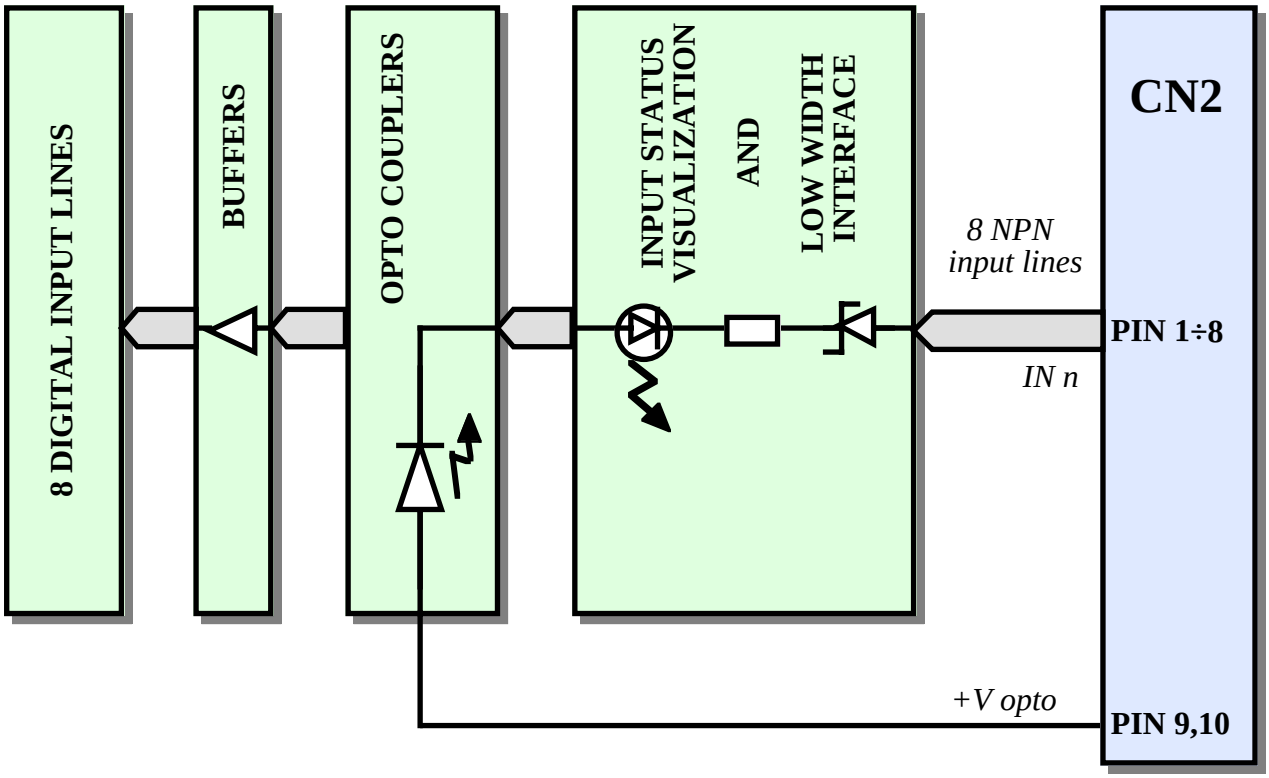


FIGURE 6: OPTOCOUPLED DIGITAL INPUTS BLOCK DIAGRAM

To connect digital inputs, please refer to above diagram and to specifications in “ELECTRIC FEATURES” paragraph.

Encoder input can be open collector (default version) or differential line driver (option **.LD**). Only one of the two interfaces can be installed on the card, so required configuration must be specified in the order to allow **grifo®** to install and test the components.

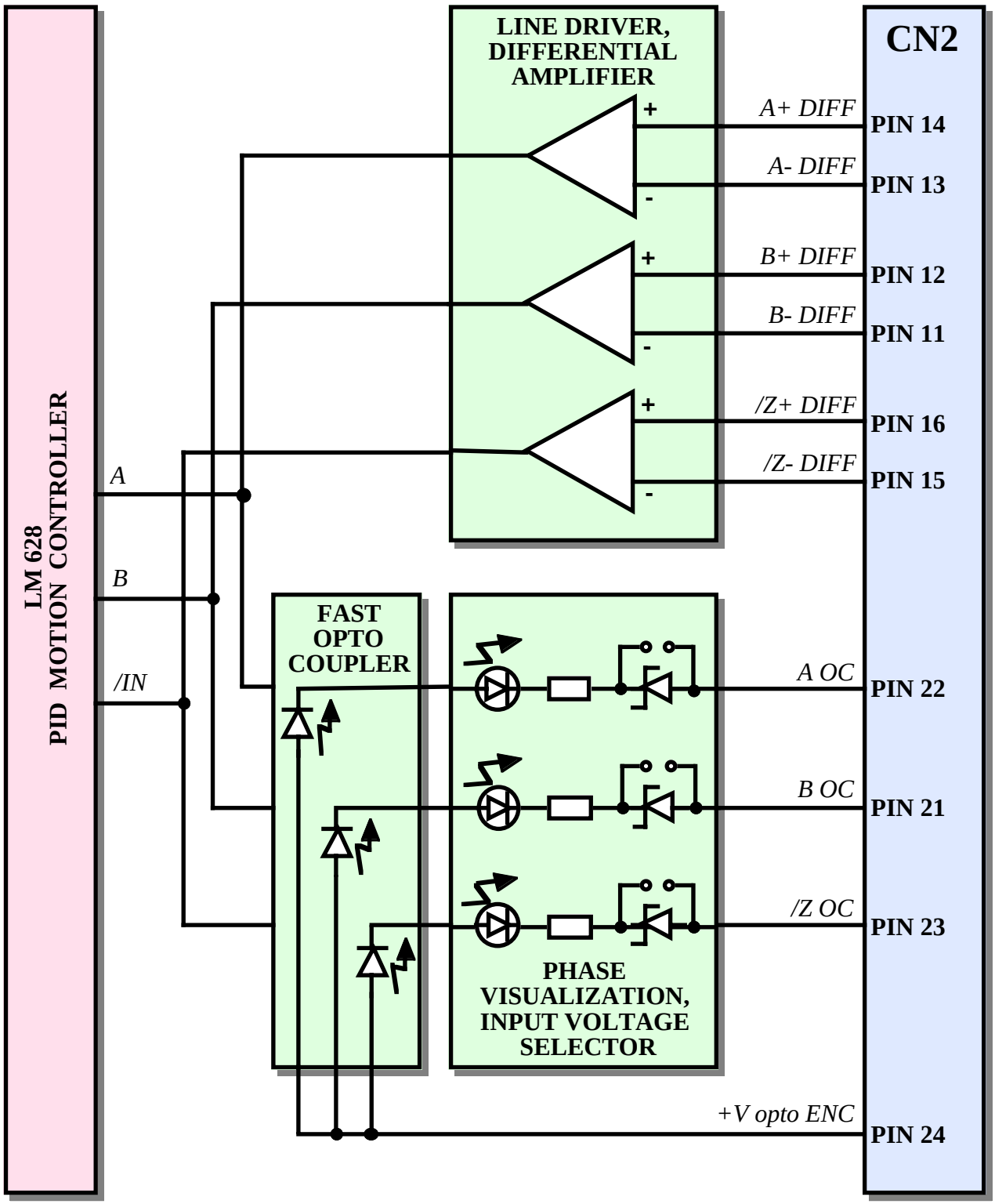


FIGURE 7: ENCODER INPUTS BLOCK DIGRAM

To connect encoder inputs, please refer to above diagram and to specifications in “ELECTRIC FEATURES” paragraph.

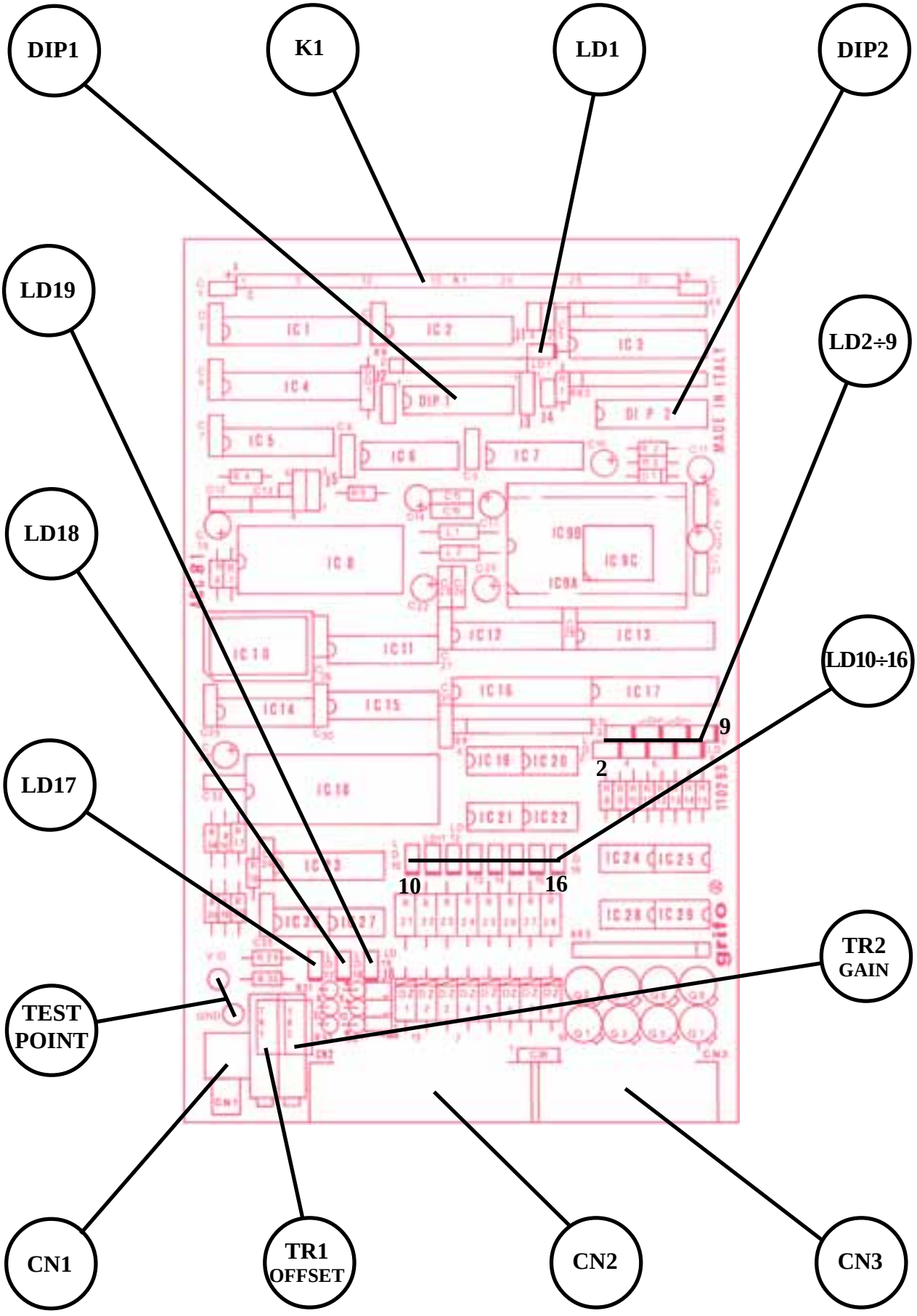


FIGURE 8: CONNECTORS, LEDS, DIP SWITCHES, ETC. LOCATION

CN3 - DIGITAL OUTPUTS CONNECTOR

CN3 is a 20 pins, low profile, 90 degreeses connector with 2.56 pitch.
Connector features open collector output signals and the common (emitter) of the 8 NPN transistor.
CN3 signal displacement has been designed to reduce interferences and to easy external cabling; this latter can be made using module **FBC 120**, to interface this connector via comfortable quick release screw terminal connectors.

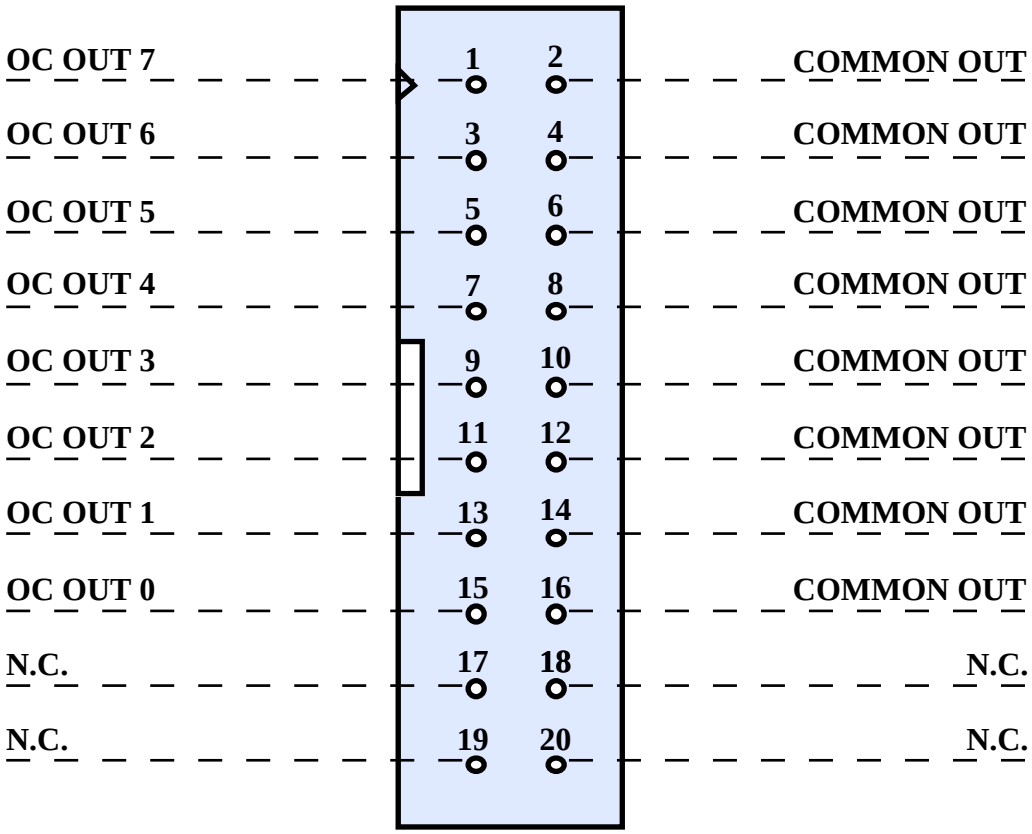


FIGURE 9: CN3 - DIGITAL OUTPUTS CONNECTOR

Signals descritpion:

OC OUT n	= O	- n-th contact of NPN open collector transistor output.
COMMON OUT	=	- Common emitter of digital output transistors.
N.C.	=	- Not connected.

Transistor digital output signals available on **ACC 01** are provided with one LED for visual signalations (LED is ON when transistor is conducting); in addition they are optocoupled to warrant galvanic separation between internal electronics and external world.
Final stage of outputs is a NPN open collector transistor whose parameters are reported in "ELECTRIC FEATURES" paragraph with common emitters: so all loads must be supplied by the same tension.
Further information are available from the following picture:

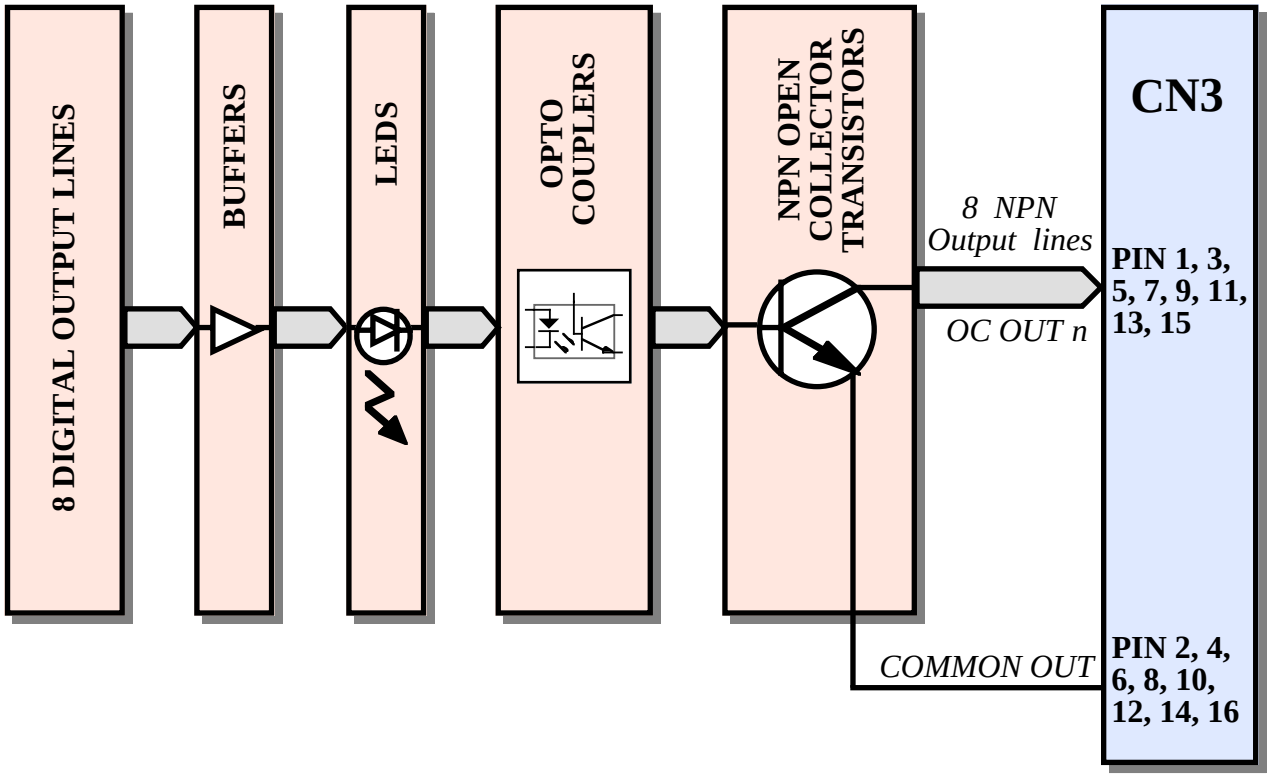


FIGURE 10: DIGITAL OUTPUTS BLOCK DIAGRAM

Lines are not provided with a suppression diode, to crunch inductive tensions produced by an inductive load like power relays, solenoids, etc.
In such cases an external protection diode must be connected between output and load power supply.

K1 - CONNECTOR FOR ABACO® BUS

The connector for **ABACO® industrial BUS**, called K1 on the board,is a DIN 41612, male, a 90 °, type C, A+C.
Here follows the pin-out of the connector installed on **LDA 01**, in addition there is the standard 8 bits and 16 bits**ABACO®** BUS pin-out.
Please remark that all the signals here described are TTL, except for the power supplies.

Row A 16 bit BUS	Row A 8 bit BUS	K1 A ACC 01	PIN	K1 C ACC 01	Row C	Row C 16 bit BUS
GND	GND	GND	1	GND	GND	GND
+5 Vdc	+5 Vdc	+5 Vdc	2	+5 Vdc	+5 Vdc	+5 Vdc
D0	D0	D0	3	N.C.	-	D8
D1	D1	D1	4	N.C.	-	D9
D2	D2	D2	5	N.C.	-	D10
D3	D3	D3	6	/INT	/INT	/INT
D4	D4	D4	7	/NMI	/NMI	/NMI
D5	D5	D5	8	N.C.	/HALT	D11
D6	D6	D6	9	N.C.	/MREQ	/MREQ
D7	D7	D7	10	/IORQ	/IORQ	/IORQ
A0	A0	A0	11	/RD	/RD	/RDLDS
A1	A1	A1	12	/WR	/WR	/WRLDS
A2	A2	A2	13	N.C.	/BUSAK	D12
A3	A3	A3	14	N.C.	/WAIT	/WAIT
A4	A4	A4	15	N.C.	/BUSRQ	D13
A5	A5	A5	16	/RESET	/RESET	/RESET
A6	A6	A6	17	/M1	/M1	/IACK
A7	A7	A7	18	N.C.	/RFSH	D14
A8	A8	A8	19	N.C.	/MEMDIS	/MEMDIS
A9	A9	A9	20	N.C.	VDUSEL	A22
A10	A10	A10	21	N.C.	/IEI	D15
A11	A11	A11	22	N.C.	-	-
A12	A12	A12	23	N.C.	CLK	CLK
A13	A13	A13	24	N.C.	-	/RDUDS
A14	A14	A14	25	N.C.	-	/WRUDS
A15	A15	A15	26	N.C.	-	A21
A16	-	A16	27	N.C.	-	A20
A17	-	A17	28	N.C.	-	A19
A18	-	N.C.	29	N.C.	/R.T.	/R.T.
+12 Vdc	+12 Vdc	N.C.	30	N.C.	-12 Vdc	-12 Vdc
+5 Vdc	+5 Vdc	+5 Vdc	31	+5 Vdc	+5 Vdc	+5 Vdc
GND	GND	GND	32	GND	GND	GND

FIGURE 11: K1 - CONNECTOR FOR ABACO® BUS

Signals description:

8 bits CPU

A0-A15	=	O	- Address BUS
D0-D7	=	I/O	- Data BUS
INT	=	I	- Interrupt request
NMI	=	I	- Non Maskable Interrupt
HALT	=	O	- Halt state
MREQ	=	O	- Memory Request
IORQ	=	O	- Input Output Request
RD	=	O	- Read cycle status
WR	=	O	- Write cycle status
BUSAK	=	O	- BUS Acknowledge
WAIT	=	I	- Wait
BUSRQ	=	I	- BUS Request
RESET	=	O	- Reset
M1	=	O	- Machine cycle one
RFSH	=	O	- Refresh for dynamic RAM
MEMDIS	=	I	- Memory Display
VDUSEL	=	O	- VDU Selection
IEI	=	I	- Interrupt Enable Input
CLK	=	O	- System clock
R.B.	=	I	- Reset button
+5 Vdc	=	I	- Power supply at +5 Vdc
+12 Vdc	=	I	- Power supply at +12 Vdc
-12 Vdc	=	I	- Power supply at -12 Vdc
GND	=		- Ground signal

16 bits CPU

A16-A22	=	O	- Address BUS
D8-D15	=	I/O	- Data BUS
RD UDS	=	O	- Read Upper Data Strobe
WR UDS	=	O	- Write Upper Data Strobe
IACK	=	O	- Interrupt Acknowledge
RD LDS	=	O	- Read Lower Data Strobe
WR LDS	=	O	- Write Lower Data Strobe

NOTE
Directionality indications as above stated are referred to a master (**GPC®**) board and have been kept untouched to avoid ambiguity in case of multi-boards systems.

I/O CONNECTIONS

To prevent possible connecting problems between **ACC 01** and the external systems, the user has to read carefully the previous paragraph information and must follow these instrunctions:

- For all TTL signals the user must follow the rules of this electric standard. The connected digital signal must be always referred to card digital ground and if an electric insulation is necessary, then an opto coupled interface must be connected. For TTL signals, the 0V level corresponds to logic state 0, while 5V level corrisponds to logic state 1.

- The optocoupled digital inputs must be connedted to the contacts to acquire and its power supply. These contacts (relays, stroke end, swithces, etc.) must connect or not connect the input signal IN x to GND opto, which is reference ground for optocouplers power supply +V opto.

- The NPN transistors output signals must be connected directly to the load to drive (power relays, etc.). The board provides an unique common terminal (COMMON OUT) for them all, so all loads must be supplied with the same voltage. Plese refer also to paragraph “DIGITAL OUTPUTS”.

- The analog outputs can erogate a maximum current of ±5 mA; for this reason they must be connected only to external circuits featuring a high impedance, which warrants not to exceed such current limit across the whole output range. Eventual connections to power actuators (motors), must be made through a specific power driver circuits, e.g., activation or inverter.

- Open collector encoder input signals must be connected to the two phases, and the eventual zero index, with their own power supply. So the encoder will have to connect or not connect input signal x OC to optocoupled ENC GND, that is reference ground of +V opto ENC.

- Line driver encoder input signals must be connected to the two phases only, and the eventual zero index. Power supply of encoder, of course, will have to be external, but this latter must be not connected to **ACC 01**.

- Both Open collector and line driver encoder input signals connections should be shielded and short, to avoid interferences especially when using encoders with a very high resolution.

- Encoders that can be connected are bidirectional, incremental with optional zero index signal active low. Regardless electric standard, the signals will have to feature following waveforms:

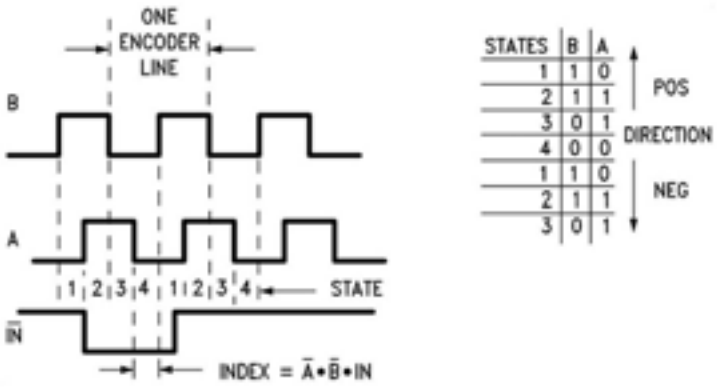


FIGURA 12: WAVEFROMS OF BIDIRECTIONAL INCREMENTAL ENCODER SIGNALS

VISUAL SIGNALATIONS

ACC 01 features 20 LEDs described in the following table:

LED	COLOUR	PURPOSE
LD1	Red	It turns ON when ACC 01 sends an interrupt request to master CPU card on BUS **ABACO®**.
LD2÷LD9	Red	They show the status of 8 digital outputsi OC OUT 0÷7: a LED ON indicates that open collector output relative to COMMON OUT common pin is closed.
LD10÷LD16	Green	They show the status of 8 digital inputsi IN 0÷7: a LED ON indicates that the corresponding input is connected to +V opto.
LD17	Yellow	Shows the zero count pin (/Z OC) status of open collector encoder connected to CN2: the LED indicates that the input is connected to +V opto ENC.
LD18	Green	Shows the phase A signal (A OC) status of open collector encoder connected to CN2: the LED indicates that the input is connected to +V opto ENC.
LD19	Red	Shows the phase B signal (B OC) status of open collector encoder connected to CN2: the LED indicates that the input is connected to +V opto ENC.

FIGURE 13: LEDS TABLE

The main function of LEDs is to inform the user about card status, with a simple visual indication and in addition to this, LEDs make easier the debug and test operations of the complete system.
To recognize the LED location on the card, please refer to figure 8.

RESET AND POWER ON

When the /RESET signal coming from **ABACO®** BUS is actived the board outputs will be set to their initial status (transistors disengaged, motion controlloer stopped and ready for a new velocitiy profile, analog outputs to half range.
Please remark that reset procedure takes 1 msec for /RESET signal and 40 msec in case of power on, so the control card must wait for this time before communicating to **ACC 01**.

JUMPERS

On **ACC 01** there are 8 jumpers for card configuration.
Here below is the jumpers list, location and function:

JUMPER	N° PINS	PURPOSE
J1	4	Allows super extended address mapping on BUS **ABACO®**.
J2	3	Connects board interrupt request to BUS **ABACO®**.
J3	3	Selects normal, extended or super extended addressing mode on BUS **ABACO®**.
J4	2	Enables signal /M1 coming from BUS **ABACO®**.
J5	7	Selects D/A converter output voltage range.
J6, J7, J8	2	Selects +V opto ENC power supply voltage for open collector encoder input.

FIGURE 14: JUMPERS SUMMARIZING TABLE

The following tables describe all the right connections of **ACC 01** jumpers with their relative functions.
To recognize these valid connections, please refer to the board printed diagram (serigraph) or to figures 2 and 20 of this manual, where the pins numeration is listed; for recognizing jumpers location, please refer to figure 16 again.
The "*" denotes the default connection, or on the other hand the connection set up at the end of testing phase, that is the configuration the user receives.

3 PINS JUMPERS

JUMPER	CONNECTION	PURPOSE	DEF.
J2	not connected	Does not connect on board interrupt request signal to BUS **ABACO®**.	*
	position 1-2	Connects on board interrupt request signal to /NMI signal of BUS **ABACO®**.	
	position 2-3	Connects on board interrupt request signal to /INT signal of BUS **ABACO®**.	
J3	position 1-2	Selects 64 KBytes extended addressing mode or 256 KBytes super extended addressing mode.	
	position 2-3	Selects 256 Bytes normal addressing mode.	*

FIGURE 15: 3 PINS JUMPERS TABLE

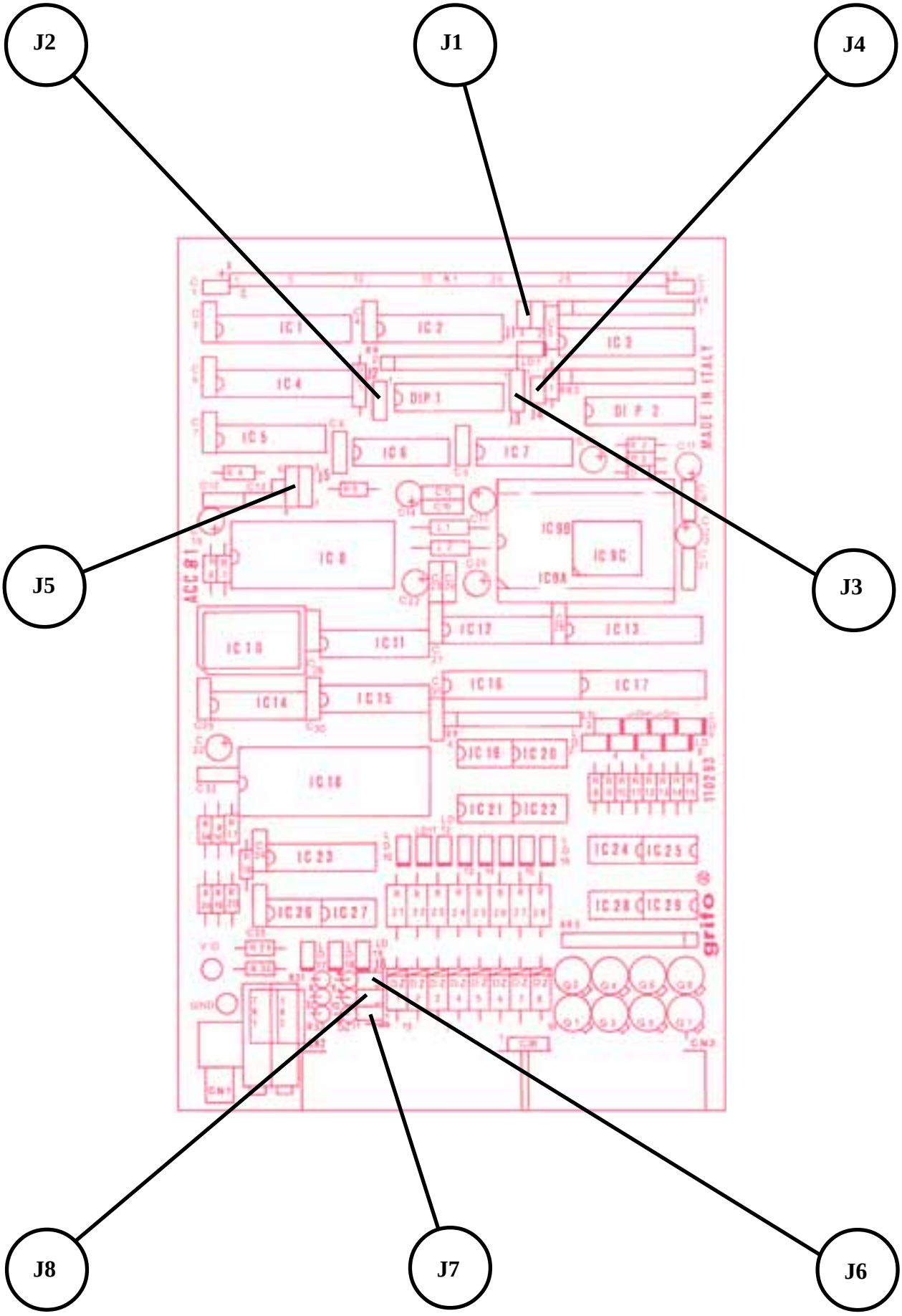


FIGURE 16: JUMPERS LOCATION

2 PINS JUMPERS

JUMPER	CONNECTION	PURPOSE	DEF.
J4	not connected	BUS **ABACO®** interface section does not manage signal /M1	*
	connected	BUS **ABACO®** interface section manages signal /M1	
J6	not connected	Configures zero count input signal (/Z OC) of open collector encoder, for +24 Vdc supply voltage.	*
	connected	Configures zero count input signal (/Z OC) of open collector encoder, for +12 Vdc supply voltage.	
J7	not connected	Configures input for phase A (A OC) of open collector encoder, for +24 Vdc supply voltage.	*
	connected	Configures input for phase A (A OC) of open collector encoder, for +12 Vdc supply voltage.	
J8	not connected	Configures input for phase B (B OC) of open collector encoder, for +24 Vdc supply voltage.	*
	connected	Configures input for phase B (B OC) of open collector encoder, for +12 Vdc supply voltage.	

FIGURE 17: 2 PINS JUMPERS TABLE

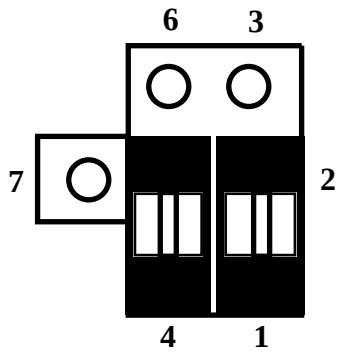
4 PINS JUMPERS

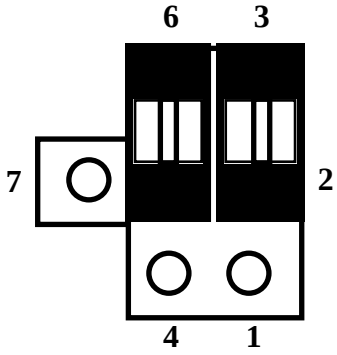
JUMPER	CONNECTION	PURPOSE	DEF.
J1	not connected	Does not connect addres signals A16 and A17 to BUS **ABACO®** interface section, so super extended addressing mode is not allowed.	*
	position 1-2	Connects addres signal A16 to BUS **ABACO®** interface section, so 128 KBytes super extended addressing mode can be used.	
	position 1-2 and 3-4	Connects addres signal A16 and A17 to BUS **ABACO®** interface section, so 256 KBytes super extended addressing mode can be used.	

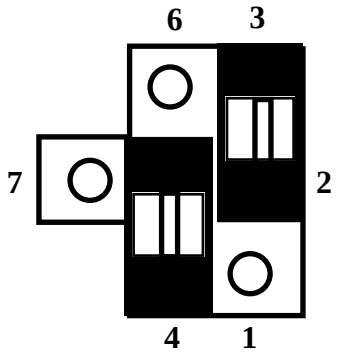
FIGURE 18: 4 PINS JUMPERS TABLE

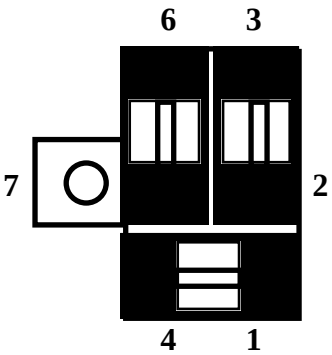
7 PINS JUMPERS

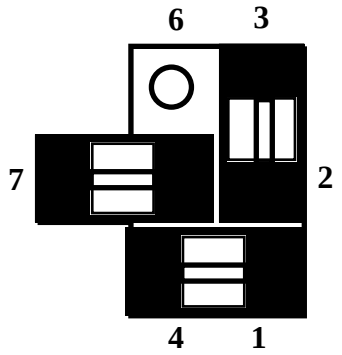
7 pins jumper, called J5, allows to configure output voltage range of D/A converter.
To easy its configuration, possible combination are shown in pictures.
Other combinations are forbidden.

<table>
<tr>
<td> 

Voltage range: ± 10 Vdc
Position: 1-2, 4-5 (DEFAULT)</td>
<td> 

Voltage range: 0÷10 Vdc
Position: 2-3, 5-6</td>
</tr>
<tr>
<td> 

Voltage range: ± 5 Vdc
Position: 2-3, 4-5</td>
<td> 

Voltage range: 0÷5 Vdc
Position: 1-4, 2-3, 5-6</td>
</tr>
<tr>
<td> 

Voltage range: ± 2.5 Vdc
Position: 1-4, 2-3, 5-7</td>
<td></td>
</tr>
</table>

FIGURE 19: 7 PINS JUMPERS TABLE

POWER SUPPLY

ACC 01 is provided with an efficent circuitery that solves in a comfortable and simple way the problem of the board's supply, under any condition of use.
Here follow the voltages nedded:

+5 Vdc, GND: must be in the range +5 Vdc ± 5% and must be provided through the specific pins of connector K1 (**ABACO®** BUS).
Board layout is designed to take supply from K1 and distribute it to all the circuitery; this explains directionality in signals description. In case of particular needs the user can try to supply the card through +5 Vdc output pins, but must be very careful. Distributed fiters improve noise immunity.
A positive booster is charged to provide the voltages needed by the digital to analog conversion section. Such DC/DC converter generates two ±15 Vdc voltages starting from the unique +5 Vdc power supply and needs no software management.
Ground of D/A section has been called GND D/A to distinguish it from supply GND, even if they are connected.

+V opto, **GND opto**: optocoupled digital input must be supplied by a +12÷24 Vdc voltage provided through specific pins of CN2.

+V opto ENC, **GND opto ENC**: optocoupled inputs of open collector encoder must be supplied by a +12÷24 Vdc voltage provided through specific pins of CN2.
According to encoder type and its power supply, jumpers J6, J7 and J8 must be opportunely configured.

To warrant great immunity to external noise and so a correct working of the board, it is essential that **all the three voltages, or at least +5 Vdc** tension is galvanically isolated.
Complete technical features are listed in paragraph “ELECTRIC FEATURES”.

TEST POINT

The board is provided with 2 test points called **VO** and **GND**, that allow to read, through a galvanically isolated multimeter, the output voltages of the digital to analog conversion sections. Their purpose is to make possible a monitoring of the analog outputs values during the set up and/ or development phases. Correspondance between test points and board signals is:

VO	->	OUT D/A signal
GND	->	GND D/A signal

To easily locate the test points contacts please refer to figure 8, while for further information about the signals they carry please refer to the previous pages that describe the connectors and figure 4.

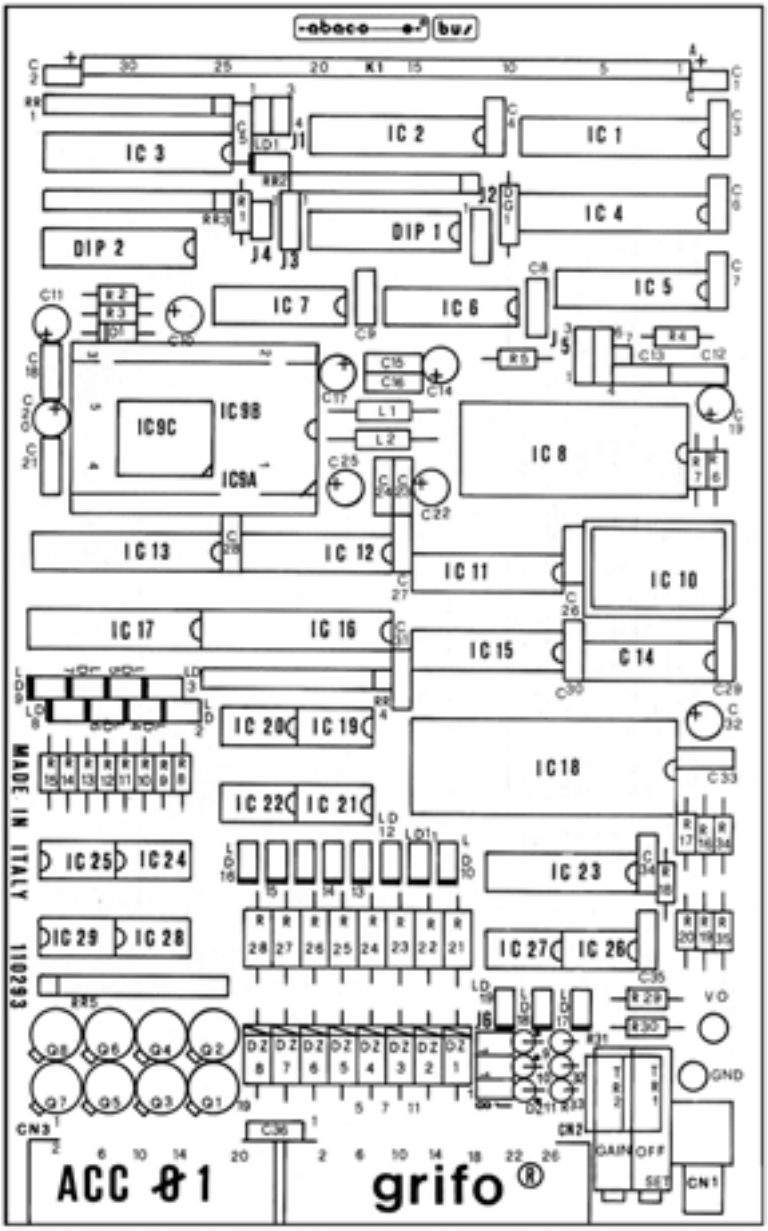


FIGURE 20: COMPONENTS MAP SOLDER SIDE

TRIMMERS AND CALIBRATION

On **ACC 01** there are two trimmers, called **TR1 and TR2**, that calibrate the output voltages of the A/D converter sections; in detail they allow to set the maximum and minimum output voltages for each section.
The **ACC 01** is subjected to a careful test that verifies and calibrates all the card sections.
The calibration is executed in laboratory, with a conntrolled +20° C room temperature, following these steps:

a) Jumper J5 is connected in 1-2, 4-5 for D/A output range ±10 Vdc (default).
b) A galvanically isolated 5 digits reference multimeter is connected between test points VO and GND.
c) An encoder, whose rotation can be hand made, is connected to the board.
d) Board is reset or tuned OFF and ON to set D/A at half range.
e) Trimmer TR1 (OFFSET) is regulated, to read 0.000 V on multimeter.
f) A random velocity profile is programmed.
g) Encoder is rotated until D/A is stabilized: so D/A is set to start or end of its range (according to encoder rotation direction).
h) Trimmer TR2 (GAIN) is regulated, to read -10,00 or +10,00 V on multimeter.
i) Calibration is fined repeating steps d÷h.
j) Trimmers della scheda are blocked with paint.

The analog interfaces use high precision components that are selected during mounting phase to avoid complicate and long calibration procedures.
After the calibration, the on board trimmers are blocked with paint to mantain calibration also in presence of mechanic stresses (vibrations, movings, delivery, etc.).
The user must not modify the card calibration, but if thermic drifts,time drifts and so on, make necessary a new calibration, the user must strictly follow the previously described procedure.
To easily locate the above mentioned components please refer to figure 8; for further information about test points please refer to the previous paragraph.

INTERRUPT

ACC 01 can generate an interrupt request when LM 628 motion controller is programmed to do so. This request can be conencted via hardware to one of the two interrupts availabe on **ABACO®** BUS, /INT or /NMI, and LED LD1 visualizes its status.
Main purpose of interrupt is to obtain control card attention when special events happen: e.g. zero index activation, position error, final position reached, etc.
Of course, interrupts allows to optimize times of management, in fact CPU control card is release from the task to keep under control **ACC 01**.
Interrupt signals reamins actived until control card performs a specific software operation to deactivate it, to warrant a correct management also in case of concorrent interrupts.

ADDRESSES AND MAPS

This chapter provides all the hardware informations needed to use **ACC 01** board.
Here the user will find informations about I/O card mapping and on board peripheral devices addressing.

BOARD MAPPING

ACC 01 board is mapped into a **4** bytes I/O addressing space (or two words in 16 bits addressing mode), that can be mapped starting from different base addresses according to how the board is configured. This feature allows to use several **LDA 01** cards on the same **ABACO®** BUS, or to install them on a BUS where other peripheral modules are installed obtaining a structure that can be expanded without any difficulty or modifications to the application software.
The base address can be defined through the specific BUS interface circuitry on the board itself; this circuitry uses the 2 eight pins dip switched called **DIP1** and **DIP2**, from which it reads the address set by the user. Here follows the corrispondance between dips configuration and address signals.

		Normal addressing (J3 in 2-3)	*Extended addressing (J3 in 1-2)*	
DIP2.1	->	**OFF**	Address A16	(*)
DIP2.2	->	**OFF**	Address A17	(*)
DIP2.3	->	Address A2	Address A2	
DIP2.4	->	Address A3	Address A3	
DIP2.5	->	Address A4	Address A4	
DIP2.6	->	Address A5	Address A5	
DIP2.7	->	Address A6	Address A6	
DIP2.8	->	Address A7	Address A7	
DIP1.1	->	*Indifferent*	Address A8	
DIP1.2	->	*Indifferent*	Address A9	
DIP1.3	->	*Indifferent*	Address A10	
DIP1.4	->	*Indifferent*	Address A11	
DIP1.5	->	*Indifferent*	Address A12	
DIP1.6	->	*Indifferent*	Address A13	
DIP1.7	->	*Indifferent*	Address A14	
DIP1.8	->	*Indifferent*	Address A15	

These dips are driven in complemented logic, this means that if a switch is **ON** generates a **logic zero**, viceversa if a switch is **OFF** generates a **logic one**.
Jumper J1 and J3, described in the previous chapter, select the number of bytes addressed amogst which the allocation address can be chosen.
Please remark the followoing conditions:

In normal addressing mode (256 byte from 00H to FFH), only DIP2 is significant for board mapping (first two switches must be OFF) and jumper J1 must be not connected while DIP1 is indifferent.

In extended addressing mode (64 Kbyte from 0000H to FFFFH), both DIP1 (first two switches must be OFF) and DIP2 are significant and jumper J1 must be not connected.

In super extended addressing mode (256 Kbyte from 00000H to 3FFFFH) both DIP1 and DIP2 are significant and jumper J1 must be connected.
Please remark that J1 determines the effective amount of KBytes in addressing space, so the two switches of DIP2 marked with (*) must be used only if really connected to addressing circuitery through J1 (please refer to table in figure 17); viceversa the ones not used must be OFF.

Also jumper J4 influences addressing circuit and must be set according to which control card (**GPC®** serie) is used.
In detail, if the board is provided with signal /M1 on **ABACO®** BUS connector, jumper J2 must be connected and viceversa.

NOTE:
Do not allocate more than one card in the same addressing space (calculate also number of bytes taken), otherwise the BUS conflicts that may derive could prevent the overall system from working properly.

As an example, here follow three possible mappings:
A titolo di esempio vengono riportati di seguito tre possibili mappaggi relativi alle tre modalità disponibili:

Addressing modes:		normal	extended	super extended
Mapping addresses:		80H	1490H	18028H
Control card:		with /M1	without /M1	without /M1
J1	->	Not connected	Not connected	Position 1-2, 3-4
J3	->	Position 2-3	Position 1-2	Position 1-2
J4	->	Connected	Not connected	Not connected
DIP2.1	->	OFF	OFF	OFF
DIP2.2	->	OFF	OFF	ON
DIP2.3	->	ON	ON	ON
DIP2.4	->	ON	ON	OFF
DIP2.5	->	ON	OFF	ON
DIP2.6	->	ON	ON	OFF
DIP2.7	->	ON	ON	ON
DIP2.8	->	OFF	OFF	ON

DIP1.1	->	Indifferent	ON	ON
DIP1.2	->	Indifferent	ON	ON
DIP1.3	->	Indifferent	OFF	ON
DIP1.4	->	Indifferent	ON	ON
DIP1.5	->	Indifferent	OFF	ON
DIP1.6	->	Indifferent	ON	ON
DIP1.7	->	Indifferent	ON	ON
DIP1.8	->	Indifferent	ON	OFF

INTERNAL REGISTERS ADDRESSING

Indicating the board base address with <**baseaddr**>, that is the address set using Dip Switches DIP1, DIP2, J1 and J3, as indicated in the previous paragraph **ACC 01** internal registers are addressable as explained in the following table.

REGISTER	ADDRESS	R/W	MEANING
STATO LM628	<baseadd>+00	R/W	Status register of motor controller LM 628.
DATI LM628	<baseadd>+01	R/W	Data register of motor controller LM 628.
OUTPUT	<baseadd>+02	W	Register for 8 digital outputs management.
INPUT	<baseadd>+02	R	Register for 8 digital inputs acquisition.

FIGURE 21: INTERNAL REGISTERS ADDRESSING TABLE

In the previous paragraph allocation addresses of all the peripherals have been reported, here follows a detailed description of function and meaning of internal registers (please always refer to the peripheral mapping tables to understand completely the following informations). Should the present documentaion be inadequate please refer to the component's manufacturer documentation.
In the following paragraphs the indications **D0÷D7** or **D0÷D15** are used to refer the bits of the byte or word involved in the I/O operations.

MOTION CONTROLLER LM 628

Motion controller LM 628 is managed through two register called STATO LM628 and DATA LM628.
First register can be used for write operation to send commands to motion controller and for read operations to acqiure its current status; data register can be used for write operations to set several parameters and coefficents of profile, according to previously sent command, or for read operations to acquire current values of motion.
LM 628 is completely managed through the four above described operations which allow, for example, to:

- initialize the controller;
- start and stop the motion;
- set eventual interrupts;
- monitor motion and controller status;
- program the trajectory;
- set PID filter coefficients;
- acquire current speed and position;

The totally software management and remarkable flexibility of LM 628 allow the user to make typical standard trapezoidal velocity profiles or any other trajectory modified or derived for these latter, as described in the following figure:

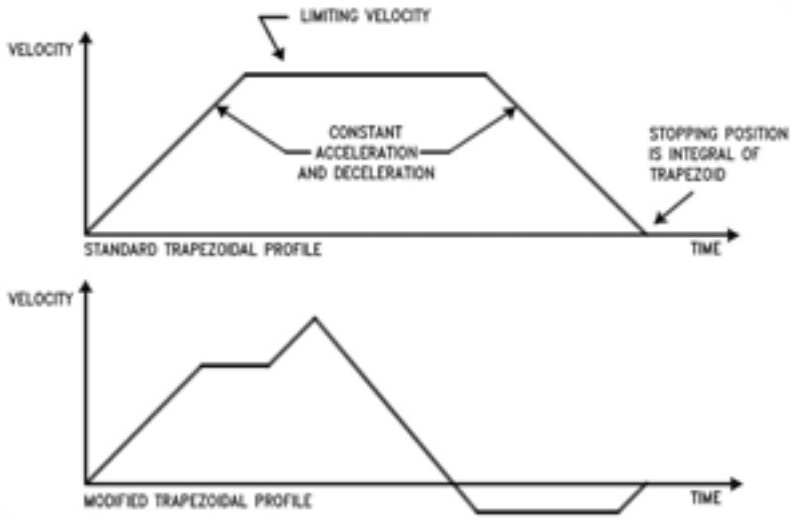


FIGURE 22: VELOCITY PROFILES

Complete description of LM628 software management (programming, control, optimozation, etc.) can be found in manufacturer documentation or in appendix A of this manual.

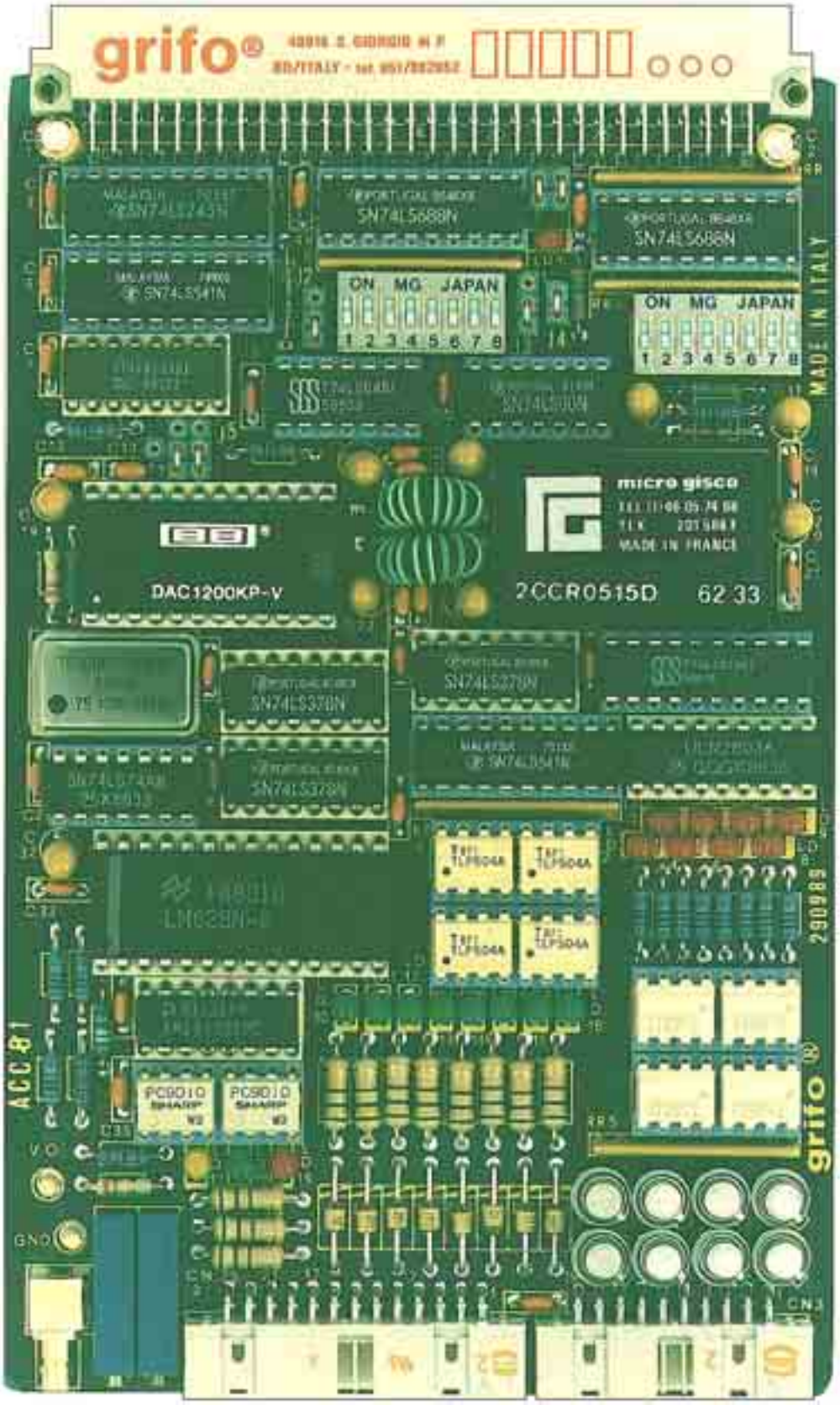


FIGURE 23: CARD PHOTO

DIGITAL OUTPUTS

Output registers OUTPUT is used to perform the management of the 8 open collector transistor output signals on **ACC 01** board. The 8 bits of these registers have the following meaning:

D7	->	OC OUT7
D6	->	OC OUT6
D5	->	OC OUT5
D4	->	OC OUT4
D3	->	OC OUT3
D2	->	OC OUT2
D1	->	OC OUT1
D0	->	OC OUT0

Performing an output operation at the address of OUTPUT the corresponding eight outputs are set by the output data .The correspondance between status of an output and value of a bit is:

Bit at logic 0	->	Output disabled	=	Transistor disabled
Bit at logic 1	->	Output enabled	=	Transistor enabled

As already said, LEDs LD2÷LD9 provided a visual indication of output status (LED ON = output actived).
All above signals are at logic 0 at power on, so all outputs are deactivated.

DIGITAL INPUTS

Input register INPUT is used to perform the management of the 8 optocoupled digital inputs on **JACC 01** board. The 8 bits of this register have the following meaning:

D7	->	IN7
D6	->	IN6
D5	->	IN5
D4	->	IN4
D3	->	IN3
D2	->	IN2
D1	->	IN1
D0	->	IN0

Performing an input operation at the address of INPUT the corresponding eight optocoupled input signals are acquired.

The correspondance between status of an input and value of a bit is:

Bit at logic 1	->	Input disabled	=	Input contact open
Bit at logic 0	->	Input enabled	=	Input contact closed

As already said, LEDs LD10÷LD16 provided a visual indication of input status (LED ON = input actived).

EXTERNAL CARDS

ACC 01 can be connected to a wide range of block modules and operator interface system produced by **grifo®**, or to many system of other companies.The on board resources can be expanded with a simple connection to the numerous peripheral **grifo®** boards,both intelligent and not, thanks to its standard **ABACO®** BUS connector. Even cards with **ABACO®** I/O BUS can be connected, by using the proper mother boards.
Hereunder some of these cards are briefly described; ask the detailed information directly to **grifo®**, if required.

MB3 01-MB4 01-MB8 01
Mother Board 3, 4, 8 slots
Motherboard featuring 3, 4 or 8 slots of **ABACO®** industrial BUS; pitch 4 TE; standard power supply connectors; LEDs for visual feed-back of power supply; holes for rack docking.

SPB 04-SPB 08
Switch Power BUS 4-8 slots
Motherboard featuring 4-8 slots of **ABACO®** industrial BUS; pitch 4 TE; standard power supply connectors; termination resistances; connector type F for **SPC xxx** supply ; holes for rack docking.

ABB 03
ABACO® Block BUS 3 slots
3 slots **ABACO®** mother board; 4 TE pitch connectors; **ABACO®** I/O BUS connector; screw terminal for power supply; connection for DIN C type and Ω rails.

ABB 05
ABACO® Block BUS 5 slots
5 slots **ABACO®** mother board with power supply. Double power supply built in; 5Vdc 2,5A section for powering the on board logic; second section at 24Vdc 400mA galvanically coupled, for the optocoupled input lines. Auxiliary connector for **ABACO®** I/O BUS. Connection for DIN Ω rails.

SBP 02-xx
Switch BLOCK Power xx version
Low cost switching power supply able to generate voltage from +5 to +40 Vdc and current up to 2.5 A; Input from 12 to 24 Vac; Connection for DIN C Type and Ω rails.

SPC 03.5S
Switch Power Card +5 Vdc
Europe format switching power supply capable to provide +5 Vdc to a load of 4 A; input voltage 12÷24 Vac; power-failure; connector for back-up battery; standard connector for mother board **SPB 0x**.

SPC 512
Switch Power Card +5 Vdc +12 Vdc
Europe format switching power supply capable to provide +5 Vdc 5A and +12 Vdc 2.5 A; input voltage 12÷24 Vac; power-failure; connector for back-up battery; standard connector for mother board **SPB 0x**.

GPC® 153

General Purpose Controller Z80

84C15 µP, 10÷16 MHz; Full CMOS; 1 RS 232 line; 1 RS 232 or RS 422-485 or Current Loop line; 16 TTL I/O lines; 8 A/D 12 bits lines; 2÷4 Timers Counters; 512K EPROM or FLASH; 512K RAM and RTC backed; 8K serial EEPROM; Buzzer; 1 Activity LED; Watch dog; 8 readable DIPs; LCD Interface.

GPC® 183

General Purpose Controller Z180

Z180 µP, 10÷16 MHz; Full CMOS; 1 RS 232 line; 1 RS 232 or RS 422-485 or Current Loop line; 24 TTL I/O lines; 11 A/D 12 bits lines; 2 Timers Counters; 512K EPROM or FLASH; 512K RAM and RTC backed; 8K serial EEPROM; Buzzer; 2 Activity LED; Watch dog; 4 readable DIPs; LCD Interface.

GPC® 324/D

"4" Type General Purpose Controller 80C32/320

80C32 or 80C320 µP, 14÷22 MHz; Full CMOS; 1 RS 232 line; 1 RS 232 or RS 422-485 or Current Loop line; 4÷16 TTL I/O lines; 3 Timers Counters; 64K EPROM; 64K RAM; 32K RAM backed; 32K DIL E2; 8K serial EEPROM; Watch dog; 1 readable DIP; LCD Interface; Abaco® I/O BUS; 5Vdc Power supply; Size: 100x50 mm.

GPC® 554

General Purpose Controller 80C552

Microprocessor 80C552 at 22 MHz; implementation completely CMOS; 32K EPROM; 32 K SRAM; 32 K EEPROM or SRAM; EEPROM; 2 RS 232 serial lines; 16 I/O TTL; 2 PWM lines; 16 bits Timer/Counter; Watch Dog; 6 signals A/D converter with resolution 10 bit; interface for **ABACO®** I/O BUS.

GPC® 154

"4" Type General Purpose Controller Z80

84C15 µP, 10÷16 MHz; Full CMOS; 1 RS 232 line; 1 RS 232 or RS 422-485 line; 16 TTL I/O lines; 2÷4 Timers Counters; 512K EPROM or FLASH; 512K RAM and RTC backed; 8K serial EEPROM; Watch dog; 2 readable DIPs; LCD Interface; Abaco® I/O BUS; 5Vdc Power supply; Size: 100x50 mm.

GPC® 884

General Purpose Controller Am188ES

Microprocessor AMD Am188ES up to 40 MHz16 bits; implementation completely CMOS; serie 4 format; 512K EPROM or FLASH; 512K SRAM backed with Lithium battery; RTC; 1 RS 232 serial line + 1 RS 232 or RS 422-485 or current loop; 16 I/O TTL; 3 timer/counter; watch dog; EEPROM; 11 signals A/D converter with 12 bit resolution; interface for **ABACO®** I/O BUS.

GPC® 323

General Purpose Controller 51 family

80C32 µP, 14 MHz; Full CMOS; 1 RS 232 line (software); 1 RS 232 or RS 422-485 or Current Loop line; 24 TTL I/O lines; 11 A/D 12 bits lines; 3 Timers Counters; 64K EPROM; 64K RAM; 32K RAM and RTC backed; 32K DIL EEPROM; 8K serial EEPROM; Buzzer; 2 Activity LED; Watch dog; 5 readable DIPs; LCD Interface.

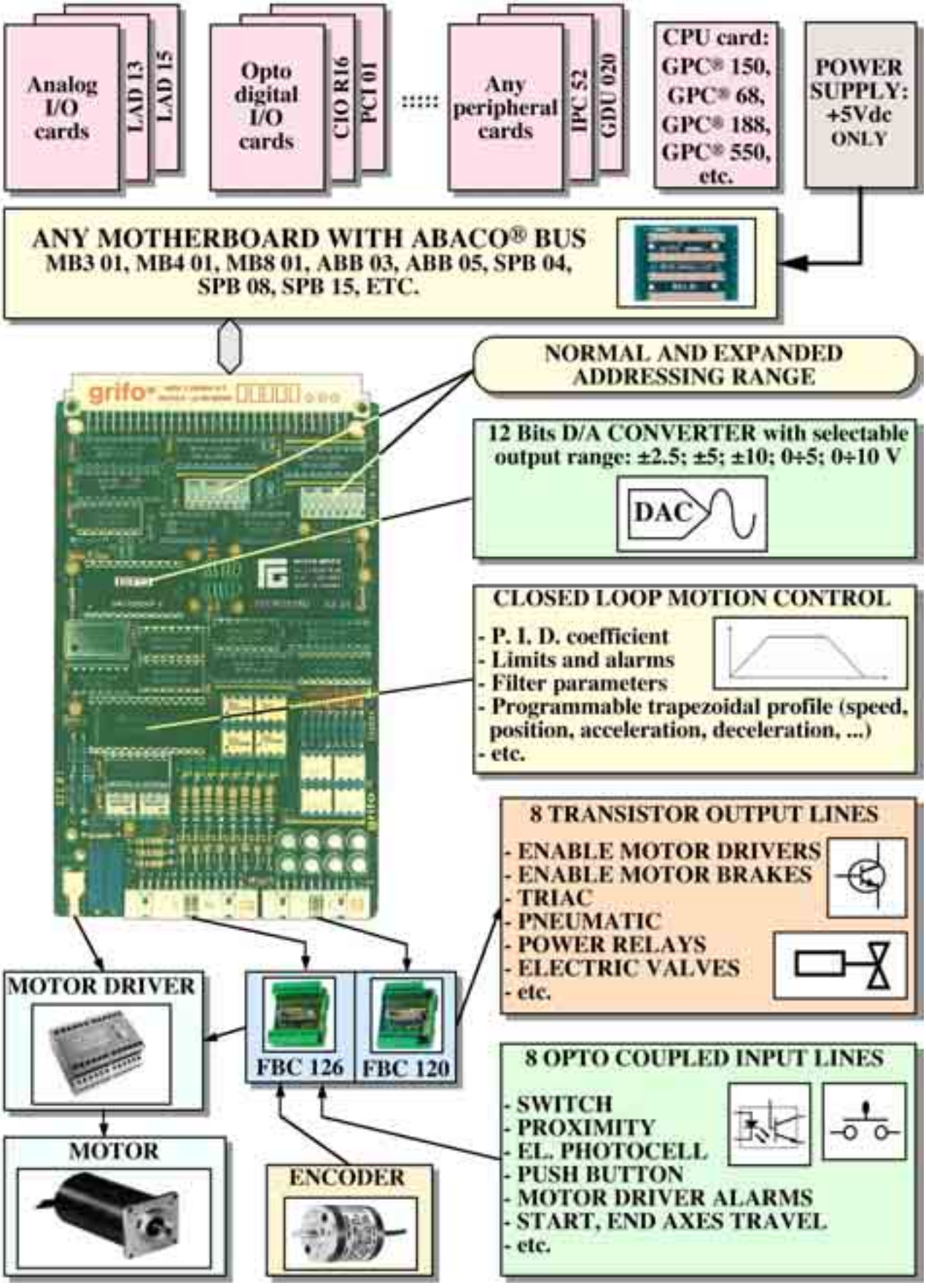


FIGURE 24: POSSIBLE CONNECTIONS DIAGRAM

BIBLIOGRAPHY

In this chapter there is a complete list of technical books, where the user can find all the necessary documentations on the components mounted on **ACC 01.**

Manual TEXAS INSTRUMENTES: *The TTL Data Book - SN54/74 Families*
Manual TEXAS INSTRUMENTES: *Linear Circuits Dtata Book - Volumi 1 e 3*

Manual NATIONAL SEMICONDUCTOR: *LM628 Precision Motion Controller*

Manual BURR-BROWN: *Integrated circuits data book supplement - Volume 33c.*

Technical Note MICRO-GISCO: *DC/DC Converter 2CCR0515D*

Technical Note MI.EL. MICROPOWER: *DC/DC Converters*

Manual MOTOROLA SEMICONDUCTORS: *Cmos Logic Data*

Manual SGS-THOMSON: *Motion Control application manual*
Manual SGS-THOMSON: *Small Signal Transistors - Data Book*

Manual TOSHIBA: *Photo Couplers - Data Book*

Please connect to the manifactures Web sites to get the latest version of all manuals and data sheets.

APPENDIX A: ON BOARD COMPONENTS DESCRIPTION

grifo® provides a free technical documentation service through its web site, where on board componentes data sheet can be downloaded.
Please refere to such documents, here follows the complete URL to retrieve it:

LM 628

Technical paper:
Link: Home | Technical Documentation Service | National Semiconductors | | Data Sheet LM628
URL: http://www.grifo.com/PRESS/DOC/National/LM628.pdf

Programming guide:
Link: Home | Technical Documentation Service | National Semiconductors | AN693 - LM628 Programming guide
URL: http://www.grifo.com/PRESS/DOC/National/AN-693.pdf

User manual:
Link: Home | Technical Documentation Service | National Semiconductors | AN706 - LM628 User guide
URL: http://www.grifo.com/PRESS/DOC/National/AN-706.pdf

DATA SHEET

National Semiconductor

January 2003

LM628/LM629
Precision Motion Controller

General Description

The LM628/LM629 are dedicated motion-control processors designed for use with a variety of DC and brushless DC servo motors, and other servomechanisms which provide a quadrature incremental position feedback signal. The parts perform the intensive, real-time computational tasks required for high performance digital motion control. The host control software interface is facilitated by a high-level command set. The LM628 has an 8-bit output which can drive either an 8-bit or a 12-bit DAC. The components required to build a servo system are reduced to the DC motor/actuator, an incremental encoder, a DAC, a power amplifier, and the LM628. An LM629-based system is similar, except that it provides an 8-bit PWM output for directly driving H-switches. The parts are fabricated in NMOS and packaged in a 28-pin dual in-line package or a 24-pin surface mount package (LM629 only). Both 6 MHz and 8 MHz maximum frequency versions are available with the suffixes -6 and -8, respectively, used to designate the versions. They incorporate an SDA core processor and cells designed by SDA.

Features

- 32-bit position, velocity, and acceleration registers
- Programmable digital PID filter with 16-bit coefficients
- Programmable derivative sampling interval
- 8- or 12-bit DAC output data (LM628)
- 8-bit sign-magnitude PWM output data (LM629)
- Internal trapezoidal velocity profile generator
- Velocity, target position, and filter parameters may be changed during motion
- Position and velocity modes of operation
- Real-time programmable host interrupts
- 8-bit parallel asynchronous host interface
- Quadrature incremental encoder interface with index pulse input
- Available in a 28-pin dual in-line package or a 24-pin surface mount package (LM629 only)

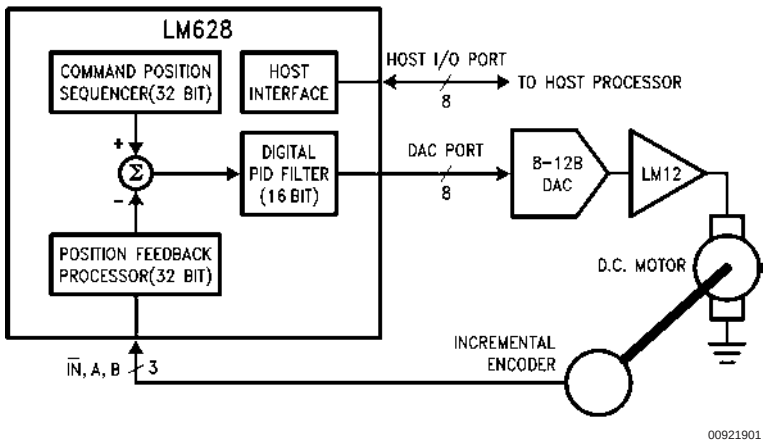


FIGURE 1. Block Diagram

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LM628 Programming Guide

National Semiconductor
Application Note 693
Steven Hunt
January 1999

Introduction

The LM628/LM629 are dedicated motion control processors. Both devices control DC and brushless DC servo motors, as well as, other servomechanisms that provide a quadrature incremental feedback signal. Block diagrams of typical LM628/LM629-based motor control systems are shown in *Figures 1, 2*.

As indicated in the figures, the LM628/LM629 are bus peripherals; both devices must be programmed by a host processor. This application note is intended to present a concrete starting point for programmers of these precision motion controllers. It focuses on the development of short programs that test overall system functionality and lay the groundwork for more complex programs. It also presents a method for tuning the loop-compensation PID filter. (Note 1)

Reference System

Figure 15 is a detailed schematic of a closed-loop motor control system. All programs presented in this paper were developed using this system. For application of the programs in other LM628-based systems, changes in basic programming structure are not required, but modification of filter coefficients and trajectory parameters may be required.

I. Program Modules

Breaking programs for the LM628 into sets of functional blocks simplifies the programming process; each block executes a specific task. This section contains examples of the principal building blocks (modules) of programs for the LM628.

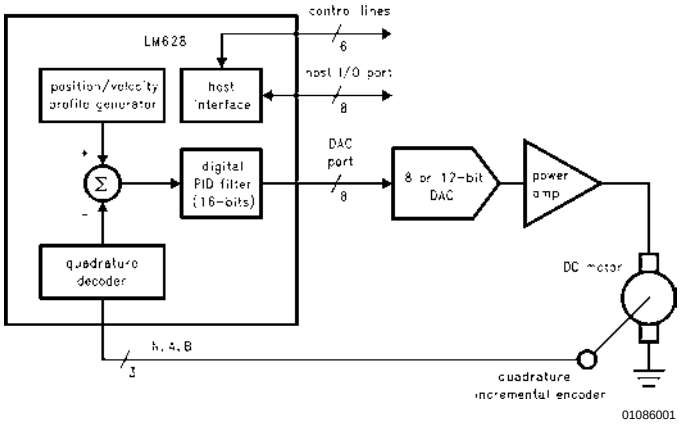

FIGURE 1. LM628-Based Motor Control System

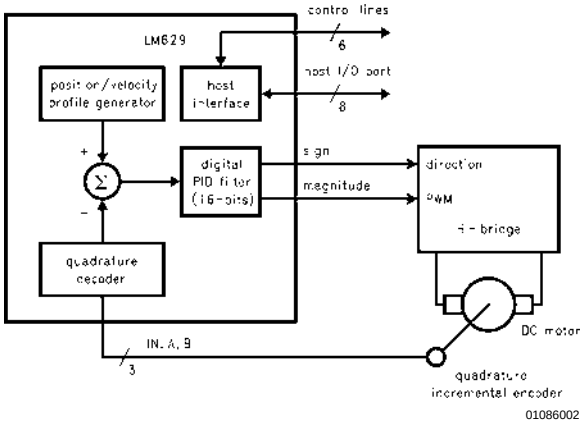

FIGURE 2. LM629-Based Motor Control System

Note 1: For the remainder of this paper, all statements about the LM628 also apply to the LM629 unless otherwise noted.

LM628/629 User Guide

National Semiconductor
Application Note 706
October 1993

1.0 Introduction

1.1 APPLICATION NOTE OBJECTIVE

This application note is intended to explain and complement the information in the data sheet and also address the common user questions. While no initial familiarity with the LM628/629 is assumed, it will be useful to have the LM628/629 data sheet close by to consult for detailed descriptions of the user command set, timing diagrams, bit assignments, pin assignments, etc.

After the following brief description of the LM628/629, Section 2.0 gives a fairly full description of the device's operation, probably more than is necessary to get going with the device. This section ends with an outline of how to tune the control system by adjusting the PID filter coefficients.

Section 3 "User Command Set" discusses the use of the LM628/629 commands. For a detailed description of each command the user should refer to the data sheet.

Section 4 "Helpful User Ideas" starts with a short description of the actions necessary to get going, then proceeds to talk about some performance enhancements and follows on with a discussion of a couple of operating constraints of the device.

Section 5 "Theory" is a short foray into theory which relates the PID coefficients that would be calculated from a continuous domain control loop analysis to those of the discrete domain including the scaling factors inherent to the LM628/629. No attempt is made to discuss control system theory as such, readers should consult the ample references available, some suggestions are made at the end of this application note. Section 5 concludes with an example trajectory calculation, reviving those perhaps forgotten ideas about acceleration, velocity, distance and time.

Section 6 "Questions and Answers", is in question and answer format and is born out of and dedicated to the many interesting discussions with customers that have taken place.

1.2 BRIEF DESCRIPTION OF LM628/629

LM628/629 is a microcontroller peripheral that incorporates in one device all the functions of a sample-data motion control system controller. Using the LM628/629 makes the potentially complex task of designing a fast and precise motion control system much easier. Additional features, such as trajectory profile generation, on the "fly" update of loop compensation and trajectory, and status reporting, are included. Both position and velocity motion control systems can be implemented with the LM628/629.

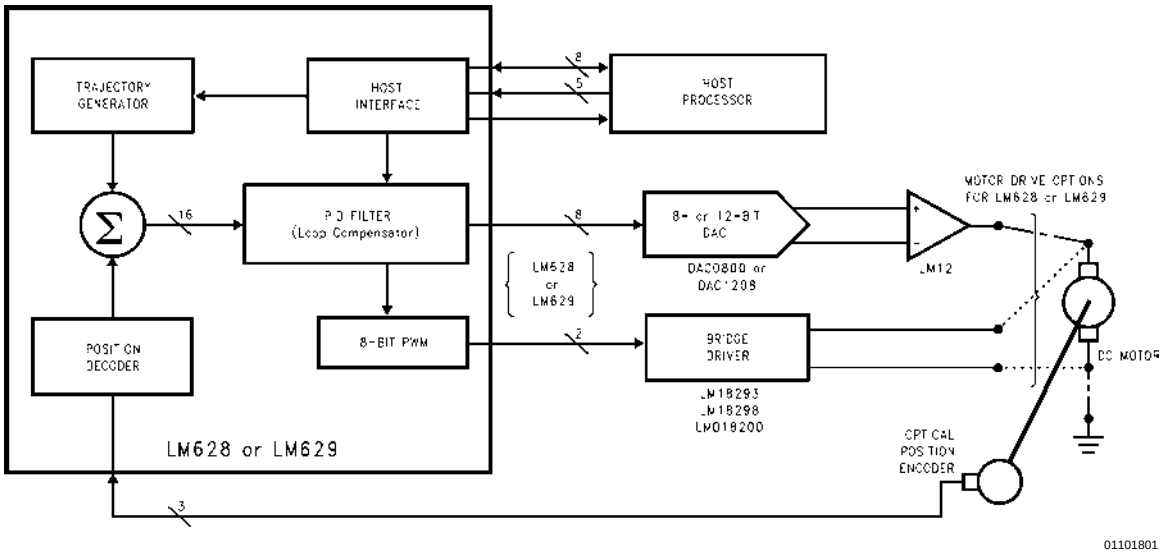

FIGURE 1. LM628 and LM629 Typical System Block Diagram

LM628/629 is itself a purpose designed microcontroller that implements a position decoder, a summing junction, a digital PID loop compensation filter, and a trajectory profile generator, *Figure 1*. Output format is the only difference between LM628 and LM629. A parallel port is used to drive an 8- or 12-bit digital-to-analog converter from the LM628 while the LM629 provides a 7-bit plus sign PWM signal with sign and magnitude outputs. Interface to the host microcontroller is via an 8-bit bi-directional data port and six control lines which includes host interrupt and hardware reset. Maximum sampling rates of either 2.9 kHz or 3.9 kHz are available by

APPENDIX B: ALPHABETICAL INDEX

SYMBOLS

A

B

C

D

E

G

I

J

L

M

O

P