PRELIMINARY DOCUMENTATION
AAC 06
(Axis Acquisition Card 6 counter)

K1 - CONNECTOR FOR ABACO® BUS

K1 is a 64 pins, male, 90°, DIN 41612 connector with 2.54 pitch.
On K1 are available all the industrial **ABACO®** BUS signals and it can be used for connections to many other peripheral cards. In the table below there are the standard pin outs both for 8 bits and 16 bits CPU and the signal connected on **ACC 06**. All signals follow TTL standard.

A 16 bits BUS	A 8 bits BUS	A AAC 06	PIN	C AAC 06	C 8 bits BUS	C 16 bits BUS
GND	GND	GND	1	GND	GND	GND
+5 Vdc	+5 Vdc	+5 Vdc	2	+5 Vdc	+5 Vdc	+5 Vdc
D0	D0	D0	3	N.C.		D8
D1	D1	D1	4	N.C.		D9
D2	D2	D2	5	N.C.		D10
D3	D3	D3	6	N.C.	/INT	/INT
D4	D4	D4	7	N.C.	/NMI	/NMI
D5	D5	D5	8	N.C.	/HALT	D11
D6	D6	D6	9	N.C.	/MREQ	/MREQ
D7	D7	D7	10	/IORQ	/IORQ	/IORQ
A0	A0	A0	11	/RD	/RD	/RDLDS
A1	A1	A1	12	/WR	/WR	/WRLDS
A2	A2	A2	13	N.C.	/BUSAK	D12
A3	A3	A3	14	N.C.	/WAIT	/WAIT
A4	A4	A4	15	N.C.	/BUSRQ	D13
A5	A5	A5	16	/RESET	/RESET	/RESET
A6	A6	A6	17	/M1	/M1	/IACK
A7	A7	A7	18	N.C.	/RFSH	D14
A8	A8	N.C.	19	N.C.	/MEMDIS	/MEMDIS
A9	A9	N.C.	20	N.C.	VDUSEL	A22
A10	A10	N.C.	21	N.C.	/IEI	D15
A11	A11	N.C.	22	N.C.		
A12	A12	N.C.	23	N.C.	CLK	CLK
A13	A13	N.C.	24	N.C.		/RDUDS
A14	A14	N.C.	25	N.C.		/WRUDS
A15	A15	N.C.	26	N.C.		A21
A16		N.C.	27	N.C.		A20
A17		N.C.	28	N.C.		A19
A18		N.C.	29	N.C.	/R.T.	/R.T.
+12 Vdc	+12 Vdc	N.C.	30	N.C.	-12 Vdc	-12 Vdc
+5 Vdc	+5 Vdc	+5 Vdc	31	+5 Vdc	+5 Vdc	+5 Vdc
GND	GND	GND	32	GND	GND	GND

FIGURE 1: K1 - ABACO® BUS CONNECTOR

Signals description:

8 bits CPU

A0-A15	=	O	- Address BUS
D0-D7	=	I/O	- Data BUS
/INT	=	I	- Interrupt request
/NMI	=	I	- Non Maskable Interrupt
/HALT	=	O	- Halt state
/MREQ	=	O	- Memory Request
/IORQ	=	O	- Input Output Request
/RD	=	O	- Read cycle status
/WR	=	O	- Write cycle status
/BUSAK	=	O	- BUS Acknowledge
/WAIT	=	I	- Wait
/BUSRQ	=	I	- BUS Request
/RESET	=	O	- Reset
/M1	=	O	- Machine cycle one
/RFSH	=	O	- Refresh for dynamic RAM
/MEMDIS	=	I	- Memory Display
/VDUSEL	=	O	- VDU Selection
/IEI	=	I	- Interrupt Enable Input
CLK	=	O	- System clock
R.T.	=	I	- Reset button
+5 Vdc	=	I	- Power supply at +5 Vdc
+12 Vdc	=	I	- Power supply at +12 Vdc
-12 Vdc	=	I	- Power supply at -12 Vdc
GND	=		- Ground signal

16 bits CPU

A16-A22	=	O	- Address BUS
D8-D15	=	I/O	- Data BUS
/RD UDS	=	O	- Read Upper Data Strobe
/WR UDS	=	O	- Write Upper Data Strobe
/IACK	=	O	- Interrupt Acknowledge
/RD LDS	=	O	- Read Lower Data Strobe
/WR LDS	=	O	- Write Lower Data Strobe
N. C.	=		- Not Connected

NOTE
Directionality indications as above stated are referred to a master (**GPC®**) board and have been kept untouched to avoid ambiguity in case of multi-boards systems.

CN1 - CONNECTOR FOR COUNTER INPUTS

CN1 is a 26 pins, female, 90°, high density D connector.
It is placed on the front side of the card and it is used to connect the inputs of the six counters, each one of these is provided of three optocoupled signals, NPN type.
The power supply of all these inputs can be +12 Vdc or +24 Vdc according with proper jumpers configurations, as described in the following paragraphs.

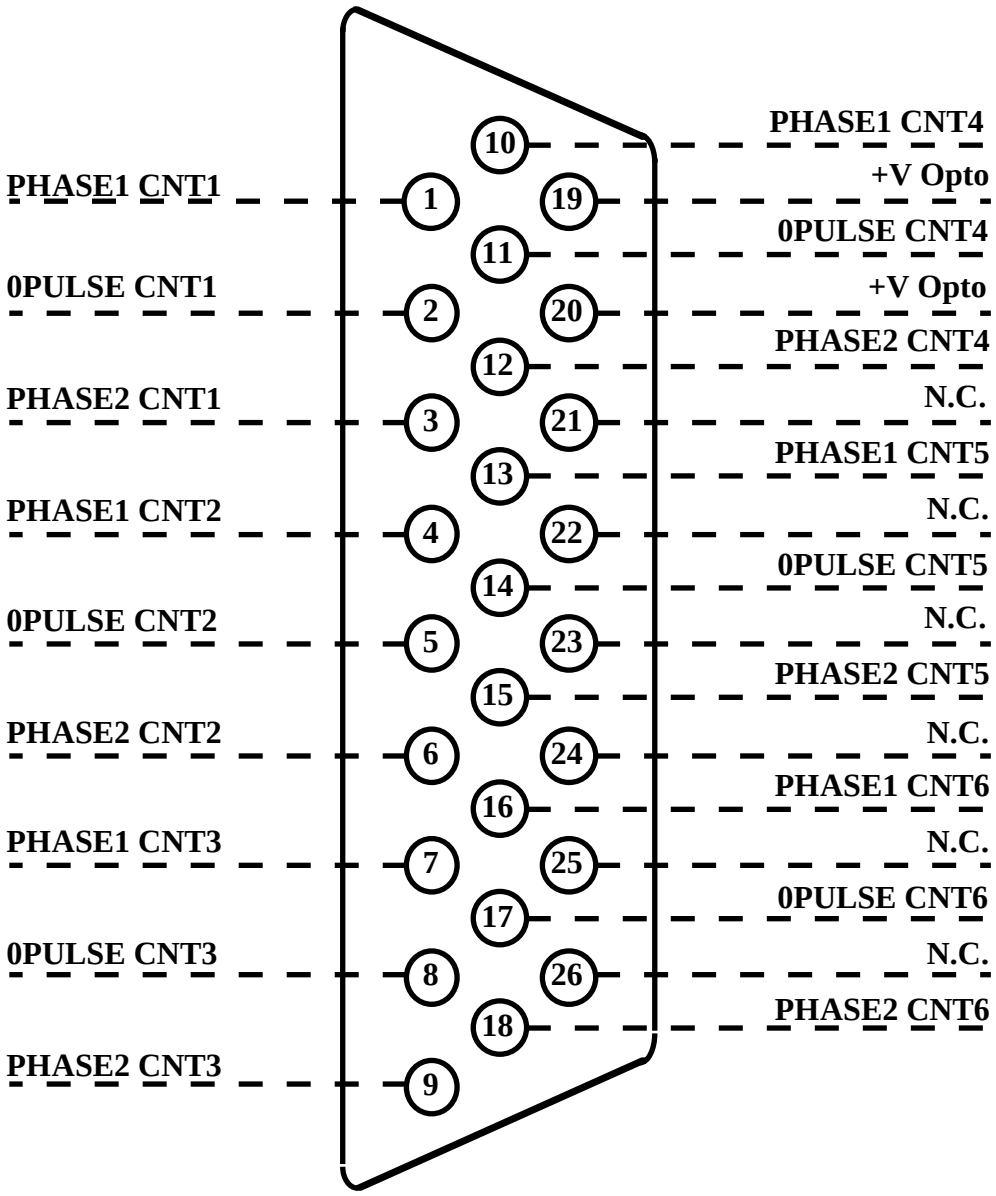


FIGURE 2: CN1 CONNECTOR FOR COUNTER INPUTS

Signals description:

PHASE1 CNTn	=	I	- Phase 1 input signal for counter n.
PHASE2 CNTn	=	I	- Phase 2 input signal for counter n.
0PULSE CNTn	=	I	- Zero pulse input signal for counter n.
+V Opto	=	I	- Gavanically insulated voltage for optocoupled NPN inputs power supply.
N.C.	=		- Not connected.

JUMPERS

On **AAC 06** there are 32 jumpers for card configuration. Connecting these jumpers, the user can define for example the counters connections, the external power supply type and so on. Below there is the jumpers list complete of relative functions:

JUMPER	POSITION	FUNCTION
J1	1-2	The card manages the signal /M1 available on K1 (pin 17C)
	2-3	The card doesn't manages the signal /M1 available on K1 (pin 17C)
J2	1-2	It connects PHASE1 CNT4 to signal for counting up (increment) of counter 4
	2-3	It connects PHASE1 CNT4 to signal for measuring with direction discriminator of counter 4
J3	1-2	It connects PHASE2 CNT4 to signal for counting down (decrement) of counter 4
	2-3	It connects PHASE2 CNT4 to signal for measuring with direction discriminator of counter 4
J4	1-2	It connects the overflow signal of counter 4 to signal for counting up (increment) of counter 5
	2-3	It connects PHASE1 CNT5 to signal for counting up (increment) of counter 5
	3-4	It connects PHASE1 CNT5 to signal for measuring with direction discriminator of counter 5
J5	1-2	It connects the underflow signal of counter 4 to signal for counting down (decrement) of counter 5
	2-3	It connects PHASE2 CNT5 to signal for counting down (decrement) of counter 5
	3-4	It connects PHASE2 CNT5 to signal for measuring with direction discriminator of counter 5
J6	1-2	It connects PHASE1 CNT6 to signal for counting up (increment) of counter 6
	2-3	It connects PHASE1 CNT6 to signal for measuring with direction discriminator of counter 6
J7	1-2	It connects PHASE2 CNT6 to signal for counting down (decrement) of counter 6
	2-3	It connects PHASE2 CNT6 to signal for measuring with direction discriminator of counter 6

J8	1-2	It connects PHASE1 CNT1 to signal for counting up (increment) of counter 1
	2-3	It connects PHASE1 CNT1 to signal for measuring with direction discriminator of counter 1
J9	1-2	It connects PHASE2 CNT1 to signal for counting down (decrement) of counter 1
	2-3	It connects PHASE2 CNT1 to signal for measuring with direction discriminator of counter 1
J10	1-2	It connects the overflow signal of counter 1 to signal for counting up (increment) of counter 2
	2-3	It connects PHASE1 CNT2 to signal for counting up (increment) of counter 2
	3-4	It connects PHASE1 CNT2 to signal for measuring with direction discriminator of counter 2
J11	1-2	It connects the underflow signal of counter 4 to signal for counting down (decrement) of counter 2
	2-3	It connects PHASE2 CNT2 to signal for counting down (decrement) of counter 2
	3-4	It connects PHASE2 CNT2 to signal for measuring with direction discriminator of counter 2
J12	1-2	It connects PHASE1 CNT3 to signal for counting up (increment) of counter 3
	2-3	It connects PHASE1 CNT3 to signal for measuring with direction discriminator of counter 3
J13	1-2	It connects PHASE2 CNT3 to signal for counting down (decrement) of counter 3
	2-3	It connects PHASE2 CNT3 to signal for measuring with direction discriminator of counter 3
J14	not connected	It doesn't connect the metallic shield of CN1 to power supply ground signal (GND)
	connected	It connects the metallic shield of CN1 to power supply ground signal (GND)
J15	not connected	It configures PHASE2 CNT6 signal for +24 Vdc power supply
	connected	It configures PHASE2 CNT6 signal for +12 Vdc power supply
J16	not connected	It configures OPULSE CNT6 signal for +24 Vdc power supply
	connected	It configures OPULSE CNT6 signal for +12 Vdc power supply
J17	not connected	It configures PHASE1 CNT6 signal for +24 Vdc power supply
	connected	It configures PHASE1 CNT6 signal for +12 Vdc power supply

J18	not connected	It configures PHASE2 CNT5 signal for +24 Vdc power supply
	connected	It configures PHASE2 CNT5 signal for +12 Vdc power supply
J19	not connected	It configures OPULSE CNT5 signal for +24 Vdc power supply
	connected	It configures OPULSE CNT5 signal for +12 Vdc power supply
J20	not connected	It configures PHASE1 CNT5 signal for +24 Vdc power supply
	connected	It configures PHASE1 CNT5 signal for +12 Vdc power supply
J21	not connected	It configures PHASE2 CNT4 signal for +24 Vdc power supply
	connected	It configures PHASE2 CNT4 signal for +12 Vdc power supply
J22	not connected	It configures OPULSE CNT4 signal for +24 Vdc power supply
	connected	It configures OPULSE CNT4 signal for +12 Vdc power supply
J23	not connected	It configures PHASE1 CNT4 signal for +24 Vdc power supply
	connected	It configures PHASE1 CNT4 signal for +12 Vdc power supply
J24	not connected	It configures PHASE2 CNT3 signal for +24 Vdc power supply
	connected	It configures PHASE2 CNT3 signal for +12 Vdc power supply
J25	not connected	It configures OPULSE CNT3 signal for +24 Vdc power supply
	connected	It configures OPULSE CNT3 signal for +12 Vdc power supply
J26	not connected	It configures PHASE1 CNT3 signal for +24 Vdc power supply
	connected	It configures PHASE1 CNT3 signal for +12 Vdc power supply
J27	not connected	It configures PHASE2 CNT2 signal for +24 Vdc power supply
	connected	It configures PHASE2 CNT2 signal for +12 Vdc power supply
J28	not connected	It configures OPULSE CNT2 signal for +24 Vdc power supply
	connected	It configures OPULSE CNT2 signal for +12 Vdc power supply
J29	not connected	It configures PHASE1 CNT2 signal for +24 Vdc power supply
	connected	It configures PHASE1 CNT2 signal for +12 Vdc power supply
J30	not connected	It configures PHASE2 CNT1 signal for +24 Vdc power supply
	connected	It configures PHASE2 CNT1 signal for +12 Vdc power supply
J31	not connected	It configures OPULSE CNT1 signal for +24 Vdc power supply
	connected	It configures OPULSE CNT1 signal for +12 Vdc power supply
J32	not connected	It configures PHASE1 CNT1 signal for +24 Vdc power supply
	connected	It configures PHASE1 CNT1 signal for +12 Vdc power supply

FIGURE 3: JUMPERS FUNCTIONS TABLE

The jumper J1 must be connected in position 1-2 when the CPU card, that controls the **AAC 06**, is based on Z80 or compatible CPU, to avoid malfunction especially during the interrupts management performed by same CPU card.

The connection of input signals to signals for measuring with directiondiscriminator allows a comfortable acquisition of bidirectional encoders, obtaining by the card an absolute combination that coincides with the current encoder position, without any intermediate calculations.

Instead the connection of input signals to signal for counting up (increment and/or down (decrement) allows the development of simple counters, frequency measurement, period measurement, up and down pulse counter, etc.

Finally the counters 1, 2 and 3, 4 can be cascade connected obtaining total 32 bits counters. For example if you want to use counter 1 and 2 in cascade, you must:
- connect the signal to measure to counter 1 inputs: PHASE1 CNT1, PHASE2 CNT1 and 0PULSE CNT1;
- connect the jumpers J8 and J9 in position 1-2 or 2-3 according with direction disriminator necessity;
- connect the jumpers J10 and J11 in position 1-2 obtaining that the overflow and underflow of counter 1 increase and decrease the counter 2;
- acquire the 4 counting registers and calculate the total 32 bits combination by using the couple of byte from counter 1 (these are the 16 less significant bits) and the couple from counter 2 (the 16 most significant bits).

If the jumper J14 is closed, the card power supply ground (GND on K1) is connected with metallic frame of CN1 connector obtaining an electric shielding on input signals. Please pay attention on this jumper connection in fact when the external connections is not performed with the proper noisy immunity techniques, it carries troubles on power supply of the entire system.

When the jumpers J15 ÷J32 are connected it is possible to connect a +V Opto = +12 Vdc while if they are open the +V Opto is +24 Vdc. On CN1 connector there is only one +V Opto signal, so if you must contemporaneously acquire both +12 Vdc and +24 Vdc inputs please ensure separation of all the ground signals of the same input signals, in fact the positive signals must be linked together and then connected to pins 19 and 20 of CN1.

COUNTER FUNCTIONALITY CONFIGURATIONON

The card **AAC 06** is based on two THCT 12316 components that are triple programmable counter that can operate in 8 different modes. For detailed information about these modalities please refer to appendix A of the manual, while for the mode selection the user must configure three dip switches DIP2, DIP3, DIP4 as below described:

DIP 4.3	DIP 4.2	DIP 4.1		MODE
ON	ON	ON	->	Mode 0 for counter 1
ON	ON	OFF	->	Mode 1 for counter 1
ON	OFF	ON	->	Mode 2 for counter 1
ON	OFF	OFF	->	Mode 3 for counter 1
OFF	ON	ON	->	Mode 4 for counter 1
OFF	ON	OFF	->	Mode 5 for counter 1
OFF	OFF	ON	->	Mode 6 for counter 1
OFF	OFF	OFF	->	Mode 7 for counter 1

DIP 4.6	DIP 4.5	DIP 4.4		MODE
ON	ON	ON	->	Mode 0 for counter 2
ON	ON	OFF	->	Mode 1 for counter 2
ON	OFF	ON	->	Mode 2 for counter 2
ON	OFF	OFF	->	Mode 3 for counter 2
OFF	ON	ON	->	Mode 4 for counter 2
OFF	ON	OFF	->	Mode 5 for counter 2
OFF	OFF	ON	->	Mode 6 for counter 2
OFF	OFF	OFF	->	Mode 7 for counter 2

DIP 3.2	DIP 4.8	DIP 4.7		MODE
ON	ON	ON	->	Mode 0 for counter 3
ON	ON	OFF	->	Mode 1 for counter 3
ON	OFF	ON	->	Mode 2 for counter 3
ON	OFF	OFF	->	Mode 3 for counter 3
OFF	ON	ON	->	Mode 4 for counter 3
OFF	ON	OFF	->	Mode 5 for counter 3
OFF	OFF	ON	->	Mode 6 for counter 3
OFF	OFF	OFF	->	Mode 7 for counter 3

DIP 2.3	DIP 2.2	DIP 2.1		MODE
ON	ON	ON	->	Mode 0 for counter 4
ON	ON	OFF	->	Mode 1 for counter 4
ON	OFF	ON	->	Mode 2 for counter 4
ON	OFF	OFF	->	Mode 3 for counter 4
OFF	ON	ON	->	Mode 4 for counter 4
OFF	ON	OFF	->	Mode 5 for counter 4
OFF	OFF	ON	->	Mode 6 for counter 4
OFF	OFF	OFF	->	Mode 7 for counter 4

DIP 2.6	DIP 2.5	DIP 2.4		MODE
ON	ON	ON	->	Mode 0 for counter 5
ON	ON	OFF	->	Mode 1 for counter 5
ON	OFF	ON	->	Mode 2 for counter 5
ON	OFF	OFF	->	Mode 3 for counter 5
OFF	ON	ON	->	Mode 4 for counter 5
OFF	ON	OFF	->	Mode 5 for counter 5
OFF	OFF	ON	->	Mode 6 for counter 5
OFF	OFF	OFF	->	Mode 7 for counter 5

DIP 3.1	DIP 2.8	DIP 2.7		MODE
ON	ON	ON	->	Mode 0 for counter 6
ON	ON	OFF	->	Mode 1 for counter 6
ON	OFF	ON	->	Mode 2 for counter 6
ON	OFF	OFF	->	Mode 3 for counter 6
OFF	ON	ON	->	Mode 4 for counter 6
OFF	ON	OFF	->	Mode 5 for counter 6
OFF	OFF	ON	->	Mode 6 for counter 6
OFF	OFF	OFF	->	Mode 7 for counter 6

Below it is described a short description of the 8 function madalities, related to signals available on CN1 connector.

Mode 0: COUNTER with increment or decrement (up or down) caused by PHASE1 CNTn and/or PHASE2 CNTn signals, without direction discriminator.

Mode 1: DIRECTION DISCRIMINATOR of a single count pulse synchronous with PHASE1 CNTn rising in forward direction and falling in backward direction.

Mode 2: DIRECTION DISCRIMINATOR of a single count pulse synchronous with PHASE2 CNTn rising in forward direction and falling in backward direction.

Mode 3: DIRECTION DISCRIMINATOR of a double count pulse synchronous with PHASE1 CNTn rising and falling.

Mode 4: DIRECTION DISCRIMINATOR of a double count pulse synchronous with PHASE2 CNTn rising and falling.

Mode 5: DIRECTION DISCRIMINATOR of a quadruple count pulse synchronous with all edges.

Mode 6: PULSE WIDHT MEASUREMENT where PHASE1 CNTn is the gate signal and PHASE2 CNTn is high for up counting and low for down counting. Count is synchronous with rising clock.

Mode 7: FREQUENCY MEASUREMENT where PHASE1 CNTn is frequency signal to be measured and PHASE2 CNTn is the gate signals of know time interval. Count is synchronous with rising edge of PHASE1 CNT n.

VISUAL FEEDBACK

On the front side of **AAC 06** board, there are two rows of eight LEDs plus other two LEDs that visualize the input signals status conditions, as described in the following table:

LEDs	COLOUR	FUNCTION
DL1	Red	Visualizes status of PHASE1 CNT1 line.
DL9	Green	Visualizes status of PHASE2 CNT1 line.
DL7	Yellow	Visualizes status of 0PULSE CNT1 line.
DL2	Red	Visualizes status of PHASE1 CNT2 line.
DL10	Green	Visualizes status of PHASE2 CNT2 line.
DL17	Yellow	Visualizes status of 0PULSE CNT2 line.
DL3	Red	Visualizes status of PHASE1 CNT3 line.
DL11	Green	Visualizes status of PHASE2 CNT3 line.
DL8	Yellow	Visualizes status of 0PULSE CNT3 line.
DL4	Red	Visualizes status of PHASE1 CNT4 line.
DL12	Green	Visualizes status of PHASE2 CNT4 line.
DL15	Yellow	Visualizes status of 0PULSE CNT4 line.
DL5	Red	Visualizes status of PHASE1 CNT5 line.
DL13	Green	Visualizes status of PHASE2 CNT5 line.
DL18	Yellow	Visualizes status of 0PULSE CNT5 line.
DL6	Red	Visualizes status of PHASE1 CNT6 line.
DL14	Green	Visualizes status of PHASE2 CNT6 line.
DL16	Yellow	Visualizes status of 0PULSE CNT6 line.

FIGURE 4: VISUAL FEEDBACK TABLE

Each LED is enabled when the relative input signal is active that is when the pin on CN1 connector is connected to ground signal of insulated inputs power supply (= reference of +V Opto).

BOARD MAPPING

AAC 06 board is mapped into a **16** consecutive I/O bytes addressing space that can be based starting from different base addresses according to how the board is configured. This feature allows to use several **AAC 06** cards on the same **ABACO® BUS**, or to install them on a BUS where other peripheral cards are installed obtaining a structure that can be expanded without any difficulty or modifications to the application software.
The base address can be defined through the specific BUS interface circuitry on the board itself; this circuitry uses one dip switch, featuring 4 pins, from which it reads the address set by the user. Here follows the corrispondance between dip switches configuration and address signals.

DIP1.1	->	Address BUS signal A4
DIP1.2	->	Address BUS signal A5
DIP1.3	->	Address BUS signal A6
DIP1.4	->	Address BUS signal A7

These dip switches are driven in complemented logic, this means that if a switch is **ON** it generates a **logic zero**, viceversa if a switch is **OFF** it generates a **logic one**.
Also jumper J1 affects the addressing section and must be set according to the type of master control board (**CPU** or **GPC®**) used to drive the **AAC 06**. In detail if the master control board is provided with signal /M1 on **ABACO® BUS** connector, then jumper J1 must be connected in position 1-2 and viceversa.

To facilitate the board use here follow two mapping examples:
If the user has to map the board starting from base address 040H, driven by a master control card provided with the signal /M1, jumper and dip swithces status must be as follows:

J1	->	Position 1-2
DIP1.1	->	ON
DIP1.2	->	ON
DIP1.3	->	OFF
DIP1.4	->	ON

If the user has to map the board starting from base address F0H, driven by a master control card not provided with the signal /M1, jumper and dip swithces status must be as follows:

J1	->	Position 2-3
DIP1.1	->	OFF
DIP1.2	->	OFF
DIP1.3	->	OFF
DIP1.4	->	OFF

To easily locate the dip swithces, please refer card serigraph.

INTERNAL REGISTERS ADDRESSING

Indicating the board base address with <**baseaddr**>, that is the address set using DIP1, as indicated in the previous paragraph, **AAC 06** internal registers are addressable as explained in the following table.

DEVICE	REG.	ADDRESS	R/W	MEANING
THCT 12316 IC8	CNT3H	<baseaddr>+02H	R/W	Read/Set High byte of counter 3
	CNT3L	<baseaddr>+03H	R/W	Read/Set Low byte of counter 3
	CNT2H	<baseaddr>+04H	R/W	Read/Set High byte of counter 2
	CNT2L	<baseaddr>+05H	R/W	Read/Set Low byte of counter 2
	CNT1H	<baseaddr>+06H	R/W	Read/Set High byte of counter 1
	CNT1L	<baseaddr>+07H	R/W	Read/Set Low byte of counter 1
THCT 12316 IC7	CNT6H	<baseaddr>+0AH	R/W	Read/Set High byte of counter 6
	CNT6L	<baseaddr>+0BH	R/W	Read/Set Low byte of counter 6
	CNT5H	<baseaddr>+0CH	R/W	Read/Set High byte of counter 5
	CNT5L	<baseaddr>+0DH	R/W	Read/Set Low byte of counter 5
	CNT4H	<baseaddr>+0EH	R/W	Read/Set High byte of counter 4
	CNT4L	<baseaddr>+0FH	R/W	Read/Set Low byte of counter 4

FIGURE 5: INTERNAL REGISTERS ADDRESSES TABLE

If using several boards on the same **ABACO® BUS**, when setting the boards mapping address the user shold be careful not to allocate more than one board in the same addressing space (consider the base address plus the bytes taken by the board addressing). If this condition is not satisfied a BUS conflict situation will occour, prejudicing the correct working of the whole system.

TRIPLE COUNTER THCT 12316 AND COMPATIBLE

For the desctription of this triple counter please refer to the specific technical documentation in the appendix A of this manual and to description available in COUNTER FUNCTIONALITY CONFIGURATION. The information reported in appendix use different names for the input signals with the following corrispondence:

Ua1n	->	PHASE1 CNTn
Ua2n	->	PHASE2 CNTn
Ua0n	->	0PULSE CNTn

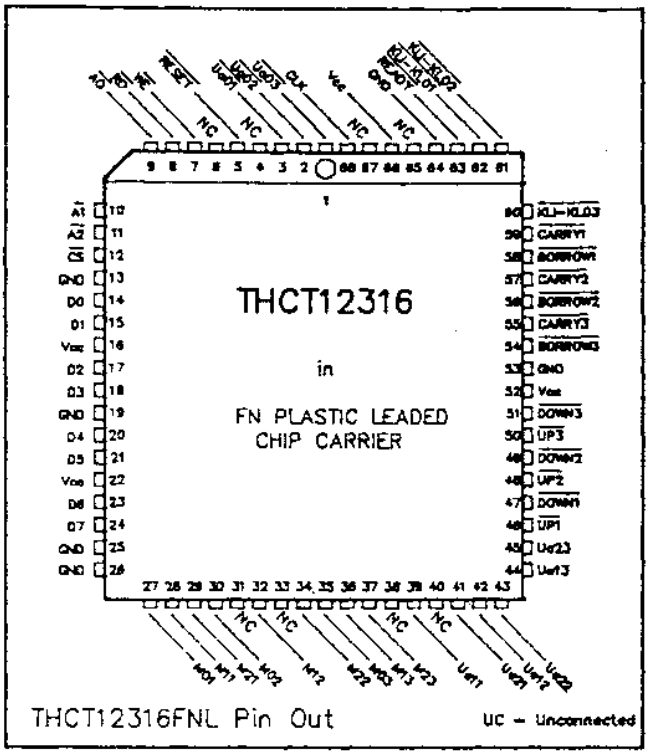
The three counters of this device can be managed through read and write operations to the allocation addresses of registers CNTnH and CNTnL, referring respectively to High and Low bytes of the n-th counter, where n can be in the range 1÷6.

APPENDIX A: COMPONENTS DESCRIPTION

Smart Part™

THCT12316 TRIPLE INCREMENTAL ENCODER INTERFACE

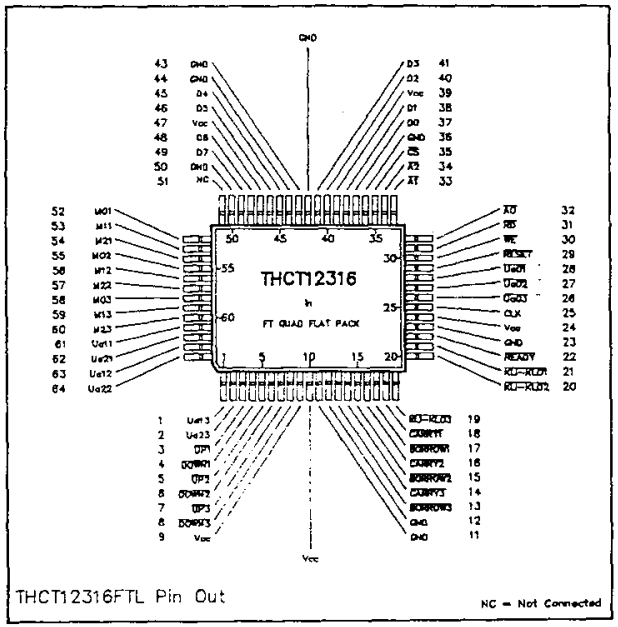
* Three independent channels in one compact surface mount device
* Each channel compatible with the popular THCT2000
* Interfaces three mechanisms/ axes to data bus
* Direction discriminators identify & measure forward/ backward rotation/direction
* Separate zero pulse input
* Pulse width measurement
* Frequency measurement
* Cascadable 16-bit counters
* TTL compatible
* 8-bit parallel 3-state bus
* Simple write/read procedure
* Choice of chip carrier or flat package
* Advanced 1.8um CMOS technology



THCT12316FNL Pin Out — UC = Unconnected

Description

The THCT12316 INCREMENTAL ENCODER INTERFACE consists of three channels each, of which can independently determine the direction and displacement of a mechanical device or axis based on two input signals from transducers in quadrature. Alternatively, each channel can measure a pulse width using a known clock rate, or a frequency, by counting input pulses over a known time interval. It includes three 16-bit counters which may also be used separately. The THCT12316 may be cascaded between channels on one device or between devices to provide accuracy greater than 16-bits, and is designed for use in many types of microprocessor-based systems.



Applications

The THCT12316 enables mechanical devices to be interfaced with microprocessors. It may be used in many diverse applications, including robotics, tracker balls (or mouse), lathes or tooling machines, automobiles, conveyor belts and transport mechanisms. Since it contains three channels each THCH12316 can support three measurements or axes of motion.

Architecture

Within each channel there are four main elements:-

1. The measurementand mode control logic generates up or down count pulses,internal signals I1 and I2, from :

   - Quadrature signals Ual *,Ua2 * and zero pulse UaOn *
   - Clock input
   - Mode controls MOn *,Mln *,M2n *

Architecture - continued

2. A 16-bit counter made up from two independently loadable 8-bit counters.

3. A 16-bit latch which "freezes" the counter value when required

4. A multiplexer that allows the processor to read either upper or lower byte in the latch.

Supporting the three channels:-

The control logic provides common microprocessor interface signals; the output multiplexer allows the processor to select data from one of the three channels and the three-state buffers place this data on the bus.

(* throughout this data sheet signals suffixed n are repeated for each channel)

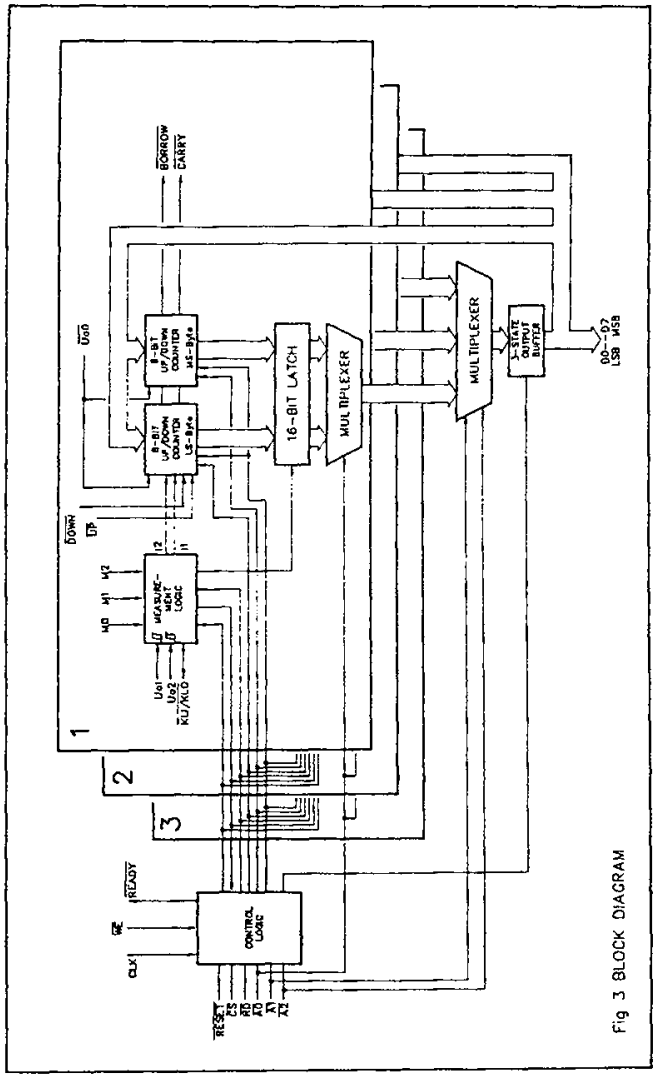


Fig 3 BLOCK DIAGRAM

Operation

The eight modes of operation of the THCT12316 are summarized in Table 1. The modes of the three channels can be selected independently.

MODE	M2n	M1n	M0n	MODE DESCRIPTION
				COUNTER
0	0	0	0	16-bit up/down counter (inhibits direction discriminator).
				DIRECTION DISCRIMINATOR
1	0	0	1	Single count pulse synchronous with Ua1n rising in forward direction and Ua1n falling in backward direction.
2	0	1	0	Single count pulse synchronous with Ua2n rising in forward direction and Ua2n falling in backward direction.
3	0	1	1	Double count pulse synchronous with Ua1n rising and falling.
4	1	0	0	Double count pulse synchronous with Ua2n rising and falling.
5	1	0	1	Quadruple count pulse synchronous with all edges.
				PULSE WIDTH MEASUREMENT
6	1	1	0	Ua1n is the gate signal Ua2n is high for up counting and low for down counting. Count is synchronous with rising clock.
				FREQUENCY MEASUREMENT
7	1	1	1	Ua1n is frequency signal to be measured Ua2n is the gate signal of known time interval. Count is synchronous with rising edge of Ua1n

Table 1

operation – continued

MODE 0: 16-BIT UP/DOWN COUNTER MODE

In this mode the THCT12316 may be used as three fast 16-bit synchronous up-/down counters with cascade capability. This is operated using the /UPn and /DOWNn inputs.

The states of the counter outputs are transferred to a 16-bit latch. The contents of this 16-bit latch are multiplexed on an 8-bit parallel data bus (D0.....D7) and enabled using /RD and /CS.

/A0 is the control input for the byte multiplexer. A high level at this input transfers the least significant byte to the data outputs; and a low level transfers the most significant byte.

The signals /A1 and /A2 select the channel for read or write according to the following table:

channel number	/A1	/A2
1	H	H
2	L	H
3	H	L
no channel selected(1)	L	L

(1) Output buffers still selected if /RD and /CS active – data bus carries invalid data

Table 2

The up/down counters are loaded in individual 8-bit bytes by the /WR and /CS signals, with the byte selected by the /A0 input, and the channel by the /A1 and /A2 inputs. The counters and the control logic may be cleared using the /SRESET signal. The counters are cleared individually using the UaOn signals.

Cascading to 32 bits is possible using the inputs /UPn and /DOWNn the outputs /BORROWn, /CARRYn and the input/outputs /KLI-KLOn.

MODES 1-5: DIRECTION DISCRIMINATOR MODES

The quadrature signals UAln and Ua2n, identify forward or backward directions. If Ualn leads Ua2n, the forward direction is indicated and the counter will count up; if Ualn lags Ua2n, the reverse direction is indicated and the counter will count down.

operation – continued

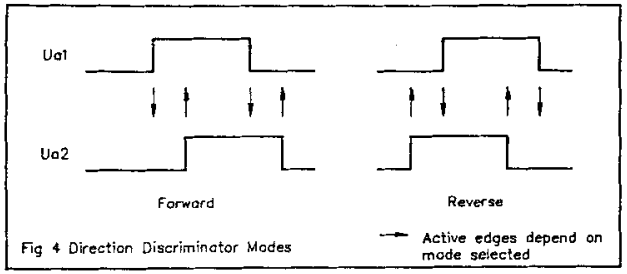


Fig 4 Direction Discriminator Modes

Ualn and Ua2n are both stored in the first of a pair of consecutive D-type flip-flops on the clock falling edge, and transferred to the next on the clock rising edge. By comparing the states of the four flip-flops and checking the mode inputs, the up or down count pulses are generated; see figures 5 and 6.

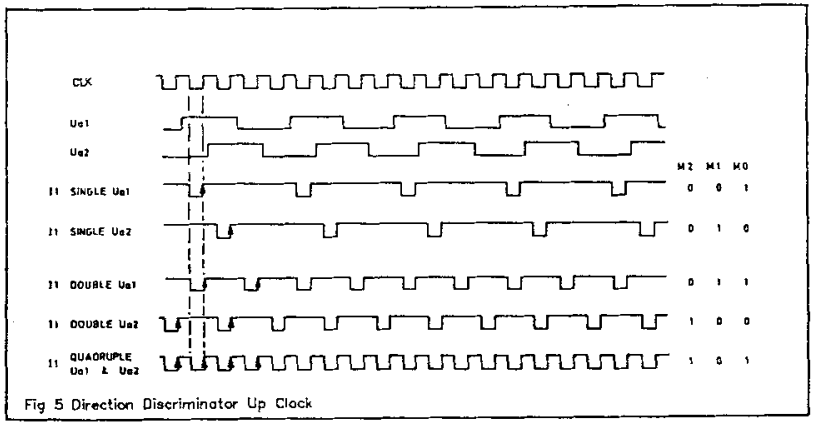


Fig 5 Direction Discriminator Up Clock

operation - continued

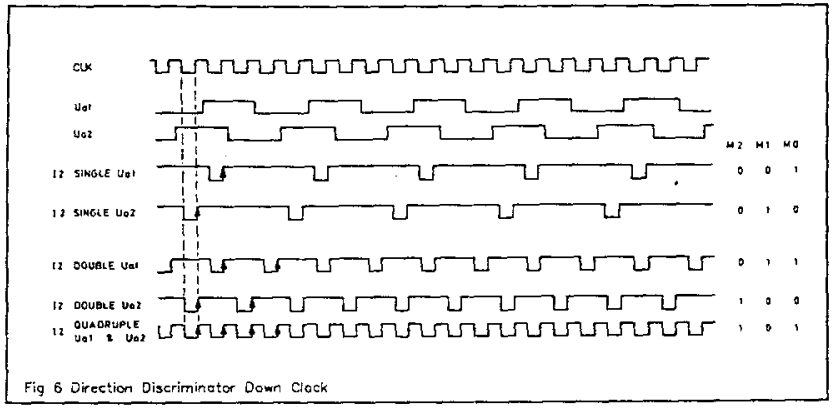


Fig 6 Direction Discriminator Down Clock

MODES 1 to 5 define which edge of the quadrature signals will be counted in accordance with Table 1.

The clock frequency should be at least four times greater than the frequencies of the quadrature signals: this will eliminate problems resulting from timing jitter in the transducer signals and will allow the quadruple counting mode to be used. The frequency of the quadrature signals, Ualn and Ua2n may be calculated from the relationship:

$$F = \frac{\text{shaft speed}}{\text{resolution of transducer}}$$

MODE 6: PULSE WIDTH MEASUREMENT MODE

In this mode, Ualn acts as a gate, and is the pulse width to be measured. Synchronised with the clock edge after a low to high transition in Ualn, count -ing begins at the input clock frequency. Similarly, synchronised with the clock edge after a high to low transition of Ualn, counting is disabled; the value in the counter is loaded in the output register; /KLI-KLOn is pulled low; and then the counter clears. See figure 7. If Ua2n is held high, the counter will count up, and if Ua2n is held low, the counter will count down.

Each counter can be preloaded in two bytes by activating /CS, /WE, and selecting the required byte with /A0, and the required channel with /A1 and /A2. This must be done while Ualn is low. The output register should be read by activating /CS, /RD, and selecting the individual bytes with /A0 after Ualn has fallen and before the next preload takes place.

operation - continued

The /KLI-KLOn signal may be used as an interrupt to indicate to the processor when the output register has been loaded. In both the pulse width and frequency modes, the output register will not be loaded via /CS and /RD, but by the falling edge of Ualn, or by pulling /KLI-KLOn low.

In pulse width mode, the minimum time that can be measured is:

Tmin = 2 (To) (Accuracy is +/- To)

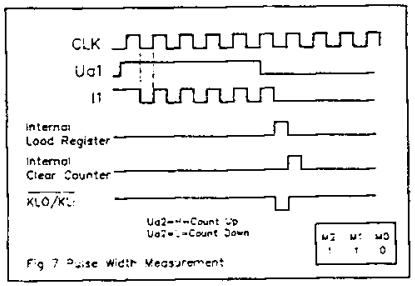


Fig 7 Pulse Width Measurement

MODE 7: FREQUENCY MEASUREMENT MODE

In Mode 7, Ualn is the signal of unknown frequency to be measured; Ua2n is a gate signal of known width. A low to high transition of Ua2n enables counting at the frequency of Ualn. When the gate (Ua2n) goes low, counting is disabled, the value of the counter is loaded into the output register, /KLI-KLOn is pulled low, and the counter is then cleared. See Figure 8.

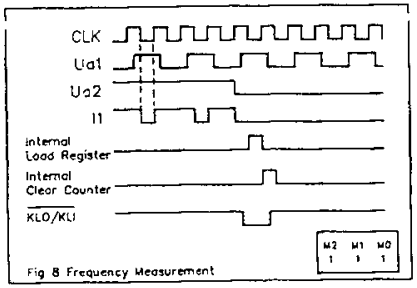


Fig 8 Frequency Measurement

operation - continued

RESET OPERATION

A total reset is initiated by pulling the /RESET pin low. This will clear the counters to zero, reset the D flip-flops at the inputs of the quadrature signals (Ua1n and Ua2n), clear the latches that inhibit the load register pulse, and load zero into the output register. To avoid a spurious count errors (+/- 1) after a reset, the Ua1n and Ua2n inputs should be held to the values indicated in Table 2 during and just after the reset pulse.

MODE	Ua1n	Ua2n
0	X	X
1-5	H	H
6-7	L	L

Table 3

CASCADING DEVICES

The /KLI-KLOn pins of all cascaded THCT12316's should be tied together, so that all of the devices load their output registers at the same time. When the 'master' generates a pulse for the other THCT12316s, /KLI-KLOn on the 'master' works as an output, and /KLI-KLOn on the 'slaves' work as inputs. The /CARRY output of one device should be tied to the /UP input of the next device in the cascade. Similarly, /BORROW should be connected to /DOWN. See 'System Application.'

READ OPERATION

A number may be preloaded into the counter by pulling /CS and /WE low while using /A0 to direct the value on the data bus to the selected byte of the counter and /A1 & /A2 to select the required channel. This will cause /READY to go low on the next falling clock edge, and remain low until /CS and /WE go high. See Figure 12.

WRITE OPERATION

When in MODES 0 to 5 the contents of the counter can be read at any time by pulling /CS and /RD low. The channel is selected by using /A1 & /A2. Within this channel the most significant byte may be selected be setting /A0 to low, and the least significant byte may be read be setting /A0 high. This will cause a load output register pulse to be generated and /KLI-KLOn will go low during the next low clock pulse. /READY will also go low as the clock goes

WRITE OPERATION - continued

low, and will stay low until /CS and/or /RD go high. The load output register pulse stores the current value of the counter in a 16-bit latch register and /A0 directs the selected byte through a multiplexer to the outputs : /CS and /RD also enable the 3-state outputs - see Figure 13. The output register will be loaded immediately if /KLI-KLOn is pulled low externally, this signal normally comes from a cascaded device.

For Modes 6 & 7 see the earlier description of these modes.

Configuration

Special consideration should be paid to the automatic configuration features of the THCT12316. The purpose of these features is to allow for the different order of byte reads (high then low or low then high) of different processors when doing a word read across a byte wide bus and also to configure cascaded devices automatically for correct word read sequence -see below.

Byte order configuration-

After a system reset has occured, the first read operation will store the value of /A0 in a latch within the device. From that time until the next system reset the load output register pulse during a read operation will only be generated if /A0 is this stored value. This means that the internal load output register pulse is correctly generated for word operations regardless of the byte order of the particular processor. Special care should be taken if reading individual bytes to ensure these operations are always done in a consistent order.

Cascaded configuration-

After a system reset the first device and channel to receive a read operation configures itself into "Master" mode and outputs a pulse on /KLI-KLO. In cascaded operation the /KLI-KLO pins of the cascaded channels are connected together and the input pulse on /KLI-KLO of the cascaded channels configures these to "Slave" mode. On all subsequent read operations the load output register pulse is only generated by the "Master" channel (for the appropriate polarity of /A0, as noted above) and this is fed to the "Slave" devices via the /KLI-KLO connection.

Special care should be taken when cascading devices or channels to always read in the same channel order, as well as the byte order already mentioned. To freeze all three channels with a single read cycle (in cascaded or non-cascaded mode) the /KLI-KLO pins of all channels are connected with a pull-up resistor to Vcc (see Systems Application). This ensures that only one channel is operating as the "Master" and all others are "Slaves".

If an external "freeze" of the positioning system is required, and external /KLI-KLO pulse will program all channels as slaves. This is derived by generating an external /KLI-KLO pulse before the first read cycle appears after system reset (See Design Checklist).

Pin Description

Pin Name	Pin Number 68 PLCC	Pin Number 64 QFP	I/O	Description
/CS	12	35	Input	Chip Select. A low enables the device.
/RD	8	31	Input	Read. When this and /CS are active(low), the data from the output register will be present on the data bus.
D0	14	37		LSB
.	15	38	Input/	Data Bus Buffer: 8-Bit Bi-directional
.	17	40	Output	buffer with 3-state outputs connected
.	18	41		to the microprocessor system.
.	20	45		
.	21	46		
.	23	48		
D7	24	49		MSB
/BORROW1	58	17		
/BORROW2	56	15	Output	Counter underflow signal
/BORROW3	54	13		
/CARRY1	59	18		
/CARRY2	57	16	Output	Counter overflow signal
/CARRY3	54	14		
/KLI-KLO1	62	21	Input/	Cascade load input/cascade load output.
/KLI-KLO2	61	20	Output	Open drain output with internal 95uA(nom)
/KLI-KLO3	60	19		pull-up. External pull-up required for full speed operation.
/READY	63	22	Output	When low signal indicates to the MPU that read or write may be completed. /READY falling edge synchronous with CLK Open drain output needs external pull-up.
M21	29	54	Input	Mode select inputs (see Table 1)
M11	28	53	"	
M01	27	52	"	
M22	34	57	"	
M12	32	56	"	
M02	30	55	"	
M23	37	60	"	
M13	36	59	"	
M03	35	58	"	

Pin Description - continued

Pin Name	Pin Number 68 PLCC	Pin Number 64 QFP	I/O	Description
Ua13	44	1	Input	Measuring input signals
Ua12	42	63	"	(Schmitt characteristics)
Ua11	39	61	"	
Ua23	45	2	"	
Ua22	43	64	"	
Ua21	41	62	"	
/Ua01	3	28	Input	Zero pulse. When active (low), the
/Ua02	2	27		counter in the appropriate channel is
/Ua03	1	26		cleared. Other logic is not affected.
CLK	68	25	Input	Clock. Used for internal synchronisation and control timing.
/A0	9	32	Input	Byte select. A high level selects the least significant byte. A low level selects the most significant byte
/A1	10	33	Input	Channel select. See Table 2.
/A2	11	34	Input	
/RESET	5	29	Input	Device reset. When active (low), the control logic is reset to a known state and the counter is cleared.
/WE	7	30	Input	Write enable. When /WE and /CS are active (low), the data that is on the bus is loaded into the counter address -ed by 1A0,1A1 and 1A3.
/DOWN1	47	4		
/DOWN2	49	6	Input	Cascade input for counting down.
/DOWN3	51	8		
/UP1	46	3		
/UP2	48	5	Input	Cascade input for counting up.
/UP3	50	7		
Vcc	16,22, 52,66	9,10, 24,39, 47		Power supply voltage 5V +/- 10%.
GND	13,19,25, 53,64	11,12,23,36 42,43,44,50		Ground.